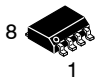
High Speed Low Power CAN, CAN FD Transceiver

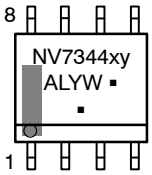
NCV7344

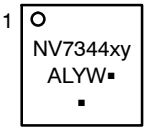


SOIC−8 NB
CASE 751−07

DFN8
MW SUFFIX
CASE 507AB

MARKING DIAGRAM

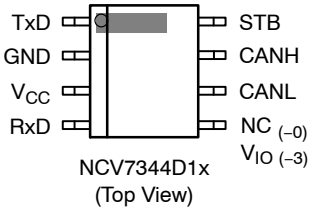




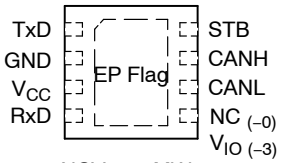
NV7344xy= Specific Device Code
x = − or A
y = 0 or 3
− = long filter time
A = short filter time
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



NCV7344D1x
(Top View)



NCV7344MWx
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Description

The NCV7344 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7344 is an addition to the CAN high−speed transceiver family complementing NCV734x CAN stand−alone transceivers and previous generations such as AMIS42665, AMIS3066x, etc.

The NCV7344 guarantees additional timing parameters to ensure robust communication at data rates beyond 1 Mbps to cope with CAN flexible data rate requirements (CAN FD). These features make the NCV7344 an excellent choice for all types of HS−CAN networks, in nodes that require a low−power mode with wake−up capability via the CAN bus.

Features

- Compatible with ISO 11898−2:2016
- Specification for Loop Delay Symmetry up to 5 Mbps
- V_{IO} pin on NCV7344−3 Version Allowing Direct Interfacing with 3 V to 5 V Microcontrollers
- Very Low Current Standby Mode with Wake−up via the Bus
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity
- Very Low EME without Common−mode (CM) Choke
- No Disturbance of the Bus Lines with an Un−powered Node
- Transmit Data (TxD) Dominant Timeout Function
- Under All Supply Conditions the Chip Behaves Predictably
- Very High ESD Robustness of Bus Pins, >8 kV System ESD Pulses
- Thermal Protection
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- Bus Pins Protected Against Transients in an Automotive Environment
- These are Pb−free Devices

Quality

- Wettable Flank Package for Enhanced Optical Inspection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

Typical Applications

- Automotive
- Industrial Networks

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BLOCK DIAGRAM

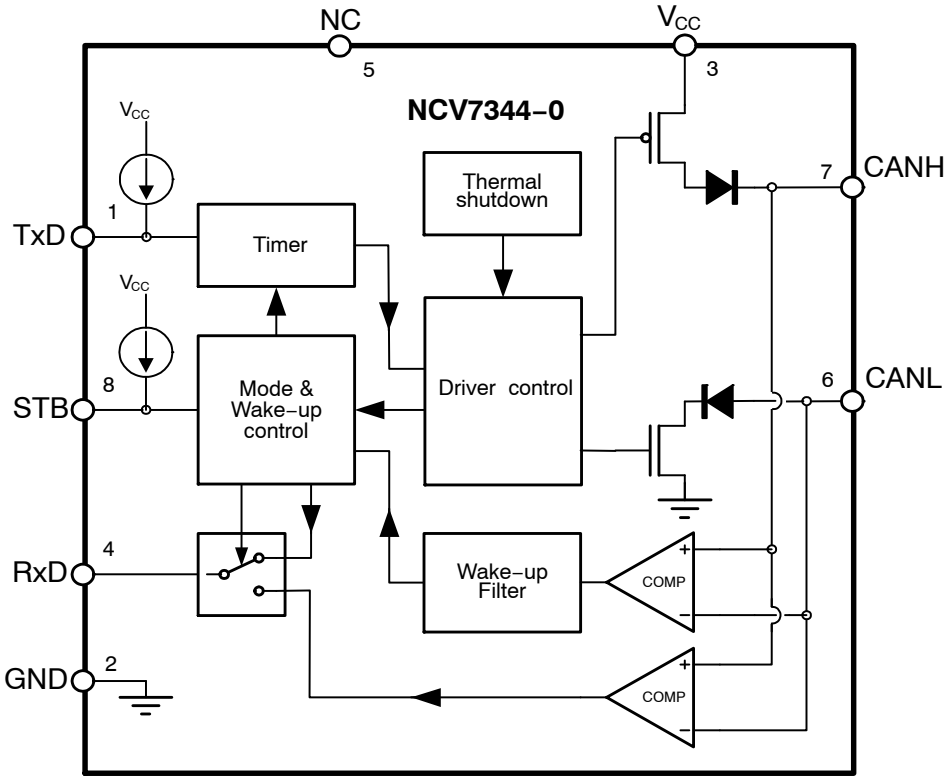


Figure 1. NCV7344−0 Block Diagram

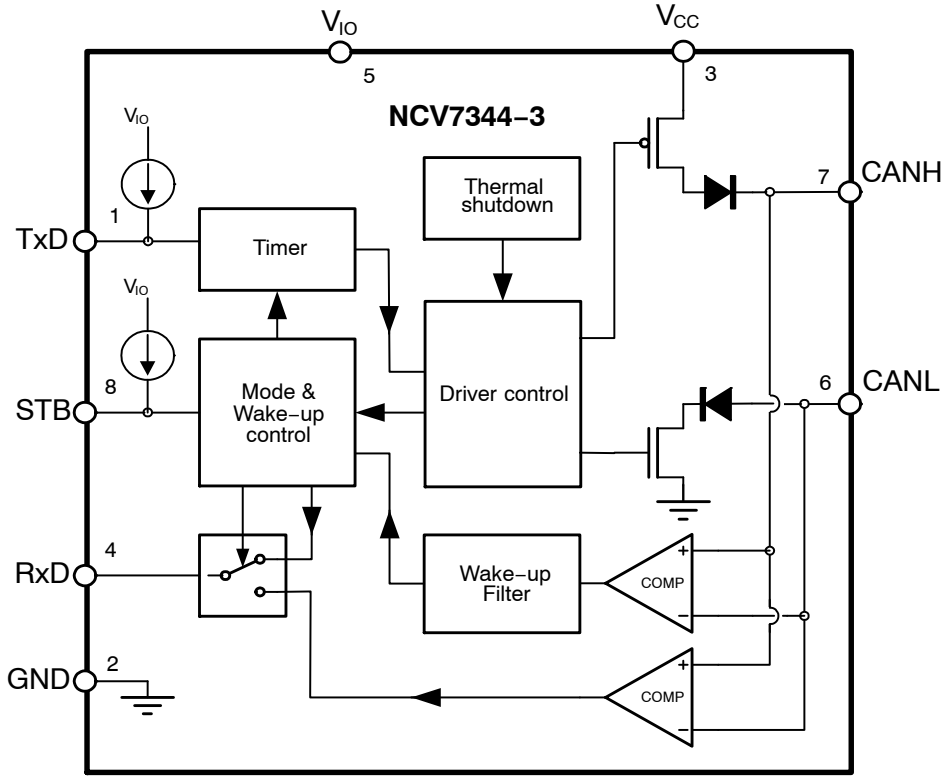


Figure 2. NCV7344−3 Block Diagram

TYPICAL APPLICATION

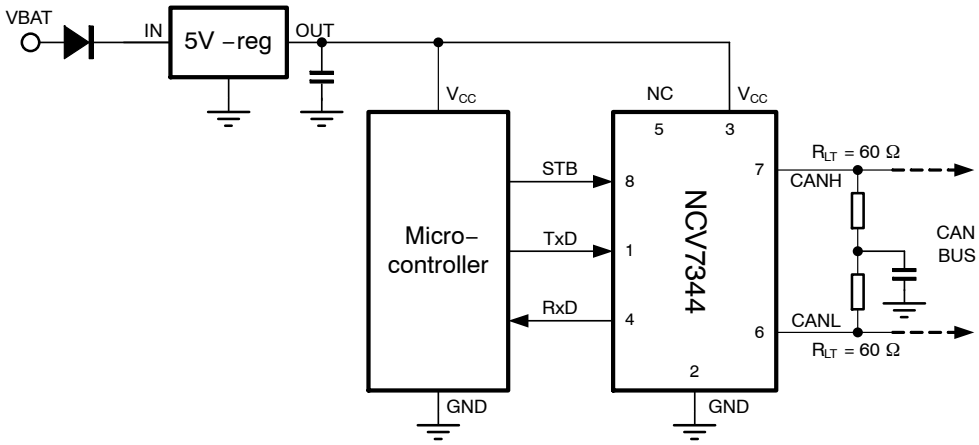


Figure 3. Application Diagram NCV7344−0

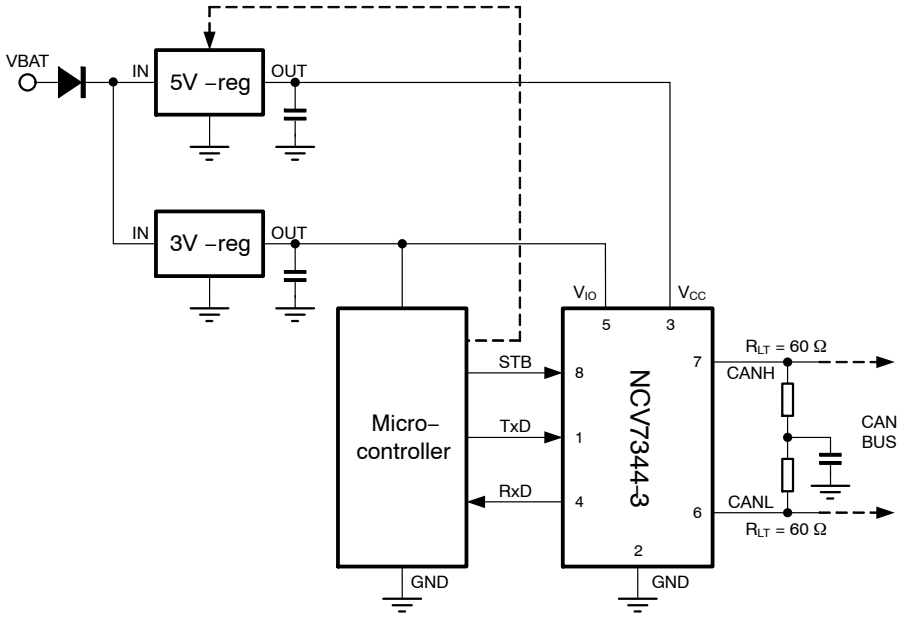


Figure 4. Application Diagram NCV7344−3

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	TxD	Transmit data input; low input → dominant driver; internal pull−up current
2	GND	Ground
3	V_{CC}	Supply voltage
4	RxD	Receive data output; dominant transmitter → low output
5 5	NC V_{IO}	Not connected. On NCV7344−0 only Digital Input / Output pins and other functions supply voltage. On NCV7344−3 only
6	CANL	Low−level CAN bus line (low in dominant mode)
7	CANH	High−level CAN bus line (high in dominant mode)
8	STB	Standby mode control input; internal pull−up current
	EP	Exposed Pad. Recommended to connect to GND or left floating in application (DFN8 package only).

FUNCTIONAL DESCRIPTION

Operating Modes

NCV7344 provides two modes of operation as illustrated in Table 2. These modes are selectable through pin STB.

Table 2. OPERATING MODES

Pin STB	Mode	Pin RxD	
Low	Normal	Low when bus dominant	High when bus recessive
High	Standby	Follows the bus when wake−up detected	High when no wake−up request detected

Normal Mode

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give low EME.

Standby Mode

In standby mode both the transmitter and receiver are disabled and a very low−power differential receiver monitors the bus lines for CAN bus activity. The bus lines are biased to ground and supply current is reduced to a minimum, typically 10 μA. When a wake−up request is detected by the low−power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of t_{wake_filt}, the RxD pin is driven low by the transceiver (following the bus) to inform the controller of the wake−up request.

Wake−up

When a valid wake−up pattern (phase in order dominant – recessive – dominant) is detected during the standby mode the RxD pin follows the bus. Minimum length of each phase is t_{wake_filt} – see Figure 5.

Pattern must be received within t_{wake_to} to be recognized as valid wake−up otherwise internal logic is reset.

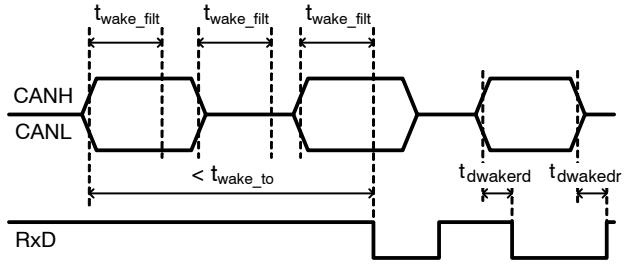


Figure 5. NCV7344 Wake−up Behavior

Overtemperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 180°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off−state resets when the temperature decreases below the shutdown threshold and pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

TxD Dominant Timeout Function

A TxD dominant timeout timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low−level on pin TxD exceeds the internal timer value $t_{dom(TxD)}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

This TxD dominant timeout time $t_{dom(TxD)}$ defines the minimum possible bit rate to 17 kbps.

Fail Safe Features

A current−limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

Standby undervoltage on VCC pin prevents the chip sending data on the bus when there is not enough VCC supply voltage by entering standby mode. Undervoltage detection on VIO pin (NCV7344−3 version only) also causes transition to standby mode. Switch−off undervoltage detection level on supply pin(s) forces transceiver to disengage from the bus until the supply is recovered. After supply is recovered TxD pin must be first released to high to allow sending dominant bits again. Recovery time from undervoltage detection is equal to td(stb−nm) time.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 7). Pins TxD and STB are pulled high internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the VCC supply be removed.

V_{IO} Supply Pin

The V_{IO} pin (available only on NCV7344−3 version) should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller the I/O levels between microcontroller and transceiver are properly adjusted. See Figure 4. Pin V_{IO} also provides the internal supply voltage for low−power differential receiver of the transceiver. This allows detection of wake−up request even when there is no supply voltage on pin V_{CC}.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

ABSOLUTE MAXIMUM RATINGS

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply voltage V_{CC}, V_{IO}		−0.3	+6	V
V_{CANH}	DC voltage at pin CANH	0 < V_{CC} < 5.25 V; no time limit	−42	+42	V
V_{CANL}	DC voltage at pin CANL	0 < V_{CC} < 5.25 V; no time limit	−42	+42	V
$V_{CANH-CANL}$	DC voltage between CANH and CANL		−42	+42	V
$V_{I/O}$	DC voltage at pin TxD, RxD, STB		−0.3	+6	V
V_{esdHBM}	Electrostatic discharge voltage at all pins, Component HBM	(Note 1)	−8	+8	kV
V_{esdCDM}	Electrostatic discharge voltage at all pins, Component CDM	(Note 2)	−750	+750	V
V_{esdIEC}	Electrostatic discharge voltage at pins CANH and CANL, System HBM (Note 4)	(Note 3)	−8	+8	kV
V_{schaff}	Voltage transients, pins CANH, CANL. According to ISO7637−3, Class C (Note 4)	test pulses 1	−100		V
		test pulses 2a		+75	V
		test pulses 3a	−150		V
		test pulses 3b		+100	V
Latch−up	Static latch−up at all pins	(Note 5)		150	mA
T_{stg}	Storage temperature		−55	+150	°C
T_J	Maximum junction temperature		−40	+170	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Standardized charged device model ESD pulses when tested according to AEC−Q100−011
3. System human body model electrostatic discharge (ESD) pulses in accordance to IEC 61000−4−2. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GND.
4. Results were verified by external test house.
5. Static latch−up immunity: Static latch−up protection level when tested according to EIA/JESD78.

Table 4. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal characteristics, SOIC−8 (Note 6)			
Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 7)	$R_{\theta JA}$	131	°C/W
Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 8)	$R_{\theta JA}$	81	°C/W
Thermal characteristics, DFN8 (Note 6)			
Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 7)	$R_{\theta JA}$	125	°C/W
Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 8)	$R_{\theta JA}$	58	°C/W

6. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
7. Values based on test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
8. Values based on test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage.

ELECTRICAL CHARACTERISTICS

Table 5. ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 to 5.25 V; T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{LT} = 100 pF, C_1 not used, C_{RxD} = 15 pF unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (Pin V_{CC})						
V_{CC}	Power supply voltage	(Note 9)	4.75	5	5.25	V
I_{CC}	Supply current	Dominant; V_{TxD} = Low	20	45	70	mA
		Recessive; V_{TxD} = High	1.9	5	10	mA
I_{CCS}	Supply current in standby mode	$T_J \le 100°C$, (Note 10)	–	10	15	μA
$V_{UVD(VCC)(stby)}$	Standby undervoltage detection V_{CC} pin		3.5	4	4.3	V
$V_{UVD(VCC)(swoff)}$	Switch−off undervoltage detection V_{CC} pin		2.0	2.3	2.6	V
V_{IO} SUPPLY VOLTAGE (Pin V_{IO}) Only for NCV7344−3 version						
V_{IO}	Supply voltage on pin V_{IO}		2.8	–	5.5	V
I_{IOS}	Supply current on pin V_{IO} in standby mode	$T_J \le 100°C$, (Note 10)	–	–	11	μA
I_{CCS}	Supply current on pin V_{CC} in standby mode	$T_J \le 100°C$, (Note 10)	–	0	4.0	μA
I_{IONM}	Supply current on pin V_{IO} during normal mode	Dominant; V_{TxD} = Low	0.45	0.65	0.9	mA
		Recessive; V_{TxD} = High	0.32	0.43	0.58	
V_{UVDVIO}	Undervoltage detection voltage on V_{IO} pin		2.0	2.3	2.6	V
TRANSMITTER DATA INPUT (Pin TxD)						
V_{IH}	High−level input voltage	Output recessive	2.0	–	–	V
V_{IL}	Low−level input voltage	Output dominant	–	–	0.8	V
I_{IH}	High−level input current	$V_{TxD} = V_{CC}/V_{IO}$	−5	0	+5	μA
I_{IL}	Low−level input current	V_{TxD} = 0 V	−300	−150	−75	μA
C_i	Input capacitance	(Note 10)	–	5	10	pF
TRANSMITTER MODE SELECT (Pin STB)						
V_{IH}	High−level input voltage	Standby mode	2.0	–	–	V
V_{IL}	Low−level input voltage	Normal mode	–	–	0.8	V
I_{IH}	High−level input current	$V_{STB} = V_{CC}/V_{IO}$	−1	0	+1	μA
I_{IL}	Low−level input current	V_{STB} = 0 V	−15	–	−1	μA
C_i	Input capacitance	(Note 10)	–	5	10	pF
RECEIVER DATA OUTPUT (Pin RxD)						
I_{OH}	High−level output current	Normal mode $V_{RxD} = V_{CC}/V_{IO} - 0.4$ V	−8	−3	−1	mA
I_{OL}	Low−level output current	V_{RxD} = 0.4 V	1	6	12	mA
BUS LINES (Pins CANH and CANL)						
$I_{o(rec)}$	Recessive output current at pins CANH and CANL	−27 V < V_{CANH}, V_{CANL} < +32 V; Normal mode	−5	–	+5	mA
I_{LI}	Input leakage current	0 Ω < R(V_{CC} to GND) < 1 MΩ $V_{CANL} = V_{CANH}$ = 5 V	−5	0	+5	μA
$V_{o(rec)(CANH)}$	Recessive output voltage at pin CANH	Normal mode, V_{TxD} = High; R_{LT} and C_{LT} not used	2.0	2.5	3.0	V
$V_{o(rec)(CANL)}$	Recessive output voltage at pin CANL	Normal mode, V_{TxD} = High; R_{LT} and C_{LT} not used	2.0	2.5	3.0	V
$V_{o(off)(CANH)}$	Recessive output voltage at pin CANH	Standby mode; R_{LT} and C_{LT} not used	−0.1	0	0.1	V

Table 5. ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 to 5.25 V; T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{LT} = 100 pF, C_1 not used, C_{RxD} = 15 pF unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUS LINES (Pins CANH and CANL)						
$V_{o(off)(CANL)}$	Recessive output voltage at pin CANL	Standby mode; R_{LT} and C_{LT} not used	−0.1	0	0.1	V
$V_{o(off)(diff)}$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	Standby mode; R_{LT} and C_{LT} not used	−0.2	0	0.2	V
$V_{o(dom)(CANH)}$	Dominant output voltage at pin CANH	V_{TxD} = 0 V; t < $t_{dom(TxD)}$; 50 Ω < R_{LT} < 65 Ω	2.75	3.5	4.5	V
$V_{o(dom)(CANL)}$	Dominant output voltage at pin CANL	V_{TxD} = 0 V; t < $t_{dom(TxD)}$; 50 Ω < R_{LT} < 65 Ω	0.5	1.5	2.25	V
$V_{o(dom)(diff)}$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	V_{TxD} = 0 V; dominant; 45 Ω < R_{LT} < 65 Ω	1.5	2.25	3.0	V
$V_{o(dom)(diff)_arb}$	Differential bus output voltage during arbitration ($V_{CANH} - V_{CANL}$)	R_{LT} = 2.24 kΩ (Note 10)	1.5	–	5.0	V
$V_{o(rec)(diff)}$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	V_{TxD} = High; recessive; no load	−50	0	+50	mV
$V_{o(dom)(sym)}$	Dominant output voltage driver symmetry ($V_{CANH} + V_{CANL}$)	R_{LT} = 60 Ω; C_1 = 4.7 nF; TxD = square wave up to 1 MHz	0.9	1.0	1.1	V_{CC}
$I_{o(sc)(CANH)}$	Short circuit output current at pin CANH	−3 V < V_{CANH} < +18 V	−100	−70	1.5	mA
$I_{o(sc)(CANL)}$	Short circuit output current at pin CANL	−3 V < V_{CANL} < +36 V	−1.5	70	100	mA
$V_{i(rec)(diff)_NM}$	Differential input voltage range recessive state	Normal or Silent mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	−3.0	–	0.5	V
$V_{i(rec)(diff)_LP}$		Standby or Sleep mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	−3.0		0.4	V
$V_{i(dom)(diff)_NM}$	Differential input voltage range dominant state	Normal or Silent mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	0.9	–	8.0	V
$V_{i(dom)(diff)_LP}$		Standby or Sleep mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	1.05		8.0	V
$V_{i(diff)(th)_NORM}$	Differential receiver threshold voltage in normal mode	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V	0.5	–	0.9	V
$V_{i(diff)(th)_NORM_H}$	Differential receiver threshold voltage in normal mode, extended range	−30 V < V_{CANL} < +35 V; −30 V < V_{CANH} < +35 V	0.4	–	1.0	V
$V_{i(diff)(th)_STDBY}$	Differential receiver threshold voltage in standby mode	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V	0.4	–	1.05	V
$R_{i(cm)(CANH)}$	Common−mode input resistance at pin CANH	−2 V ≤ V_{CANH} ≤ +7 V; −2 V ≤ V_{CANL} ≤ +7 V	15	26	37	kΩ
$R_{i(cm)(CANL)}$	Common−mode input resistance at pin CANL	−2 V ≤ V_{CANH} ≤ +7 V; −2 V ≤ V_{CANL} ≤ +7 V	15	26	37	kΩ
$R_{i(cm)(m)}$	Matching between pin CANH and pin CANL common mode input resistance	V_{CANH} = V_{CANL} = +5 V	−1	0	+1	%
$R_{i(diff)}$	Differential input resistance	−2 V ≤ V_{CANH} ≤ +7 V; −2 V ≤ V_{CANL} ≤ +7 V	25	50	75	kΩ
$C_{i(CANH)}$	Input capacitance at pin CANH	V_{TxD} = High; (Note 10)	–	7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	V_{TxD} = High; (Note 10)	–	7.5	20	pF
$C_{i(diff)}$	Differential input capacitance	V_{TxD} = High; (Note 10)	–	3.75	10	pF

Table 5. ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 to 5.25 V; T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{LT} = 100 pF, C_1 not used, C_{RxD} = 15 pF unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TIMING CHARACTERISTICS (see Figures 6 and 8)						
$t_{d(TxD-BUSon)}$	Delay TxD to bus active		–	75	–	ns
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive		–	85	–	ns
$t_{d(BUSon-RxD)}$	Delay bus active to RxD		–	24	–	ns
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD		–	32	–	ns
t_{pd_dr}	Propagation delay TxD to RxD dominant to recessive transition		50	100	210	ns
t_{pd_rd}	Propagation delay TxD to RxD recessive to dominant transition		50	120	210	ns
$t_{d(stb-nm)}$	Delay standby mode to normal mode		5	11	20	μs
t_{wake_filt}	Filter time for wake−up via bus	NCV7344 version	0.5	–	5	μs
		NCV7344A version	0.15	–	1.8	μs
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions)	Valid bus wake−up event	0.5	2.6	6	μs
$t_{dwakedr}$	Delay to flag wake event (dominant to recessive transitions)	Valid bus wake−up event	0.5	2.6	6	μs
t_{wake_to}	Bus time for wake−up timeout	Standby mode	1	–	10	ms
$t_{dom(TxD)}$	TxD dominant time for timeout	V_{TxD} = Low; Normal mode	1	–	10	ms
$t_{Bit(RxD)}$	Bit time on RxD pin	$t_{Bit(TxD)}$ = 500 ns	400	–	550	ns
		$t_{Bit(TxD)}$ = 200 ns	120	–	220	ns
$t_{Bit(Vi(diff))}$	Bit time on bus (CANH − CANL pin)	$t_{Bit(TxD)}$ = 500 ns	435	–	530	ns
		$t_{Bit(TxD)}$ = 200 ns	155	–	210	ns
Δt_{Rec}	Receiver timing symmetry $\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit(Vi(diff))}$	$t_{Bit(TxD)}$ = 500 ns	−65	–	+40	ns
		$t_{Bit(TxD)}$ = 200 ns	−45	–	+15	ns
THERMAL SHUTDOWN						
$T_{J(sd)}$	Shutdown junction temperature	Junction temperature rising	160	180	200	°C

9. In the range between VUVD(VCC)(stby) and 4.75 V and from 5.25 V to 6 V the chip is fully functional; some parameters may be outside of the specification.
10. Values based on design and characterization, not tested in production

MEASUREMENT SETUPS AND DEFINITIONS

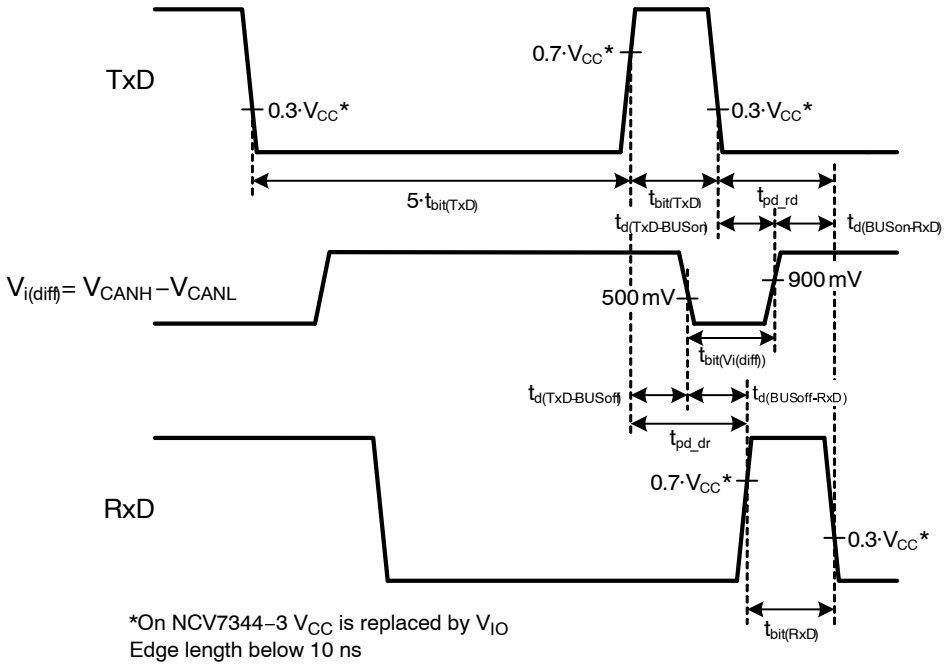


Figure 6. Transceiver Timing Diagram

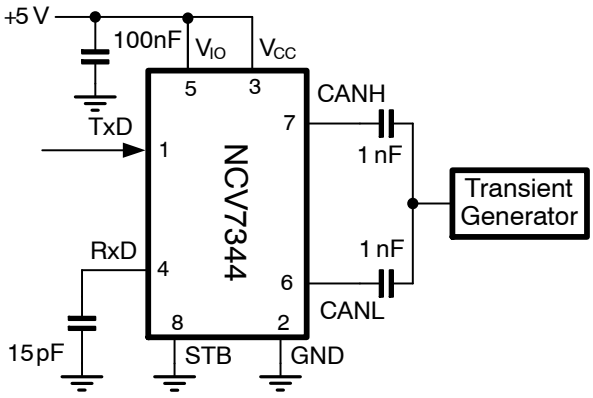


Figure 7. Test Circuit for Automotive Transients

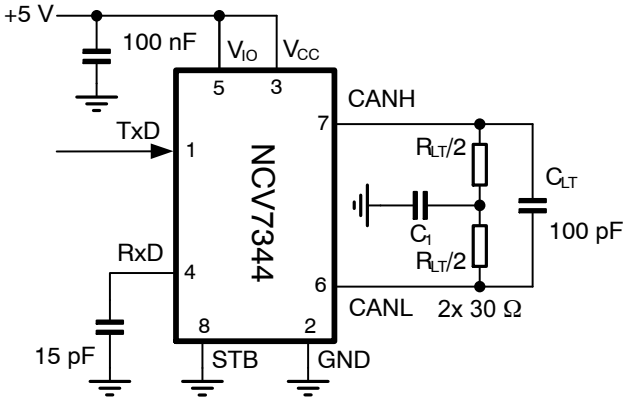


Figure 8. Test Circuit for Timing Characteristics

Table 6. ISO 11898−2:2016 Parameter Cross−Reference Table

ISO 11898−2:2016 Specification		NCV7344 Datasheet
Parameter	**Notation**	**Symbol**
Dominant output characteristics		
Single ended voltage on CAN_H	V_{CAN_H}	$V_{o(dom)(CANH)}$
Single ended voltage on CAN_L	V_{CAN_L}	$V_{o(dom)(CANL)}$
Differential voltage on normal bus load	V_{Diff}	$V_{o(dom)(diff)}$
Differential voltage on effective resistance during arbitration	V_{Diff}	$V_{o(dom)(diff)_arb}$
Differential voltage on extended bus load range (optional)	V_{Diff}	$V_{o(dom)(diff)}$
Driver symmetry		
Driver symmetry	V_{SYM}	$V_{o(dom)(sym)}$
Driver output current		
Absolute current on CAN_H	I_{CAN_H}	$I_{o(SC)(CANH)}$
Absolute current on CAN_L	I_{CAN_L}	$I_{o(SC)(CANL)}$
Receiver output characteristics, bus biasing active		
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{o(rec)(CANH)}$
Single ended output voltage on CAN_L	V_{CAN_L}	$V_{o(rec)(CANL)}$
Differential output voltage	V_{Diff}	$V_{o(rec)(diff)}$
Receiver output characteristics, bus biasing inactive		
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{o(off)(CANH)}$
Single ended output voltage on CAN_L	V_{CAN_L}	$V_{o(off)(CANL)}$
Differential output voltage	V_{Diff}	$V_{o(off)(diff)}$
Optional transmit dominant timeout		
Transmit dominant timeout, long	t_{dom}	$t_{dom(TxD)}$
Transmit dominant timeout, short	t_{dom}	NA
Static receiver input characteristics, bus biasing active		
Recessive state differential input voltage range	V_{Diff}	$V_{i(rec)(diff)_NM}$
Dominant state differential input voltage range	V_{Diff}	$V_{i(dom)(diff)_NM}$
Static receiver input characteristics, bus biasing inactive		
Recessive state differential input voltage range	V_{Diff}	$V_{i(rec)(diff)_LP}$
Dominant state differential input voltage range	V_{Diff}	$V_{i(dom)(diff)_LP}$
Receiver input resistance		
Differential internal resistance	R_{Diff}	$R_{i(diff)}$
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	$R_{i(cm)(CANH)}$ $R_{i(cm)(CANL)}$
Receiver input resistance matching		
Matching a of internal resistance	m_R	$R_{i(cm)(m)}$
Implementation loop delay requirement		
Loop delay	t_{Loop}	t_{pd_rd} t_{pd_dr}
Optional implementation data signal timing requirements for use with bit rates above 1 Mbit/s and up to 2 Mbit/s		
Transmitted recessive bit width @ 2 Mbit/s	$t_{Bit(Bus)}$	$t_{Bit(Vi(diff))}$
Received recessive bit width @ 2 Mbit/s	$t_{Bit(RXD)}$	$t_{Bit(RxD)}$

Table 6. ISO 11898−2:2016 Parameter Cross−Reference Table

Parameter	Notation	Symbol
Receiver timing symmetry @ 2 Mbit/s	Δt_{Rec}	Δ_{tRec}
Optional implementation data signal timing requirements for use with bit rates above 2 Mbit/s and up to 5 Mbit/s		
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(Bus)}$	$t_{Bit(Vi(diff))}$
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{Bit(RxD)}$
Received recessive bit width @ 5 Mbit/s	Δt_{Rec}	Δt_{Rec}
Maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}		
Maximum rating V_{Diff}	V_{Diff}	$V_{CANH-CANL}$
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_{CANH} V_{CANL}
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	NA
Maximum leakage currents on CAN_H and CAN_L, unpowered		
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_{LI}
Bus biasing control timings		
CAN activity filter time, long	t_{Filter}	t_{wake_filt}
CAN activity filter time, short	t_{Filter}	t_{wake_filt}
Wake−up timeout, short	t_{Wake}	NA
Wake−up timeout, long	t_{Wake}	t_{wake_to}
Timeout for bus inactivity (Required for selective wake−up implementation only)	$t_{Silence}$	NA
Bus Bias reaction time (Required for selective wake−up implementation only)	t_{Bias}	NA

DEVICE ORDERING INFORMATION (High Speed Low Power CAN, CANFD Transceiver)

Part Number	Long FT	Short FT	Vio	NC	Temperature Range	Package	Shipping†
NCV7344D10R2G	X			X	−40°C to +150°C	SOIC 150 8 GREEN (Matte Sn, JEDEC MS−012) (Pb−Free)	3000 / Tape & Reel
NCV7344D13R2G	X		X				
NCV7344AD10R2G		X		X			
NCV7344AD13R2G		X	X				
NCV7344MW0R2G	X			X		DFN 8 Wettable Flank (Pb−Free)	
NCV7344MW3R2G	X		X				
NCV7344AMW0R2G		X		X			
NCV7344AMW3R2G		X	X				

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

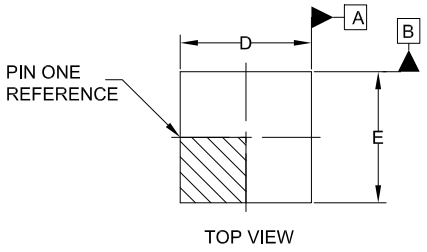
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

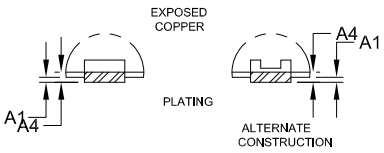
SCALE 2:1

DFNW8 3x3, 0.65P
CASE 507AB
ISSUE E

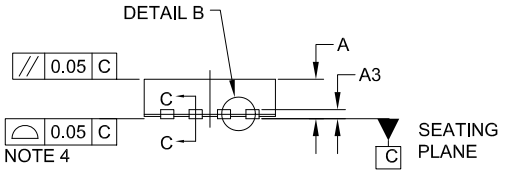
DATE 02 JUL 2021



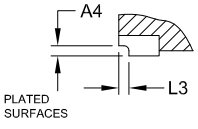
TOP VIEW



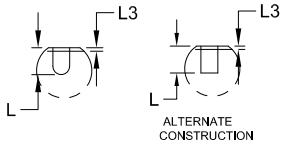
DETAIL B



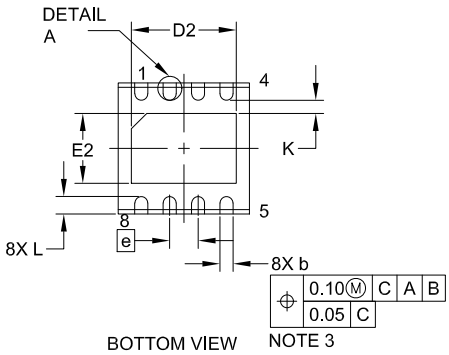
SIDE VIEW



SECTION C-C



DETAIL A

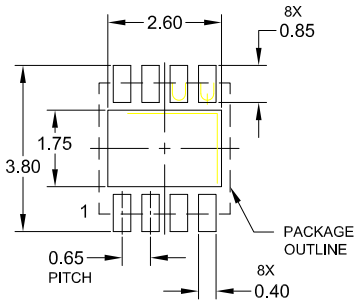


BOTTOM VIEW

NOTES:

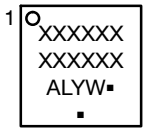
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	—	---	0.05
A3		0.20 REF	
A4	0.10	---	—
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
E	2.95	3.00	3.05
E2	1.50	1.60	1.70
e		0.65 BSC	
K		0.30 REF	
L	0.35	0.40	0.45
L3	0.00	0.05	0.10



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW8 3x3, 0.65P**	**PAGE 1 OF 1**

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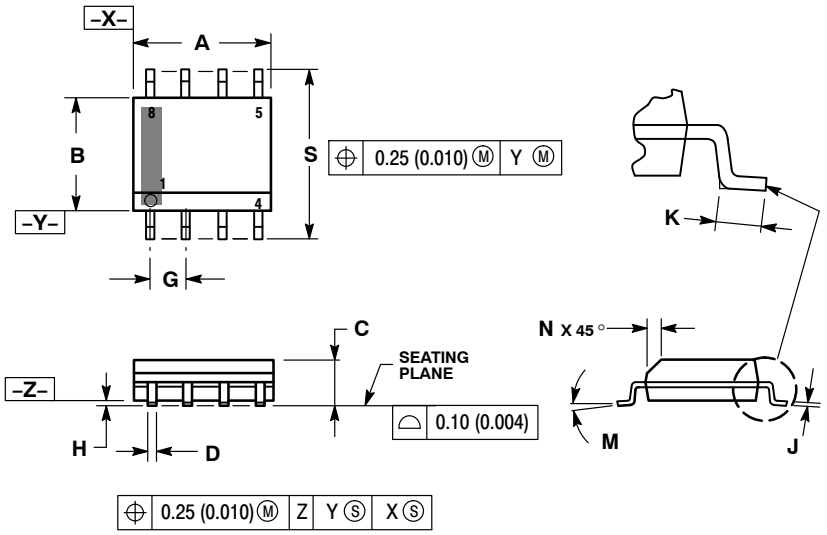
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

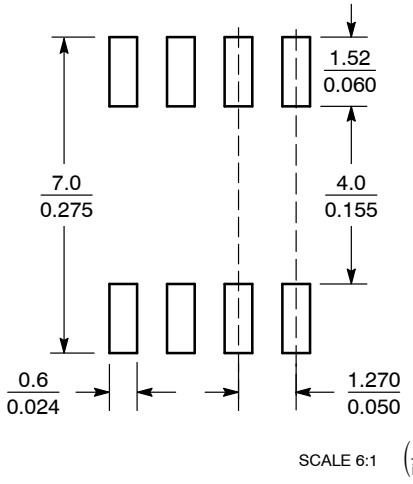
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

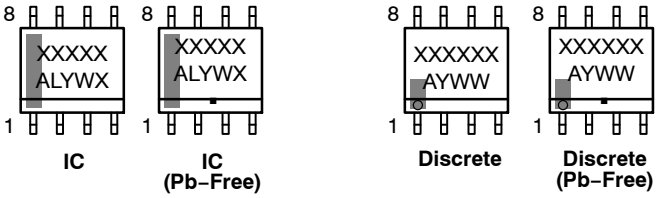
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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