Data Sheet

AD9694-EP

Enhanced Product

14-Bit, 500 MSPS, JESD204B, Quad Analog-to-Digital Converter

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Lane rates up to 15 Gbps
- 1.66 W total power dissipation at 500 MSPS
  - 415 mW per ADC channel
- SFDR = 82 dBFS at 305 MHz (1.80 V p-p input range)
- SNR = 66.8 dBFS at 305 MHz (1.80 V p-p input range)
- Noise density = −151.5 dBFS/Hz (1.80 V p-p input range)
- 0.975 V, 1.8 V, and 2.5 V dc supply operation
- No missing codes
- Internal ADC voltage reference
- Analog input buffer
- On-chip dithering to improve small signal linearity
- Flexible differential input range
  - 1.44 V p-p to 2.16 V p-p (1.80 V p-p nominal)
- 1.4 GHz analog input full power bandwidth
- Amplitude detect bits for efficient AGC implementation
- 4 integrated wideband digital processors
  - 48-bit NCO, up to 4 cascaded half-band filters
- Differential clock input
- Integer clock divide by 1, 2, 4, or 8 (see Figure 1)
- On-chip temperature diode
- Flexible JESD204B lane configurations

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +105°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, W-CDMA, GSM, LTE, LTE-A
- General-purpose software radios
- Ultrawideband satellite receivers
- Instrumentation
- Radars
- Signals intelligence (SIGINT)

FUNCTIONAL BLOCK DIAGRAM

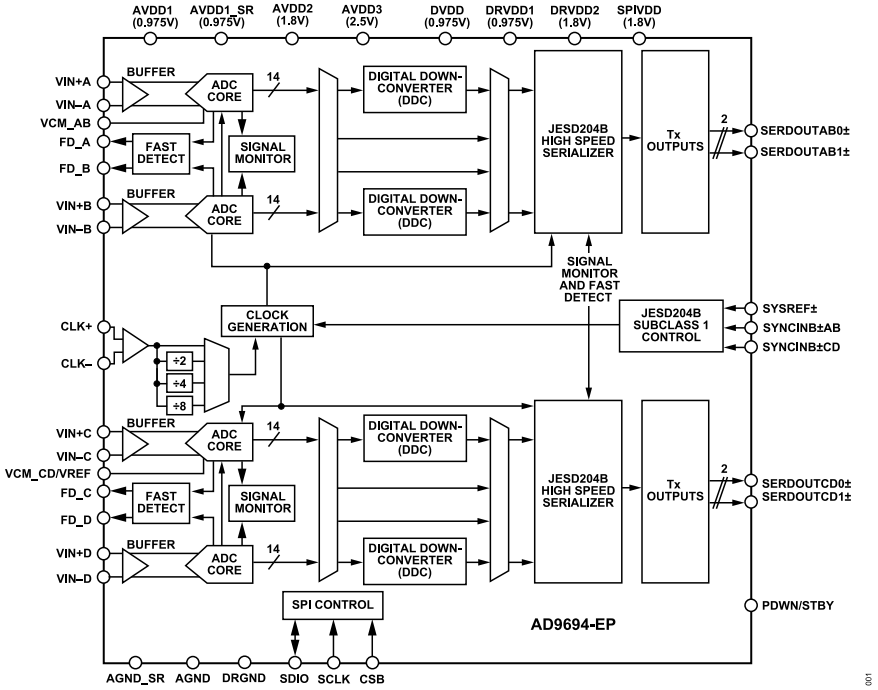

Figure 1. Functional Block Diagram

Rev. A

DOCUMENT FEEDBACK

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REVISION HISTORY

5/2023—Rev. 0 to Rev. A

Changes to Accuracy, Gain Error Parameter, Table 1 4

3/2023—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9694-EP is a quad, 14-bit, 500 MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This device is designed for sampling wide bandwidth analog signals of up to 1.4 GHz. The AD9694-EP is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The quad ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The analog inputs and clock signals are differential inputs. Each pair of ADC data outputs is internally connected to two digital downconverters (DDCs) through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 48-bit frequency translator, numerically controlled oscillator (NCO) and up to four half-band decimation filters.

In addition to the DDC blocks, the AD9694-EP has several functions that simplify the automatic gain control (AGC) function in the communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure each pair of intermediate frequency (IF) receiver outputs onto either one or two lanes of Subclass 1 JESD204B-based, high speed serialized outputs, depending on the decimation ratio and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF±, SYNCINB±AB, and SYNCINB±CD input pins.

The AD9694-EP has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using the 1.8 V capable, 3-wire serial port interface (SPI).

The AD9694-EP is available in a Pb-free, 72-lead LFCSP and is specified over the −55°C to +105°C ambient temperature range.

Additional application and technical information can be found in the AD9694 data sheet.

PRODUCT HIGHLIGHTS

1. Low power consumption per channel.
2. JESD204B lane rate support up to 15 Gbps.
3. Wide full power bandwidth supports IF sampling of signals up to 1.4 GHz.
4. Buffered inputs ease filter design and implementation.
5. Four integrated wideband decimation filters and NCO blocks supporting multiband receivers.
6. Programmable fast overrange detection.
7. On-chip temperature diode for system thermal management.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, and analog input (A_{IN}) = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_A range of −55°C to +105°C. Typical specifications represent performance at T_A = 25°C.

Table 1. DC Specifications

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
ACCURACY				
No Missing Codes		Guaranteed		
Offset Error		0		% FSR
Offset Matching		0		% FSR
Gain Error	16		24	% FSR
Gain Matching		1.0	3.7	% FSR
Differential Nonlinearity (DNL)	−0.7	±0.4	+0.7	LSB
Integral Nonlinearity (INL)	−5.1	±1.0	+5.1	LSB
TEMPERATURE DRIFT				
Offset Error		8		ppm/°C
Gain Error		214		ppm/°C
INTERNAL VOLTAGE REFERENCE		0.5		V
INPUT REFERRED NOISE		2.6		LSB RMS
ANALOG INPUTS				
Differential Input Voltage Range (Programmable)	1.44	1.80	2.16	V p-p
Common-Mode Voltage (V_{CM})		1.34		V
Differential Input Capacitance[1]		1.75		pF
Differential Input Resistance		200		Ω
Analog Input Full Power Bandwidth		1.4		GHz
POWER SUPPLY				
AVDD1	0.95	0.975	1.00	V
AVDD1_SR	0.95	0.975	1.00	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
DVDD	0.95	0.975	1.00	V
DRVDD1	0.95	0.975	1.00	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD	1.71	1.8	1.89	V
AVDD1 Current (I_{AVDD1})		319	482	mA
AVDD1_SR Current (I_{AVDD1_SR})		21	53	mA
AVDD2 Current (I_{AVDD2})		438	473	mA
AVDD3 Current (I_{AVDD3})		87	103	mA
DVDD Current (I_{DVDD})[2]		121	180	mA
DRVDD1 Current (I_{DRVDD1})[1]		162	207	mA
DRVDD2 Current (I_{DRVDD2})[1]		23	29	mA
SPIVDD Current (I_{SPIVDD})		1	1.6	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)[2]		1.66	2.07	W
Power-Down Dissipation		325		mW
Standby[3]		1.20		W

SPECIFICATIONS

[1] All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.

[2] Full bandwidth mode.

[3] Standby mode is controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, and A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_A range of −55°C to +105°C. Typical specifications represent performance at T_A = 25°C.

Table 2. 500 MSPS AC Specifications

	A_{IN} Full Scale = 1.44 V p-p			A_{IN} Full Scale = 1.80 V p-p			A_{IN} Full Scale = 2.16 V p-p			
Parameter[1]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE		1.44			1.80			2.16		V p-p
NOISE DENSITY[2]		−149.7			−151.5			−153.0		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]										
Input frequency (f_{IN}) = 10 MHz		65.4			67.1			68.4		dBFS
f_{IN} = 155 MHz		65.3		64.8	67.0			68.3		dBFS
f_{IN} = 305 MHz		65.2			66.8			68.0		dBFS
f_{IN} = 450 MHz		65.0			66.6			67.8		dBFS
f_{IN} = 765 MHz		64.8			66.5			67.5		dBFS
f_{IN} = 985 MHz		64.5			66.0			66.9		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)										
f_{IN} = 10 MHz		65.3			67.0			68.2		dBFS
f_{IN} = 155 MHz		65.2		64.5	66.8			67.9		dBFS
f_{IN} = 305 MHz		65.1			66.6			67.6		dBFS
f_{IN} = 450 MHz		65.0			66.4			67.3		dBFS
f_{IN} = 765 MHz		64.7			66.1			66.9		dBFS
f_{IN} = 985 MHz		64.2			65.5			66.2		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)										
f_{IN} = 10 MHz		10.5			10.8			11.0		Bits
f_{IN} = 155 MHz		10.5		10.4	10.8			10.9		Bits
f_{IN} = 305 MHz		10.5			10.7			10.9		Bits
f_{IN} = 450 MHz		10.5			10.7			10.8		Bits
f_{IN} = 765 MHz		10.4			10.6			10.8		Bits
f_{IN} = 985 MHz		10.3			10.6			10.7		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)										
f_{IN} = 10 MHz		89			90			80		dBFS
f_{IN} = 155 MHz		89		75	85			77		dBFS
f_{IN} = 305 MHz		82			82			78		dBFS
f_{IN} = 450 MHz		82			83			77		dBFS
f_{IN} = 765 MHz		77			75			72		dBFS
f_{IN} = 985 MHz		82			79			76		dBFS
SFDR AT −3 dBFS										
f_{IN} = 10 MHz		94			94			86		dBFS
f_{IN} = 155 MHz		94			90			82		dBFS
f_{IN} = 305 MHz		89			90			83		dBFS
f_{IN} = 450 MHz		87			86			84		dBFS
f_{IN} = 765 MHz		82			80			77		dBFS

SPECIFICATIONS

Table 2. 500 MSPS AC Specifications (Continued)

Parameter[1]	A_{IN} Full Scale = 1.44 V p-p			A_{IN} Full Scale = 1.80 V p-p			A_{IN} Full Scale = 2.16 V p-p			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{IN} = 985 MHz		85			82			79		dBFS
WORST HARMONIC, SECOND OR THIRD										
f_{IN} = 10 MHz		−89			−90			−80		dBFS
f_{IN} = 155 MHz		−89			−85	−75		−77		dBFS
f_{IN} = 305 MHz		−82			−82			−78		dBFS
f_{IN} = 450 MHz		−82			−83			−77		dBFS
f_{IN} = 765 MHz		−77			−75			−72		dBFS
f_{IN} = 985 MHz		−82			−79			−76		dBFS
WORST HARMONIC, SECOND OR THIRD AT −3 dBFS										
f_{IN} = 10 MHz		−94			−94			−86		dBFS
f_{IN} = 155 MHz		−94			−90			−82		dBFS
f_{IN} = 305 MHz		−89			−90			−83		dBFS
f_{IN} = 450 MHz		−87			−86			−84		dBFS
f_{IN} = 765 MHz		−82			−80			−77		dBFS
f_{IN} = 985 MHz		−85			−82			−79		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC										
f_{IN} = 10 MHz		−96			−98			−99		dBFS
f_{IN} = 155 MHz		−97			−97	−86		−97		dBFS
f_{IN} = 305 MHz		−97			−98			−97		dBFS
f_{IN} = 450 MHz		−95			−96			−96		dBFS
f_{IN} = 765 MHz		−92			−91			−88		dBFS
f_{IN} = 985 MHz		−90			−89			−86		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS										
f_{IN1} = 154 MHz and f_{IN2} = 157 MHz		−93			−90			−84		dBFS
f_{IN1} = 302 MHz and f_{IN2} = 305 MHz		−90			−90			−84		dBFS
CROSSTALK[4]		82			82			82		dB
FULL POWER BANDWIDTH[3]		1.4			1.4			1.4		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

[2] Noise density is measured at a low A_{IN} frequency (30 MHz).

[3] See the AD9694 data sheet for more details.

[4] Crosstalk is measured at 155 MHz with a −1.0 dBFS A_{IN} on one channel and no input on the adjacent channel.

Table 3. 600 MSPS AC Specifications, A_{IN} = 1.80 V p-p

Parameter[1]	Min	Typ	Max	Unit
A_{IN} FULL SCALE		1.80		V p-p
SNR				
f_{IN} = 10 MHz		66.6		dBFS
f_{IN} = 155 MHz		67		dBFS
f_{IN} = 305 MHz		66.8		dBFS
f_{IN} = 450 MHz		66.4		dBFS
f_{IN} = 765 MHz		66		dBFS
f_{IN} = 985 MHz		65.5		dBFS
SINAD				
f_{IN} = 10 MHz		66.5		dBFS

SPECIFICATIONS

Table 3. 600 MSPS AC Specifications, A_{IN} = 1.80 V p-p (Continued)

Parameter[1]	Min	Typ	Max	Unit
f_{IN} = 155 MHz		66.8		dBFS
f_{IN} = 305 MHz		66.5		dBFS
f_{IN} = 450 MHz		66.3		dBFS
f_{IN} = 765 MHz		65.4		dBFS
f_{IN} = 985 MHz		64.8		dBFS
SFDR				
f_{IN} = 10 MHz		86		dBFS
f_{IN} = 155 MHz		81		dBFS
f_{IN} = 305 MHz		81		dBFS
f_{IN} = 450 MHz		84		dBFS
f_{IN} = 765 MHz		76		dBFS
f_{IN} = 985 MHz		75		dBFS
WORST HARMONIC, SECOND OR THIRD				
f_{IN} = 10 MHz		−86		dBFS
f_{IN} = 155 MHz		−81		dBFS
f_{IN} = 305 MHz		−81		dBFS
f_{IN} = 450 MHz		−84		dBFS
f_{IN} = 765 MHz		−76		dBFS
f_{IN} = 985 MHz		−75		dBFS

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

Table 4. 600 MSPS Power Consumption

Parameter	Min	Typ	Max	Unit
POWER SUPPLY				
AVDD1	0.95	0.975	1.00	V
AVDD1_SR	0.95	0.975	1.00	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
DVDD	0.95	0.975	1.00	V
DRVDD1	0.95	0.975	1.00	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD	1.71	1.8	1.89	V
I_{AVDD1}		352	513	mA
I_{AVDD1_SR}		23	55	mA
I_{AVDD2}		443	478	mA
I_{AVDD3}		87	104	mA
I_{DVDD}[1]		146	200	mA
I_{DRVDD1}[2]		183	235	mA
I_{DRVDD2}		23	28	mA
I_{SPIVDD}		1	1.6	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)		1.75	2.16	W

[1] Full bandwidth mode.

[2] All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.

SPECIFICATIONS

DIGITAL SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_A range of −55°C to +105°C. Typical specifications represent performance at T_A = 25°C.

Table 5. Digital Specifications

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+AND CLK−)				
Logic Compliance		LVDS/LVPECL[1]		
Differential Input Voltage	600	800	1600	mV p-p
Input Common-Mode Voltage		0.69		V
Input Resistance (Differential)		32		kΩ
Input Capacitance			0.9	pF
SYSTEM REFERENCE INPUTS (SYSREF±)[2]				
Logic Compliance		LVDS/LVPECL[1]		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		kΩ
Input Capacitance (Single-Ended per Pin)		0.7		pF
LOGIC INPUTS (PDWN/STBY)				
Logic Compliance		CMOS[3]		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		10		MΩ
LOGIC INPUTS (SDIO, SCLK, AND CSB)				
Logic Compliance		CMOS[3]		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		56		kΩ
LOGIC OUTPUT (SDIO)				
Logic Compliance		CMOS[3]		
Logic 1 Voltage (I_{OH} = 800 µA)	SPIVDD − 0.45 V			V
Logic 0 Voltage (I_{OL} = 50 µA)	0		0.45	V
SYNCIN INPUT (SYNCINB±AB AND SYNCINB±CD)				
Logic Compliance		LVDS/LVPECL/CMOS[1, 3]		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		kΩ
Input Capacitance (Single Ended per Pin)		0.7		pF
LOGIC OUTPUTS (FD_A, FD_B, FD_C, AND FD_D)				
Logic Compliance		CMOS[3]		
Logic 1 Voltage	0.8 × SPIVDD			V
Logic 0 Voltage	0		0.5	V
Input Resistance		56		kΩ
DIGITAL OUTPUTS (SERDOUTABx± AND SERDOUTCDx±, x = 0 OR 1)				
Logic Compliance		CML[4]		
Differential Output Voltage		455.8		mV p-p
Short-Circuit Current ($I_{D\ SHORT}$)		15		mA
Differential Termination Impedance		100		Ω

SPECIFICATIONS

[1] LVDS is low voltage differential signaling, and LVPECL is low voltage positive emitter-coupled logic.

[2] DC-coupled input only.

[3] CMOS is a complementary metal–oxide semiconductor.

[4] CML is current mode logic.

SWITCHING SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, and A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_A range of −55°C to +105°C. Typical specifications represent performance at T_A = 25°C.

Table 6. Switching Specifications

Parameter	Min	Typ	Max	Unit
CLOCK				
Clock Rate at CLK+ and CLK− Pins	0.3		2.4	GHz
Maximum Sample Rate[1]	600			MSPS
Minimum Sample Rate[2]	240			MSPS
Clock Pulse Width High	125			ps
Clock Pulse Width Low	125			ps
OUTPUT				
Unit Interval (UI)[3]	66.67	100	593	ps
Rise Time (t_R), 20% to 80% into 100 Ω Load		31.25		ps
Fall Time (t_F), 20% to 80% into 100 Ω Load		31.37		ps
Phase-Locked Loop (PLL) Lock Time		5		ms
Data Rate per Channel (Nonreturn to Zero (NRZ))[4]	1.6875	10	15	Gbps
LATENCY[5]				
Pipeline Latency		54		Sample clock cycles
Fast Detect Latency			30	Sample clock cycles
WAKE-UP TIME				
From Standby		3		ms
From Power-Down		10		ms
APERTURE				
Aperture Delay (t_A)		160		ps
Aperture Uncertainty (Jitter, t_j)		44		fs rms
Out of Range Recovery Time		1		Sample clock cycles

[1] The maximum sample rate is the clock rate after the divider.

[2] The minimum sample rate operates at 240 MSPS with number of lanes (L) = 2 or L = 1. See SPI Register 0x011A in the AD9694 data sheet to reduce the threshold of the clock detection circuit.

[3] Baud rate = 1/UI. A subset of this range can be supported.

[4] Default L = 2 for each link. This number can be changed based on the sample rate and decimation ratio.

[5] No DDCs used. L = 2, number of converters (M) = 2, and number of octets/frames (F) = 2 for each link.

TIMING SPECIFICATIONS

Table 7. Timing Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 3				
t_{SU_SR}	Device clock to SYSREF+ setup time		−44.8		ps
t_{H_SR}	Device clock to SYSREF+ hold time		64.4		ps

SPECIFICATIONS

Table 7. Timing Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

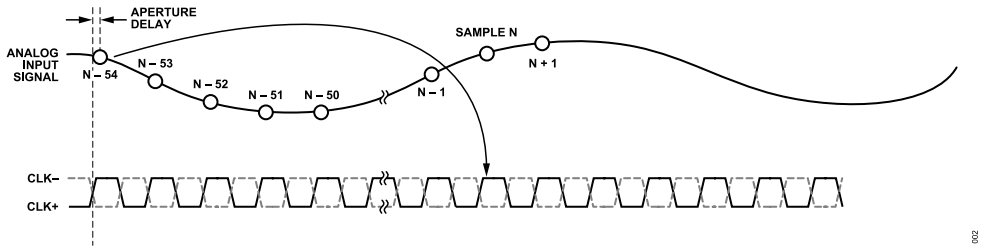


Figure 2. Data Output Timing (Full Bandwidth Mode, L = 4, M = 2, and F = 1)

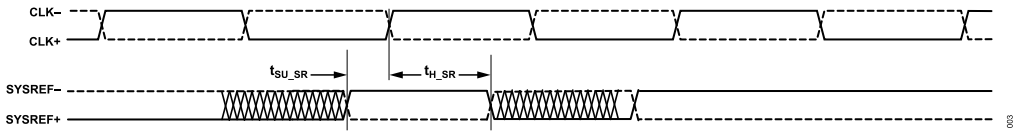


Figure 3. SYSREF± Setup and Hold Timing

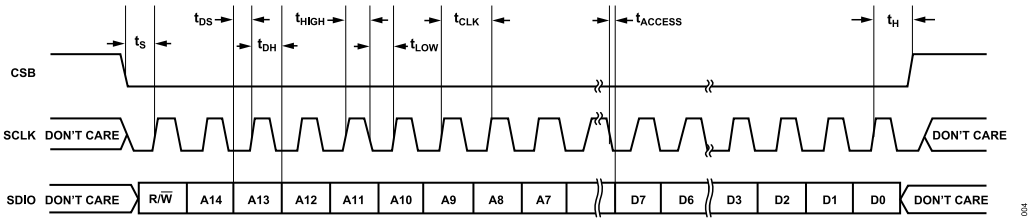


Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.00 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.00 V
SPIVDD to AGND	2.00 V
VIN±x to AGND	−0.3 V to AVDD3 + 0.3 V
CLK± to AGND	−0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	−0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND_SR	0 V to 2.5 V
SYNCINB±AB/SYNCINB±CD to DRGND	0 V to 2.5 V
Environmental	
Operating T_A Range	−55°C to +105°C
Maximum T_J	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, θ_{JC_BOT} is the bottom junction to case thermal resistance, ψ_{JT} is the junction-to-top thermal characterization, and ψ_{JB} is the junction-to-board thermal characterization.

Table 9. Thermal Resistance

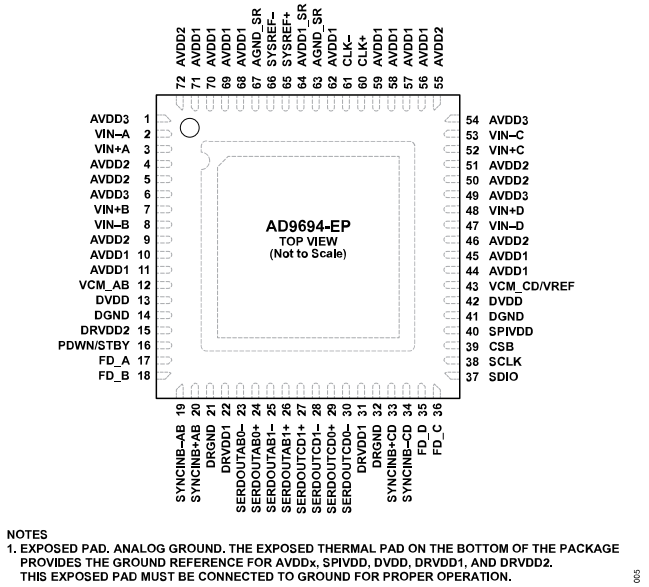
PCB Type	θ_{JA}	θ_{JC_BOT}	ψ_{JT}	ψ_{JB}	Unit
JEDEC					
2s2p Board	20.69[1]	0.41	0.07	6.75	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. ANALOG GROUND. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFERENCE FOR AVDDx, SPIVDD, DVDD, DRVDD1, AND DRVDD2. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 5. Pin Configuration (Top View)

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
0	AGND/EPAD	Ground	Exposed Pad. Analog Ground. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx, SPIVDD, DVDD, DRVDD1, and DRVDD2. This exposed pad must be connected to ground for proper operation.
1, 6, 49, 54	AVDD3	Supply	Analog Power Supply (2.5 V Nominal).
2, 3	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
4, 5, 9, 46, 50, 51, 55, 72	AVDD2	Supply	Analog Power Supply (1.8 V Nominal).
7, 8	VIN+B, VIN−B	Input	ADC B Analog Input True/Complement.
10, 11, 44, 45, 56 to 59, 62, 68 to 71	AVDD1	Supply	Analog Power Supply (0.975 V Nominal).
12	VCM_AB	Output	Common-Mode Level Bias Output for Analog Input Channel A and Channel B.
13, 42	DVDD	Supply	Digital Power Supply (0.975 V Nominal).
14, 41	DGND	Ground	Ground Reference for DVDD and SPIVDD.
15	DRVDD2	Supply	Digital Power Supply for JESD204B PLL (1.8 V Nominal).
16	PDWN/STBY	Input	Power-Down Input/Standby (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby. This pin requires an external 10 kΩ pull-down resistor.
17, 18, 35, 36	FD_A, FD_B, FD_D, FD_C	Output	Fast Detect Outputs for Channel A, Channel B, Channel C, and Channel D.
19	SYNCINB−AB	Input	Active Low JESD204B LVDS Sync Input Complement for Channel A and Channel B.
20	SYNCINB+AB	Input	Active Low JESD204B LVDS/CMOS Sync Input True for Channel A and Channel B.
21, 32	DRGND	Ground	Ground Reference for DRVDD1 and DRVDD2.
22, 31	DRVDD1	Supply	Digital Power Supply for SERDOUTABx±/SERDOUTCDx± Pins (0.975 V Nominal).
23, 24	SERDOUTAB0−, SERDOUTAB0+	Output	Lane 0 Output Data Complement/True for Channel A and Channel B.
25, 26	SERDOUTAB1−, SERDOUTAB1+	Output	Lane 1 Output Data Complement/True for Channel A and Channel B.
27, 28	SERDOUTCD1+, SERDOUTCD1−	Output	Lane 1 Output Data True/Complement for Channel C and Channel D.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type	Description
29, 30	SERDOUTCD0+, SERDOUTCD0−	Output	Lane 0 Output Data True/Complement for Channel C and Channel D.
33	SYNCINB+CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input True for Channel C and Channel D.
34	SYNCINB−CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input Complement for Channel C and Channel D.
37	SDIO	Input/output	SPI Serial Data Input/Output.
38	SCLK	Input	SPI Serial Clock.
39	CSB	Input	SPI Chip Select (Active Low).
40	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V Nominal).
43	VCM_CD/VREF	Output/input	Common-Mode Level Bias Output for Analog Input Channel C and Channel D/0.5 V Reference Voltage Input. This pin is configurable through the SPI as an output or an input. Use this pin as the common-mode level bias output if using the internal reference. This pin requires a 0.5 V reference voltage input if using an external voltage reference source.
47, 48	VIN−D, VIN+D	Input	ADC D Analog Input Complement/True.
52, 53	VIN+C, VIN−C	Input	ADC C Analog Input True/Complement.
60, 61	CLK+, CLK−	Input	Clock Input True/Complement.
63, 67	AGND_SR	Ground	Ground Reference for SYSREF±.
64	AVDD1_SR	Supply	Analog Power Supply for SYSREF± (0.975 V Nominal).
65, 66	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement. DC-coupled input only.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.80 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, and A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_A range of −55°C to +105°C. Typical specifications represent performance at T_A = 25°C. See the AD9694 data sheet for a full set of Typical Performance Characteristics plots.

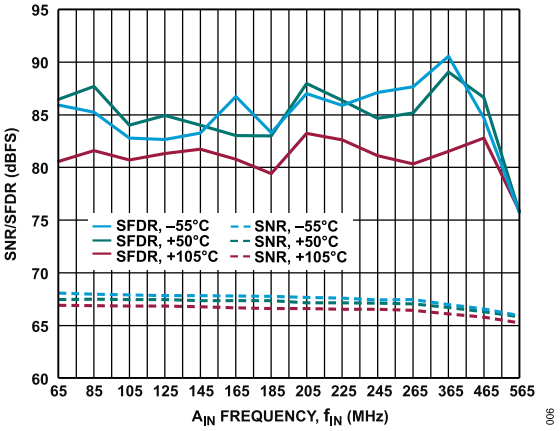


Figure 6. SNR/SFDR vs. A_{IN} Frequency (f_{IN})

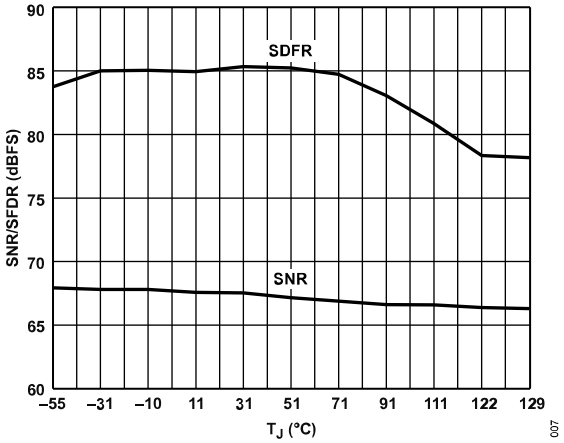


Figure 7. SNR/SFDR vs. T_J, f_{IN} = 155 MHz

OUTLINE DIMENSIONS

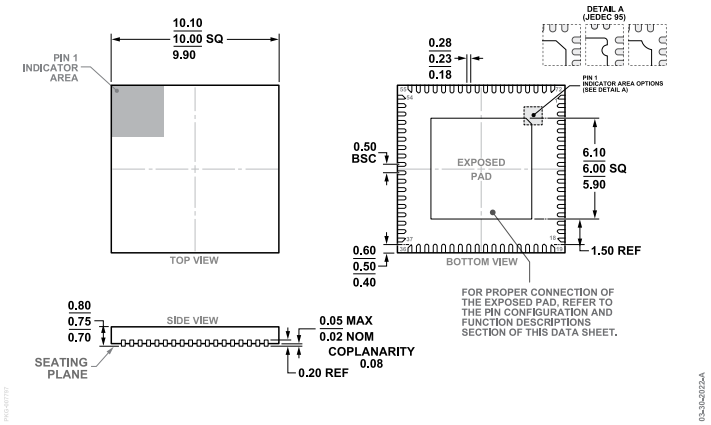


Figure 8. 72-Lead Lead Frame Chip Scale Package [LFCSP]
10 mm × 10 mm Body and 0.75 mm Package Height
(CP-72-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Ambient Temperature Range	Package Description	Package Option
AD9694TCPZ-500-EP	−55°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP]	CP-72-13

[1] Z = RoHS Compliant Part.