



High-Bandwidth, Low Voltage, Dual SPDT Analog Switch

FEATURES

- Single Supply (1.8 V to 5.5 V)
- Low On-Resistance - r_{ON} : 2.4 Ω
- Crosstalk and Off Isolation: -81 dB @ 1 MHz
- QFN-12 (3 x 3 mm) Package

BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- Low-Voltage Logic Compatible
- High Bandwidth

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Low-Voltage Data Acquisition
- ATE

DESCRIPTION

The DG2032 is a monolithic CMOS dual single-pole/double-throw (SPDT) analog switch. It is specifically designed for low-voltage, high bandwidth applications.

The DG2032's on-resistance (3 Ω @ 2.7 V), matching and flatness are guaranteed over the entire analog voltage range. Wide dynamic performance is achieved with better than -80 dB for both cross-talk and off-isolation at 1 MHz.

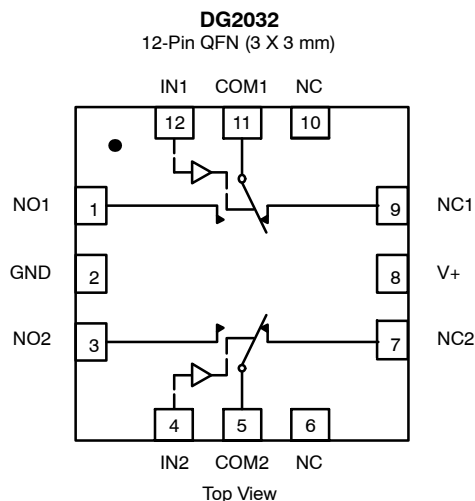
Both SPDT's operate with independent control logic, conduct equally well in both directions and block signals up to the

power supply level when off. Break-before-make is guaranteed.

With fast switching speeds, low on-resistance, high bandwidth, and low charge injection, the DG2032 is ideally suited for audio and video switching with high linearity.

Built on Vishay Siliconix's low voltage CMOS technology, the DG2032 contains an epitaxial layer which prevents latch-up.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	12-Pin QFN (3 x 3 mm)	DG2032DN



ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	 -0.3 to +6 V
IN, COM, NC, NO ^a	 -0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	 ± 50 mA
Peak Current	 ± 200 mA
(Pulsed at 1 ms, 10% duty cycle)	
Storage Temperature (D Suffix)	 -65 to 150°C
Power Dissipation (Packages) ^b	
12-Pin QFN (3 x 3) ^c	 1295 mW
Package Solder Reflow Conditions ^d	
12-Pin QFN (3 x 3)	 240°C

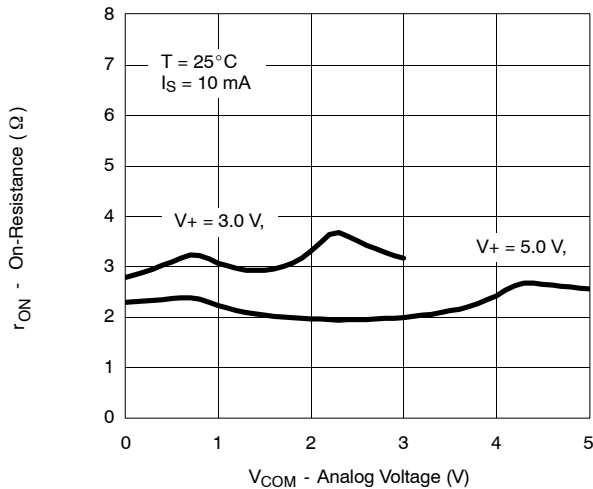
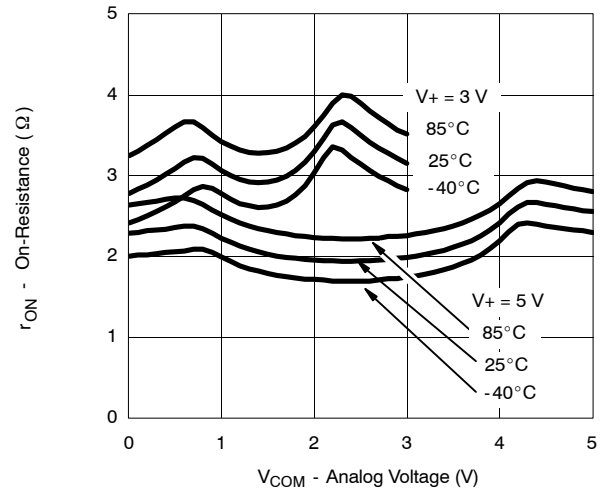
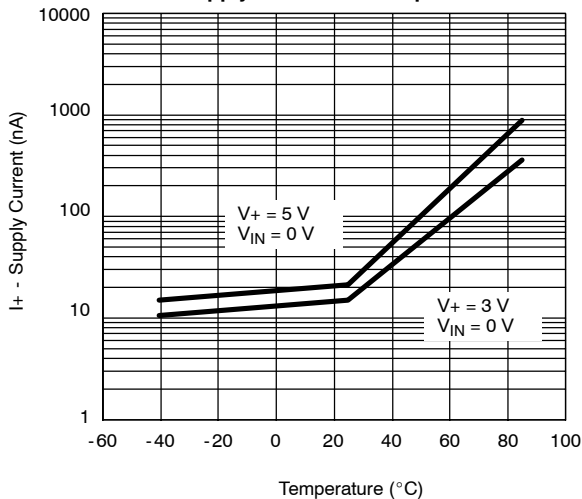
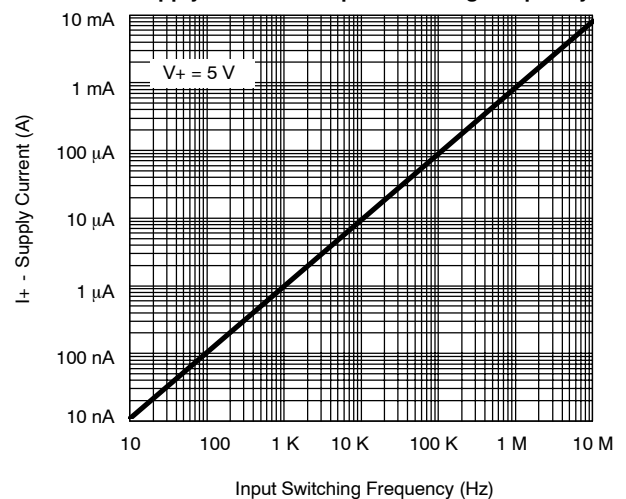
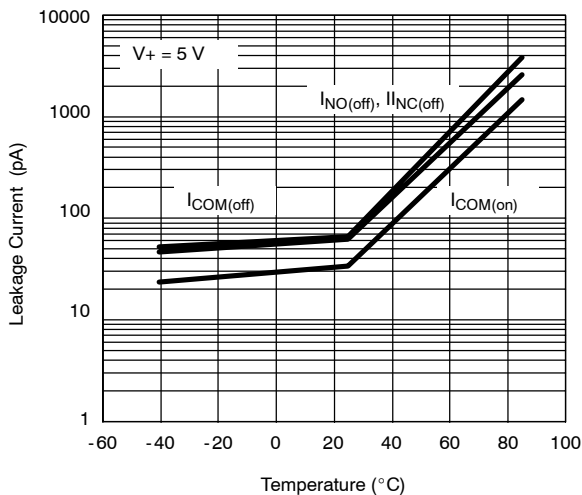
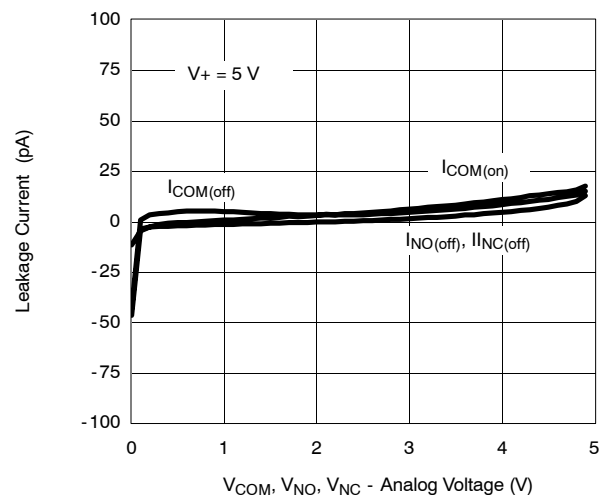
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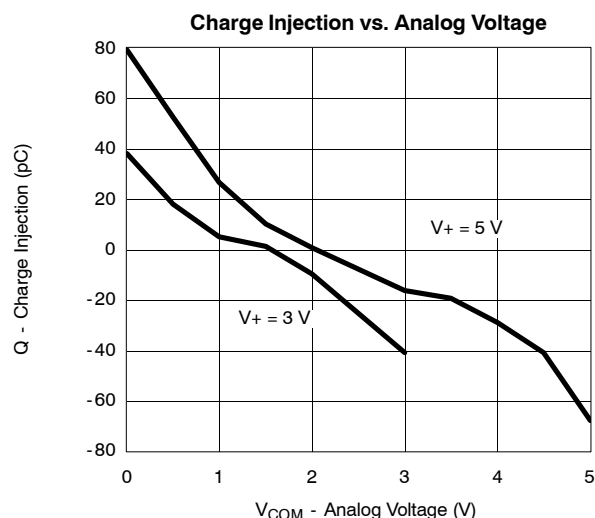
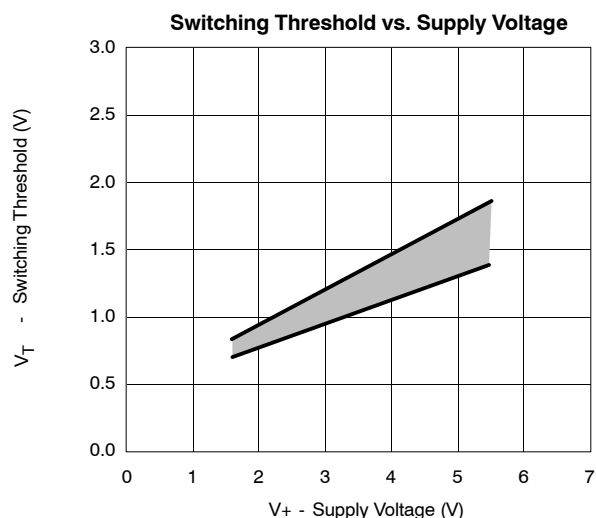
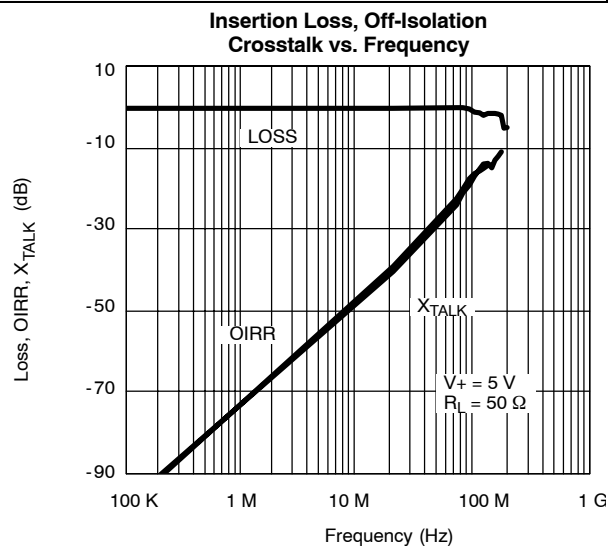
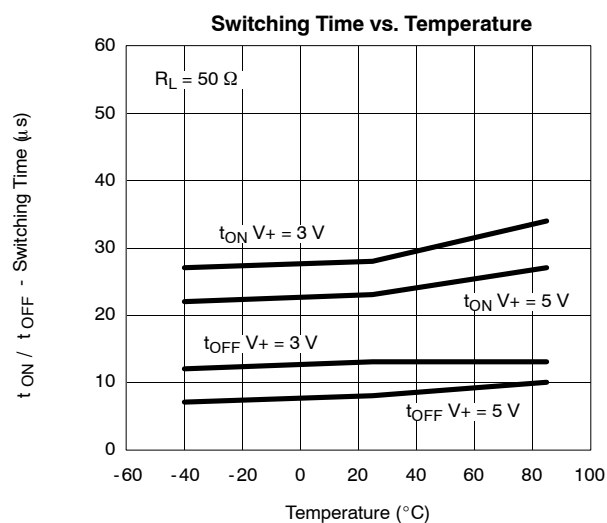
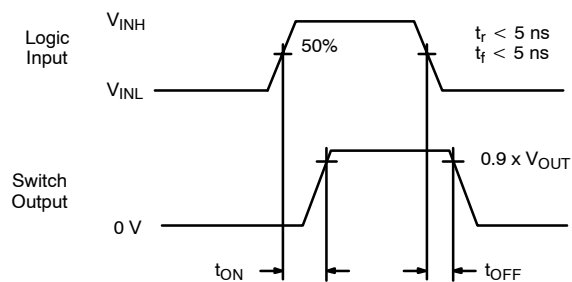
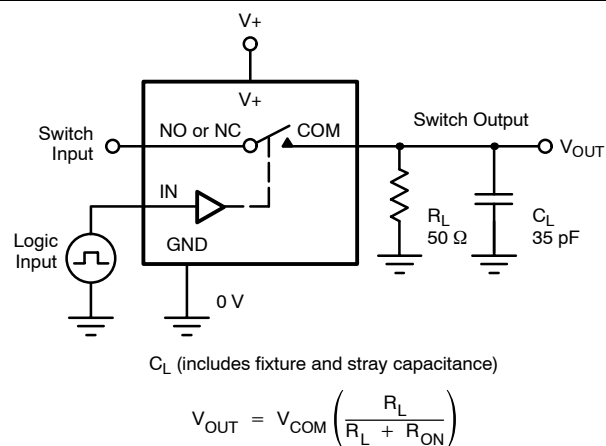
- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 16.2 mW/°C above 70°C
- Manual soldering with an iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10%, VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	VNO, VNC, VCOM		Full	0		V+	V
On-Resistance	rON	V+ = 2.7 V, VCOM = 0.2 V/1.5 V INO, INC = 10 mA	Room Full		3.0	5 6.5	Ω
rON Flatness	rON Flatness	V+ = 2.7 V VCOM = 0 to V+, INO, INC = 10 mA	Room			1.6	
rON Match Between Channels	ΔrON		Room			0.4	
Switch Off Leakage Current	INO(off), INC(off)	V+ = 3.3 V, VNO, VNC = 0.3 V/3 V VCOM = 3 V/0.3 V	Room Full	-1 -10	0.01	1 10	nA
	ICOM(off)		Room Full	-1 -10	0.01	1 10	
Channel-On Leakage Current	ICOM(on)	V+ = 3.3 V, VNO, VNC = VCOM = 0.3 V/3 V	Room Full	-1 -10	0.01	1 10	
Digital Control							
Input High Voltage	VINH		Full	2.0			V
Input Low Voltage	VINL		Full			0.4	
Input Capacitance	Cin		Full		5		pF
Input Current	IINL or IINH	VIN = 0 or V+	Full	1		1	μA
Dynamic Characteristics							
Turn-On Time	tON	VNO or VNC = 2.0 V, RL = 50 Ω, CL = 35 pF	Room Full		28	53 59	ns
Turn-Off Time	tOFF		Room Full		13	38 38	
Break-Before-Make Time	td	VNO or VNC = 2.0 V, RL = 50 Ω, CL = 35 pF	Full	1			
Charge Injection ^d	QINJ	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω	Room		38		pC
Off-Isolation ^d	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		-78		dB
Crosstalk ^d	XTALK		Room		-82		
NO, NC Off Capacitance ^d	CNO(off)	VIN = 0 or V+, f = 1 MHz	Room		15		pF
	CNC(off)		Room		15		
Channel-On Capacitance ^d	CNO(on)		Room		49		
	CNC(on)		Room		45		
Power Supply							
Power Supply Current	I+	VIN = 0 or V+	Full		0.01	1.0	μA

Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.

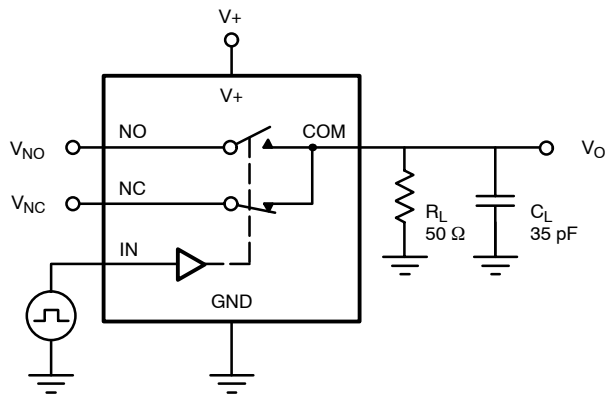
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)** **r_{ON} vs. V_{COM} and Supply Voltage** **r_{ON} vs. Analog Voltage and Temperature****Supply Current vs. Temperature****Supply Current vs. Input Switching Frequency****Leakage Current vs. Temperature****Leakage vs. Analog Voltage**

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

TEST CIRCUITS


Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

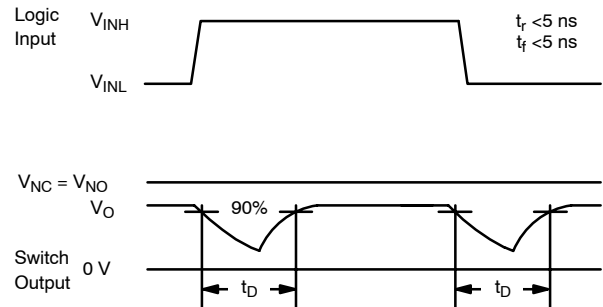
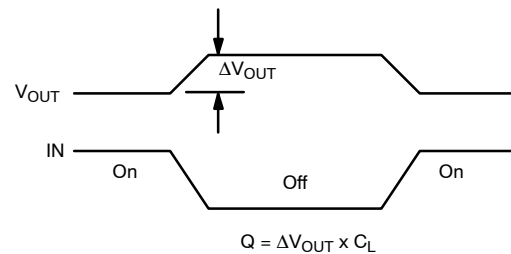
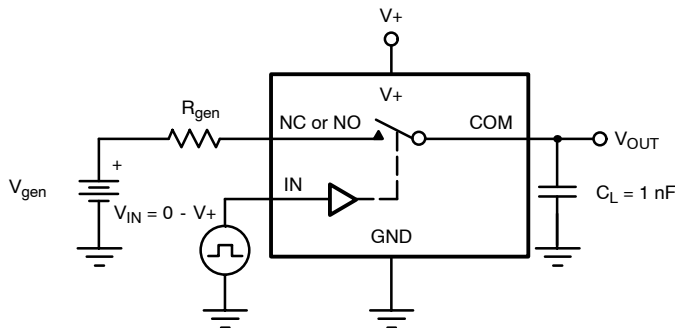


FIGURE 5. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection

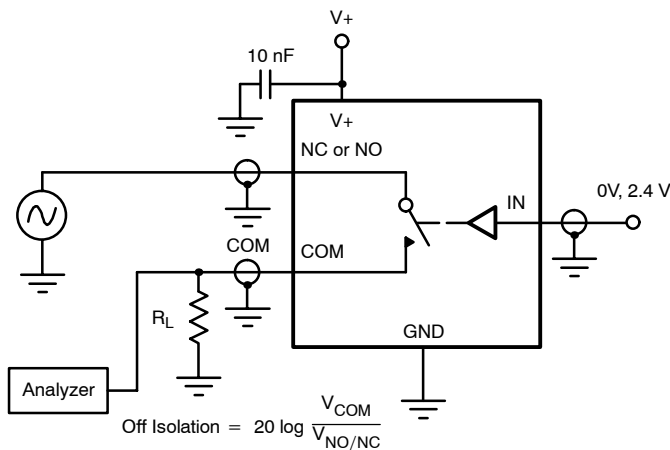


FIGURE 3. Off-Isolation

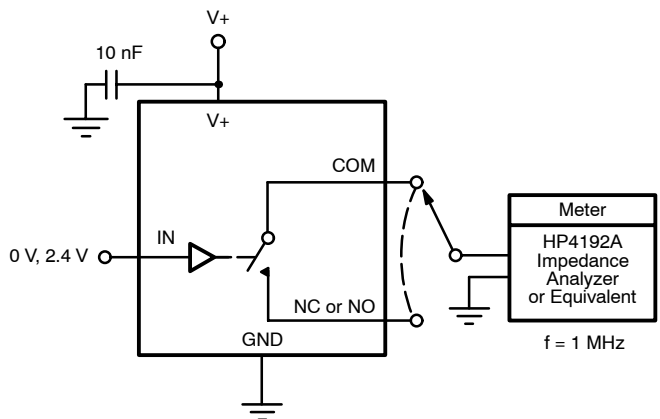


FIGURE 4. Channel Off/On Capacitance



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