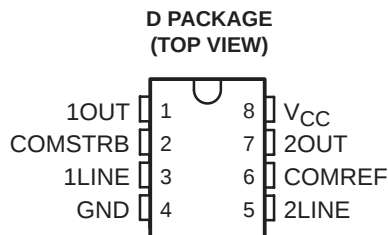


- Single 5-V Supply
- $\pm 100\text{-mV}$ Sensitivity
- For Application as:
 - Single-Ended Line Receiver
 - Gated Oscillator
 - Level Comparator
- Adjustable Reference Voltage
- TTL Outputs
- TTL-Compatible Strobe
- Designed for Party-Line (Data-Bus) Applications
- Common Reference-Voltage Pin
- Common Strobe



description/ordering information

This device consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 V to 3.4 V, making it possible to optimize noise immunity for a given system design. Due to the low input current (less than 100 μA), the device is suited ideally for party-line (data-bus) systems.

The SN74LS2323 has a common reference-voltage pin and a common strobe.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube	SN74LS2323D	LS2323
		Tape and reel	SN74LS2323DR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

(each receiver)

LINE INPUT	STROBE	OUTPUT
$\leq (V_{REF} - 100\text{ mV})$	L	H
$\geq (V_{REF} + 100\text{ mV})$	X	L
X	H	L

H = high level, L = low level, X = irrelevant



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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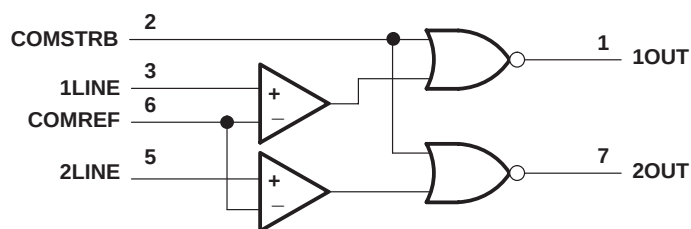
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SN74LS2323

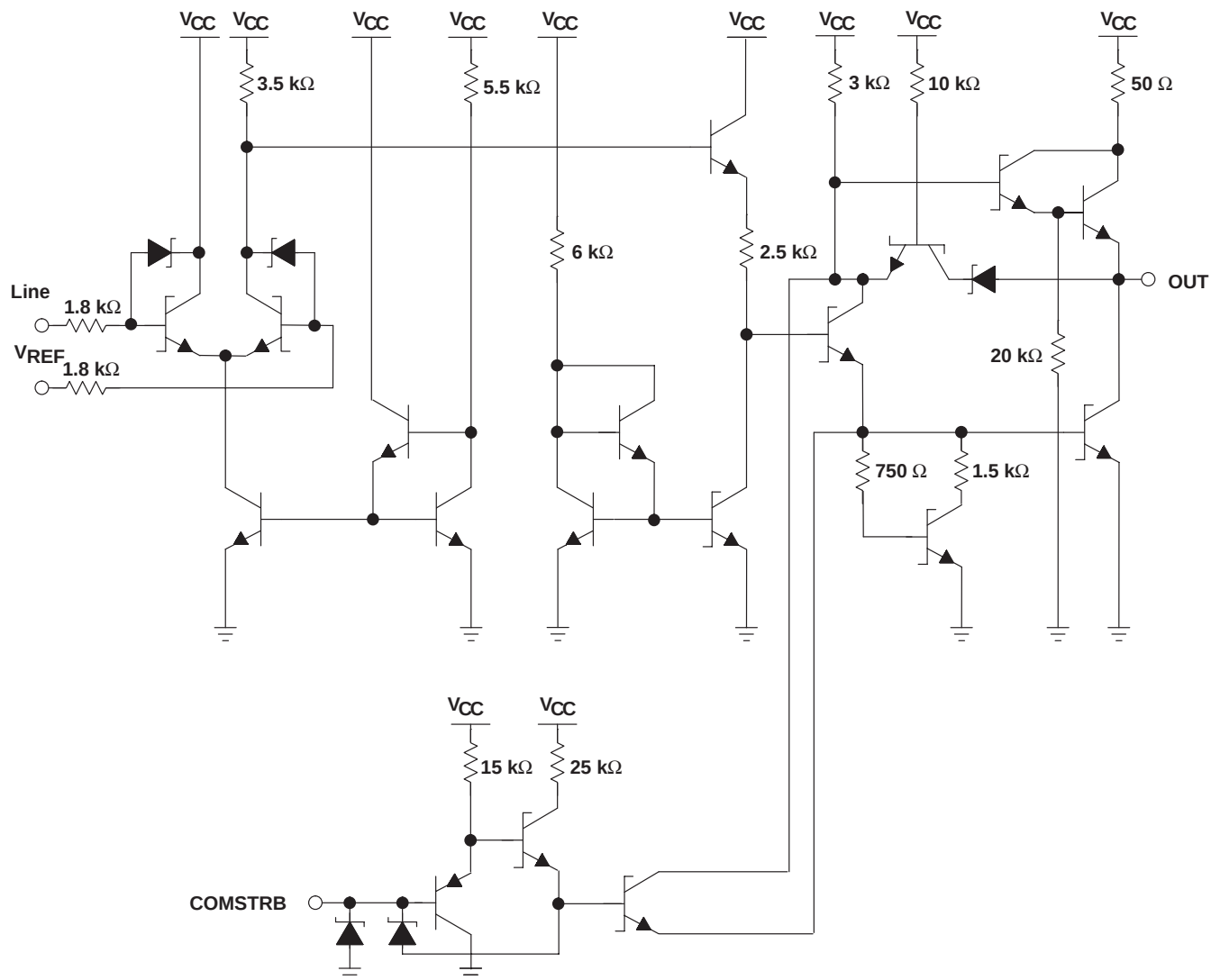
DUAL LINE RECEIVER

SDLS965 – OCTOBER 2004

logic diagram (positive logic)



schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Reference input voltage, V_{REF}	5.5 V
Line input voltage range with respect to GND	-2 V to 7 V
Line input voltage with respect to V_{REF}	± 5 V
Strobe input voltage, $V_{I(S)}$	7 V
Package thermal impedance, θ_{JA} (see Note 2)	97°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{Stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise specified, voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{ref}	Reference input voltage	1.8		[‡]	V
$V_{I(L)}$	High-level line input voltage	0		$V_{CC} - 1$	V
$V_{I(S)}$	High-level strobe input voltage	0		7	V
T_A	Operating free-air temperature range	0		70	°C

[‡] Max = $V_{CC} - 1.5$ V > $V_{REF} < 3.4$ V

SN74LS2323

DUAL LINE RECEIVER

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electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 10\%$, $V_{REF} = 1.5\text{ V to } 3.5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V _{IH(L)}	High-level line input voltage	V _{I(S)} = 0.8 V, I _{OL} = 12 mA, V _{REF} = 2.5 V, V _{OL} ≤ 0.6 V	V _{CC} = 4.5 V	2.62	6	V
		V _{I(S)} = 0.8 V, I _{OL} = 16 mA, V _{REF} = 3.4 V, V _{OL} ≤ 0.5 V	V _{CC} = 5.5 V	3.5	7	
V _{IL(L)}	Low-level line input voltage	V _{I(S)} = 0.8 V, I _{OH} = −0.4 mA, V _{REF} = 2.5 V, V _{OH} ≥ 2 V	V _{CC} = 4.5 V	−2	2.38	V
		V _{I(S)} = 0.8 V, I _{OH} = −0.4 mA, V _{REF} = 3.4 V, V _{OH} ≥ 3.2 V	V _{CC} = 5.5 V	−2	3.3	
V _{IH(S)}	High-level output control input voltage	V _{I(L)} = 1.8 V, V _{REF} = 2.5 V, V _O ≤ 0.4 V	V _{CC} = 4.5 V	2		V
V _{IL(S)}	Low-level output control input voltage	V _{I(L)} = 1.8 V, V _{REF} = 2.5 V, V _O ≥ 2.4 V	V _{CC} = 4.5 V		0.8	V
V _{OH}	High-level output voltage	V _{I(L)} = 1.4 V, V _{I(S)} = 0.8 V, I _{OH} = −1 mA, V _{REF} = 2.5 V	V _{CC} = 4.5 V	2		V
			V _{CC} = 5 V	2.7		
			V _{CC} = 5.5 V	2.7		
V _{OL}	Low-level output voltage	V _{I(L)} = 3.8 V, V _{I(S)} = 0.8 V, V _{REF} = 2.5 V	V _{CC} = 4.5 V, I _{OL} = 16 mA		0.6	V
			V _{CC} = 5 V, I _{OL} = 24 mA		0.5	
			V _{CC} = 5.5 V, I _{OL} = 24 mA		0.5	
I _{IH(S)}	High-level input current	V _{I(L)} = 3.8 V, V _{REF} = 2.5 V	V _{CC} = 5.5 V, V _{I(S)} = 2.4 V		20	μA
			V _{CC} = 5.5 V, V _{I(S)} = 7 V		100	
I _{IH(L)}	High-level input current	V _{I(S)} = 2.4 V, V _{REF} = 2.5 V	V _{CC} = 5 V, V _{I(L)} = 5 V		100	μA
			V _{CC} = 5 V, V _{I(L)} = 5.5 V		2	mA
I _{IH(REF)}	High-level input current	V _{I(S)} = 2.4 V, V _{REF} = 3.4 V	V _{CC} = 5.5 V, V _{I(L)} = 2.5 V		500	μA
I _{IL(S)}	Low-level input current	V _{I(L)} = 1.8 V, V _{REF} = 0.1 V	V _{CC} = 5.5 V, V _{I(S)} = 0.4 V		−400	μA
I _{IL(L)}	Low-level input current at Line input	V _{I(L)} = 0.1 V, V _{REF} = 1.8 V	V _{CC} = 5.5 V, V _{I(S)} = 0.4 V		−100	μA
I _{IL(REF)}	Low-level input current at REF pin	V _{I(L)} = 1.8 V, V _{REF} = 0.1 V	V _{CC} = 5.5 V, V _{I(S)} = 0.4 V		−100	μA
I _{OS}	Short-circuit output current [‡]	V _{I(L)} = 1.8 V, V _{REF} = 2.8 V	V _{CC} = 5.5 V V _{I(S)} = 0.4 V	−30	−130	mA
I _{CCH}	Supply current, output high	V _{I(S)} = 0, V _{CC} = 5.5 V V _{I(L)} = V _{REF} − 100 mV			12	mA
I _{CCL}	Supply current, output low	V _{I(S)} = 0, V _{CC} = 5.5 V V _{I(L)} = V _{REF} + 100 mV			16	mA

[†] Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.



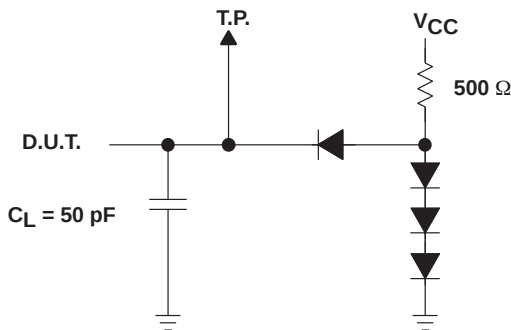
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switching characteristics, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{REF} = 2.5\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C

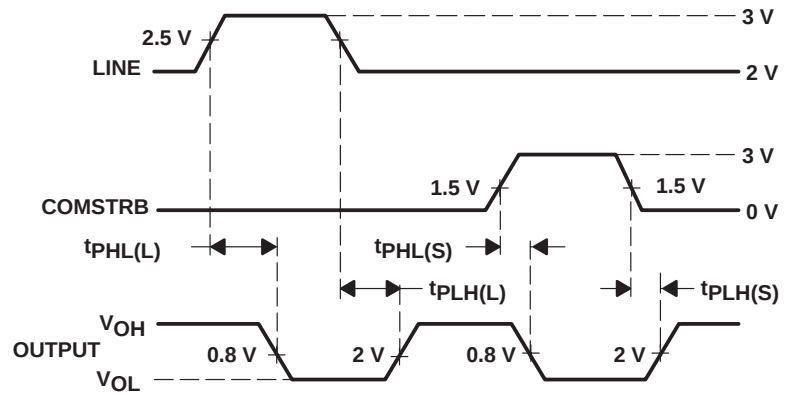
PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
$t_{PLH(L)}$ Propagation delay time, low- to high-level output from LINE	$C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, See Figure 1	10	25	35	ns
$t_{PHL(L)}$ Propagation delay time, high- to low-level output from LINE	$C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, See Figure 1	10	25	35	ns
$t_{PLH(S)}$ Propagation delay time, low- to high-level output from COMSTRB	$C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, See Figure 1		11	22	ns
$t_{PHL(S)}$ Propagation delay time, high- to low-level output from COMSTRB	$C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, See Figure 1		8	15	ns

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



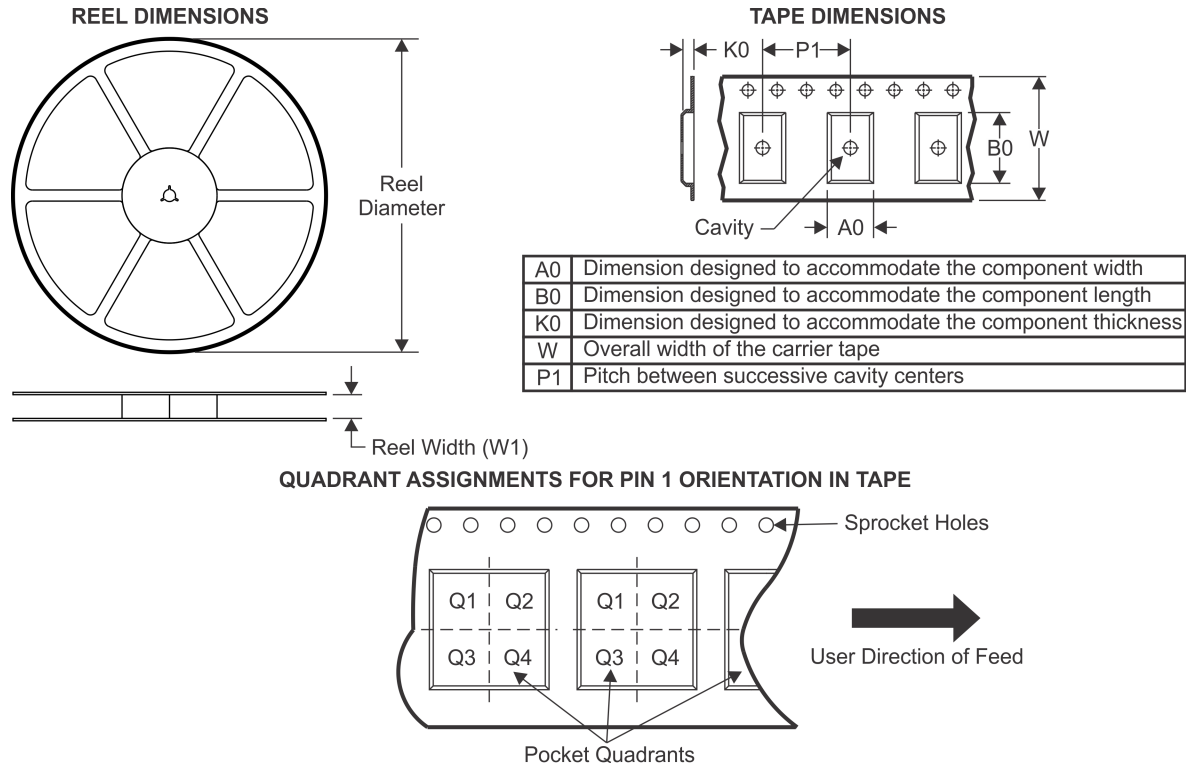
TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, t_r and $t_f \leq 2\text{ ns}$, and duty cycle = 50%.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N914 (or equivalent).
- D. The outputs are measured one at a time, with one input transition per measurement.

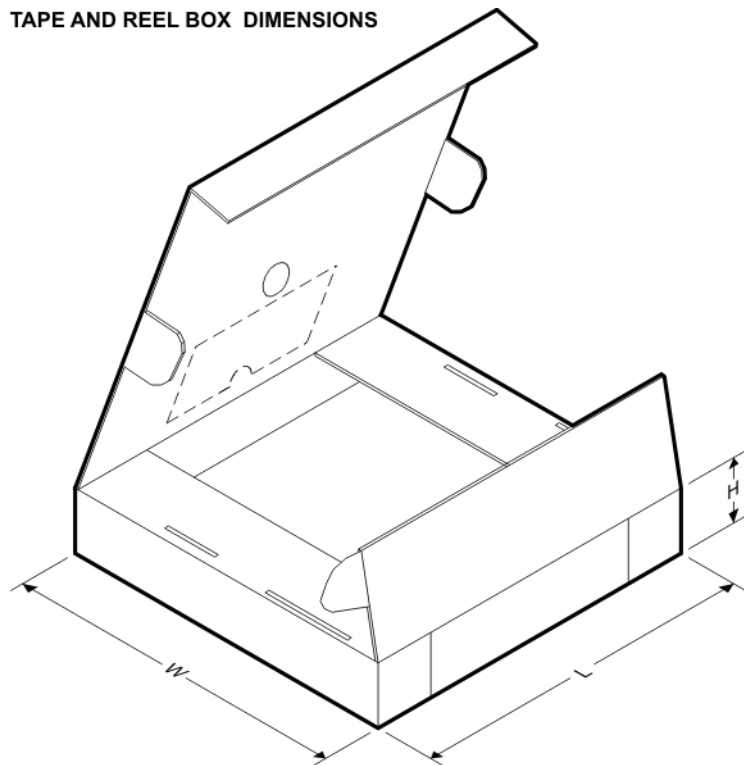
Figure 1. Load Circuit and Voltage Waveforms

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS2323DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS2323DR	SOIC	D	8	2500	340.5	336.1	25.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



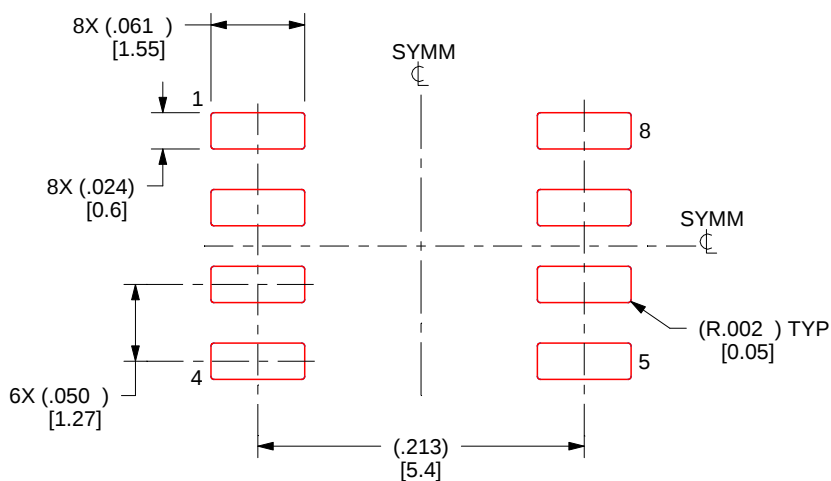
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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