National Semiconductor

T-46-09-05

MM54HC195/MM74HC195 4-Bit Parallel Shift Register

General Description

The MM54HC195/MM74HC195 is a high speed 4-bit SHIFT REGISTER utilizes advanced silicon-gate CMOS technology to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads at LS type speeds.

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, SHIFT/LOAD control input, and a direct overriding CLEAR. This shift register can operate in two modes: PARALLEL LOAD; SHIFT from Q_A towards Q_D.

Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/LOAD control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/LOAD control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or TOGGLE flip flop as shown in the truth table.

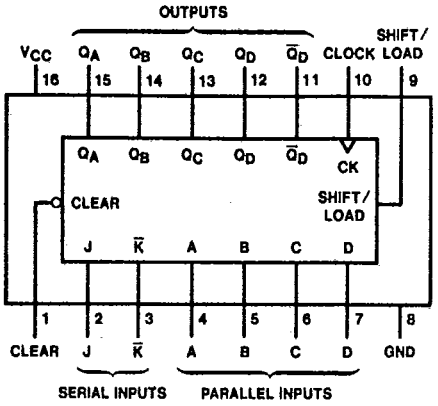
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: 16 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



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Top View

Order Number MM54HC195* or MM74HC195*

*Please look into Section 8, Appendix D for availability of various package types.

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent transition of the clock.

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

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AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		14	24	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		16	25	ns
t_{REM}	Minimum Removal Time, Shift/Load to Clock			0	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock			5	ns
t_S	Minimum Setup Time, (A, B, C, D, J, $\overline{K}$ to Clock)			20	ns
t_S	Minimum Setup Time, Shift/Load to Clock			20	ns
t_W	Minimum Pulse Width Clock or Reset			16	ns
t_H	Minimum Hold Time, any Input except Shift/Load			0	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 45 50	6 30 35	5 24 28	4 20 24	MHz MHz MHz
t_{PHL}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		2.0V 4.5V 6.0V	70 15 12	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	70 15 12	145 29 25	183 37 31	216 43 37	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_{REM}	Minimum Removal Time, Shift Load to Clock		2.0V 4.5V 6.0V	−2 −2 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock		2.0V 4.5V 6.0V		5 5 5	5 5 5	5 5 5	ns ns ns
t_S	Minimum Setup Time, (A, B, C, D, J, $\overline{K}$ to Clock)		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Setup Time, Shift/Load to Clock		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time any Input except Shift/Load		2.0V 4.5V 6.0V	−10 −2 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width, Clock or Reset		2.0V 4.5V 6.0V	30 10 9	80 16 14	100 20 18	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

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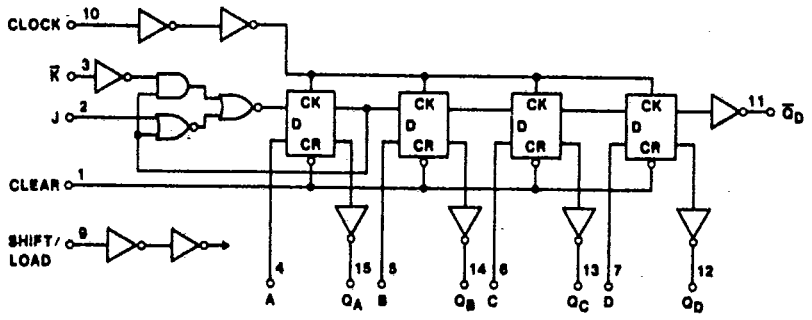
Logic and Timing Diagrams



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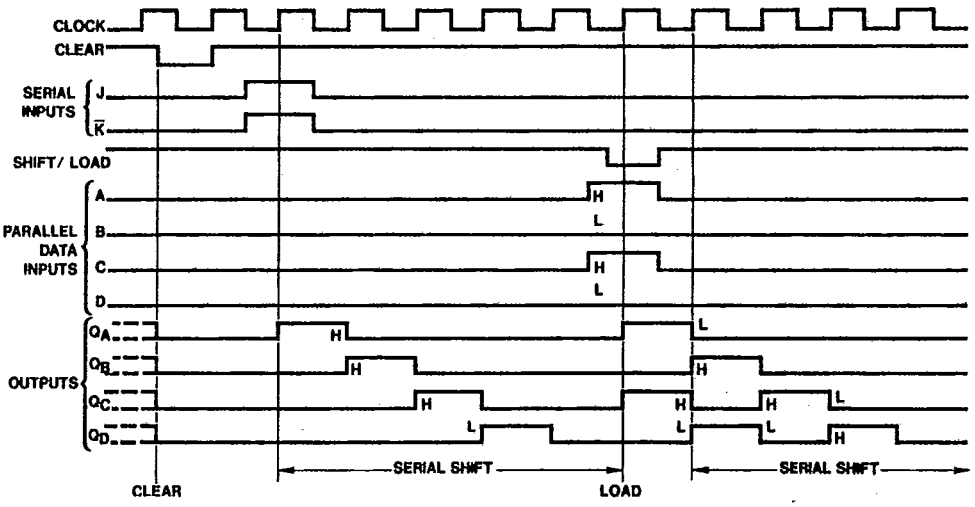

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