CD54AC139/3A
CD54ACT139/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays A0, A1 to Outputs	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4.4 3.2	131 14.7 10.5•	ns
$\bar{E}$ to Outputs	t_{PLH} t_{PHL}	1.5 3.3 5	— 1.9 1.6	131 14.7 10.5•	ns
Power Dissipation Capacitance	C_{PD}§	—	83 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays A0, A1 to Outputs	t_{PLH} t_{PHL}	5†	3.5	11.5•	ns
E to Outputs	t_{PLH} t_{PHL}	5	3.6	12•	ns
Power Dissipation Capacitance	C_{PD}§	—	83 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

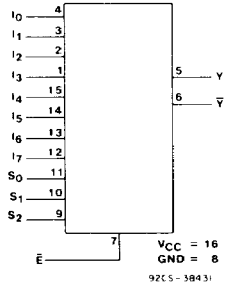
§C_{PD} is used to determine the dynamic power consumption per decoder/demultiplexer.
For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

CD54AC151/3A
CD54ACT151/3A

8-Input Multiplexer

The RCA CD54AC151/3A and CD54ACT151/3A are 8-input digital multiplexers that utilize the new RCA ADVANCED CMOS LOGIC technology. They have three binary control inputs (S0, S1, and S2) and an active-LOW Enable ($\bar{E}$) input. The three binary inputs select 1 of 8 channels. The output is both inverting ($\bar{Y}$) and non-inverting (Y).

The CD54AC151/3A and CD54ACT151/3A are supplied in 16-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Package Specifications

See Section 11, Fig. 11

CD54AC151/3A
CD54ACT151/3A

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				+25		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (MSI) I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
I (All)	1
$\overline{E}$	1
S	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

6

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54AC/ACT151	5,6	1-4,7-15	16	5,6	8	1-4,7,9-16
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	25 kHz
CD54AC/ACT151	1,3,7-9, 12-15	5,6	2,4,16	11	10	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54AC151/3A
CD54ACT151/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays Any Data to Y	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 3.5 2.3	169 18.9 13.5•	ns
Any Data to $\overline{Y}$	t_{PLH} t_{PHL}	1.5 3.3 5	— 3.8 2.5	186 20.9 14.9•	ns
Any Select to Y	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.7 3.1	228 25.5 18.2•	ns
Any Select to $\overline{Y}$	t_{PLH} t_{PHL}	1.5 3.3 5	— 5 3.4	245 27.4 19.6•	ns
Any $\overline{Enable}$ to Y	t_{PLH} t_{PHL}	1.5 3.3 5	— 3.2 2.1	153 17.1 12.2•	ns
Any $\overline{Enable}$ to $\overline{Y}$	t_{PLH} t_{PHL}	1.5 3.3 5	— 3.5 2.3	169 18.9 13.5•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Input Capacitance	C_I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays Any Data to Y	t_{PLH} t_{PHL}	5*	2.7	15.5•	ns
Any Data to $\overline{Y}$	t_{PLH} t_{PHL}	5	2.9	16.9•	ns
Any Select to Y	t_{PLH} t_{PHL}	5	3.5	20.2•	ns
Any Select to $\overline{Y}$	t_{PLH} t_{PHL}	5	3.7	21.6•	ns
Any $\overline{Enable}$ to Y	t_{PLH} t_{PHL}	5	2.1	12.1•	ns
Any $\overline{Enable}$ to $\overline{Y}$	t_{PLH} t_{PHL}	5	2.3	13.5•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Input Capacitance	C_I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§C_{PD} is used to determine the dynamic power consumption per device.
For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage