

HIGH-POWER & LOW-VOLTAGE AUDIO POWER AMPLIFIER

■ GENERAL DESCRIPTION

The **NJU7089** is an audio power amplifier designed for telephone applications. No external coupling capacitors are required because of the differential outputs. The closed loop gain is adjusted by two external resistors, and a SD pin permit power down with muting the input signal.

The **NJU7089** improves high output power compared with other amplifier.

■ PACKAGE OUTLINE



NJU7089R



NJU7089VC3



NJU7089KV1



NJU7089VP1

■ FEATURES

- Operating Voltage
- Operating Current
- Output Power
- Supply Current in Shutdown Mode
- Thermal Shutdown Circuit
- Pop Noise Suppression Circuit
- Over Current Protection Circuit
- C-MOS Technology
- Package Outline

$V^+ = 1.8$ to $5.5V$

$I_{DD1} = 3.0mA$ typ. ($V^+ = 5V, R_L = \infty$, no signal)

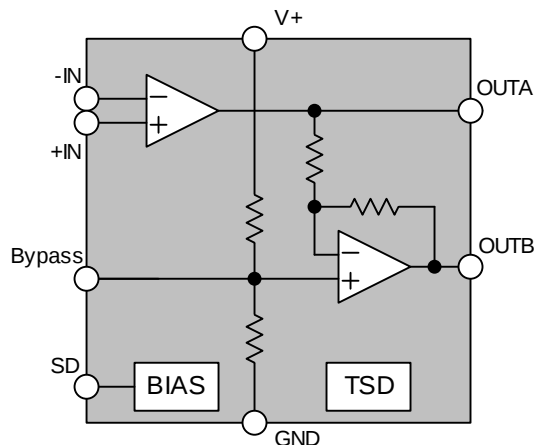
$I_{DD1} = 2.5mA$ typ. ($V^+ = 3V, R_L = \infty$, no signal)

$P_O = 1.2W$ typ. ($V^+ = 5V, R_L = 8\Omega, THD = 1\%$)

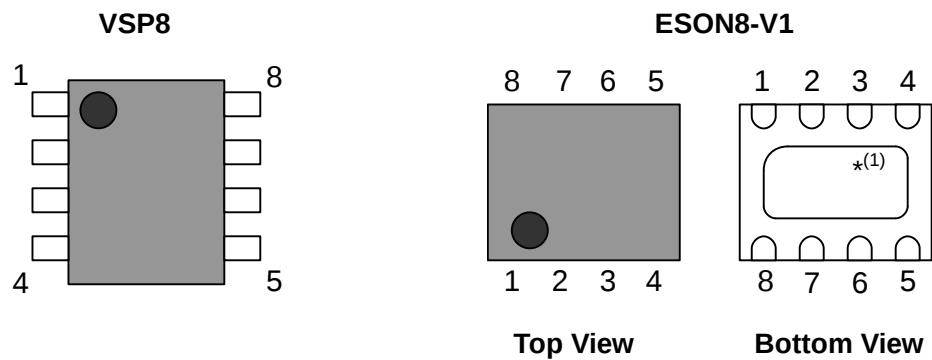
$P_O = 500mW$ typ. ($V^+ = 3.3V, R_L = 8\Omega, THD = 1\%$)

VSP8 / SSOP20-C3 / ESON8-V1 / HTSSOP24-P1

■ PIN CONFIGURATION & BLOCK DIAGRAM

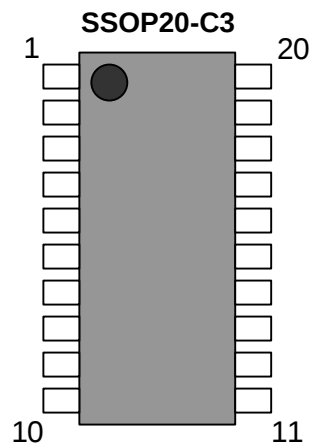


PIN CONFIGURATION

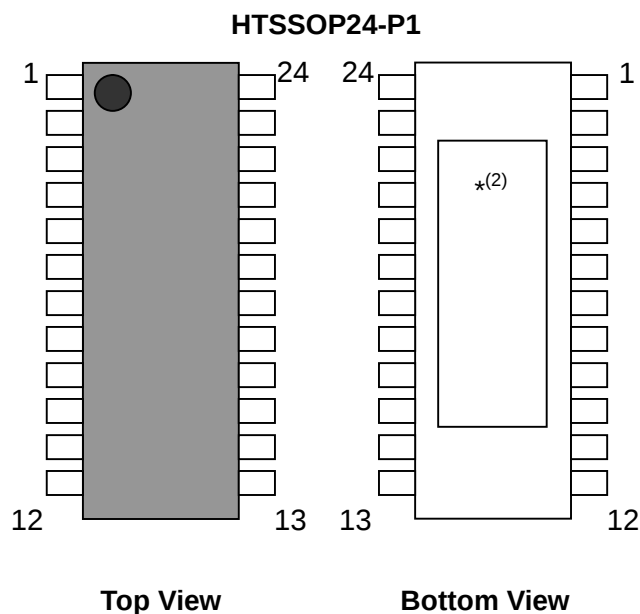


*(1) The PAD in the center part on the back is connected with the internal GND, therefore it connects to GND

No.	Symbol	Function
1	SD	Shutdown Enable
2	Bypass	Reference Voltage
3	+IN	Noninverted Input
4	-IN	Inverted Input
5	OUTA	Output A
6	V+	Supply Voltage
7	GND	Ground
8	OUTB	Output B



No.	Symbol	Function	No.	Symbol	Function
1	NC	No Connect	11	NC	No Connect
2	NC	No Connect	12	NC	No Connect
3	NC	No Connect	13	NC	No Connect
4	SD	Shutdown Enable	14	OUTA	Output A
5	Bypass	Reference Voltage	15	V+	Supply Voltage
6	+IN	Noninverted Input	16	GND	Ground
7	-IN	Inverted Input	17	OUTB	Output B
8	NC	No Connect	18	NC	No Connect
9	NC	No Connect	19	NC	No Connect
10	NC	No Connect	20	NC	No Connect



*(2) The PAD in the center part on the back is connected with the internal GND, therefore it connects to GND

No.	Symbol	Function	No.	Symbol	Function
1	NC	No Connect	13	NC	No Connect
2	NC	No Connect	14	NC	No Connect
3	NC	No Connect	15	NC	No Connect
4	NC	No Connect	16	NC	No Connect
5	SD	Shutdown Enable	17	OUTA	Output A
6	Bypass	Reference Voltage	18	V+	Supply Voltage
7	+IN	Noninverted Input	19	GND	Ground
8	-IN	Inverted Input	20	OUTB	Output B
9	NC	No Connect	21	NC	No Connect
10	NC	No Connect	22	NC	No Connect
11	NC	No Connect	23	NC	No Connect
12	NC	No Connect	24	NC	No Connect

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	+7	V
Power Dissipation	P _D	570 ^{*1)} / 770 ^{*2)} (VSP8) 970 ^{*1)} / 1400 ^{*2)} (SSOP20-C3) 570 ^{*3)} / 1700 ^{*4)} (ESON8-V1) 1000 ^{*5)} / 3000 ^{*6)} (HTSSOP24-P1)	mW
Output Peak Current	I _{op}	600	mA
Input Voltage Range	V _{IN}	-0.3 to V ⁺ +0.3 ^{*7)}	V
Operating Temperature Range	T _{opr}	-40 to +85	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

^{*1)} EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 2layers, FR-4) mounting.

^{*2)} EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 4layers, FR-4) mounting.

^{*3)} EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 2layers, FR-4) mounting. The PAD connecting to GND in the center part on the back

^{*4)} EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 4layers, FR-4, Applying a thermal via hole to a board based on JEDEC standard JESD51-5) mounting. The PAD connecting to GND in the center part on the back

^{*5)} EIA/JEDEC STANDARD Test board (114.5 x 101.5 x 1.6mm, 2layers, FR-4) mounting. The PAD connecting to GND in the center part on the back

^{*6)} EIA/JEDEC STANDARD Test board (114.5 x 101.5 x 1.6mm, 4layers, FR-4, Applying a thermal via hole to a board based on JEDEC standard JESD51-5) mounting. The PAD connecting to GND in the center part on the back

^{*7)} SD, IN⁺, IN⁻, OUTA, OUTB terminals.

■ RECOMMENDED OPERATING VOLTAGE RANGE (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V ⁺	-	1.8	3.0	5.5	V

■ ELECTRICAL CHARACTERISTICS

● Amplifier

(Ta=25°C, V⁺=5V, G_V=6dB, f=1kHz, R_L=8Ω, Active)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current 1	I _{DD1}	No signal, R _L =∞	-	3.0	6	mA
Operating Current 2	I _{DD2}	No signal, R _L =∞, V _{SD} =0.25V	-	-	2	μA
Output Power 1	P _{O1}	THD≤1%	0.9	1.2	-	W
Output Power 2	P _{O2}	V ⁺ =3.3V, THD≤1%	375	500	-	mW
Output Power 3	P _{O3}	V ⁺ =1.8V, THD≤1%	-	125	-	mW
Total Harmonic Distortion (THD+N)	THD+N	P _O =1W	-	0.1	-	%
Shutdown Attenuation	ATT _{SD}	V _{in} =1Vrms, Shutdown	-	-135	-	dB
Supply Voltage Rejection Ratio	PSRR	V _{ripple} =100mVrms	-	55	-	dB
Output Offset Voltage	V _{OD}	No signal	-	-	35	mV

(Ta=25°C, V⁺=3V, G_V=6dB, f=1kHz, R_L=8Ω, Active)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current 1	I _{DD1}	No signal, R _L =∞	-	2.5	4	mA
Operating Current 2	I _{DD2}	No signal, R _L =∞, V _{SD} =0.25V	-	-	2	μA
Total Harmonic Distortion (THD+N)	THD+N	P _O =400mW	-	0.1	-	%
Shutdown Attenuation	ATT _{SD}	V _{in} =500mVrms, Shutdown	-	-130	-	dB
Supply Voltage Rejection Ratio	PSRR	V _{ripple} =100mVrms	-	55	-	dB
Output Offset Voltage	V _{OD}	No signal	-	-	35	mV

V_{SD}: SD Terminal Voltage

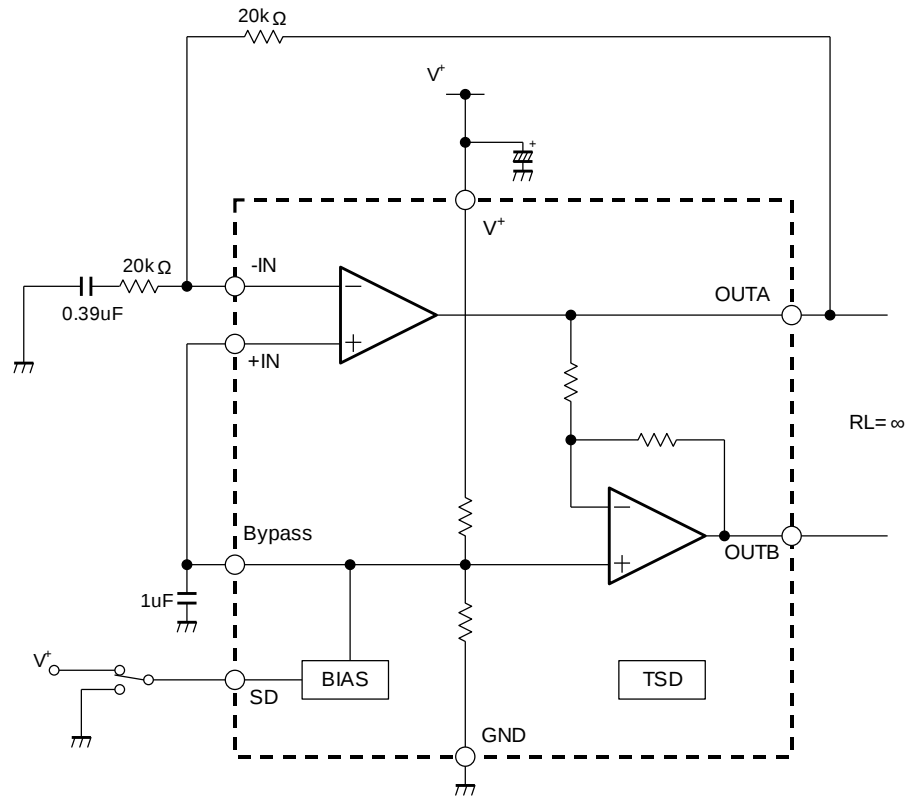
● Mode Control (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage	V_{IH}	-	1.5	-	V^+	V
Low Level Input Voltage	V_{IL}	-	0	-	0.25	

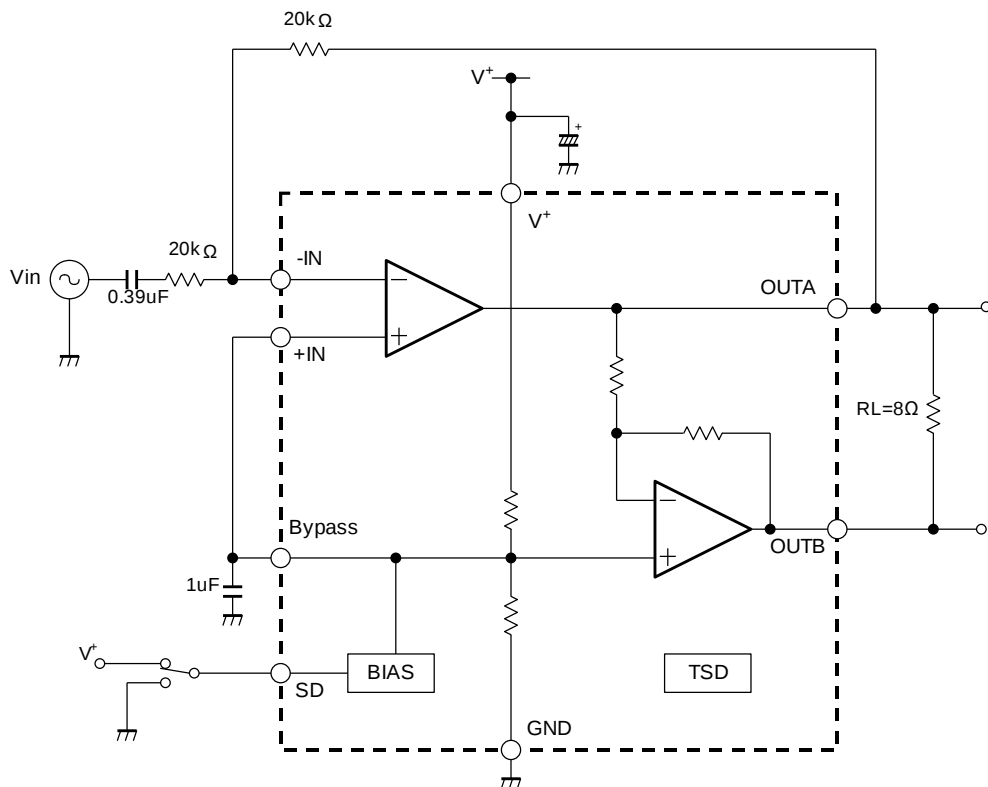
■ CONTROL TERMINAL EXPLANATION

MODE	CONTROL SIGNAL (SD Terminal)	STATUS
Shutdown	L(= V_{IL})	IC is standby.
Active	H(= V_{IH})	IC is active.

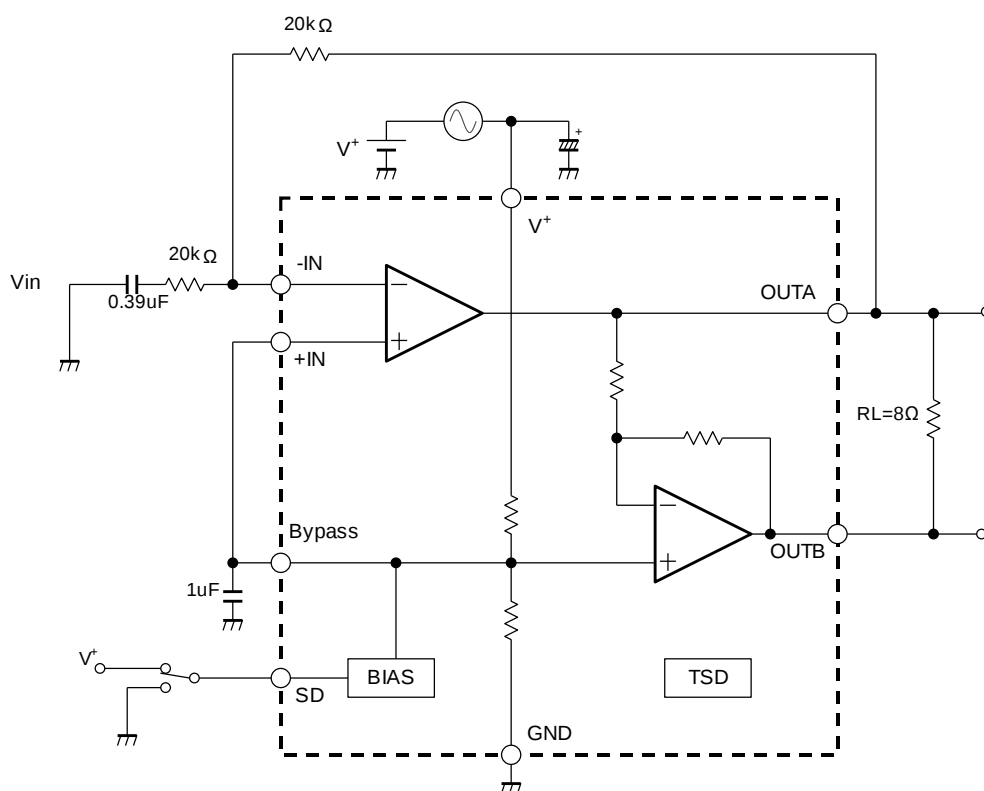
■ TEST CIRCUIT (I_{DD1} , I_{DD2} , V_{OD})



■ TEST CIRCUIT (P_{O1} , P_{O2} , P_{O3} , THD+N, ATT_{SD})



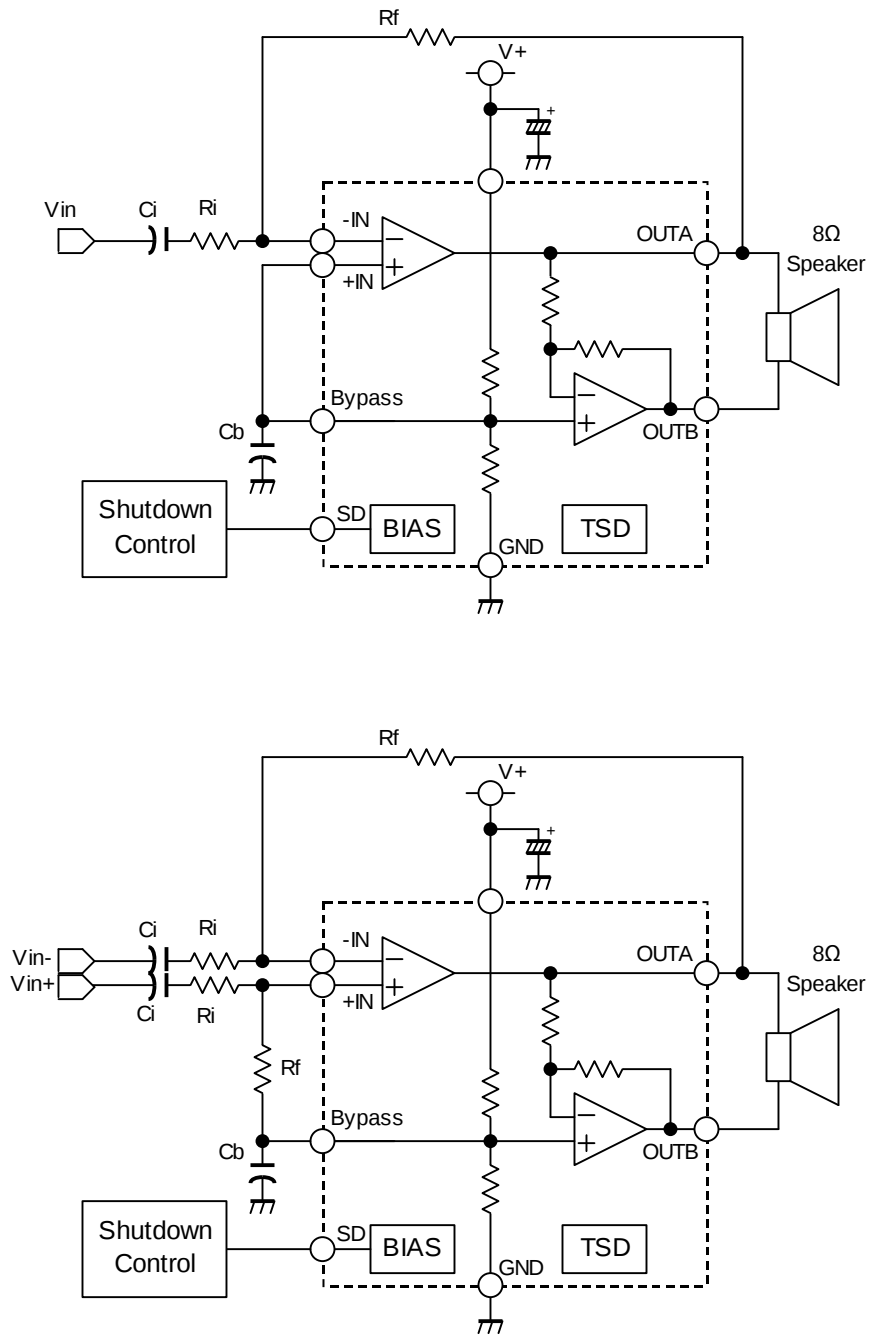
■ TEST CIRCUIT (PSRR)



■ TERMINAL DESCRIPTION

TERMINAL			SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
VSP8, ESON8	SSOP 20	HTSSOP 24				
1	4	5	SD	Shutdown Enable		0V
2	5	6	Bypass	Reference Voltage		$V^+/2$
3	6	7	+IN	Noninverted Input		$V^+/2$
4	7	8	-IN	Inverted Input		$V^+/2$
5 8	14 17	17 20	OUTA OUTB	Output A Output B		$V^+/2$

■ APPLICATION CIRCUIT



The NJU7089 is a 1.2W mono bridge-tied-load [BTL] amplifier designed to drive a speaker with 8Ω impedance. The NJU7089 can run from a 1.8V to 5.5V supply. The voltage gain is set by the user-selected resistor (R_i , R_f). The NJU7089 is equipped with a shutdown [SD] mode that will reduce the supply current and pop noise during the SD mode ON/OFF.

In this application note, detailed information on the usage of this IC and its operation are discussed.

1. Operating Overview

Fig.1 shows the NJU7089 internal circuit. It comprises of two power amps (Amp-A, Amp-B), a bias circuit, and a thermal shutdown[TSD] circuit. Pin 4 and Pin 3 are the inverting and noninverting terminal to Amp-A. A reference voltage is provided at Pin 2, which should be connected to Pin 3. Pin 5 is the output terminal to Amp-A. A second operational amplifier, Amp-B is configured with a fixed gain of $A_v = -1$ and produces the inverted signal of Pin 5. The NJU7089 outputs at Pin 5 and Pin 8 produce a bridged configuration output to which a speaker can be connected. Twice the output voltage and four times output power in a bridged amplifier are possible as compared to a single-ended amplifier. When a SD mode is active, the internal switch(SW) turns off to stop an internal bias current. As a result, a SD mode reduces the supply current. The external capacitor (C_b) and Internal resistance eliminate disturbing pop noise during the SD mode ON/OFF. (Ref. Page 3) The external capacitor (C_b) value depends on the turn-on time. (Ref. Page 7)

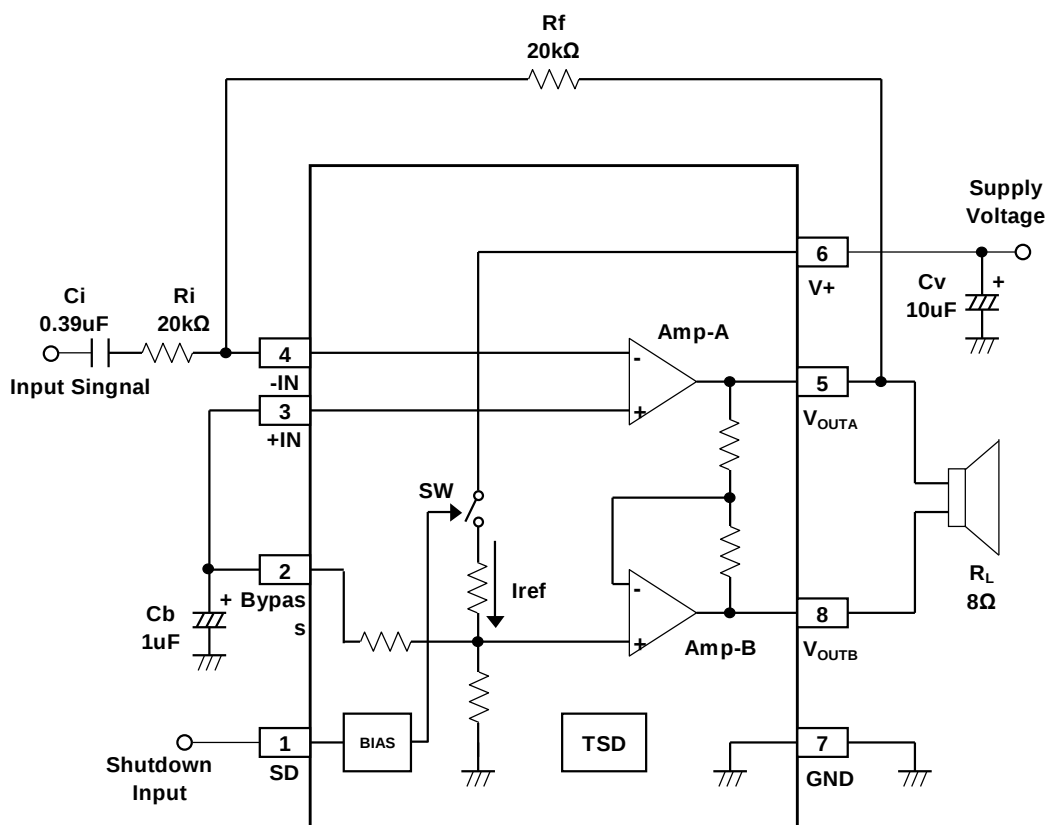


Fig1. Block diagram and Application circuit

Technical Information

2. External Component

2.1 Bypass Capacitor

Power source bypass capacitor (Cv) should have margin for temperature characteristics and the better characteristic in high frequency. Design to provide low impedance for the wiring between the IC and the capacitor.

2.2 Input Resistor and Feedback Resistor

The voltage gain is set by the user-selected resistor(Ri, Rf) [1].

$$Gv = 20\text{Log}\left(\frac{2R_f}{R_i}\right) \dots\dots [1] \quad \text{*Gain setting for BTL output}$$

Design to lower the resistance value for Ri and Rf, because of the increase in output noise voltage and disturbing pop noise. Ri forms a HPF with the input coupling capacitor (Ci). (Ref. 2.3)

2.3 Input Coupling Capacitor

The input coupling capacitor (Ci) is necessary for DC cut. Ci forms a HPF with Ri. The cutoff frequency is calculated using [2].

$$C_i = \frac{1}{2\pi R_i f_c} \dots\dots [2] \quad \text{*}f_c\text{=Cut-off frequency}$$

2.4 Bypass Capacitor for Reference Voltage

The capacitor (Cb) stabilizes DC bias voltage. As Cb becomes lager, PSRR and pop noise are improved but turn on time becomes longer.

Component	Function	Default value	Recommendation Ranges
Cv	Supply bypass capacitor	10uF	1uF<Cv
Ri	input resistor	20kΩ	10kΩ<Ri<50kΩ
Rf	feedback resistor	20kΩ	10kΩ<Rf<50kΩ
Ci	Input coupling capacitor	0.39uF	0.047uF<Ci
Cb	Bypass pin capacitor	1uF	0.1uF<Cb
RL	Load resistor(speaker)	8Ω	4Ω<RL

Table 1 Cv,Ri,Rf,Ci,Cb,and RL has limits in below table.

Please set these component values in the ranges.

3. Pop Noise during SD mode ON/OFF

NJU7089 builds anti-pop circuit, but Pop noise is dependent on the value of external elements.

3.1 Shutdown (SD terminal = Low) -> Active (SD terminal=High)

BTL amplifier does not generate sound, if there is no voltage difference between two outputs. But, common power amplifier generates pop noise according to the voltage difference of IN- and IN+ resulting from the difference of the charge time of C_i and C_b . NJU7089 does not generate pop noise by changing amp1(Fig3) from amp2(Fig2), after C_i and C_b are charged.

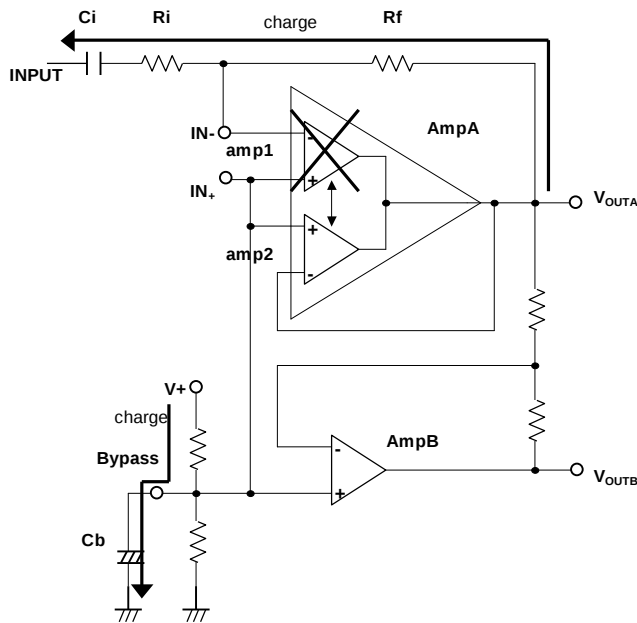


Fig2. Voltage follower amplifier

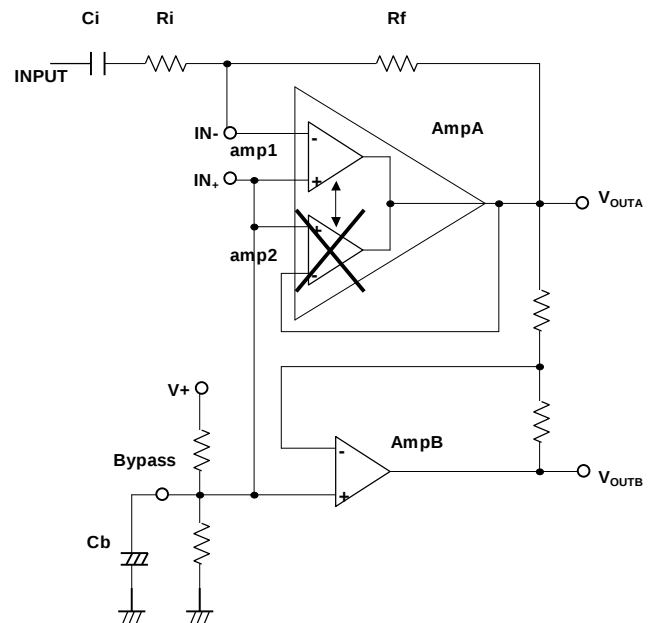


Fig3. Inverting amplifier

Technical Information

The terminal voltage in application circuit and the relation of time are shown in Fig. 4.

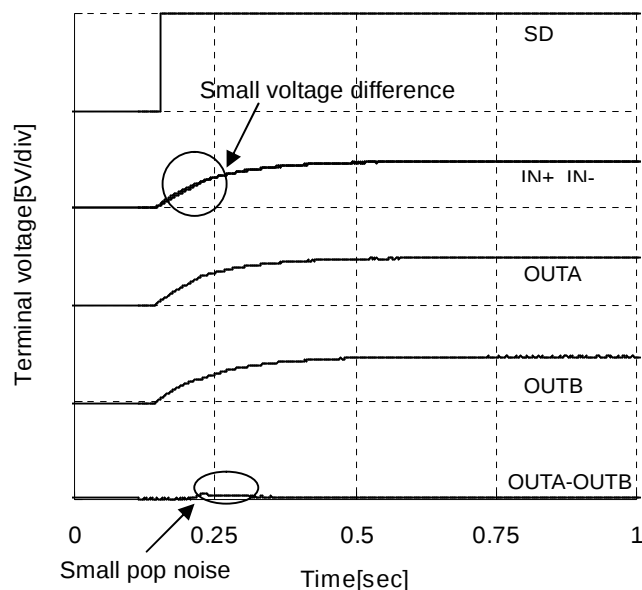


Fig4. Terminal Voltage at application circuit

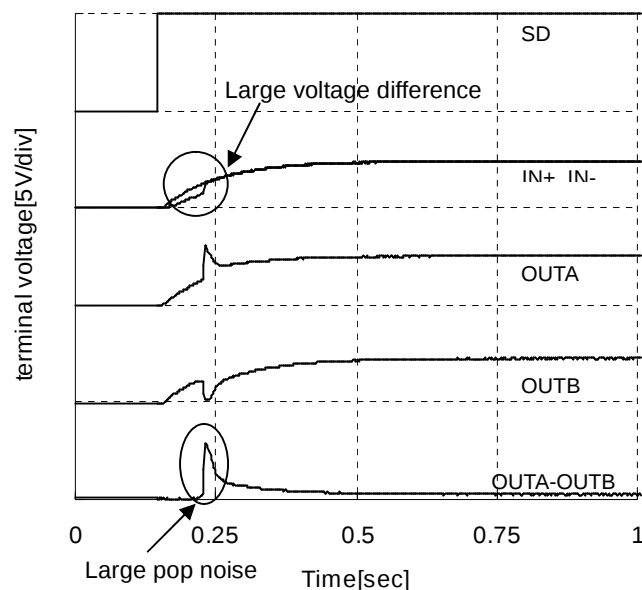


Fig5. Terminal Voltage at $R_f=100k\Omega$

Fig. 5 shows that the pop noise became large by the input terminal voltage difference resulting from change of the time constant.

In order to make small the pop noise which became large by increase of R_f , etc., it is necessary to enlarge C_b and to make small C_i . (However, C_b influences a turn on time, and C_i influences a frequency characteristic.)

Table2~6 show the value of C_b for realizing the pop noise at an application circuit.

Technical Information

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Cin	0.047uF	01uF	0.33uF	0.33uF	0.33uF	0.33uF
	0.1uF	0.33uF	0.33uF	1uF	1uF	1uF
	0.39uF	1uF	1uF	2uF	2uF	3.3uF
	0.47uF	1uF	2uF	2uF	3.3uF	3.3uF
	1uF	2uF	3.3uF	4.7uF	10uF	10uF

Table2 the value of Cb at Ri=10kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Cin	0.047uF	01uF	0.33uF	0.33uF	0.33uF	0.33uF
	0.1uF	0.33uF	0.33uF	1uF	1uF	1uF
	0.39uF	1uF	1uF	2uF	2uF	3.3uF
	0.47uF	1uF	2uF	2uF	3.3uF	3.3uF
	1uF	2uF	3.3uF	4.7uF	10uF	10uF

Table3 the value of Cb at Ri=20kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Cin	0.047uF	01uF	0.33uF	0.33uF	0.33uF	0.33uF
	0.1uF	0.33uF	0.33uF	1uF	1uF	1uF
	0.39uF	1uF	1uF	2uF	2uF	3.3uF
	0.47uF	1uF	2uF	2uF	3.3uF	3.3uF
	1uF	2uF	3.3uF	4.7uF	10uF	10uF

Table4 the value of Cb at Ri=30kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Cin	0.047uF	01uF	0.33uF	0.33uF	0.33uF	0.33uF
	0.1uF	0.33uF	0.33uF	1uF	1uF	1uF
	0.39uF	1uF	1uF	2uF	2uF	3.3uF
	0.47uF	1uF	2uF	2uF	3.3uF	3.3uF
	1uF	2uF	3.3uF	4.7uF	10uF	10uF

Table5 the value of Cb at Ri=40kΩ

		Rf				
		10kΩ	20kΩ	30kΩ	40kΩ	50kΩ
Cin	0.047uF	01uF	0.33uF	0.33uF	0.33uF	0.33uF
	0.1uF	0.33uF	0.33uF	1uF	1uF	1uF
	0.39uF	1uF	1uF	2uF	2uF	3.3uF
	0.47uF	1uF	2uF	2uF	3.3uF	3.3uF
	1uF	2uF	3.3uF	4.7uF	10uF	10uF

Table6 the value of Cb at Ri=50kΩ

Technical Information

3.2 Active (SD terminal = High) -> Shutdown (SD terminal=Low)

When changing to a shutdown, pop noise is very small, because the voltage of OUTA and OUTB falls steeply and simultaneously. (This theory is realized only BTL)

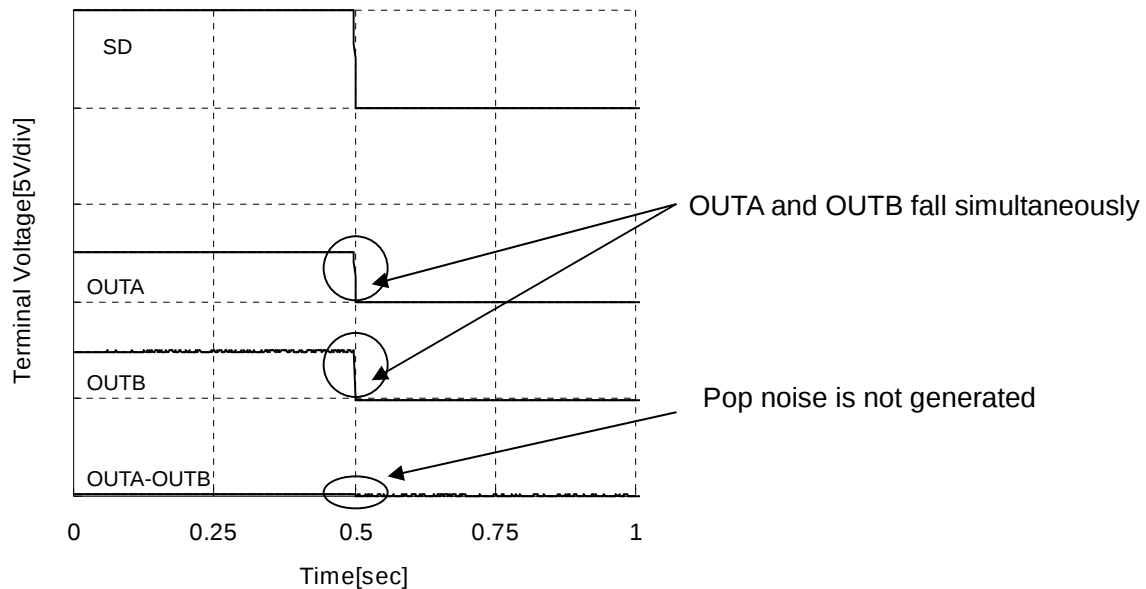


Fig6. Terminal Voltage at Shutdown

3.3 Cut-off frequency

In order to make small the pop noise, it is necessary to make small C_i . But, The value of C_i affects the low frequency performance of the circuit, because C_i forms with R_i a high-pass filter.

$$f_c = \frac{1}{2\pi R_i C_i} \quad (\text{Hz})$$

4. Turn on/off time

As C_b becomes smaller, turn on time becomes shorter but pop noise and PSRR become worse. Turn off time is always very short. (It does not depend on the value of C_b .)

Relationship of turn on time and the value of C_b are shown in Fig. 7~8.

$$T_{ON} = -C_b \cdot 100k\Omega \cdot \ln\left(0.5 - \frac{0.5}{V^+}\right) \quad (\text{sec})$$

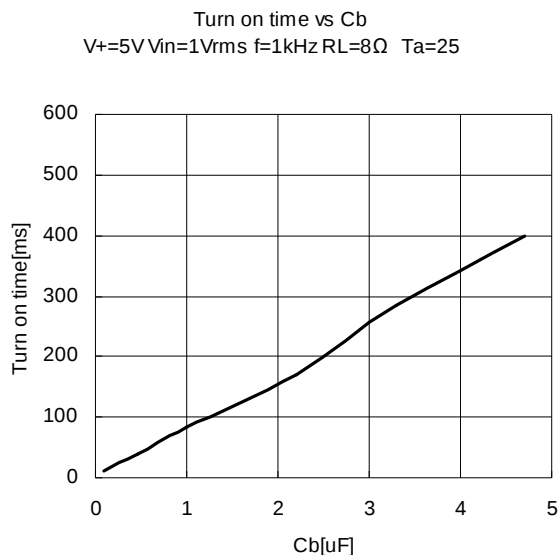


Fig.7. Turn on time vs C_b ($V^+=5V$)

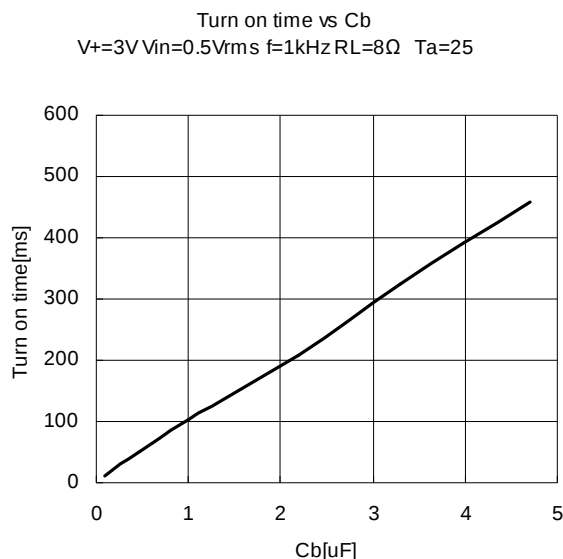


Fig.8 Turn on time vs C_b ($V^+=3V$)

5. PSRR vs C_b

As C_b becomes larger, PSRR becomes good.

Relationship of PSRR and the value of C_b are shown in Fig. 9~10.

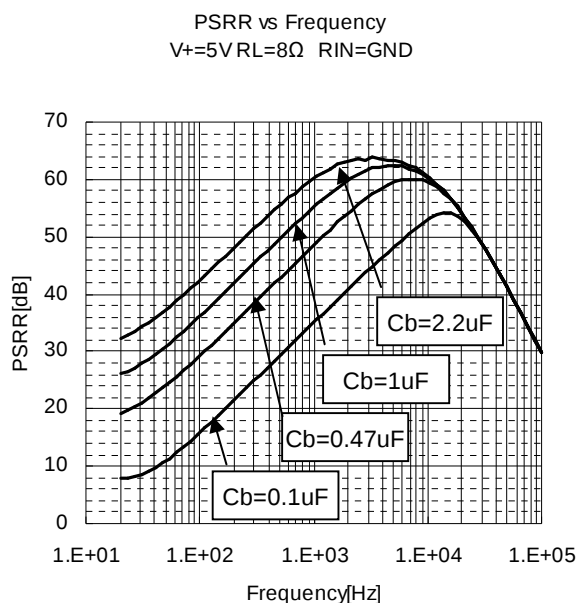


Fig.9. PSRR vs Frequency ($V^+=5V$)

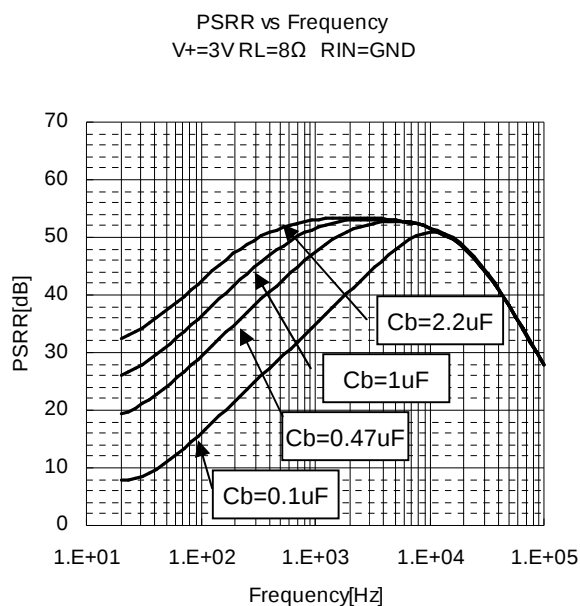


Fig.10. PSRR vs Frequency ($V^+=3V$)

Technical Information

6. Power dissipation and Output Power

P_d is the maximum permissible power at $T_a=25^{\circ}\text{C}$. P_d is dependent on the ambient temperature, which shown in Fig.11.

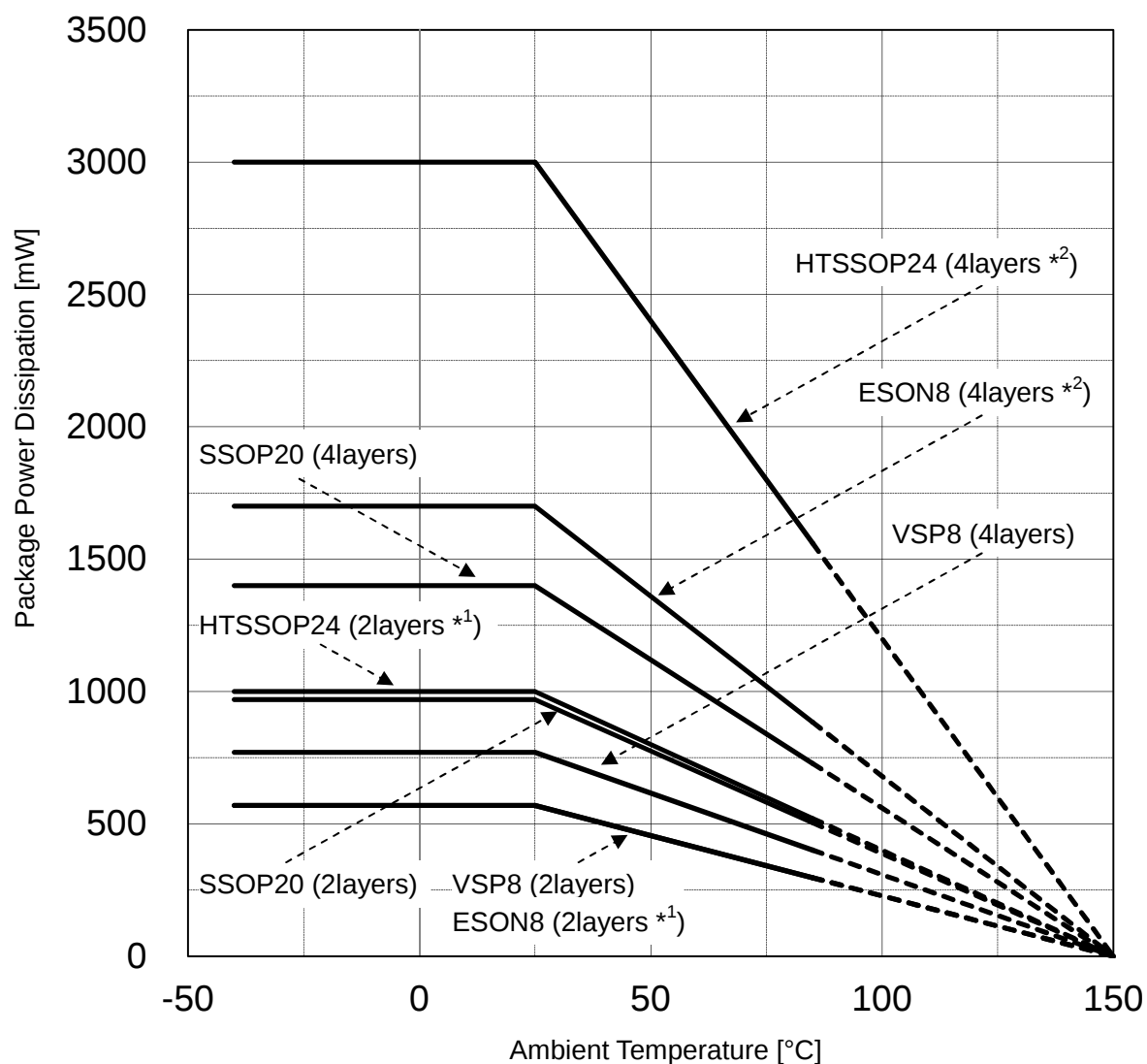


Fig11. Power derating curves

*¹ The PAD connecting to GND in the center part on the back.

*² The PAD connecting to GND in the center part on the back. Applying a thermal via hole to a board.

Technical Information

Maximum output power can be determined from Power dissipation vs Output Power characteristics with P_D (ABSOLUTE MAXIMUM RATINGS). An example is shown in Fig.12.

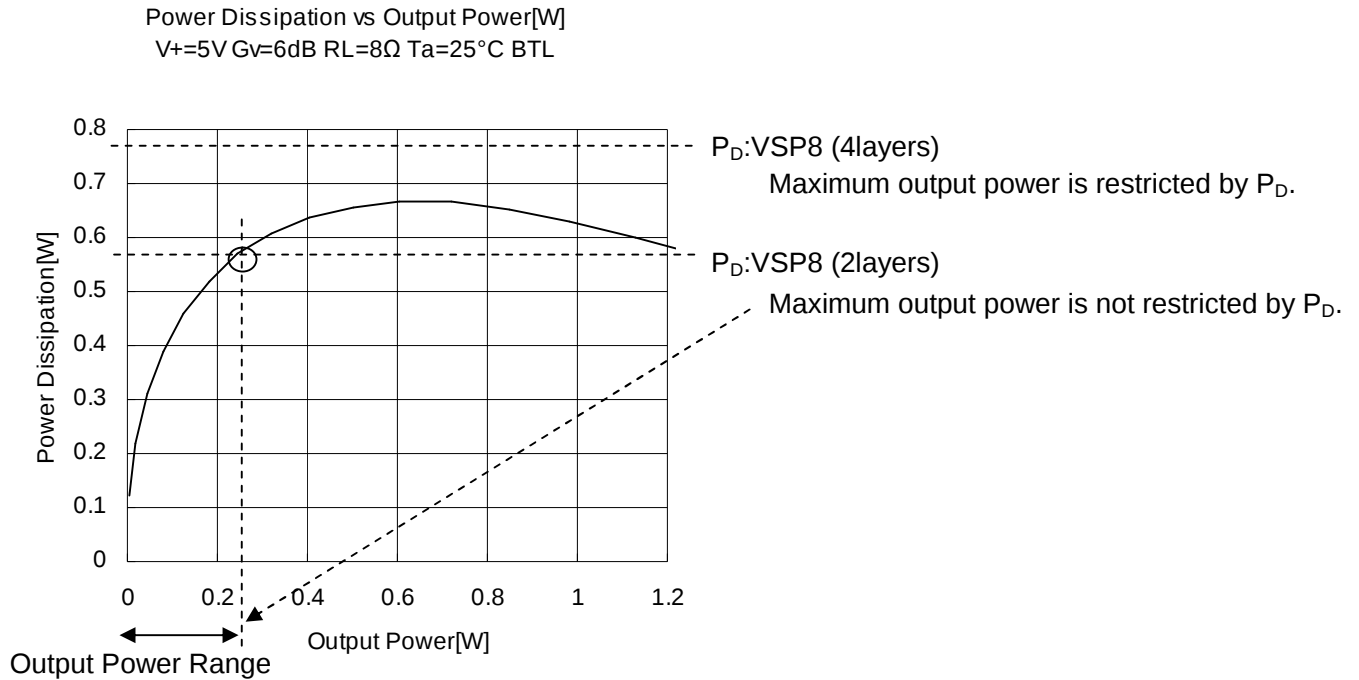
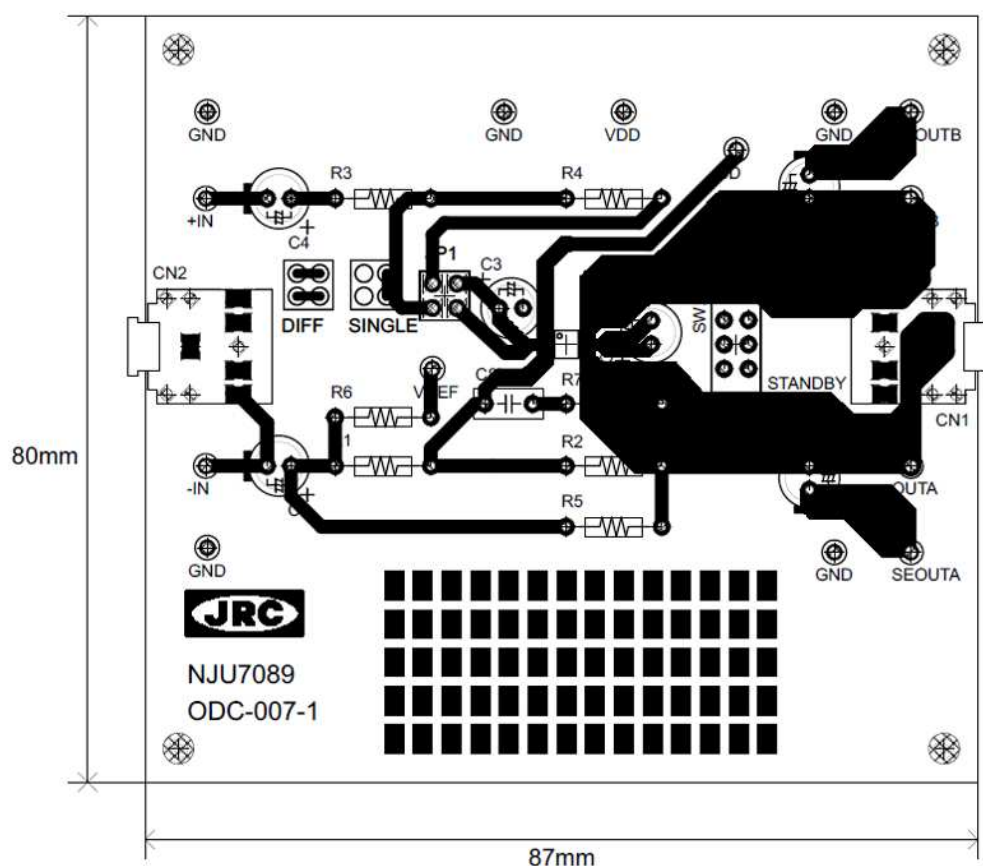


Fig12. Power dissipation vs Output Power

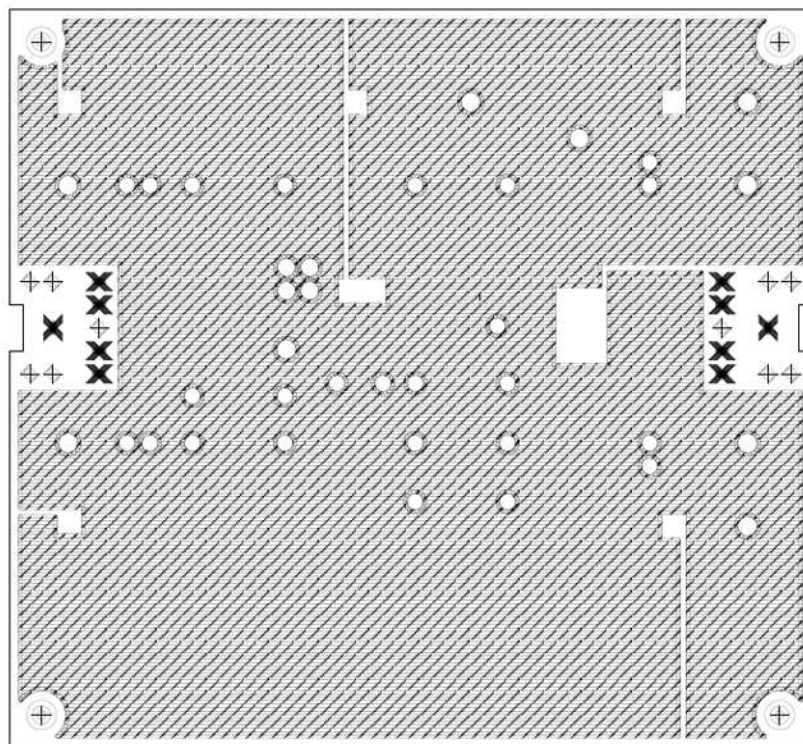
7. PCB layout

In order to demonstrate the performance of IC, it is necessary to design a PCB appropriately. Power line, GND line, and signal line should be drawn so that wiring resistance may become small. And please connect all the GND to the single point of Cv.

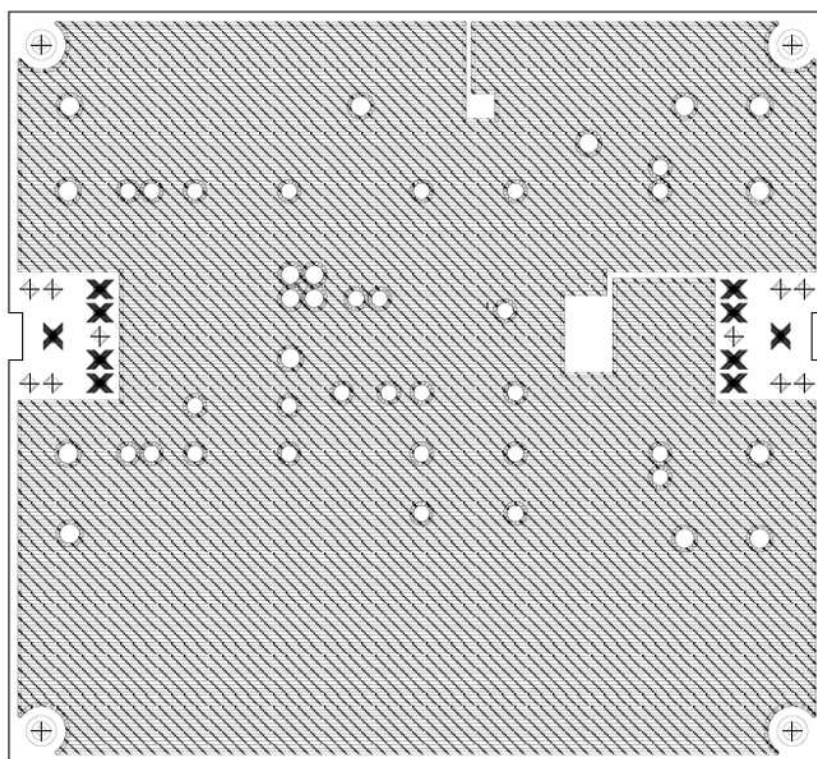
- NJU7089 demo board layout pattern



Layer1(Top Layer)

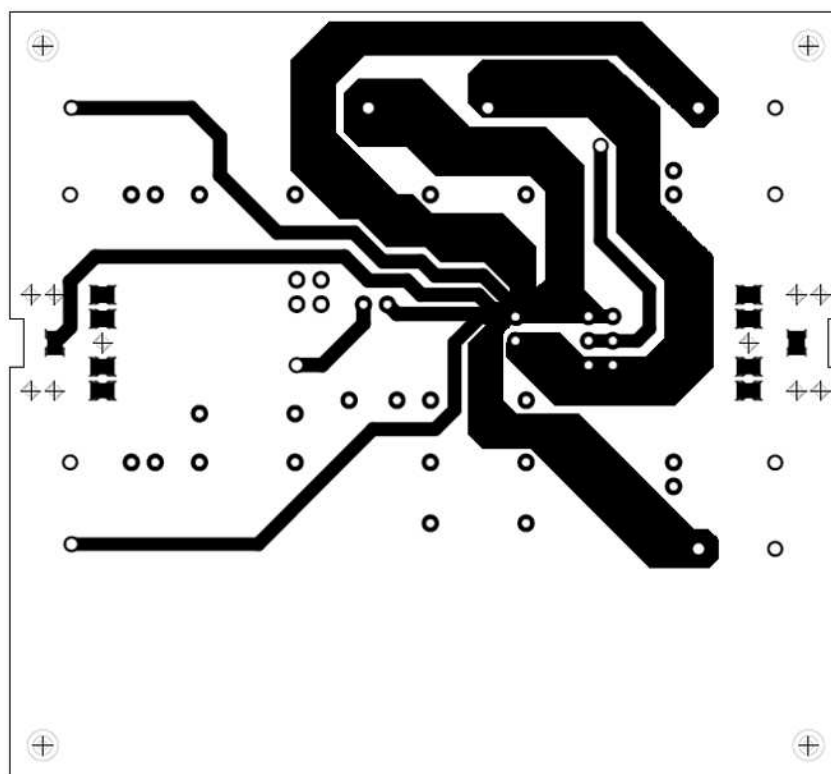


Layer2(Ground plane)



Layer3(Power plane)

Technical Information

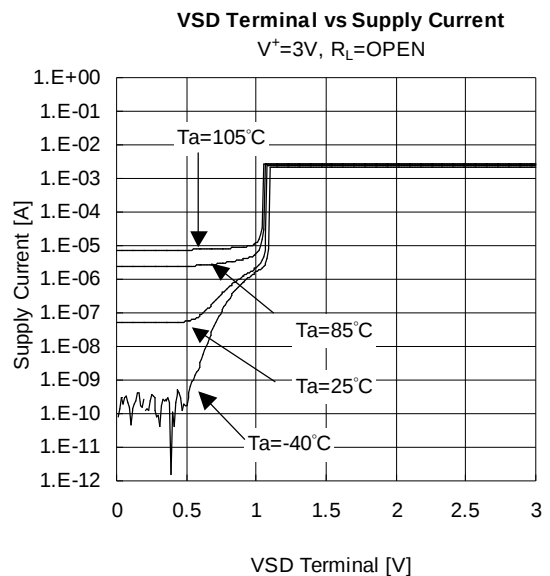
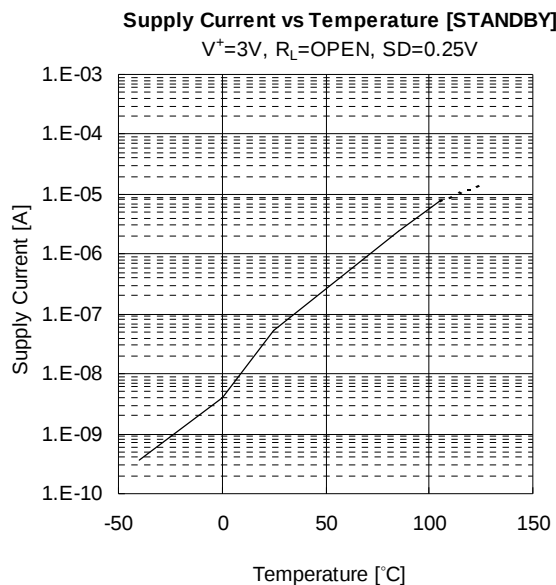
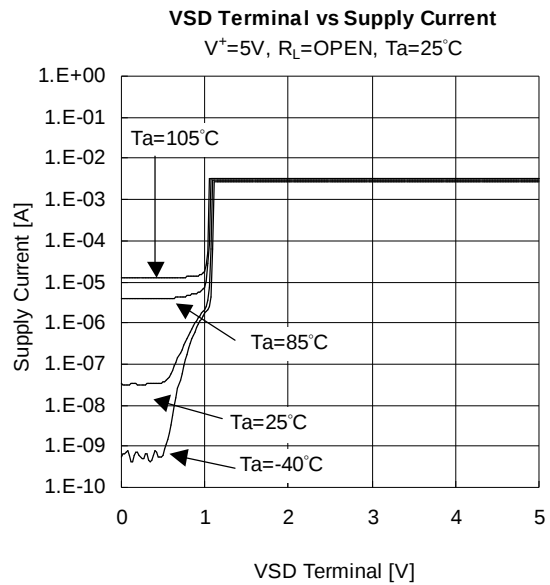
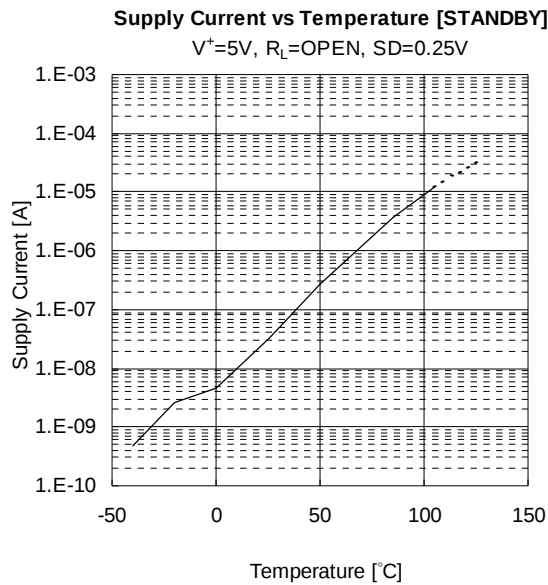
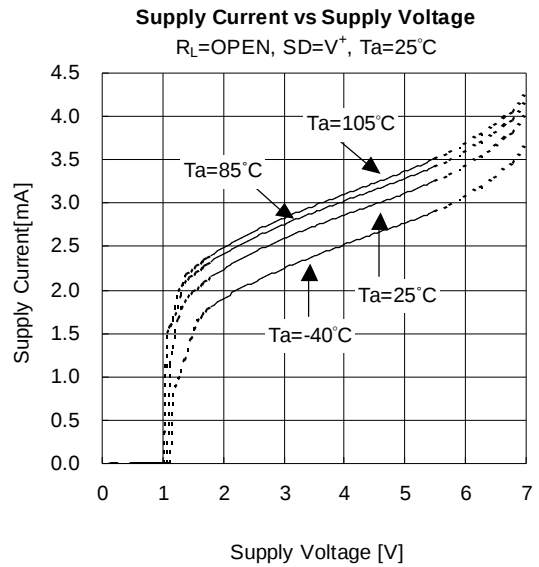
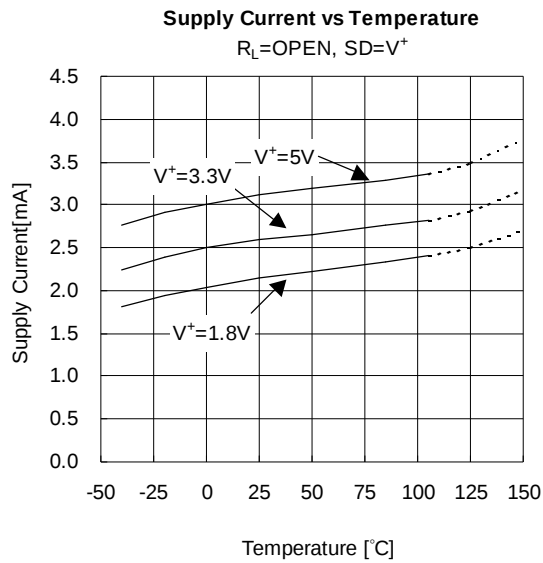


Layer4(Bottom Layer)

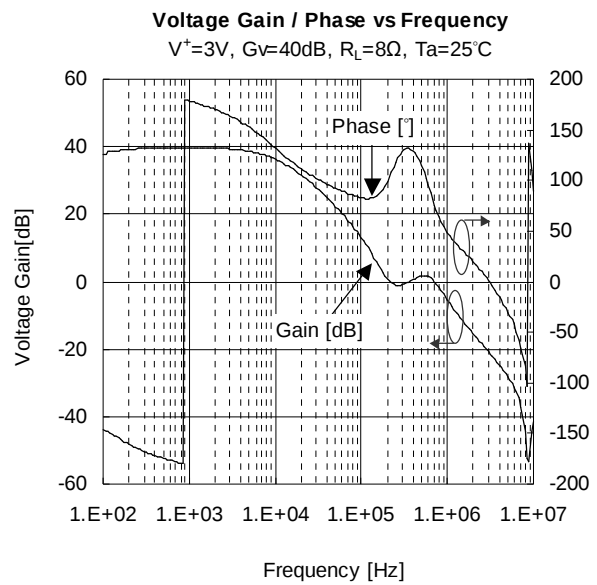
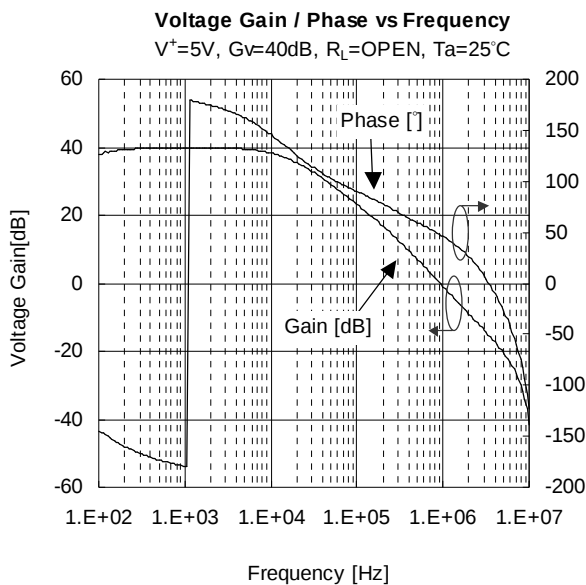
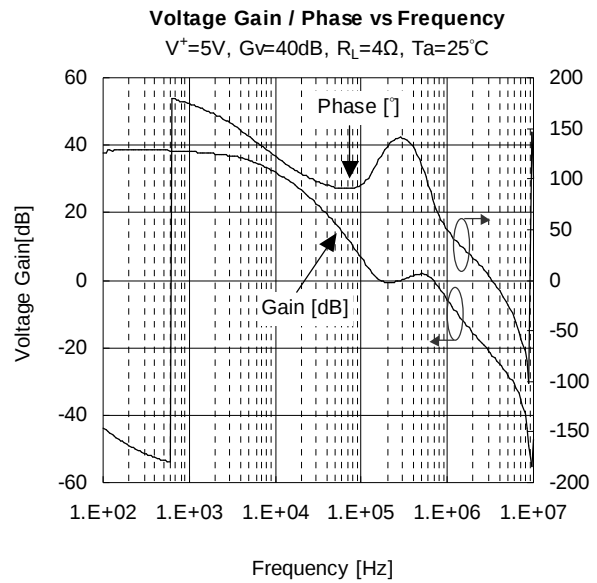
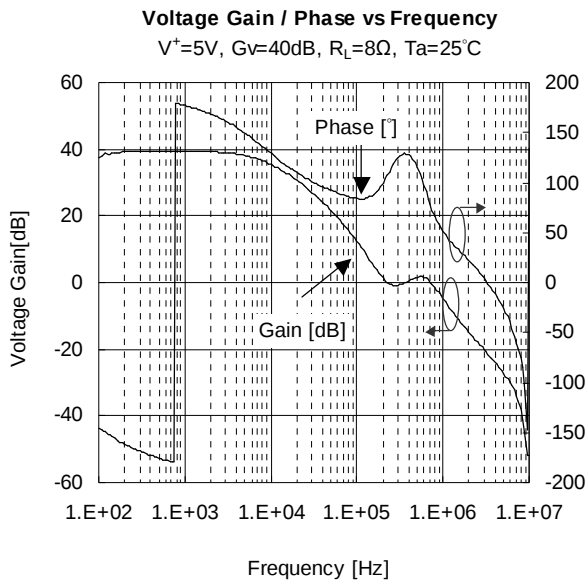
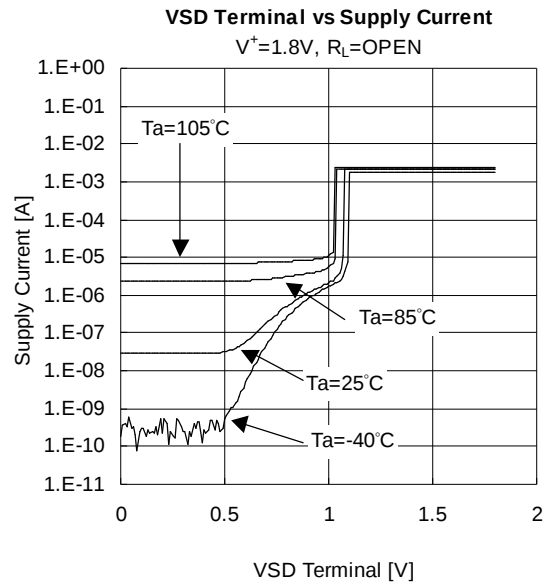
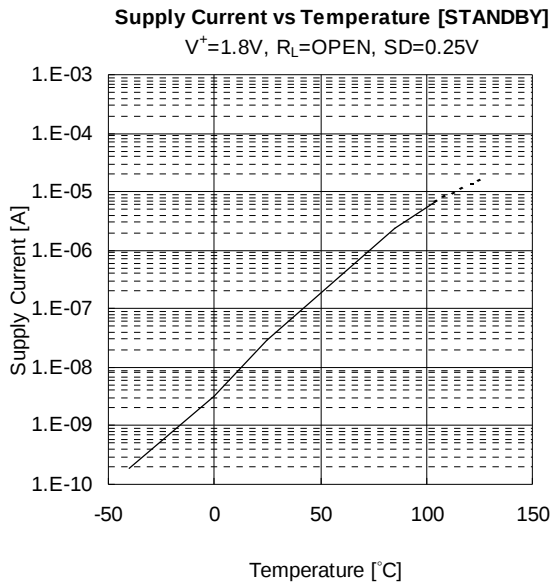
[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

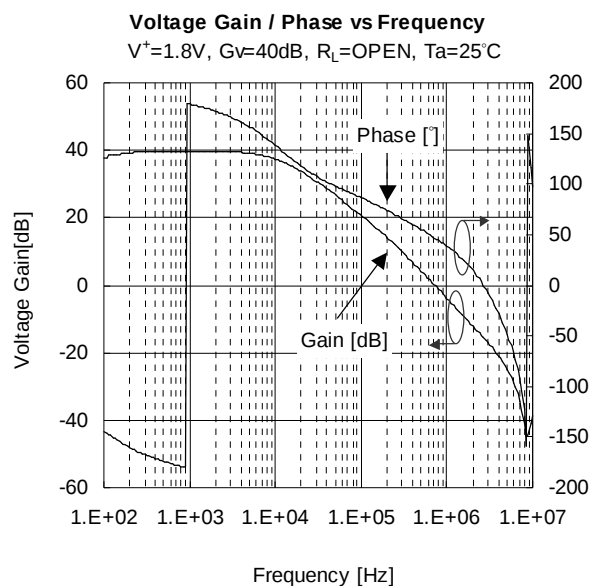
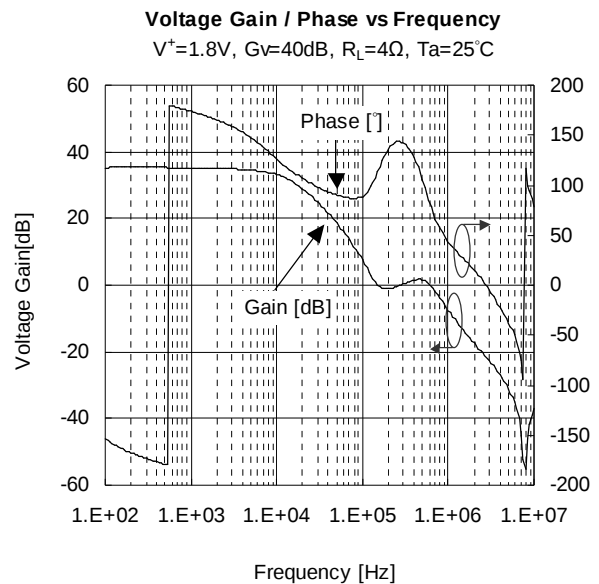
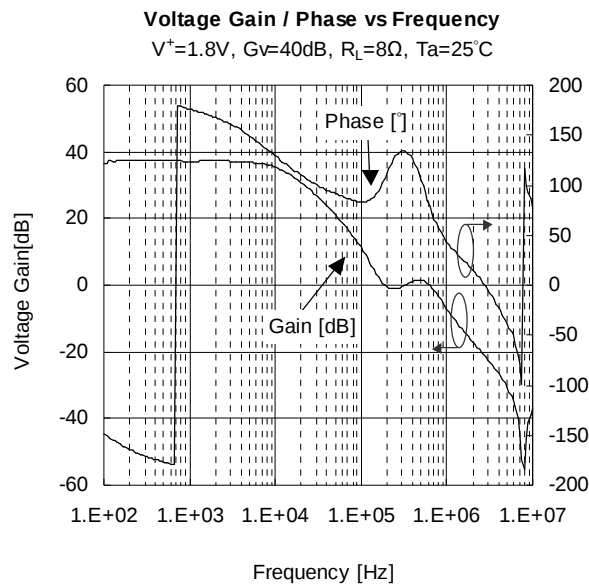
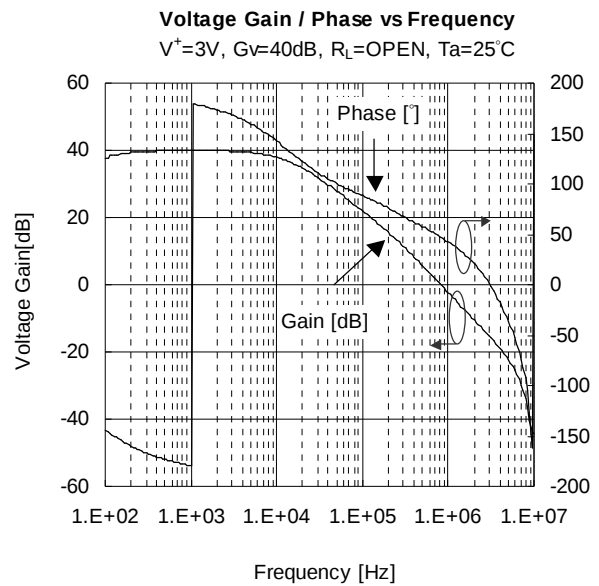
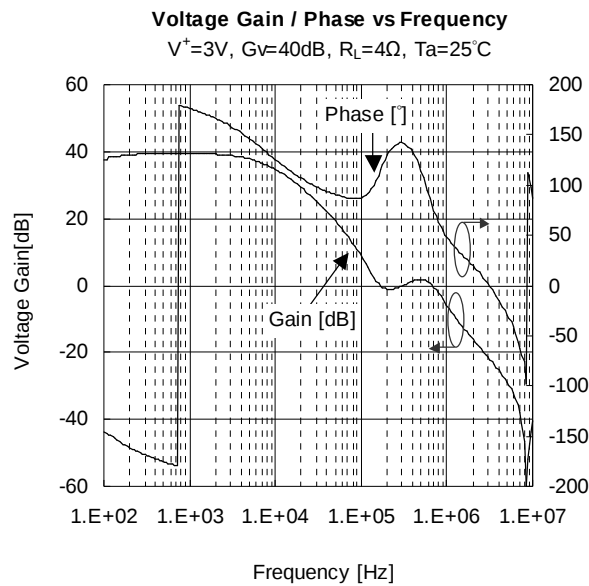
■ TYPICAL CHARACTERISTICS



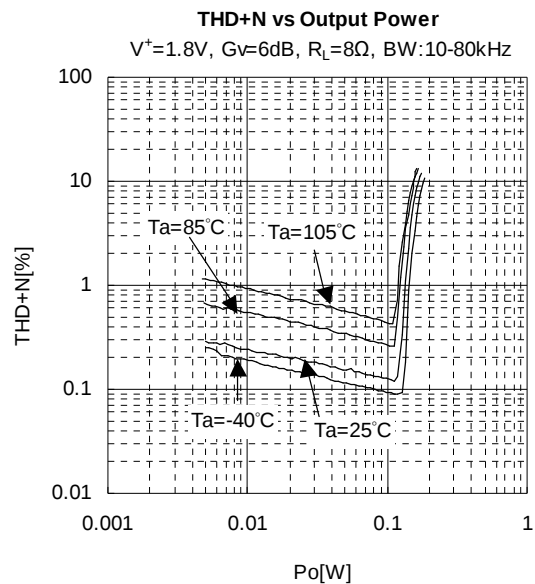
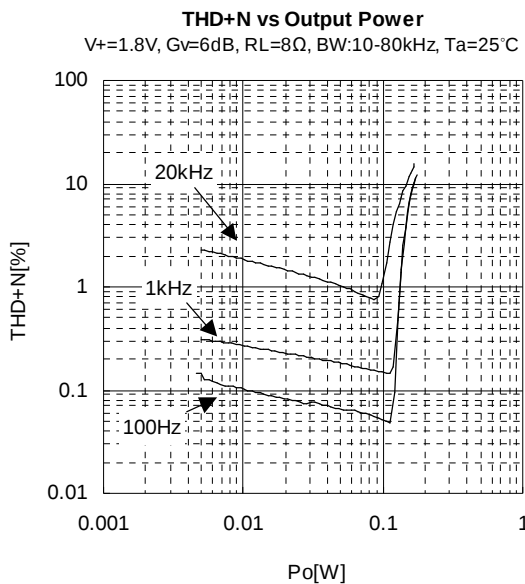
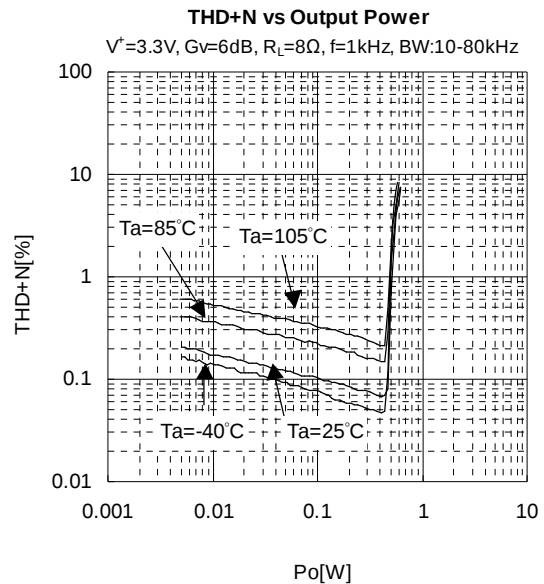
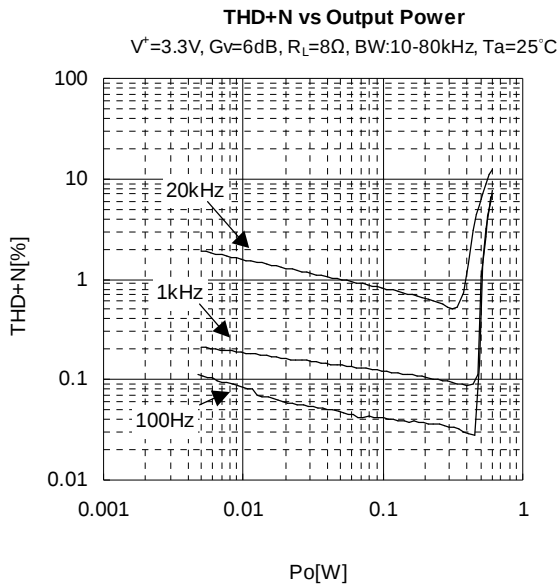
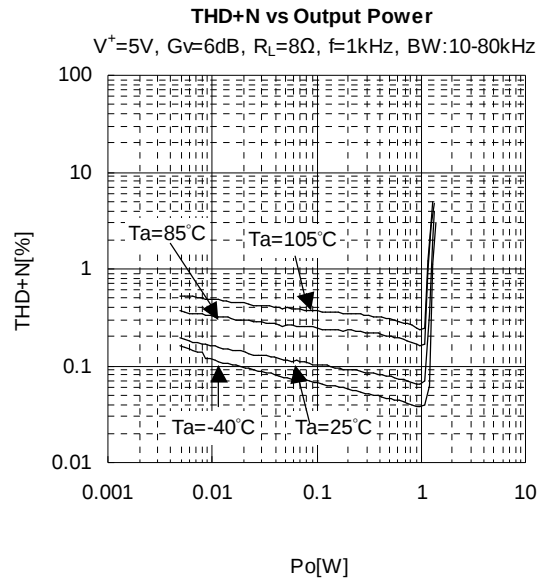
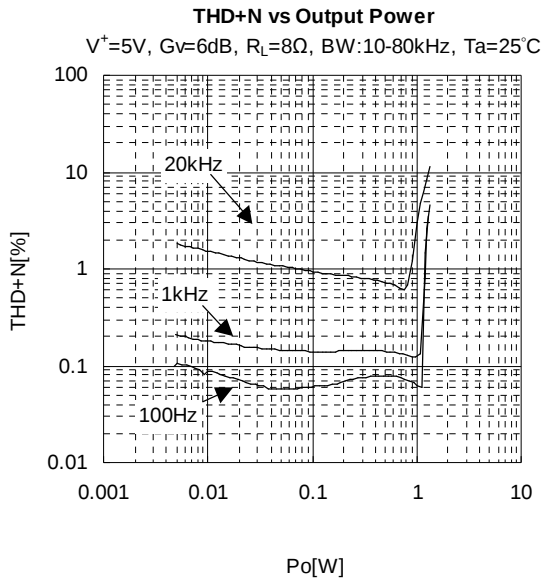
■ TYPICAL CHARACTERISTICS



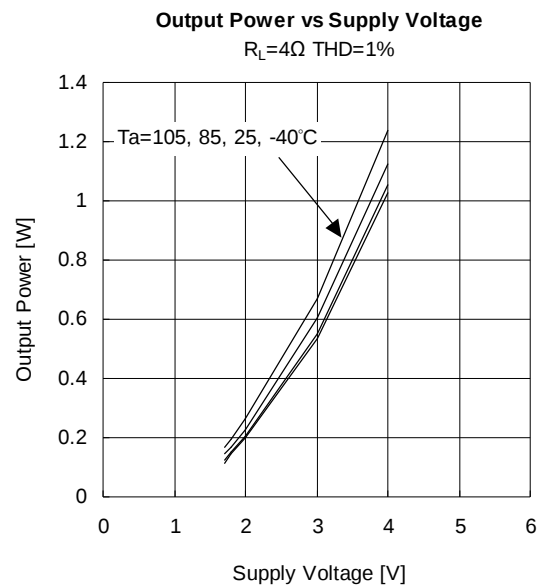
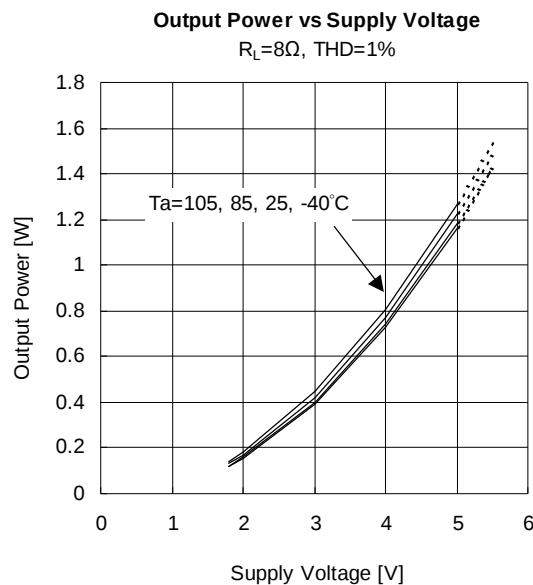
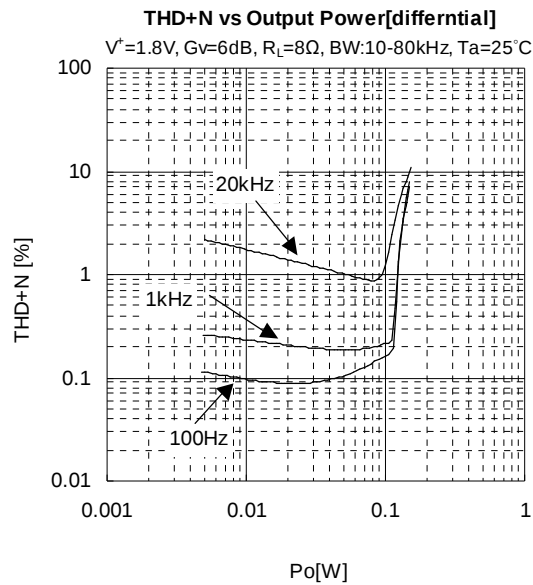
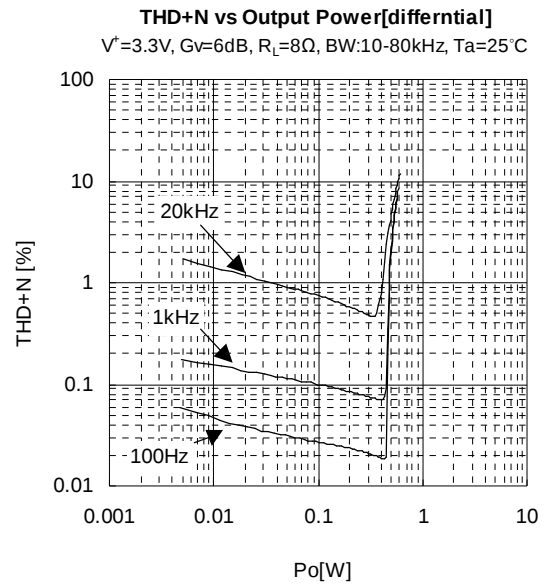
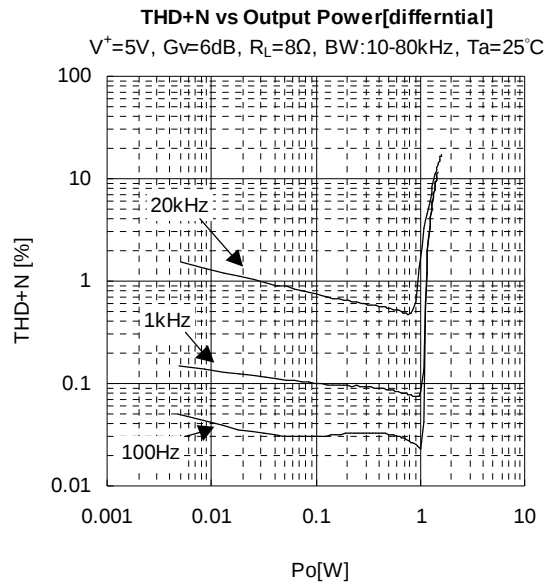
■ TYPICAL CHARACTERISTICS



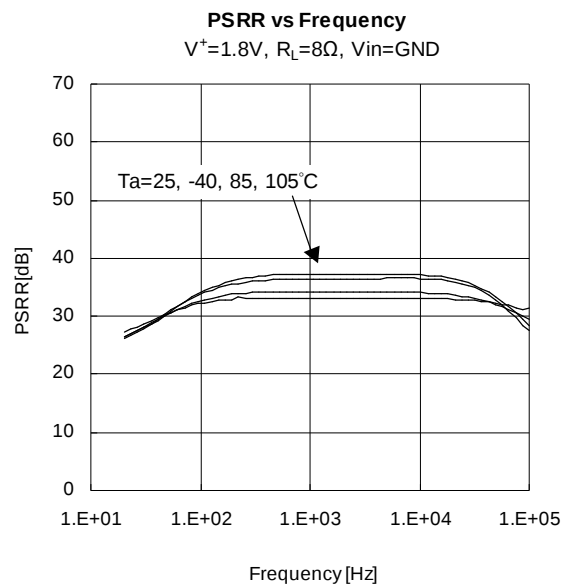
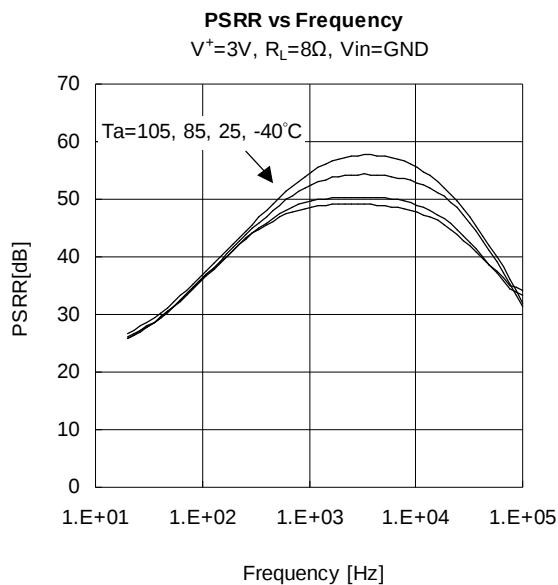
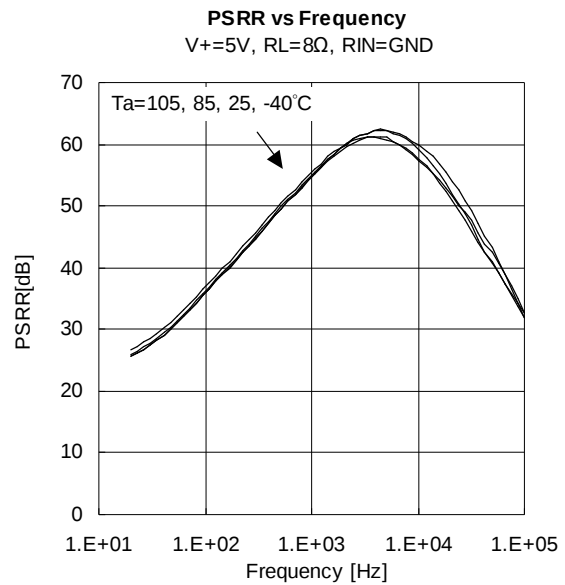
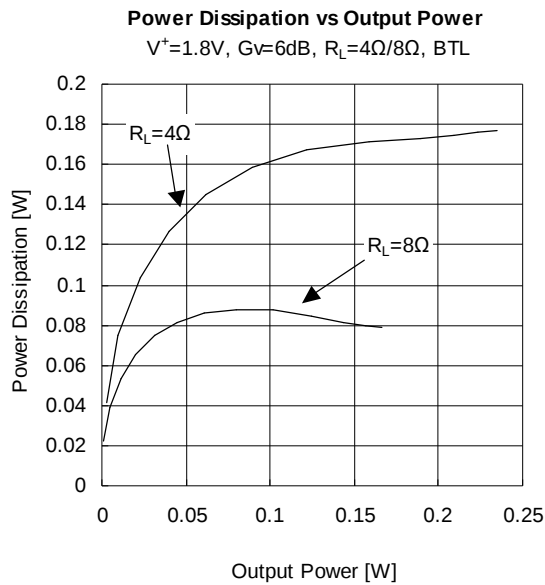
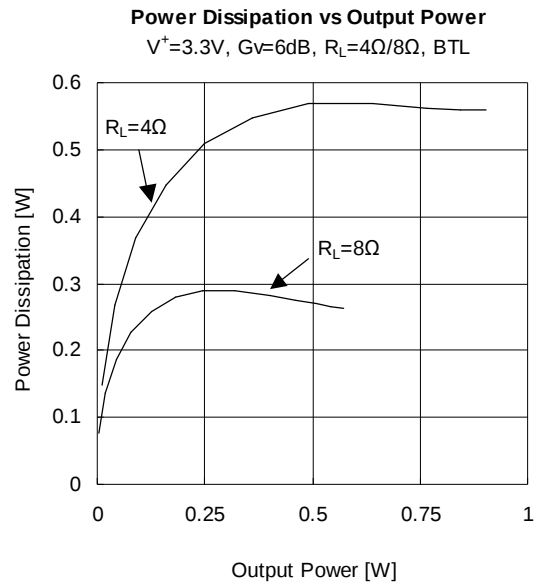
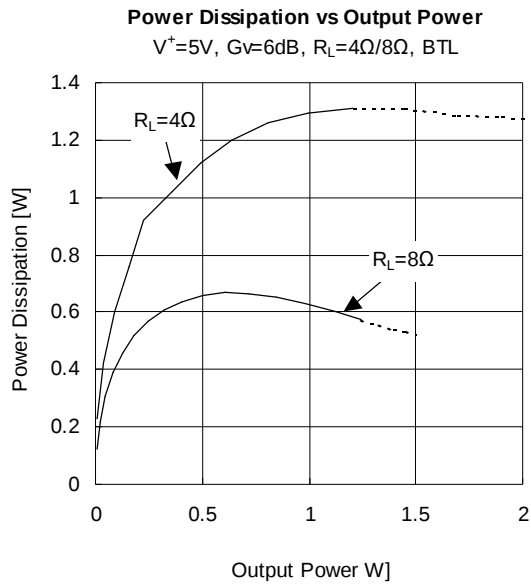
■ TYPICAL CHARACTERISTICS



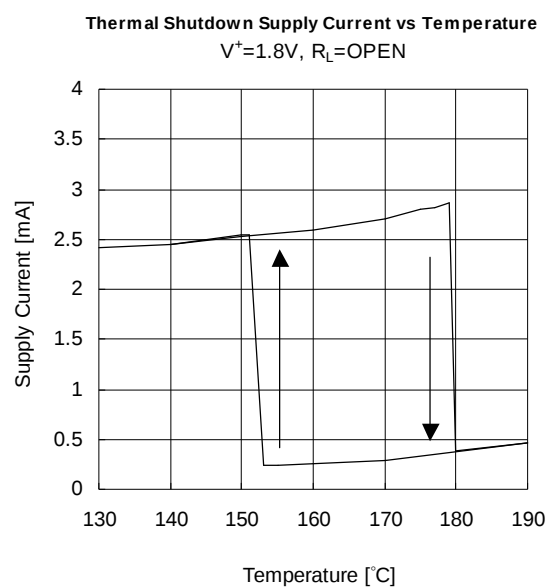
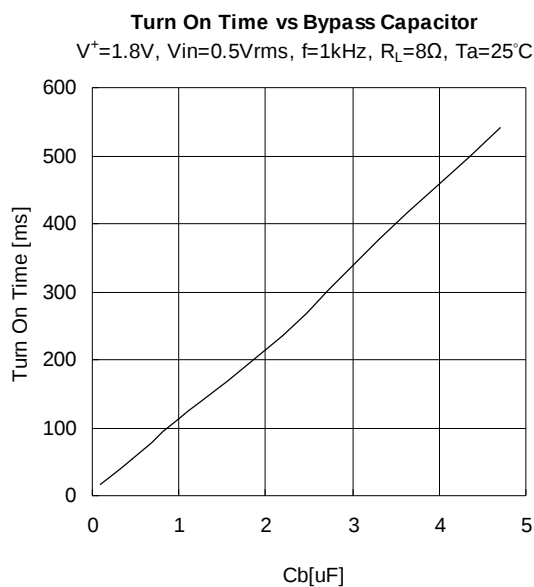
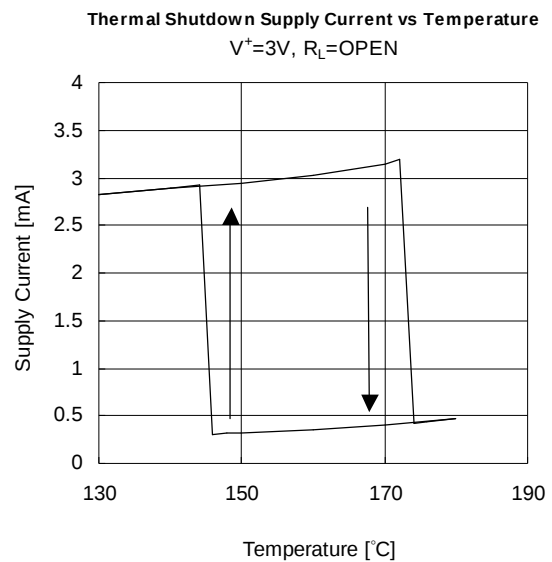
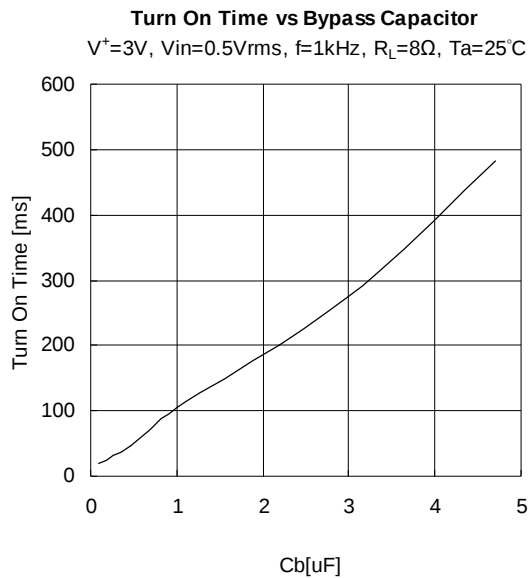
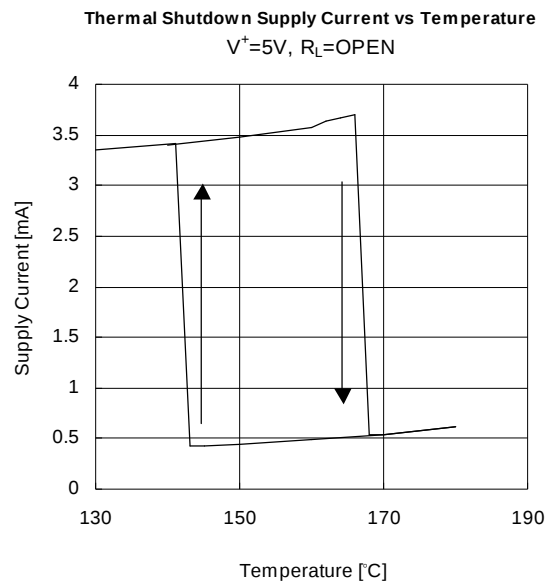
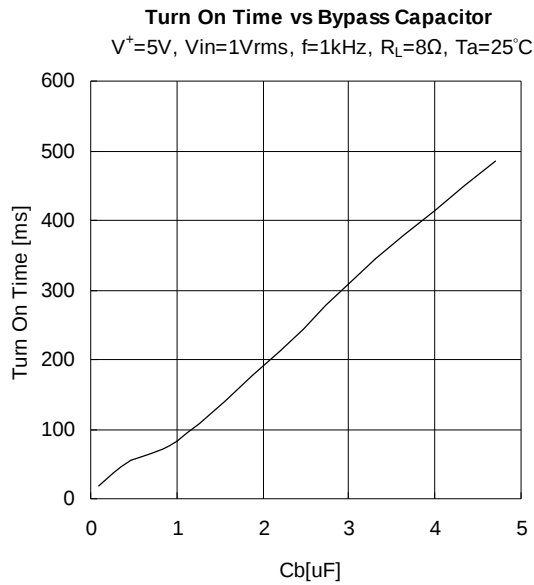
■ TYPICAL CHARACTERISTICS



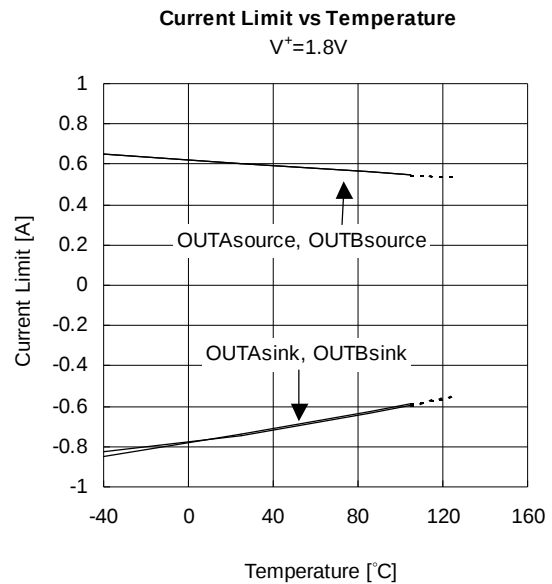
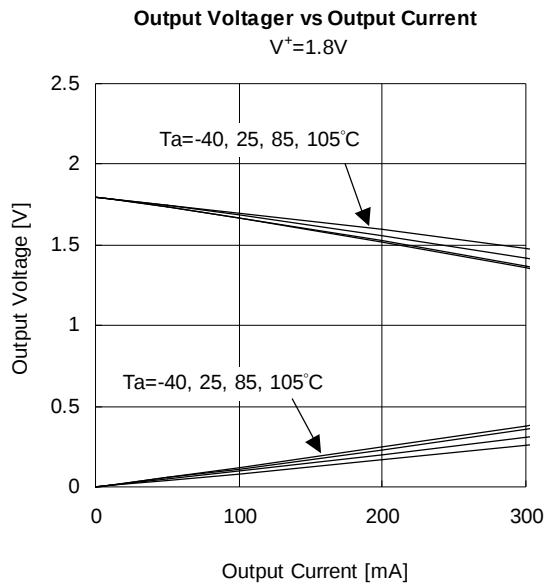
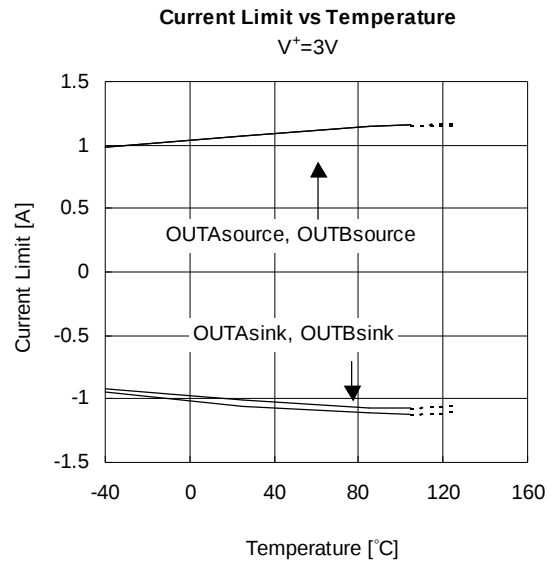
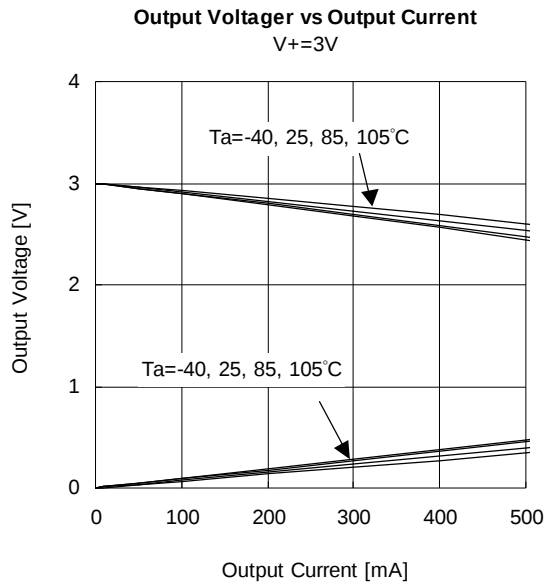
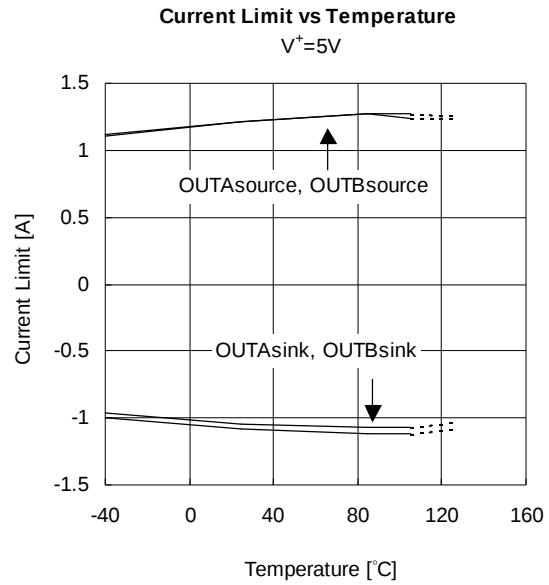
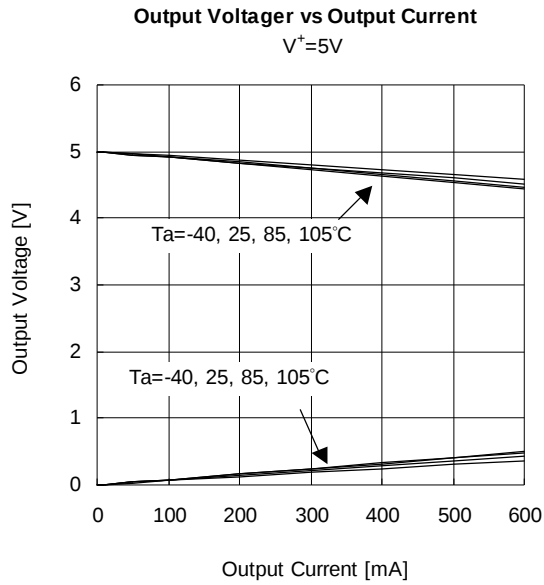
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



[CAUTION]

The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.