R2A20052NS

Lithium-Ion Battery Charger IC with Auto load current distribution

R03DS0079EJ0200
Rev.2.00
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Description

R2J20052NS is a semiconductor integrated circuit designed for Lithium-ion battery charger control IC.
Built-in constant current and constant voltage control circuit suitable to charge Lithium-ion battery.
Built-in dual input (AC adaptor and USB) and dual output (system and battery) control circuit allows to supply the system power and the battery charging power simultaneously from AC adaptor or USB power input.
The input current limitation of AC adaptor and USB can be set individually.
Built-in Low Ron MOSFET between the battery and the system realizes highly efficient power supply from the battery to the system when both AC adaptor and USB are not connected or the system load exceeds input current limit.

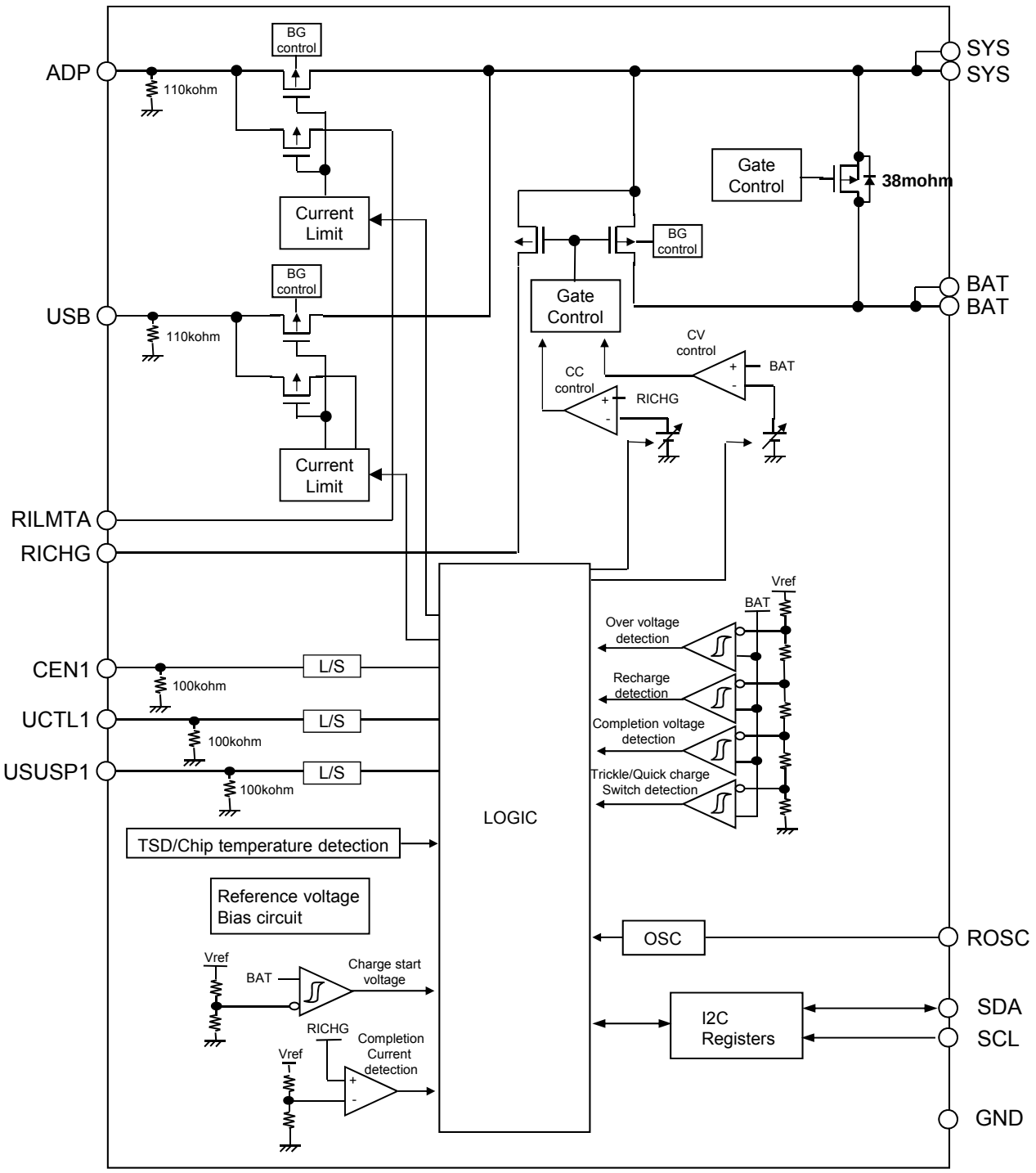
Features

- Available for 1cell Li-ion Battery
- Adaptor or USB auto source selection
- Auto power path management between the system power supply and the battery charge
- Built-in Low Ron MOSFET between the system and the battery (38mohm)
- Input current limitation (ADP:2Amax, USB:100/500/900/1800mA)
- Compliance with PSE (Adjustable CC current/CV voltage by I2C)
- Charge control voltage : 4.2V+/-30mV (+/-0.7% precision)
- CC/CV charge control
- Chip temperature detection
- Thermal shutdown
- Safety timer

Application

- DSC
- Mobile phone
- PDA
- Portable audio player
- Handheld game machine

Block Diagram

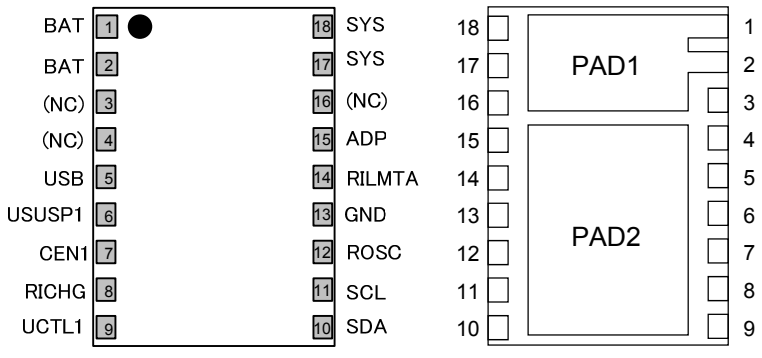


At least one input of USB/ADP is needed to read/write I2C port.

Pin description

Pin No.	Pin name	I/O	Description
1, 2	BAT	O	Battery connection terminal
5	USB	I	USB power input terminal
14	RILMTA	I	Resistor connection terminal for setting ADP input current limitation
7	CEN1	I	Charge enable Low: Charge stop, High: Charge start (CEN2="1")
8	RICHG	I	Resistor connection terminal for setting charge current
9	UCTL1	I	USB input current limitation setting terminal Low: 100mA max, High: 500mA max (USBMD="0")
13	GND	-	Ground
11	SCL	I	Serial clock input
10	SDA	I/O	Serial data input/output
6	USUSP1	I	USB suspend terminal Low: USB input enable, High: USB input disable (USBMD="0")
12	ROSC	I	Resistor connection terminal for setting oscillation frequency
15	ADP	I	AC adaptor power input terminal
17, 18	SYS	O	System power output (Each SYS terminal must be shortcircuited on the board)
3, 4, 16	(NC)	-	No connection
PAD1	PAD1	O	Must be connected to BAT plane
PAD2	PAD2	-	Must be connected to Ground plane (for heat radiation)

Pin configuration



TOP VIEW BOTTOM VIEW

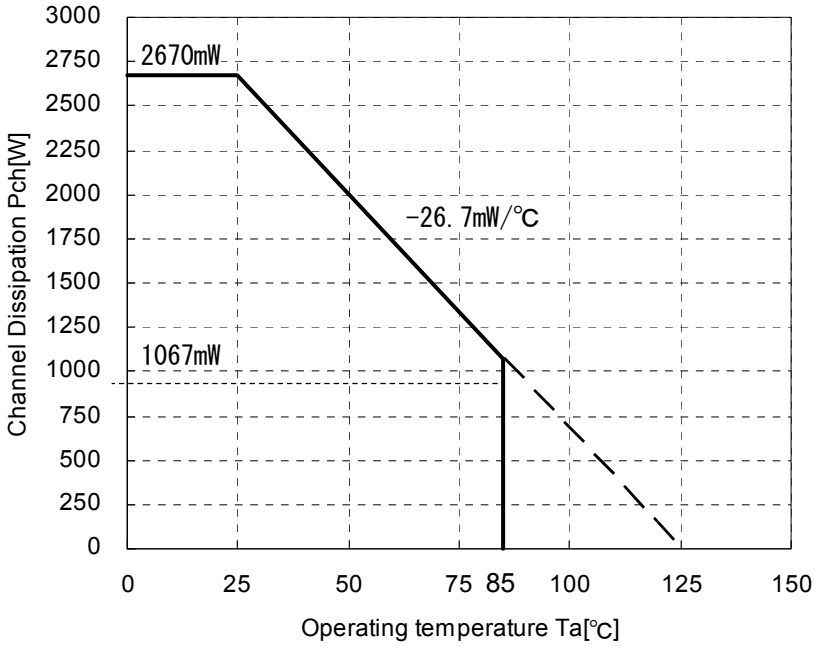
PKG : DFN-18 3.4mm x 4.5mm x 0.6mmt

Absolute maximum ratings

(Ta=25ºC, unless otherwise specified.)

Symbol	Items	Ratings	Unit
Vmax	Terminal voltage (All terminal)	-0.3 ~ 6.5	V
IADPmax	ADP terminal input current	2.5	A
IUSBmax	USB terminal input current	2.0	A
ISYSmax	SYS terminal output current	2.5	A
IBATmax	BAT terminal input/output current	2.5	A
Topr	Operating temperature range	-30 ~ 85	ºC
Tstg	Storage temperature range	-40 ~ 125	ºC
Tj	Maximum junction temperature	125	ºC
Pd*1	Power dissipation	2.67	W

*1) When using the glass epoxy board (50mm x 50mm x 1.6mm),
It is a value in the state that back die pad is connected to the board.
Ambient temperature [Ta]=25℃
Please note that Power dissipation changes on EVB condition.



Recommended operating condition

(Ta=25ºC, unless otherwise specified.)

Symbol	Item	Value			Unit
		Min.	Typ.	Max.	
VADP	ADP input voltage	4.5	5.0	5.8	V
VUSB	USB input voltage	4.5	5.0	5.8	V
VDVDD	I/O voltage	1.5	-	5.5	V
IADP	ADP input current	-	-	2.0	A
IUSB	USB input current	-	-	1.8	A

Electrical Characteristics

(Ta=25ºC, VADP=5V or VUSB=5V, unless otherwise specified.)

Item	Symbol	Condition		Rated value			Unit
				Min.	Typ.	Max.	
All							
ADP input detection voltage	VOKAL	POKA(02H bit0), VBAT=3.5V 300mV hysteresis		4.2	4.3	4.4	V
USB input detection voltage	VOKUL	POKU(02H bit1), VBAT=3.5V 300mV hysteresis		4.2	4.3	4.4	V
ADP input circuit current	ICCA	Battery non-connection			2.5		mA
USB input circuit current	ICCU	Battery non-connection			2.5		mA
USB suspend current	ICCUsus	When USB input is suspended				1.8	mA
Battery discharge current	ICCB	When charging is completed			3	6	uA
Input high level (CEN1,UCTL1, USUSP1)	VINH			1.2			V
Input Low level (CEN1,UCTL1, USUSP1)	VINL					0.5	V
Input high level (SDA, SCL)	VINH(I2C)			2.5			V
Input Low level (SDA, SCL)	VINL(I2C)					0.3	V
SDA output Low level	VOL_SDA	Isource=3mA		-	-	0.6	V
On resistance between ADP and SYS	RONA	ISYS=200mA, When charging stops			0.3	0.45	ohm
On resistance between USB and SYS	RONU	ISYS=200mA, When charging stops			0.3	0.45	ohm
ADP current limit [1)]	ILIMA0	RILMTA=2.7Kohm, VSYS=4V	*1	900	1000	1100	mA
RILMTA resistance range				1.3		30	kohm
USB current limit [1)]	ILIMU0	USB 1800mA Mode, VSYS=4V	*1	1500	1710	1800	mA
	ILIMU1	USB 900mA Mode, VSYS=4V	*1	720	810	900	mA
	ILIMU2	USB 500mA Mode, VSYS=4V		440	470	500	mA
	ILIMU3	USB 100mA Mode, VSYS=4V		80	90	100	mA
Input current soft start time [2)]	TSOFT		*1		1.0		ms
Chip temperature detection	Ttreg	Chip temperature, 10ºC hysteresis	*1		93		ºC
Chip temperature reset detection	Ttrgrst	Chip temperature	*1		120		ºC
Thermal shutdown temperature	Tsd	Chip temperature, 10ºC hysteresis	*1		150		ºC

*1 : design guarantee

1) Current limit value decreases when SYS≤2.5V.
2) Soft start function doesn't operate when switching input source (ADP/USB).

Electrical Characteristics

(Ta=25ºC, VADP=5V or VUSB=5V, unless otherwise specified.)

Item	Symbol	Condition		Rated value			Unit
				Min.	Typ.	Max.	
Battery voltage detection block							
Charge start voltage (Overdischarge protection)	Vstart	When battery voltage rising, 100mV hysteresis	*2	1.4	1.5	1.6	V
Quick charge start voltage	Vqchgon	When battery voltage rising, 100mV hysteresis		2.9	3.0	3.1	V
Recharge start voltage	Vrechg	When battery voltage falling, 100mV hysteresis		3.70	3.80	3.90	V
Charge control voltage (4.00V)	Vchg1	VCHG=4.00V		3.95	4.00	4.05	V
Charge control voltage (4.05V)	Vchg2	VCHG=4.05V		4.00	4.05	4.10	V
Charge control voltage (4.10V)	Vchg3	VCHG=4.10V		4.05	4.10	4.15	V
Charge control voltage (4.15V)	Vchg4	VCHG=4.15V		4.10	4.15	4.20	V
Charge control voltage (4.20V)	Vchg5	VCHG=4.20V		4.17	4.20	4.23	V
Overvoltage detection voltage	Vov	When battery voltage rising		4.27	4.35	4.43	V
Charge current detection block							
Quick charge current (0.5C)	Irapchg1	RICHG=2.7kohm, VBAT=3.5V		200	250	300	mA
Quick charge current (1.0C)	Irapchg2	RICHG=2.7kohm, VBAT=3.5V		450	500	550	mA
Trickle charge current (0.1C)	Iprechg	RICHG=2.7kohm, VBAT=2.5V		25	50	75	mA
Charge completion current (0.1C)	Ifc	RICHG=2.7kohm, CV control		25	50	75	mA
Timer circuit block							
Oscillation frequency	Foc	ROSC=110kohm		57.6	64	70.4	KHz
Trickle charge timer (normal)	Tdchg1	ROSC=110kohm, TIMER=normal Time from trickle charge start to Quick charge start	*1	54	60	66	min
Trickle charge timer (slow)	Tdchg2	ROSC=110kohm, TIMER=slow Time from trickle charge start to Quick charge start	*1	216	240	264	min
Quick charge timer (normal)	Tchg1	ROSC=110kohm, TIMER=normal Time from Quick charge start to Charge completion	*1	270	300	330	min
Quick charge timer (slow)	Tchg2	ROSC=110kohm, TIMER=slow Time from Quick charge start to Charge completion	*1	1080	1200	1320	min

*1 : design guarantee
*2 : Battery connection detection is shared

Electrical Characteristics

(Ta=25ºC, VADP=5V or VUSB=5V, unless otherwise specified.)

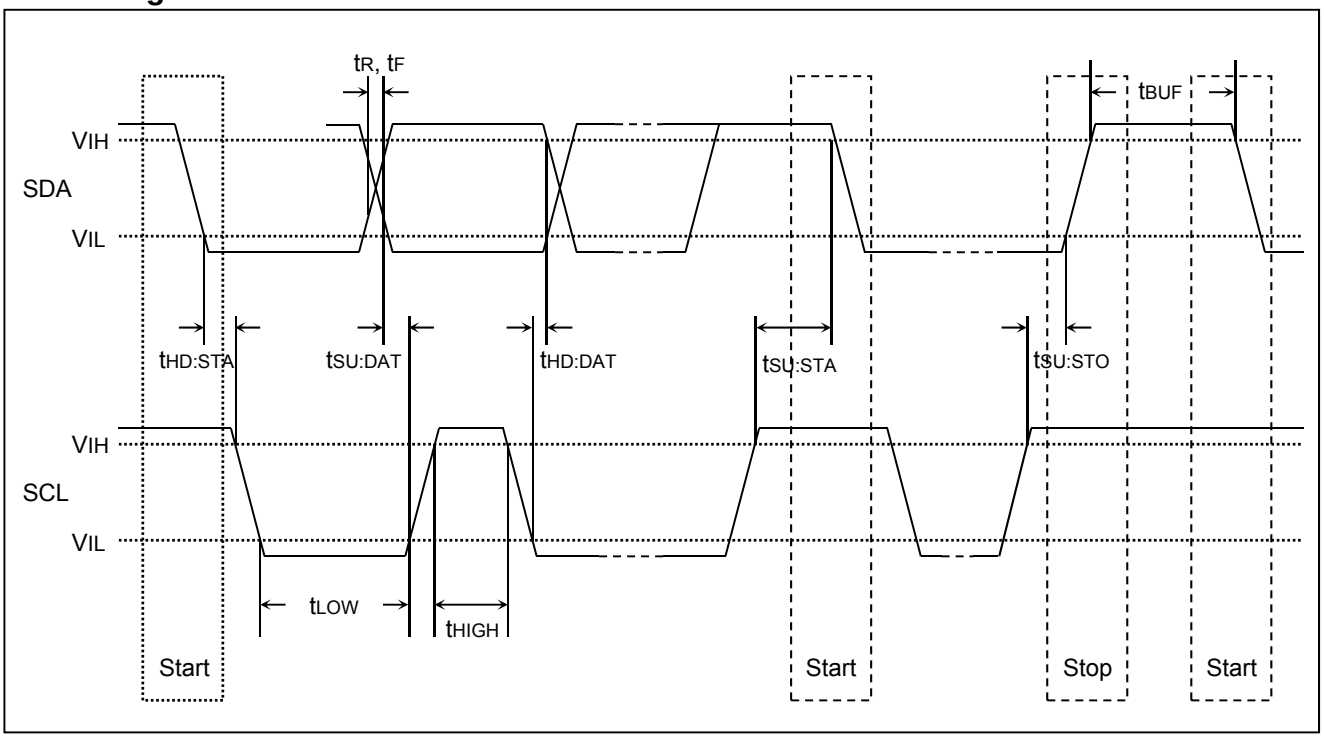
Item	Symbol	Condition		Rated value			Unit
				Min.	Typ.	Max.	
Charge control blcok							
Path SW On resistance between BAT and SYS	Ronb1	BAT to SYS current =0.5A VBAT=4.2V			38		mohm
Regulation voltage from BAT to SYS	Vregb	USB 100mA mode, Isys=200mA, BAT=4V			100		mV

I²C BUS Line Characteristics

Item	Symbol	Min.	Max.	Unit
SCL clock frequency	fSCL	0	400	kHz
Bus free time between STOP condition and START condition	tBUF	1.3	-	µs
START condition hold time (After this period, the first clock pulse is generated)	tHD:STA	0.6	-	µs
SCL low period	tLOW	1.3	-	µs
SCL high period	tHIGH	0.6	-	µs
START condition setup time	tSU:STA	0.6	-	µs
Data hold time	tHD:DAT	0	0.9	µs
Data setup time	tSU:DAT	100	-	ns
Rise time (SDA and SCL)	tR	-	300	ns
Fall time (SDA and SCL)	tF	-	300	ns
STOP condition setup time	tSU:STO	0.6	-	µs
Bus line capacitive load	Cb	-	400	pF

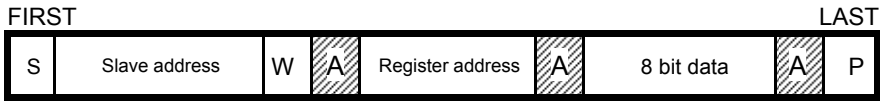
Note : Above values are specified by VIHmin and VILmax.

I²C Timing Chart

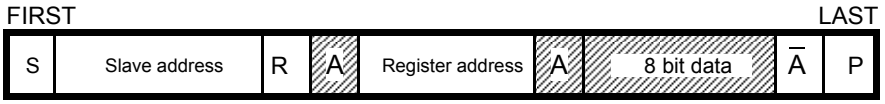


Digital Data Formats

1.Write mode: Data input from Master to R2J20052NS



2.Read mode: Data output from R2J20052NS to Master
(Master must input STOP condition without confirming Acknowledge bit when receiving last data.)

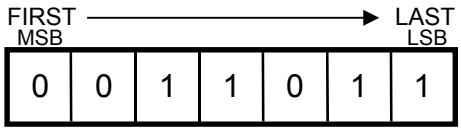


From Master to Slave(R2J20052NS)

From Slave(R2J20052NS) to Master

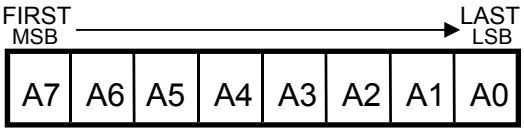
S : START condition
SDA goes High to Low when SCL=High.

Slave address

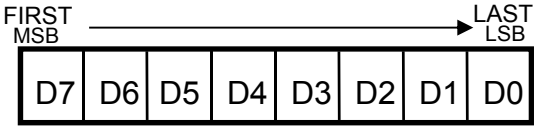


W : Write (SDA=Low)
R : Read (SDA=High)
A : Acknowledge bit (Master must set SDA=Low whenever receive slave data)
*$\overline{A}$: Master must input STOP condition without confirming Acknowledge bit when receiving last data in read mode. (Set SDA=High)

Register Address



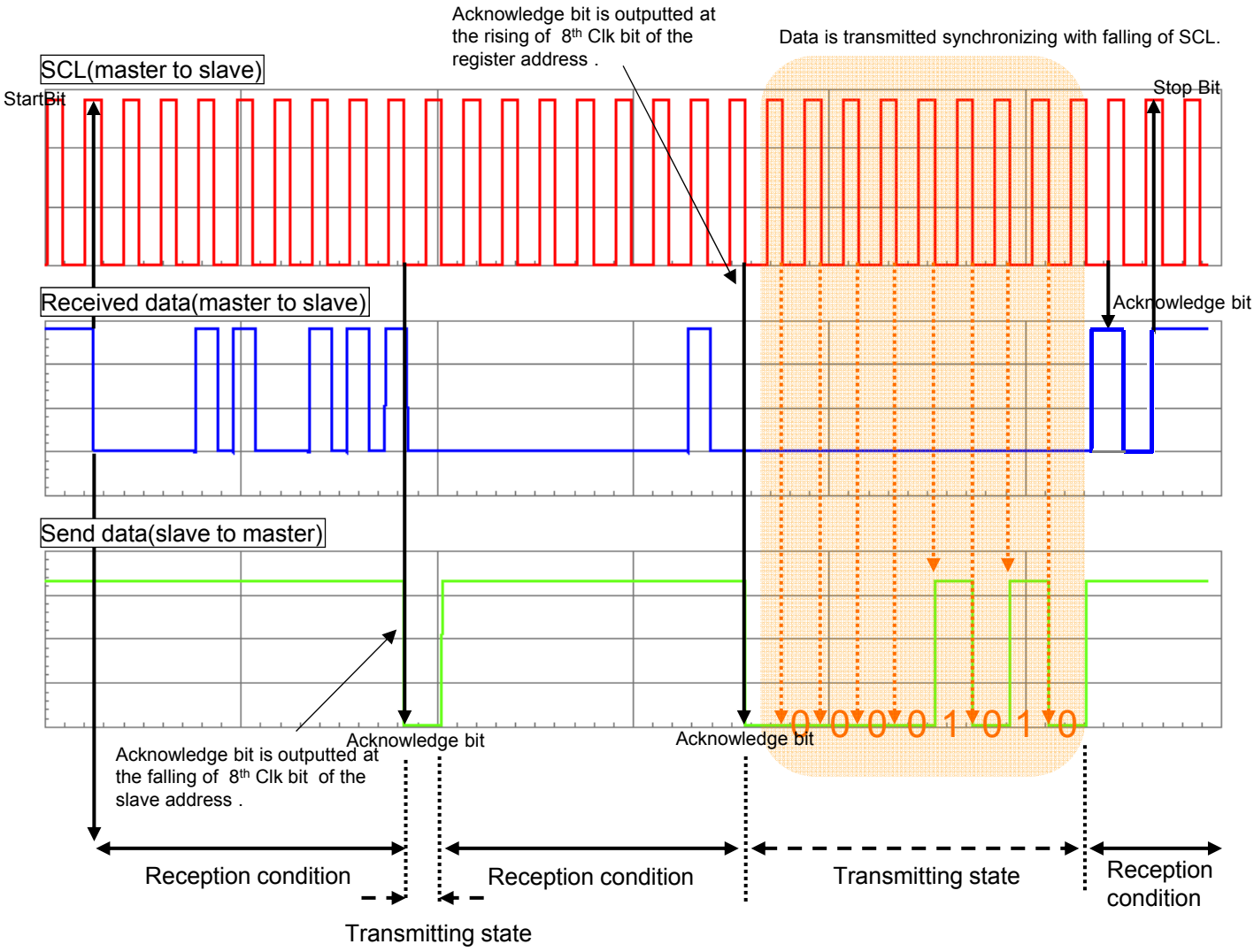
Data



P : STOP condition
SDA goes Low to High when SCL=High.

Timing chart when transmitting data to the I2C master from R2J20052NS

Conditions：Read [02H]
TOUT(Timeout)=H , /POKU=H(USB input voltage detect)=H



Register Map

ADR		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	R/W	(TEST2)	(TEST1)	(TEST0)		VCHG			ICHG
01H	R/W	USBMD	FULMD	TIMER		UCTL2			CEN2
02H	R		VBATH	NOBAT	FULL	TOUT	TSD	POKU	POKA
03H	R	(TEST5)	(TEST4)	(TEST3)		STAT3	STAT2	STAT1	STAT0

Note :
00H, 03H, and TEST0 ~ 6 : Must be set “0” (prohibited to use)

02H : Status Register (Read only)

	0	1
POKA	ADP voltage non-detection	ADP voltage detection
POKU	USB voltage non-detection	USB voltage detection
TSD	Nornal chip temperature	Abnornal chip temperature(IC stop)
TOUT	Timer OK	Timer OUT (Charge stop)
FULL	Charge non-completion	Charge completion
NOBAT	Battery detection	Battery non-detection
VBATH	Battery normal voltage	Battery over voltage

Note:
- When charge stops(CEN1=L or CEN2=0), FULL and TOUT are fixed “0”.
- When USB suspend mode ([(USBMD=0 and USUSP1=H) or (USBMD=1 and USUSP2=1)), FULL, TOUT, and POKU are fixed “0” regardless of the charge condition.

03H : Charge status register (Read only)

STAT3	STAT2	STAT1	STAT0	Input	Status
0	0	0	0	-	Default
0	0	0	1	ADP	Forced charge
0	0	1	0	ADP	Trickle charge
0	0	1	1	ADP	Quick charge
0	1	0	0	ADP	High temp. charge-1
0	1	0	1	ADP	High temp. charge-2
0	1	1	0	ADP	Charge completion
0	1	1	1	ADP/USB	Error
1	0	0	0	ADP/USB	Battery non-connection
1	0	0	1	USB	Forced charge
1	0	1	0	USB	Trickle charge
1	0	1	1	USB	Quick charge
1	1	0	0	USB	High temp. charge-1
1	1	0	1	USB	High temp. charge-2
1	1	1	0	USB	Charge completion

Register setting

*:Default setting

ADR=00H	ICHG	Quick charge current	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	*	0.5C	X	X	X	X	X	X	X	0
		1.0C	X	X	X	X	X	X	X	1
	VCHG	Charge voltage	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	*	4.00V	X	X	X	X	0	0	0	X
		4.05V	X	X	X	X	0	0	1	X
		4.10V	X	X	X	X	0	1	0	X
		4.15V	X	X	X	X	0	1	1	X
		4.20V	X	X	X	X	1	0	0	X

ADR=01H	CEN2	Charge enable	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W		Disable	X	X	X	X	X	X	X	0
	*	Enable	X	X	X	X	X	X	X	1
	UCTL2	USB input current limit	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	*	100mA	X	X	X	X	X	0	0	X
		500mA	X	X	X	X	X	0	1	X
		900mA	X	X	X	X	X	1	0	X
		1800mA	X	X	X	X	X	1	1	X
	USUSP2	USB suspend control	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	*	USB ENABLE	X	X	X	X	0	X	X	X
		USB SUSPEND	X	X	X	X	1	X	X	X
	TIMER	Timer control	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	*	Disable(reset)	X	X	0	0	X	X	X	X
		Enable(normal)	X	X	0	1	X	X	X	X
		Enable(slow) *2)	X	X	1	0	X	X	X	X
		Enable(count stop) *3)	X	X	1	1	X	X	X	X
	FULMD	Operation after charge completion detection	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	*	Stop charging	X	0	X	X	X	X	X	X
		Continue to charge(inform FULL status)	X	1	X	X	X	X	X	X
	USBMD	USB control select	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	*	Depend on UCTL1 terminal *1)	0	X	X	X	X	X	X	X
		Depend on UCTL2 register *1)	1	X	X	X	X	X	X	X

*1) When USBMD=0, Terminal setting (UCTL1 and USUSP1) is valid.
When USBMD=1, Register setting (UCTL2 and SUSP2) is valid.

*2) Slow : 4 times of normal mode (Trickle charge timer=240min., Quick charge timer=1200min.)

*3) Count stop : Timer is suspended. (Not reset)

Truth table of CEN1 and CEN2

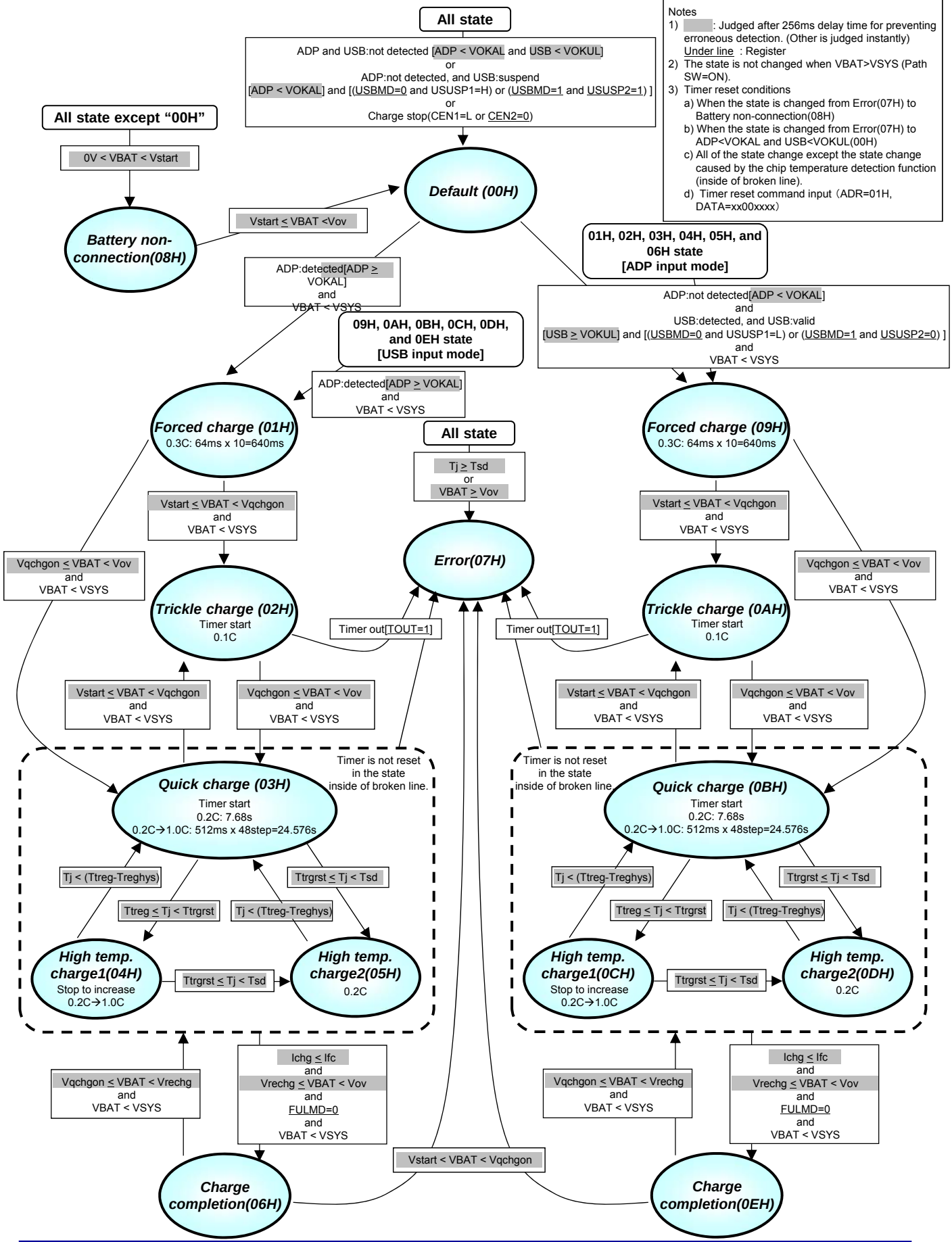
CEN1	CEN2	Operation
Terminal	Register	
Low	0	Charge disable
High	0	Charge disable
Low	1	Charge disable
High	1	Charge enable

Truth table of USUSP1 and USUSP2

USUSP1	USUSP2	USBMD	Operation
Terminal	Register	Register	
Low	-	0	USB normal
High	-	0	USB SUSPEND
-	0	1	USB normal
-	1	1	USB SUSPEND

When ADP>VOKAL, IC operates normally regardless of USUSPx.
When USB SUSPEND, USB input is invalid.

Charge state diagram



Recovery from Error status (07H)

Thermal shutdown

Once IC enters the error mode by thermal shutdown, IC cannot recover from the error mode automatically even if chip temperature falls under tsd.
For recovering from the error mode, the recovery sequence is needed after chip temperature falls under tsd.

Battery over-voltage detection

Once IC enters the error mode by battery over-voltage, IC cannot recover from the error mode automatically even if VBAT falls under Vov.
For recovering from the error mode, the recovery sequence is needed after VBAT falls under Vov.

Timer out

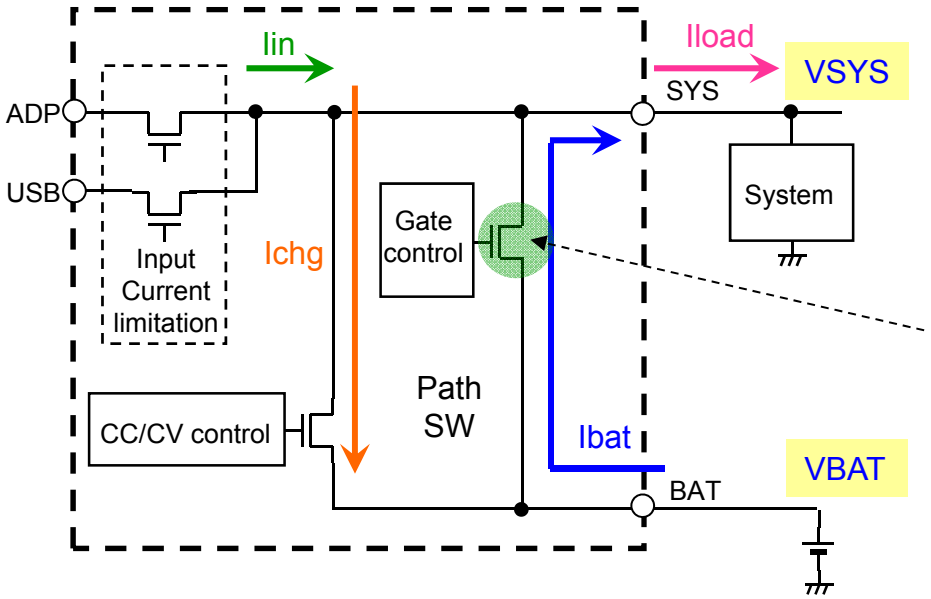
The recovery sequence is needed to reset timer and restart to charge after entering to the error mode by timer out.

***) The recovery sequence :**

"Disconnect both ADP and USB (ADP < VOKAL and USB < VOKUL)" or
"Disconnect the battery (0V < VBAT < Vstart)"

Function

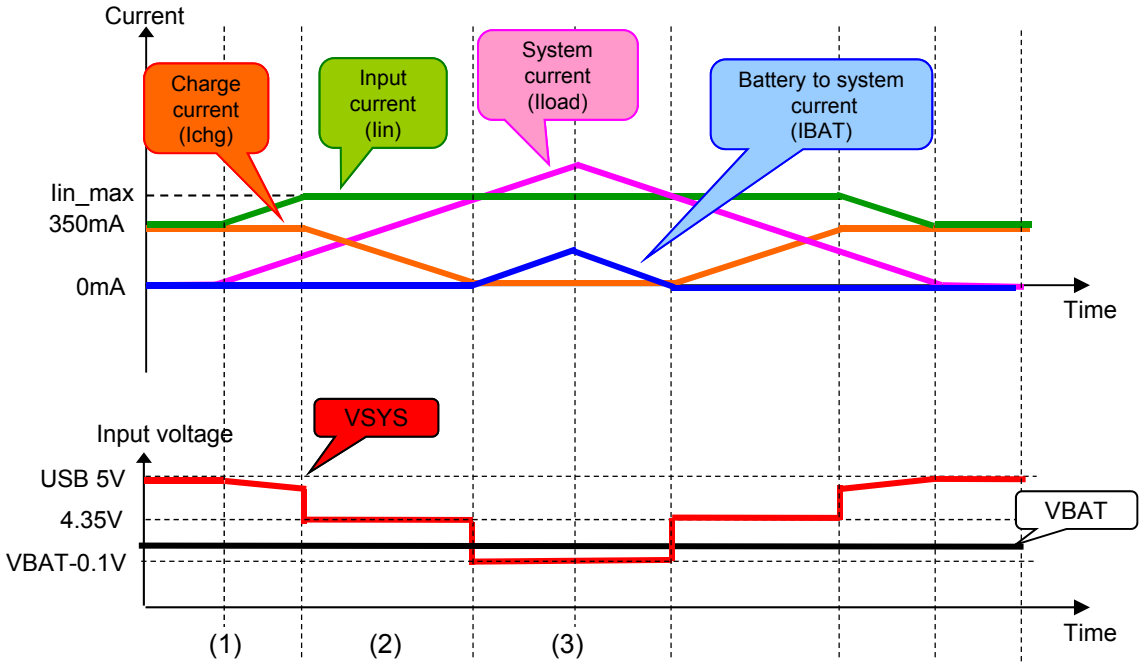
Power path control



Condition	Path SW
VSYS > VBAT	Off
VSYS < VBAT	On

Example of system current control

Conditions : USB=5.0V is connected, Iin_max=500mA, Ichg=350mA, Chargeable battery is connected

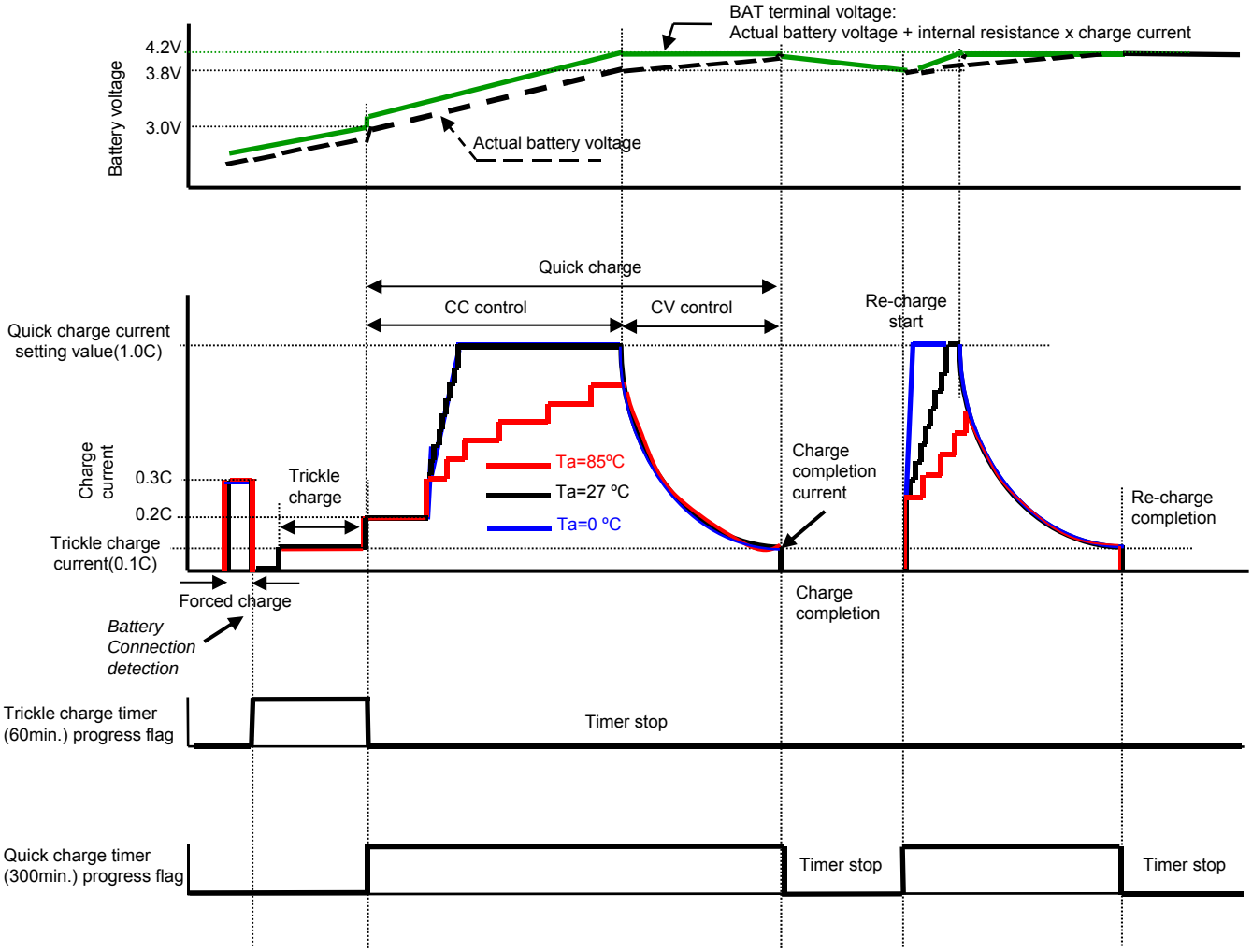


(1) IC charges the battery at Ichg=350mA and supplies the system current(Iload) within Iin_max=500mA.

(2) When the system current(Iload) increases and the total sum of Iload and Ichg reachs Iin_max, IC reduces the charge current.. (the power not used by the system charges the battery)

(3) When the system current (Iload) increases more and Iload exceeds Iin_max, VSYS falls to Vbat-0.1V and the battery supplies the load current to system through the Path SW. (IC attempts to sustain the system voltage no matter what causes it to drop.)

Timing chart



Note:
During quick charge, junction temperature is monitored to limit charge current value between 0.2C-1.0C so that the junction temperature may not exceed Ttreg.

Operating examination

ADP input current limit setting

ADP input current limit setting value = (Ref. voltage 1.44V/RILMTA [KΩ]) X (1800～2200*) (mA)
* coefficient changes by ADP input current limit setting value.

Standard characteristics of ADP input current limit (for reference)

RILMTA resister setting (KΩ)	ADPinput current limit setting (mA)
27.00	102
5.40	524
2.70	1024
1.80	1500
1.50	1784
1.35	1958
1.30	2035

Quick charging current setting (1.0C CC charging)

charging current 1.0C= (Ref, voltage 1.64V/RICHG [KΩ]) X (720～880*) (mA)
* coefficient changes by charging current.

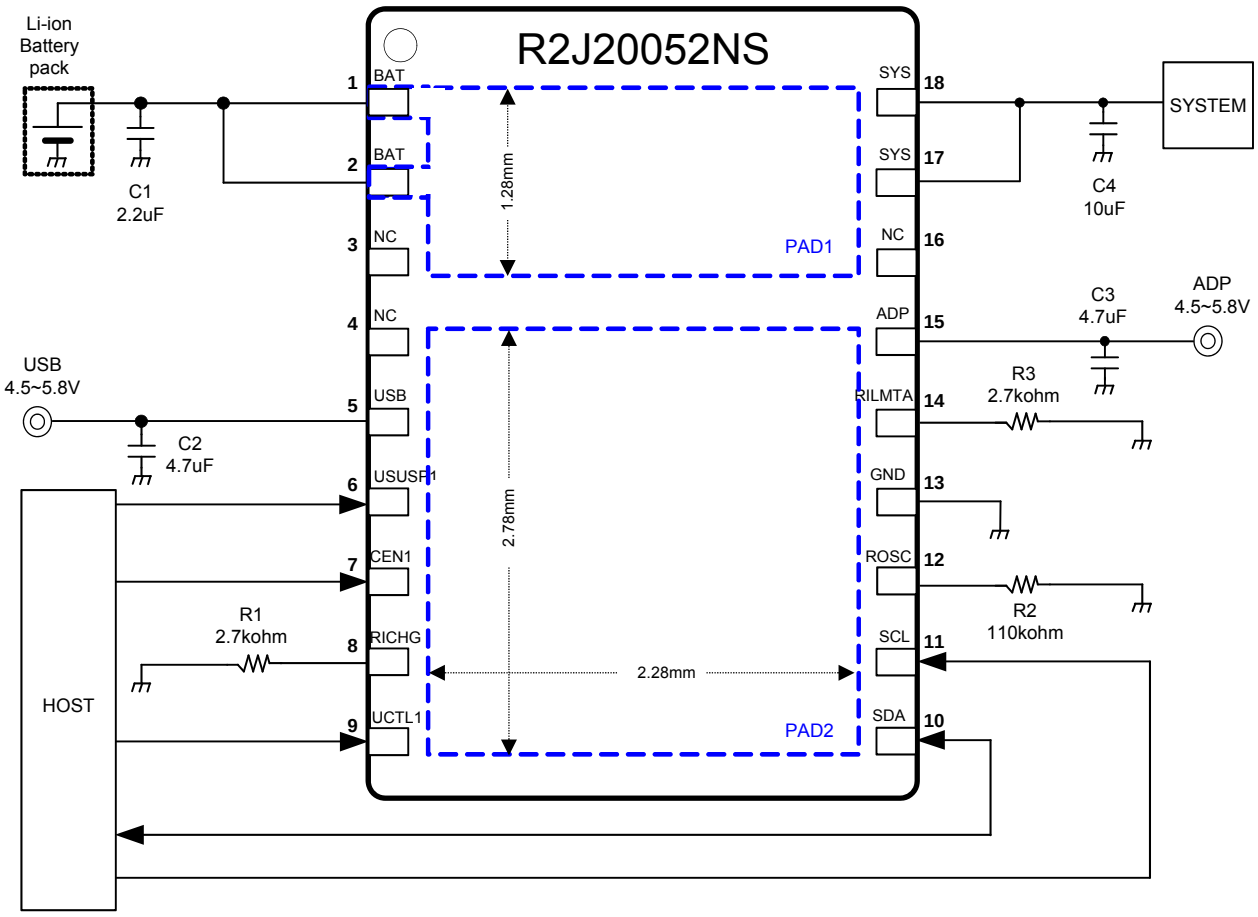
Standard specification of charging current setting (for reference)

Quick charging current setting (mA)	Ref. current (uA)	RICHG resistance setting value (kΩ)
1000	1280	1.28
900	1130	1.45
800	1000	1.64
700	870	1.89
600	720	2.28
500	608	2.70
400	482	3.40
300	361	4.54
200	241	6.80

Reference of ROSC setting resistance value, oscillation frequency and timer

ROSC resistance value (kΩ)	oscillation frequency (kHz)	Timer calculate value			
		trickle charge timer60(min) (normal)	trickle charge timer240(min) (slow)	quick charge timer300(min) (normal)	quick charge timer1200(min) (slow)
GND short	1172.0	3.3	13.1	16.4	65.5
10	419.6	9.2	36.6	45.8	183.0
20	264.0	14.5	58.2	72.7	290.9
55	116.6	32.9	131.7	164.6	658.5
110	64.0	60.0	240.0	300.0	1200.0
195	37.8	101.6	406.2	507.8	2031.0
510	15.4	249.0	995.9	1244.9	4979.5

Application circuit



Note :

PAD1: Must be connected to BAT plane (Terminal-1,2)

PAD2: Must be connected to Ground plane (for heat radiation)

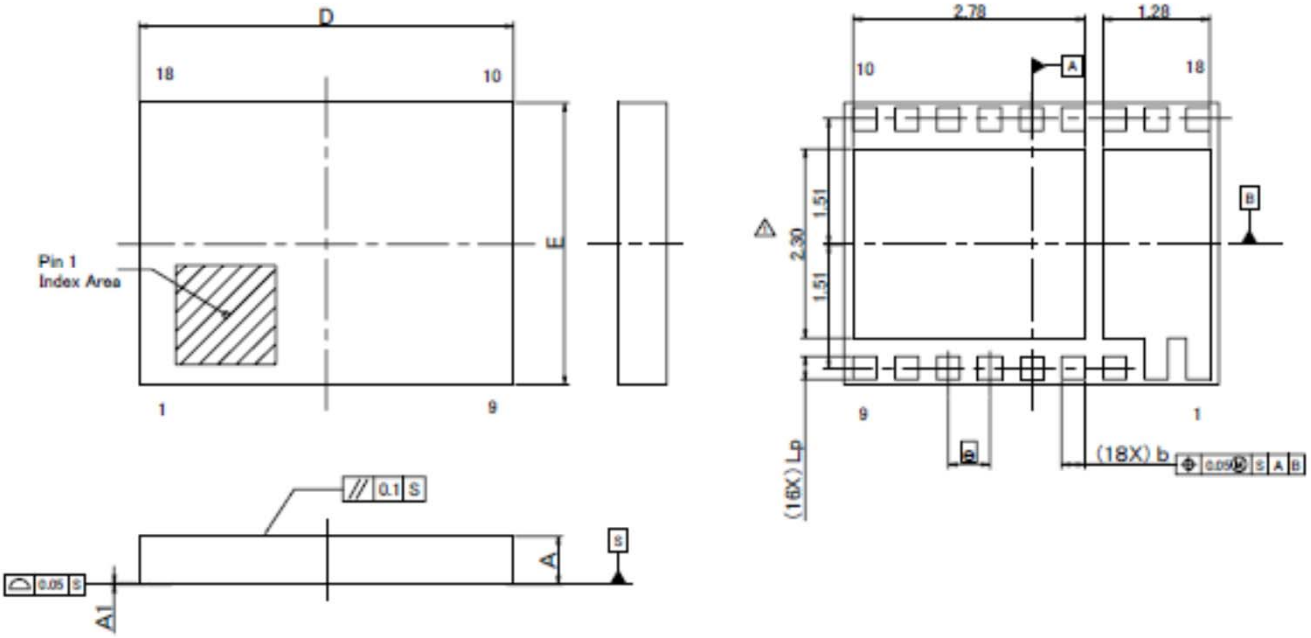
Notes on usage

1) SYS terminal must not be shortcircuited to GND. If SYS terminal is shortcircuited to GND when the battery is connected, Large current may flow from BAT terminal to SYS terminal via Path SW(built-in 38mohm MOSFET).
   If large current continues to flow, IC may be damaged seriously.

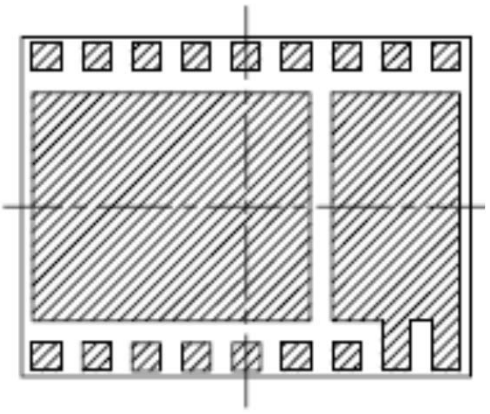
2) In case of FULMD=1, FULL register outputs “1” and IC continues to charge even if when charge current falls below 0.1C. Host side needs to stop charging.
   In this case, the safety timer is activated even if when charge current falls below 0.1C.
   So charge operation is stopped after 300min quick charge timer.
   But if TIMER register is set to Enable(count stop), charge operation is not stopped.

3) IC power dissipation must not exceed the package allowance power dissipation(Pd).
   PAD2 must be soldered to large ground plane for heat radiation.

Package dimensions



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	0.60
A_1	0	–	0.01
b	0.23	0.28	0.33
D	4.40	4.50	4.60
E	3.30	3.40	3.50
e	——	0.5	——
Lp	0.23	0.28	0.33



パッケージ裏面ソルダビリティ保証範囲
Solderability effective area

UNIT:mm