Click here for production status of specific part numbers.

MAX98395

Digital Input Class DG Amplifier with I/V Sense and Ultra-Low Quiescent Power

General Description

The MAX98395 is a high-efficiency, mono Class-DG speaker amplifier with industry leading quiescent power featuring I/V sense and dynamic headroom tracking (DHT). Precision output current and voltage monitoring (I/V sense) enables speaker protection algorithms to be run by a host device. Spread spectrum modulation (SSM) and edge rate control minimize EMI and eliminate the need for the output filtering found in traditional Class-D devices.

To achieve industry-leading quiescent power, the Class-DG amplifier employs two supply rails, VBAT and PVDD, to supply the speaker amplifier. Additionally, as the power-supply voltage varies due to sudden transients and declining battery life, DHT automatically optimizes the headroom available to the Class-DG amplifier to maintain consistent distortion and listening levels. The DHT block provides both a dynamic range compressor (DRC) and a limiter that can operate as either a signal distortion limiter (SDL) or standard signal level limiter (SLL).

The device provides a PCM interface for audio data and a standard I^2C interface for control data communication. The PCM interface supports audio playback using I^2S, left-justified, and TDM audio data formats. In TDM mode, the device can support up to 16 channels of audio data. A unique clocking structure eliminates the need for an external master clock for PCM communication, which reduces pin count and simplifies board layout.

Thermal-foldback protection ensures robust behavior when the thermal limits of the device are reached. When enabled, it automatically reduces the output power when the temperature exceeds a user-specified threshold. This allows for uninterrupted music playback even at high ambient temperatures. Traditional thermal protection is also available in addition to robust overcurrent protection.

The device is available in a 0.4mm pitch, 28-bump wafer-level package (WLP). The device operates over the extended -40°C to +85°C temperature range.

Applications

- Mobile Speakers
- Smart Speakers
- Smart IoT
- Tablets
- Notebook Computers
- Soundbars

Benefits and Features

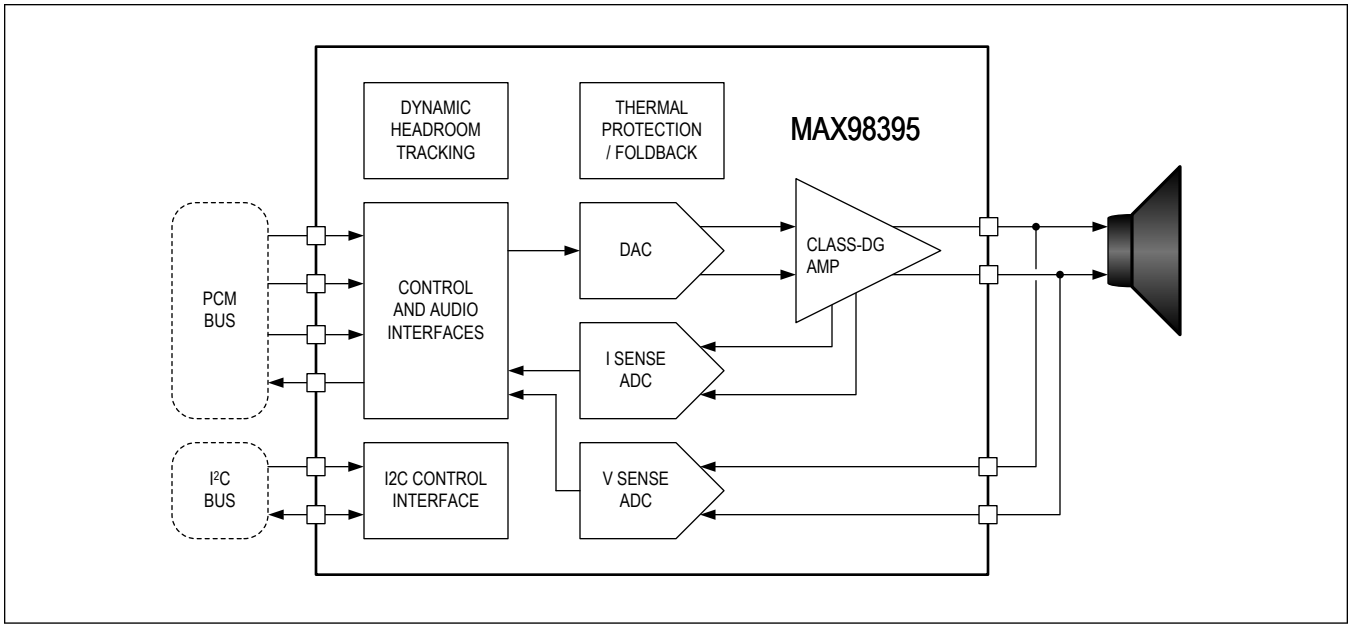
- Wide Input Supply Range (3.0V to 14V)
- Class-DG Operation Enables Industry Leading Quiescent Power
  - 16mW at V_{PVDD} = 3.8V
  - 15mW at V_{PVDD} = 12V
- Ultra-Low Noise Floor
  - 11µV_{RMS} Output Noise
  - 116dB Dynamic Range
- Low Distortion
  - -83dB THD+N at 2W into 8Ω, f = 1kHz and 3kHz
  - -77dB THD+N at 2W into 8Ω, f = 6kHz
- Output Power at 1% THD+N:
  - 7.7W into 8Ω, V_{PVDD} = 12V
  - 11.7W into 4Ω, V_{PVDD} = 12V
- Speaker Amplifier Efficiency:
  - 88% at 5W into 8Ω, V_{PVDD} = 12V
- Class-D EMI Reduction Enables Filterless Operation
  - Spread-Spectrum Modulation
  - Switching Edge Rate Control
- Integrated Speaker Current and Voltage Sense Requires no External Components
- I^2S/16-Channel TDM and I^2C Digital Interfaces
- Playback and IV Paths Support Sample Rates up to 96kHz
- Dynamic Headroom Tracking (DHT) Maintains a Consistent Listening Experience
- Extensive Click-and-Pop Suppression
- 28-Bump WLP (1.62mm x 2.88mm x 0.5mm, 0.4mm Pitch)

***Ordering Information* appears at end of data sheet.**

19-100672; Rev 0; 10/19

maxim integrated™

Simplified Block Diagram



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AGND, DGND to PGND ..... -0.1V to +0.1V
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OUTP, OUTN to PGND ..... -0.3V to V_{PVDD} + 0.3V
OUTPSNS, OUTNSNS to PGND ..... -0.3V to +16V
VREFC to GND ..... -0.3V to +5.5V
I2C1, I2C2, ADDR to GND ..... -0.3V to +4.0V
All Other Digital Pins to DGND ..... -0.3V to V_{DVDDIO} + 0.3V
Short-Circuit Duration Between OUTP, OUTN and PGND, or PVDD or VBAT ..... Continuous
Short-Circuit Duration Between OUTP and OUTN ..... Continuous
Continuous Power Dissipation for Multilayer Board (T_A = +70°C, derate 23.47mW/°C above +70°C.) 1.88W
Junction Temperature ..... +150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28 Bump WLP

Package Code	N281B2+2
Outline Number	21-100393
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	42.6°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
VBAT Power-Supply Operating Voltage Range	V_{VBAT}		3.0		5.5	V
VBAT Voltage	V_{VBAT}	No sustained oscillations	2.3			V
PVDD Power-Supply Operating Voltage Range	V_{PVDD}		3.0		14	V
PVDD Voltage	V_{PVDD}	No sustained oscillations	2.3			V
AVDD Power-Supply Voltage Range	V_{AVDD}		1.71	1.8	1.89	V
DVDD Power-Supply Voltage Range	V_{DVDD}		1.14	1.2	1.89	V

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DVDDIO Power-Supply Voltage Range	V_{DVDDIO}			1.14	1.2	1.26	V
				1.71	1.8	1.89	
VBAT Undervoltage Lockout	V_{VBAT_UVLO}	V_{VBAT} falling		1.8		2.2	V
PVDD Undervoltage Lockout	V_{PVDD_UVLO}	V_{PVDD} falling		1.93		2.26	V
VBAT UVLO Hysteresis		Note 3		35			mV
PVDD UVLO Hysteresis		Note 3		30			mV
Supply Ramp Rate PVDD				0.1		100	V/ms
POWER CONSUMPTION / QUIESCENT POWER CONSUMPTION							
Total Power Consumption	P_Q	All supplies, IV sense enabled	V_{PVDD} = 12V, DG mode		14.5	24	mW
			V_{PVDD} = 12V, PVDD mode		43	70	
Total Power Consumption	P_Q	All supplies, IV sense enabled	V_{PVDD} = 3.8V, PVDD mode		15.3	24	mW
			V_{PVDD} = 12V, DG mode, noise gate enabled		1.52	2.8	
Total Power Consumption	P_Q	All supplies, IV sense disabled	V_{PVDD} = 12V, DG mode		10.6		mW
Total Power Consumption	P_Q	All supplies, IV sense disabled	V_{PVDD} = 12V, noise gate enabled		1.5		mW
PVDD Quiescent Current	I_{Q_PVDD}	IV sense enabled, V_{PVDD} = 12V, DG mode			275	450	µA
VBAT Quiescent Current	I_{VBAT}	IV sense enabled, V_{PVDD} = 12V, DG mode			1.7	2.7	mA
AVDD Quiescent Current	I_{AVDD}	IV sense enabled, V_{PVDD} = 12V, DG mode			1.9	3.3	mA
DVDD Quiescent Current	I_{DVDD}	IV sense enabled, V_{PVDD} = 12V, DG mode			1.1	1.6	mA
DVDDIO Quiescent Current	I_{DVDDIO}	IV sense enabled, V_{PVDD} = 12V, DG mode			10	85	µA
POWER CONSUMPTION / SOFTWARE SHUTDOWN							
VBAT Software Shutdown Supply Current	$I_{SHDN\_SW\_VBAT}$	VBAT = 3.8V, no BCLK/LRCLK/DIN transactions, T_A = +25°C			1	5	µA
		VBAT = 3.8V, no BCLK/LRCLK/DIN transactions, T_A = +85°C				15	

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PVDD Software Shutdown Supply Current	$I_{SHDN\_SW\_PVDD}$	PVDD = 3.8V, no BCLK/LRCLK/DIN transactions, T_A = +25°C		1	5	µA
		PVDD = 3.8V, no BCLK/LRCLK/DIN transactions, T_A = +85°C			15	
		PVDD = 12V, no BCLK/LRCLK/DIN transactions, T_A = +25°C		1	5	
		PVDD = 12V, no BCLK/LRCLK/DIN transactions, T_A = +85°C			15	
AVDD Software Shutdown Supply Current	$I_{SHDN\_SW\_AVDD}$	No BCLK/LRCLK/DIN transactions, T_A = +25°C		10	20	µA
		No BCLK/LRCLK/DIN transactions, T_A = +85°C			30	
DVDDIO+DVDD Software Shutdown Supply Current	$I_{SHDN\_SW\_DVDD\_DVDDIO}$	No BCLK/LRCLK/DIN transactions, T_A = +25°C		6.5	15	µA
		No BCLK/LRCLK/DIN transactions, T_A = +85°C			18	
POWER CONSUMPTION / HARDWARE SHUTDOWN						
VBAT Hardware Shutdown Supply Current	$I_{SHDN\_HW\_VBAT}$	VBAT = 3.8V, T_A = +25°C		0.5	5	µA
		VBAT = 3.8V, T_A = +85°C			15	
PVDD Hardware Shutdown Supply Current	$I_{SHDN\_HW\_PVDD}$	PVDD = 3.8V, T_A = +25°C		0.5	5	µA
		PVDD = 3.8V, T_A = +85°C			15	
		PVDD = 12V, T_A = +25°C		1	5	
		PVDD = 12V, T_A = +85°C			15	
AVDD Hardware Shutdown Supply Current	$I_{SHDN\_HW\_AVDD}$	T_A = +25°C		0.1	1	µA
		T_A = +85°C			10	
DVDDIO+DVDD Hardware Shutdown Supply current	$I_{SHDN\_HW\_DVDD\_DVDDIO}$	T_A = +25°C		0.14	5.8	µA
		T_A = +85°C			6.4	
TURN-ON/OFF TIME						
Turn-On Time	t_{ON}	From EN bit set to 1 to full operation, volume ramp disabled (Note 4)		1.2	3	ms
		From EN bit set to 1 to full operation, volume ramp enabled (Note 4)		2.9	6	ms
		From SPK_EN bit set to 1 to full operation, EN = 1, volume ramp disabled		0.75		ms

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_s = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-Off Time	t_{OFF}	From full operation, EN bit set to 0 to software shutdown, volume ramp disabled		30	100	µs
		From full operation, EN bit set to 0 to software shutdown, volume ramp enabled		1.9	6	ms
		From SPK_EN bit set to 0 to amplifier disabled, EN = 1		0.025		ms
DIGITAL AUDIO PATH						
DIGITAL AUDIO PATH / GAIN CONTROLS / DIGITAL VOLUME CONTROL						
Digital Volume Control (max)	A_{SPK_VOL}	SPK_VOL[6:0] = 0x00		0		dB
Digital Volume Control (min)	A_{SPK_VOL}	SPK_VOL[6:0] = 0x7E		-63		dB
Digital Volume Control Step Size				0.5		dB
DIGITAL AUDIO PATH / FILTERING / DIGITAL HIGHPASS FILTER CHARACTERISTICS (Note 5)						
DC Attenuation			80			dB
DC Blocking Cut Off Frequency		Across all sample rates		1.872		Hz
DIGITAL AUDIO PATH / FILTERING / DIGITAL FILTER CHARACTERISTICS (LRCLK < 50kHz) (Note 5)						
Valid Sample Rates			16		48	kHz
Passband Cutoff	f_{PLP}	Ripple < δ_P	0.454 x f_S			Hz
	f_{PLP}	Droop < -3dB	0.459 x f_S			Hz
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}	Attenuation > δ_S			0.49 x f_S	Hz
Stopband Attenuation	δ_S	f > f_{SLP}	75			dB
Group Delay		f = 1kHz		8		samples
DIGITAL AUDIO PATH / FILTERING / DIGITAL FILTER CHARACTERISTICS (LRCLK > 50kHz) (Note 5)						
Valid Sample Rates			88.2		96	kHz
Passband Cutoff	f_{PLP}	Ripple < δ_P, 88.2kHz ≤ f_S ≤ 96kHz	0.227 x f_S			Hz
	f_{PLP}	Droop < -3dB, 88.2kHz ≤ f_S ≤ 96kHz	0.314 x f_S			Hz
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz	-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}	Attenuation < δ_S			0.49 x f_S	Hz
Stopband Attenuation	δ_S	f > f_{SLP}	80			dB

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Max Group Delay		f = 1kHz		12		samples
Max Device-to-Device Group Delay Variability		f_{IN} = 1kHz		1		µs
CLASS-DG AMPLIFIER						
Output Offset Voltage	V_{OS}	T_A = 25C, Z_{SPK} = 8Ω + 33µH, DRE_EN = 0, SPK_GAIN_MAX = 0xE	-3	±1	+3	mV
Click-and-Pop Level	K_{CP}	Peak voltage, EN 0-->1 or EN 1-->0, audio playback silent, A-weighted, 32 samples per second, T_A = +25°C (Note 6)		-66		dBV
Efficiency	η_{SPK}	P_{OUT} = 5W, Z_L = 8Ω + 33µH, f_{IN} = 1kHz		89		%
	η_{SPK}	P_{OUT} = 5W, Z_L = 4Ω + 33µH, f_{IN} = 1kHz		81.5		
Output Power	P_{OUT}	V_{PVDD} = 12V, Z_L = 8Ω + 33µH, THD+N ≤ 1%, f_{IN} = 1kHz		7.7		W
		V_{PVDD} = 14V, Z_L = 8Ω + 33µH, THD+N ≤ 1%, f_{IN} = 1kHz		10.5		
		V_{PVDD} = 12V, Z_L = 4Ω + 33µH, THD+N ≤ 1%, f_{IN} = 1kHz		11.7		
		V_{PVDD} = 12V, Z_L = 8Ω + 33µH, THD+N ≤ 10%, f_{IN} = 1kHz		9.6		
		V_{PVDD} = 14V, Z_L = 8Ω + 33µH, THD+N ≤ 10%, f_{IN} = 1kHz		12.9		
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1kHz, P_{OUT} = 2W, Z_L = 8Ω + 33µH, Note 3	-73	-83		dB
		f_{IN} = 1kHz, P_{OUT} = 2W, Z_L = 4Ω + 33µH		-79		
		f_{IN} = 6kHz, P_{OUT} = 2W, Z_L = 8Ω + 33µH	-70	-77		
		f_{IN} = 6kHz, P_{OUT} = 2W, Z_L = 4Ω + 33µH		-75		
Intermodulation Distortion		ITU-R standard, f_{IN}= 19kHz/20kHz, V_{IN} = -3dBFS		-76		dB
Dynamic Range	DR	Measured using EIAJ method, -60dB at 1kHz output signal referenced to output power at 1%THD+N, A-weighted (Note 3)	112	116		dB
Output Noise	e_N	A-weighted		11		μV_{RMS}
CLASS-DG AMPLIFIER / POWER-SUPPLY RIPPLE REJECTION						
VBAT Supply DC Rejection	PSRR	V_{VBAT} = 3.0 to 5.5V		90		dB

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VBAT Supply Rejection AC	PSRR	V_{RIPPLE} = 100mV_{P-P}	f_{RIPPLE} = 217Hz (Note 3)	77	90		dB
			f_{RIPPLE} = 1kHz (Note 3)	77	87		
			f_{RIPPLE} = 20kHz (Note 3)	56	65		
PVDD Supply DC Rejection	PSRR	V_{PVDD} = 3.0 to 14V			100		dB
PVDD Supply Rejection AC	PSRR	V_{RIPPLE} = 100mV_{P-P}	f_{RIPPLE} = 217Hz (Note 3)	93	100		dB
			f_{RIPPLE} = 1kHz (Note 3)	93	100		
			f_{RIPPLE} = 20kHz (Note 3)	73	78		
AVDD Supply DC Rejection	PSRR	V_{AVDD} = 1.71V to 1.89V			100		dB
AVDD Supply Rejection AC	PSRR	V_{RIPPLE} = 100mV_{P-P}	f_{RIPPLE} = 217Hz		90		dB
			f_{RIPPLE} = 1khz		90		
			f_{RIPPLE} = 20Khz		85		
DVDD Supply DC Rejection	PSRR	V_{DVDD} = 1.14 to 1.89V			100		dB
DVDD Supply Rejection AC	PSRR	V_{RIPPLE} = 100mV_{P-P}	f_{RIPPLE} = 217Hz		90		dB
			f_{RIPPLE} = 1khz		90		
			f_{RIPPLE} = 20Khz		90		
DVDDIO Supply DC Rejection	PSRR	V_{DVDDIO} = 1.14 to 1.89V			100		dB
DVDDIO Supply Rejection AC	PSRR	V_{RIPPLE} = 100mV_{P-P}	f_{RIPPLE} = 217Hz		95		dB
			f_{RIPPLE} = 1khz		95		
			f_{RIPPLE} = 20Khz		95		

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CLASS-DG AMPLIFIER / POWER-SUPPLY INTERMODULATION							
Power-Supply Intermodulation		f_{IN} = 1kHz, P_{OUT} = 400mW	V_{VBAT}, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{P-P}		-75		dB
			V_{PVDD}, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{P-P}		-85		
			V_{AVDD}, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{P-P}		-70		
			V_{DVDD}, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{P-P}		-70		
			V_{DVDDIO}, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{P-P}		-70		
Output Switching Frequency		Constant across all sample rates in the 48kHz family			472		kHz
		Constant across all sample rates in the 44.1kHz family			451		
Frequency Response Deviation		Across the bandwidth 20Hz to 20kHz referenced to f_{IN} = 1kHz (Note 3)		-0.25		+0.25	dB
Gain Error	A_{VERROR}			-0.5		+0.5	dB
Channel-to-Channel Phase Error		Output phase shift between multiple devices from 20Hz to 20kHz, across all sample rates and DAI operating modes			1		°
Minimum Load Resistance					3.2		Ω
Minimum Load Inductance		In series with a 3.2Ω load			0		µH
Maximum Load Inductance		In series with a 3.2Ω load			100		µH
Current Limit	I_{LIM}			4.5	6.0		A
SPEAKER VOLTAGE ADC							
Resolution					16		Bits
Sample Rate	$f_{SVSNS\ ADC}$			8		192	kHz
Voltage Range	V_{SPK}				±15.4		V
Dynamic Range	DNR	f_{IN} = 1kHz, AC measurement bandwidth = 20Hz-20kHz, unweighted			80.5		dB
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1kHz, V_{SPK} = 6V_{RMS}			-68		dB

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_s = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Mode Gain		T_A = +25°C	0.98		1.02	
Differential Mode Gain Variability		Across supplies, T_A = -40°C to +85°C	-1.0		+1.1	%
Maximum Common Mode Gain		T_A = +25°C		-60		dB
Maximum Common Mode Gain Variability		Across supplies, T_A = -40°C to +85°C		0.1		dB
DC Offset Voltage		DC blocking filter enabled	-0.2		+0.2	mV
		DC blocking filter disabled, T_A = +25°C	-10		+10	
DC Offset Variability		Across supplies, T_A = -40°C to +85°C		7		mV
Highpass Cutoff Frequency		-3dB limit, across all sample rates			2	Hz
SPEAKER VOLTAGE ADC / DIGITAL FILTER CHARACTERISTICS (f_S < 50kHz) (Note 5)						
Passband Ripple		$f_{IN} \le f_{PLP}$	-0.225		+0.225	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	-3dB limit	$0.44f_S$			Hz
Lowpass Filter Stopband Frequency	f_{SLP}	-40dB limit			$0.58 \times f_S$	Hz
Lowpass Filter Stopband Attenuation			40			dB
Max Group Delay		f_{IN} = 1kHz		8		Samples
SPEAKER VOLTAGE ADC / DIGITAL FILTER CHARACTERISTICS (f_S > 50kHz) (Note 5)						
Passband Ripple		$f_{IN} \le f_{PLP}$	-0.1		+0.1	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	-3dB limit	$0.23f_S$			Hz
Lowpass Filter Stopband Frequency	f_{SLP}	-40dB limit			$0.58f_S$	Hz
Lowpass Filter Stopband Attenuation			40			dB
Max Group Delay		f_{IN} = 1kHz		10		Samples
SPEAKER CURRENT ADC						
Resolution				16		Bits
Sample Rate	$f_{SISNS\ ADC}$		8		96	kHz
Current Range	I_{SPK}			±3		A
Dynamic Range	DNR	f_{IN} = 1kHz, AC measurement bandwidth = 20Hz to 20kHz, unweighted, referred to $2A_{PEAK}$		73		dB
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1kHz, $I_{SPK} = 0.75A_{RMS}$		-60		dB

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_s = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Mode Gain			0.98		1.02	
Differential Mode Gain Variability		Across supplies, T_A = -40°C to +85°C	-2.5		+2.5	%
Maximum Common Mode Gain				-60		dB
Common Mode Gain Variability		Across supplies, T_A = -40°C to +85°C		0.1		dB
Highpass Cutoff Frequency		-3dB limit, across all sample rates			2	Hz
DC Offset Current		DC blocking filter enabled, T_A = +25°C	-0.12		+0.12	mA
		DC blocking filter disabled, T_A = +25°C (Note 3)	-3		+3	
DC Offset Variability		Across supplies, T_A = -40°C to +85°C, DC blocking filter disabled		2		mA
Voltage and Current Accuracy Drift Tracking		T_A = 0°C to +85°C, relative to +25°C		0.4		%
SPEAKER CURRENT ADC / DIGITAL FILTER CHARACTERISTICS (f_S < 50 kHz) (Note 5)						
Passband Ripple		$f_{IN} \le f_{PLP}$	-0.225		+0.225	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	-3dB limit	$0.44f_S$			Hz
Lowpass Filter Stopband Frequency	f_{SLP}	-40dB limit			$0.58f_S$	Hz
Lowpass Filter Stopband Attenuation			40			dB
Max Group Delay		f_{IN} = 1kHz		8		Samples
SPEAKER CURRENT ADC / DIGITAL FILTER CHARACTERISTICS (f_S > 50 kHz) (Note 5)						
Passband Ripple		$f_{IN} \le f_{PLP}$	-0.1		+0.1	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	-3dB limit	$0.23f_S$			Hz
Lowpass Filter Stopband Frequency	f_{SLP}	-40dB limit			$0.58f_S$	Hz
Lowpass Filter Stopband Attenuation			40			dB
Max Group Delay		f_{IN} = 1kHz		10		Samples
MEASUREMENT ADC						
PVDD Channel Input Voltage Range			2.5		14.5	V
PVDD Channel Voltage Resolution				23.4375		mV

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_s = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PVDD Channel Measurement Accuracy		Note 3	-100		+100	mV
VBAT Channel Input Voltage Range			2.5		5.5	V
VBAT Channel Voltage Resolution				23.4375		mV
VBAT Channel Measurement Accuracy		Note 3	-100		+100	mV
THERMAL PROTECTION						
Thermal Shutdown Trigger Point		THERMSHDN_THRESH = 0x27	140	150	160	°C
DIGITAL I/O / INPUT—DIN, BCLK, LRCLK, $\overline{RESET}$, ICC						
Input Voltage High	V_{IH}		0.7 x V_{DVDDIO}			V
Input Voltage Low	V_{IL}				0.3 x V_{DVDDIO}	V
Input Leakage Current			-1		+1	µA
Input Hysteresis	V_{HYS}	Note 3	75			mV
Maximum Input Capacitance	C_{IN}			10		pF
Internal Pulldown Resistance	R_{PD}	BCLK, LRCLK, and ICC		3		MΩ
DIGITAL I/O / INPUT—I2C1, I2C2, ADDR						
Input Voltage High	V_{IH}		0.7 x V_{DVDDIO}			V
Input Voltage Low	V_{IL}				0.3 x V_{DVDDIO}	V
Input Leakage Current		T_A = +25°C, input high	-1		+1	µA
Input Hysteresis	V_{HYS}	Note 3	75			mV
Maximum Input Capacitance	C_{IN}			10		pF
DIGITAL I/O / OPEN DRAIN OUTPUT—I2C1, I2C2, IRQ, LV_EN						
Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Output High Leakage Current	I_{OH}	T_A = +25°C	-1		+1	µA

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_s = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL I/O / PUSH-PULL OUTPUT—DOUT, ICC, IRQ						
Output Voltage High	V_{OH}	I_{OH} = 3mA	V_{DVDDIO} - 0.3			V
Output Voltage Low	V_{OL}	I_{OL} = 3mA			0.3	V
Output Current	I_{OH}	Maximum-drive mode		8		mA
		High-drive mode		6		
		Normal-drive mode		4		
		Reduced-drive mode		2		
PCM AUDIO INTERFACE TIMING						
LRCLK Frequency Range	f_{LRCLK}	All DAI operating modes	16		96	kHz
BCLK Frequency Range	f_{BCLK}	I^2S/left-justified modes	1.024		6.144	MHz
		TDM mode	1.024		24.576	
BCLK Duty Cycle	DC		45		55	%
BCLK Period	t_{BCLK}	I^2S/left-justified only	160			ns
		TDM mode	40			
Maximum BCLK Input Low-Frequency Jitter		Maximum allowable jitter before a -20dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter ≤ 40kHz		0.2		ns
Maximum BCLK Input High-Frequency Jitter		Maximum allowable jitter before a -60dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter > 40kHz		1		ns
PCM AUDIO INTERFACE TIMING / INTERFACE TIMING						
LRCLK to BCLK Active Edge Setup Time	$t_{SYNCSET}$		4			ns
LRCLK to BCLK Active Edge Hold Time	$t_{SYNCHOLD}$		4			ns
DIN to BCLK Active Edge Setup Time	t_{SETUP}		4			ns
DIN to BCLK Active Edge Hold Time	t_{HOLD}		4			ns
DIN Frame Delay After LRCLK Edge		Measured in number of BCLK cycles, set by selected TDM mode	0		2	cycles
PCM AUDIO INTERFACE TIMING / INTERFACE TIMING / PCM DATA OUTPUT (DOUT)						
BCLK Inactive Edge to DOUT Delay	t_{CLKTX}				14	ns
BCLK Active Edge to DOUT Hi-Z Delay	t_{HIZ}		4		18	ns

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_s = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BCLK Inactive Edge to DOUT Active Delay	t_{ACTV}		0		14	ns
PCM AUDIO INTERFACE TIMING / INTERFACE TIMING / INTERCHIP COMMUNICATION (ICC)						
ICC to BCLK Active Edge Setup Time	t_{SETUP}		4			ns
ICC to BCLK Active Edge Hold Time	t_{HOLD}		4			ns
BCLK Inactive Edge to ICC Delay	t_{CLKTX}				14	ns
BCLK Active Edge to ICC Hi-Z Delay	t_{HIZ}		4		16	ns
BCLK Inactive Edge to ICC Active Delay	t_{ACTV}		0		14	ns
I^2C INTERFACE TIMING						
Serial Clock Frequency	f_{SCL}				1000	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.5			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.26			µs
Data Hold Time	$t_{HD,DAT}$		0		450	ns
Data Setup Time	$t_{SU,DAT}$		50			ns
SDA and SCL Receiving Rise Time	t_R		20		120	ns
SDA and SCL Receiving Fall Time	t_F		20 x V_{DVDDIO}/5.5V		120	ns
SDA Transmitting Fall Time	t_F		20 x V_{DVDDIO}/5.5V		120	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.26			µs
Bus Capacitance	C_B				550	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Electrical Characteristics (continued)

(V_{VBAT} = 3.8V, V_{PVDD} = 12V, V_{AVDD} = 1.8V, V_{DVDD} = 1.2V, V_{DVDDIO} = $\overline{RESET}$ = 1.2V, C_{VBAT} = 1x10µF, 1x0.1µF, C_{PVDD} = 1x220µF, 1x10µF, 1x0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{DVDDIO} = 0.1µF, C_{VREFC} = 1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 22kHz, SPK_GAIN_MAX = 0xB (15dB), Data Width = 24-bit, , T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, typical values are at T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$ TIMING						
/RESET Low	t_{RESET_LOW}	Minimum low time for $\overline{RESET}$ to ensure device enters hardware shutdown		1		µs
Release from /RESET	$t_{I^2C\_READY}$	Time from $\overline{RESET}$ = 1 to I^2C communication available (software shutdown)			1.5	ms

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Note 2: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design. Typical values are based on 1 sigma characterization data unless otherwise noted.

Note 3: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Note 4: Assumes device is fully programmed (SPK_EN = 1) and EN = 1 is the last I^2C write in the sequence, SPK_SPEEDUP = 1.

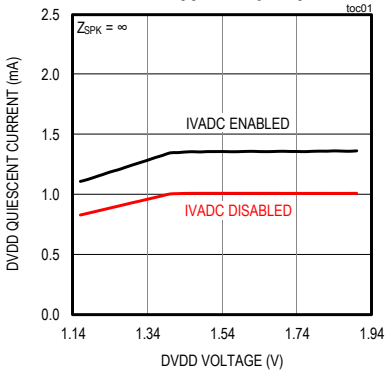
Note 5: Digital filter performance is invariant over temperature and is production tested at T_A = +25°C.

Note 6: Applies to all transitions in/out of full operation with noise gate enabled/disabled. Does not include state transitions due to fault conditions.

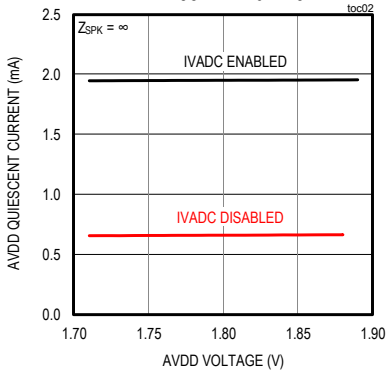
Typical Operating Characteristics

(V_{VBAT} = 3.8V, V_{DVDD} = 1.2V, $_{DVDDIO}$ = 1.2V, V_{AVDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, V_{PVDD} = 12V, C_{VBAT} = 10µF + 0.1µF , C_{PVDD} = 0.1µF + 10µF + 220µF, C_{DVDDIO} = 0.1µF, C_{DVDD} = 1µF, C_{VAVDD} = 1µF, C_{VREFC} = 1µF, A_V = 15dB, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, f_S = 48kHz, 24-bit data, f_{BCLK} = 3.072MHz. Typical values are at T_A = +25°C)

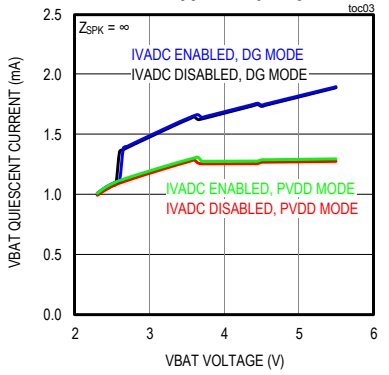
DVDD QUIESCENT CURRENT vs. DVDD SUPPLY VOLTAGE



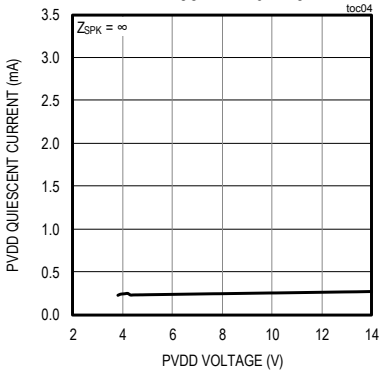
AVDD QUIESCENT CURRENT vs. AVDD SUPPLY VOLTAGE



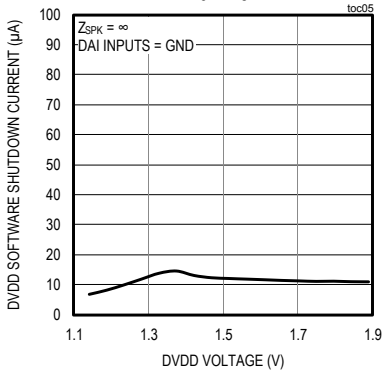
VBAT QUIESCENT CURRENT vs. VBAT SUPPLY VOLTAGE



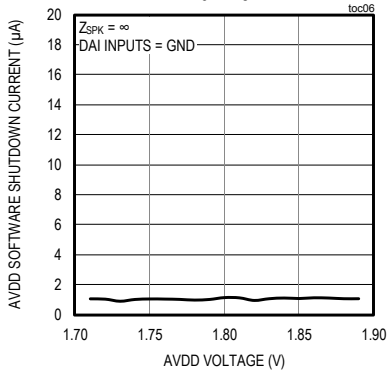
PVDD QUIESCENT CURRENT vs. PVDD SUPPLY VOLTAGE



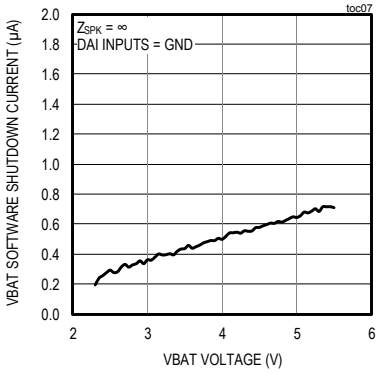
DVDD SOFTWARE SHUTDOWN CURRENT vs. DVDD SUPPLY VOLTAGE



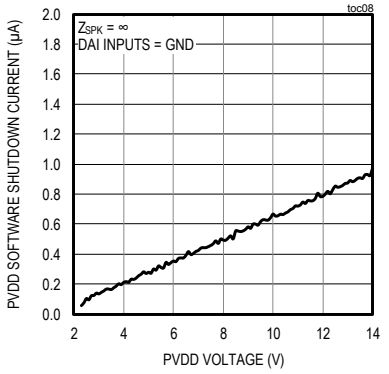
AVDD SOFTWARE SHUTDOWN CURRENT vs. AVDD SUPPLY VOLTAGE



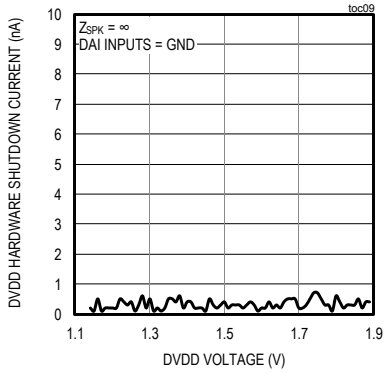
VBAT SOFTWARE SHUTDOWN CURRENT vs. VBAT SUPPLY VOLTAGE



PVDD SOFTWARE SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



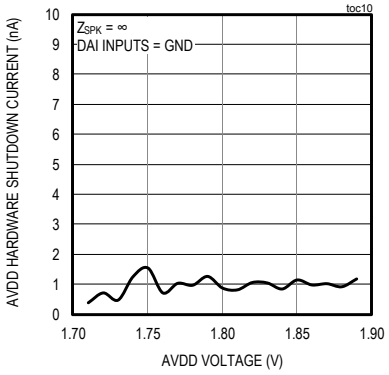
DVDD HARDWARE SHUTDOWN CURRENT vs. DVDD SUPPLY VOLTAGE



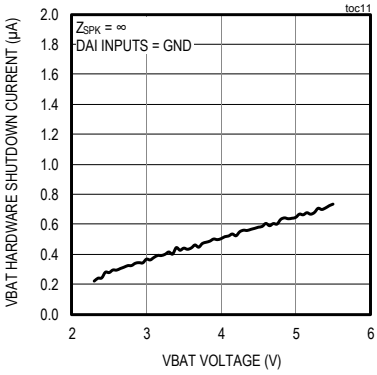
Typical Operating Characteristics (continued)

(V_{VBAT} = 3.8V, V_{DVDD} = 1.2V, $_{DVDDIO}$ = 1.2V, V_{AVDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, V_{PVDD} = 12V, C_{VBAT} = 10µF + 0.1µF , C_{PVDD} = 0.1µF + 10µF + 220µF, C_{DVDDIO} = 0.1µF, C_{DVDD} = 1µF, C_{VAVDD} = 1µF, C_{VREFC} = 1µF, A_V = 15dB, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, f_S = 48kHz, 24-bit data, f_{BCLK} = 3.072MHz. Typical values are at T_A = +25°C)

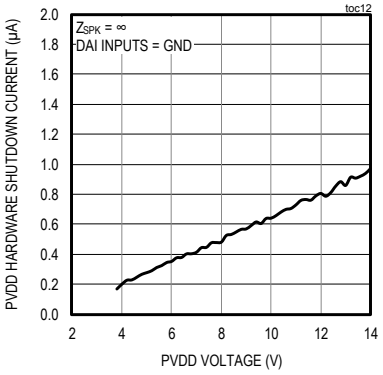
AVDD HARDWARE SHUTDOWN CURRENT vs. AVDD SUPPLY VOLTAGE



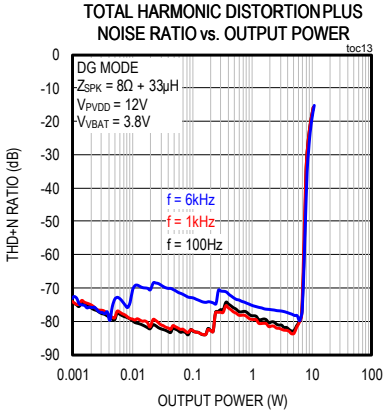
VBAT HARDWARE SHUTDOWN CURRENT vs. VBAT SUPPLY VOLTAGE



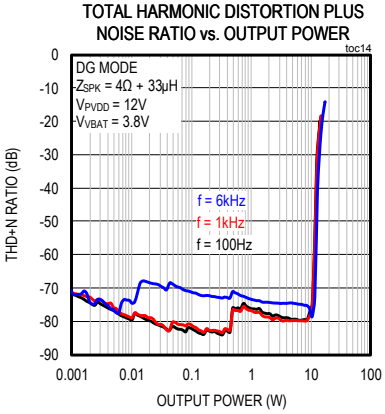
PVDD HARDWARE SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



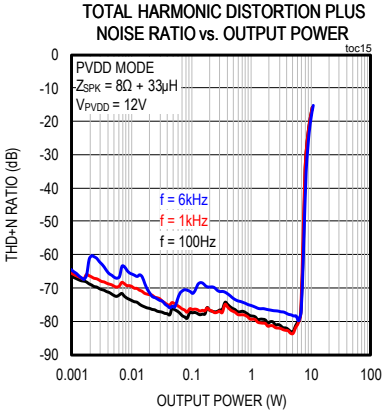
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



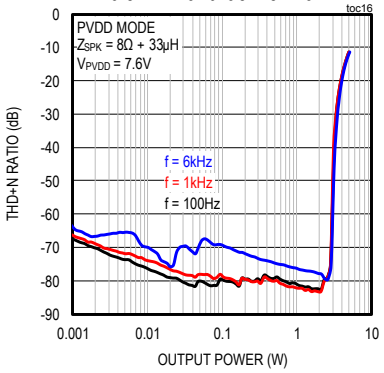
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



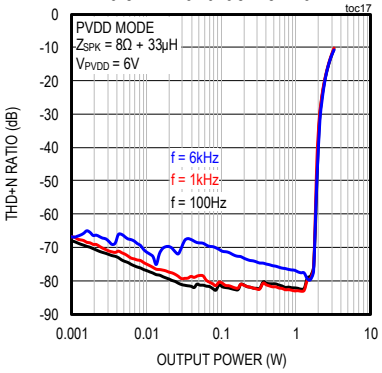
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



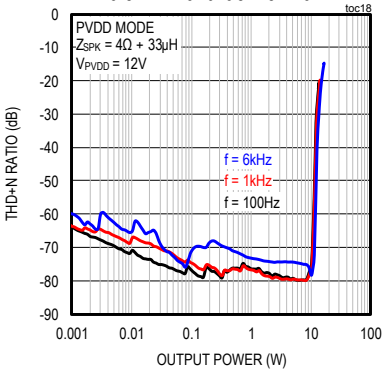
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



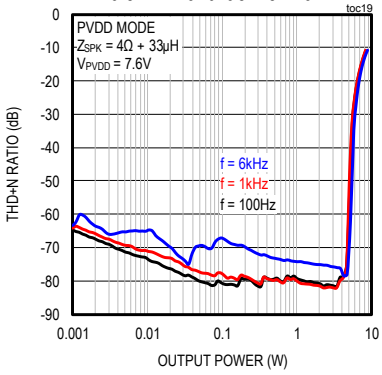
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



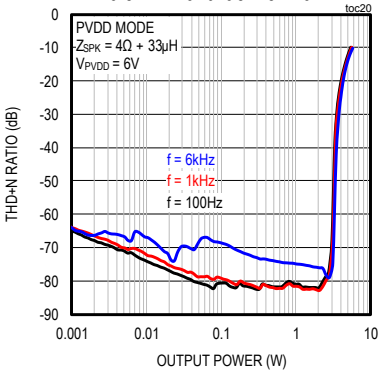
Typical Operating Characteristics (continued)

(V_{VBAT} = 3.8V, V_{DVDD} = 1.2V, $_{DVDDIO}$ = 1.2V, V_{AVDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, V_{PVDD} = 12V, C_{VBAT} = 10µF + 0.1µF , C_{PVDD} = 0.1µF + 10µF + 220µF, C_{DVDDIO} = 0.1µF, C_{DVDD} = 1µF, C_{VAVDD} = 1µF, C_{VREFC} = 1µF, A_V = 15dB, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, f_S = 48kHz, 24-bit data, f_{BCLK} = 3.072MHz. Typical values are at T_A = +25°C)

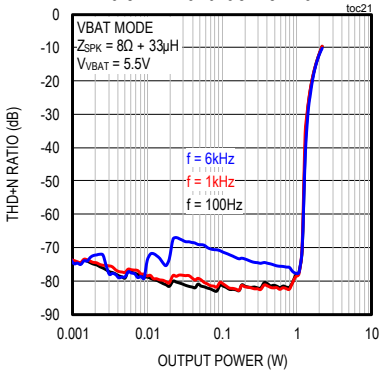
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



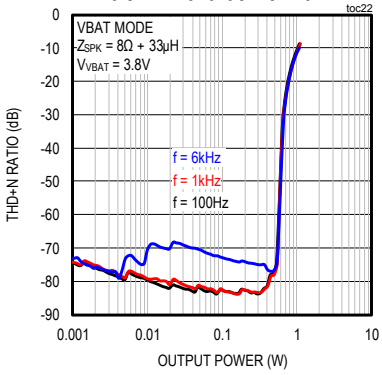
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



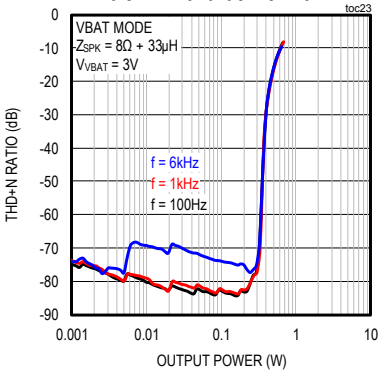
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



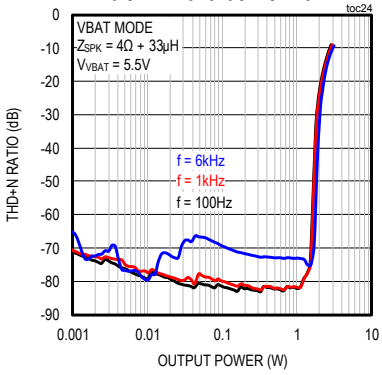
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



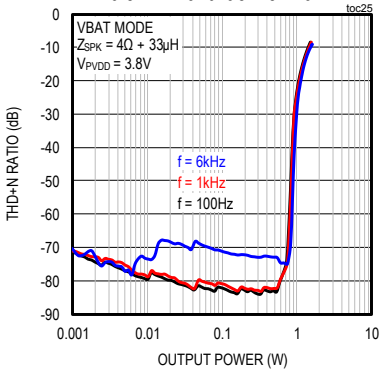
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



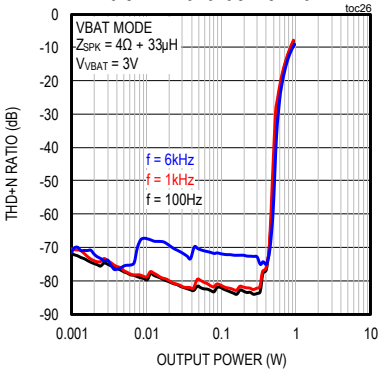
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



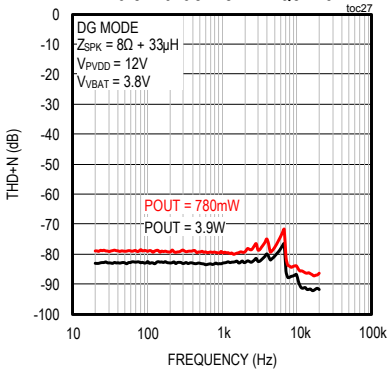
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



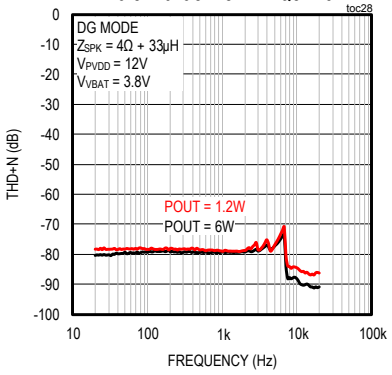
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



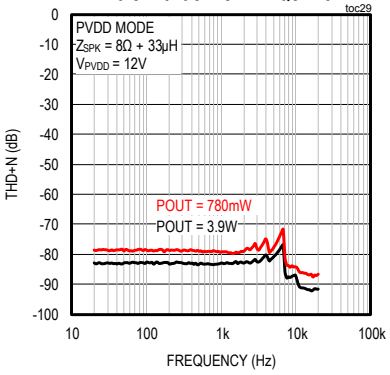
Typical Operating Characteristics (continued)

(V_{VBAT} = 3.8V, V_{DVDD} = 1.2V, $_{DVDDIO}$ = 1.2V, V_{AVDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, V_{PVDD} = 12V, C_{VBAT} = 10µF + 0.1µF , C_{PVDD} = 0.1µF + 10µF + 220µF, C_{DVDDIO} = 0.1µF, C_{DVDD} = 1µF, C_{VAVDD} = 1µF, C_{VREFC} = 1µF, A_V = 15dB, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, f_S = 48kHz, 24-bit data, f_{BCLK} = 3.072MHz. Typical values are at T_A = +25°C)

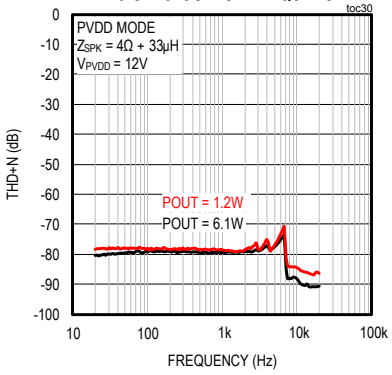
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



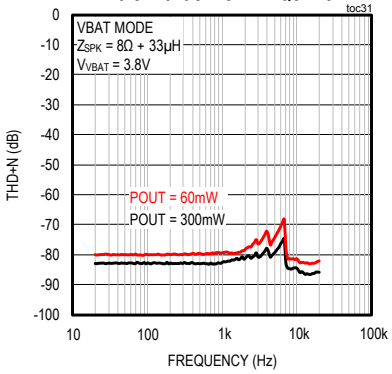
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



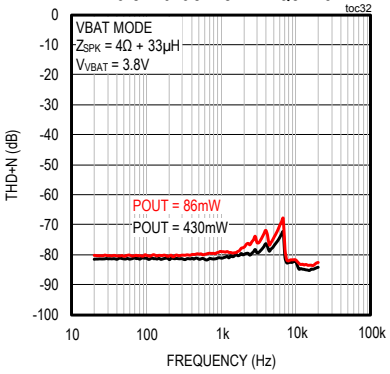
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



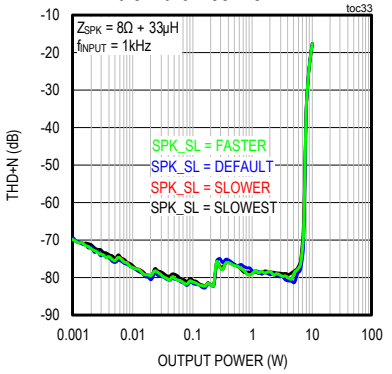
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



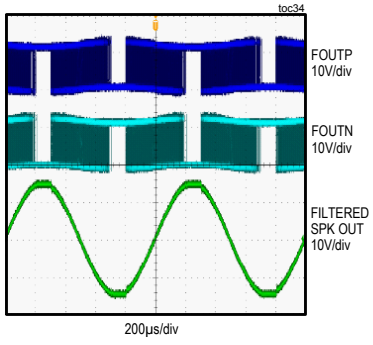
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



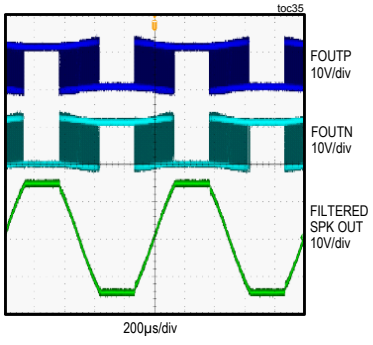
TOTAL HARMONIC DISTORTION PLUS NOISE vs. CLASS-D SLEW RATE



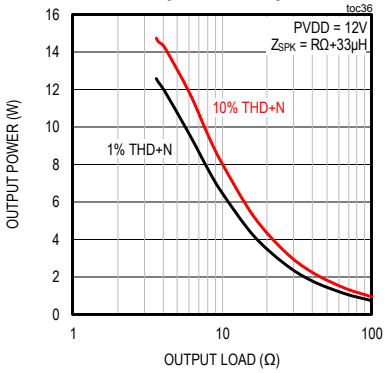
CLIPPING RESPONSE FOR 1% TOTAL HARMONIC DISTORTION PLUS NOISE



CLIPPING RESPONSE FOR 10% TOTAL HARMONIC DISTORTION PLUS NOISE



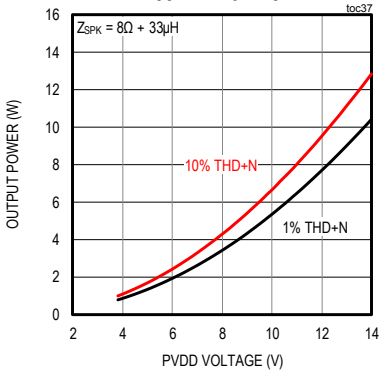
OUTPUT POWER vs. LOAD IMPEDANCE



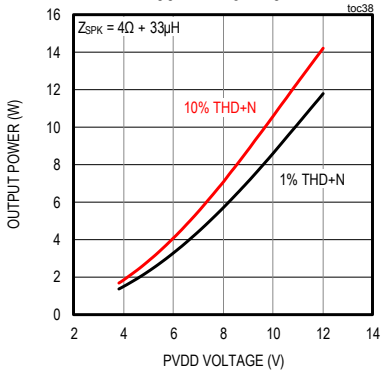
Typical Operating Characteristics (continued)

(V_{VBAT} = 3.8V, V_{DVDD} = 1.2V, $_{DVDDIO}$ = 1.2V, V_{AVDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, V_{PVDD} = 12V, C_{VBAT} = 10µF + 0.1µF , C_{PVDD} = 0.1µF + 10µF + 220µF, C_{DVDDIO} = 0.1µF, C_{DVDD} = 1µF, C_{VAVDD} = 1µF, C_{VREFC} = 1µF, A_V = 15dB, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, f_S = 48kHz, 24-bit data, f_{BCLK} = 3.072MHz. Typical values are at T_A = +25°C)

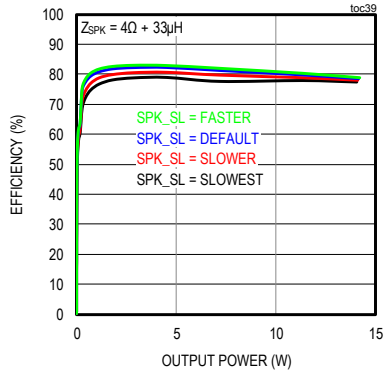
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



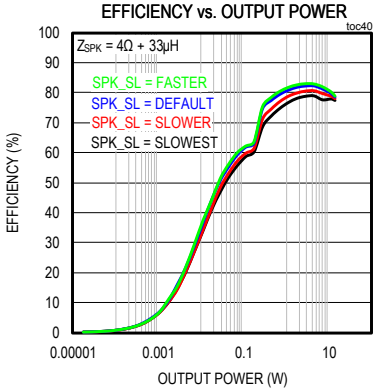
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



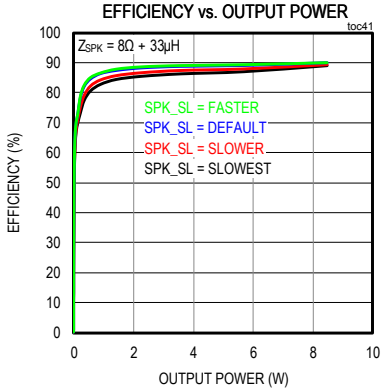
EFFICIENCY vs. OUTPUT POWER



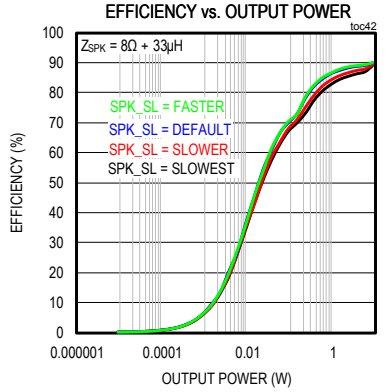
EFFICIENCY vs. OUTPUT POWER



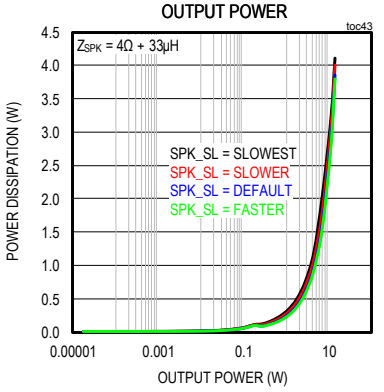
EFFICIENCY vs. OUTPUT POWER



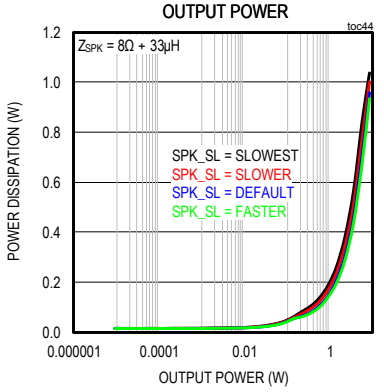
EFFICIENCY vs. OUTPUT POWER



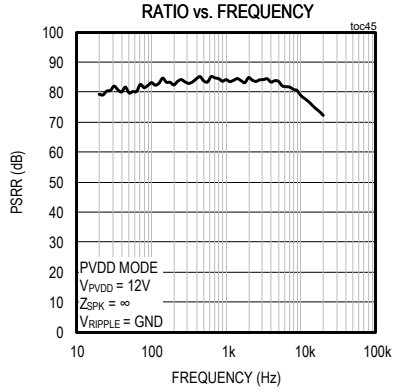
POWER DISSIPATION vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



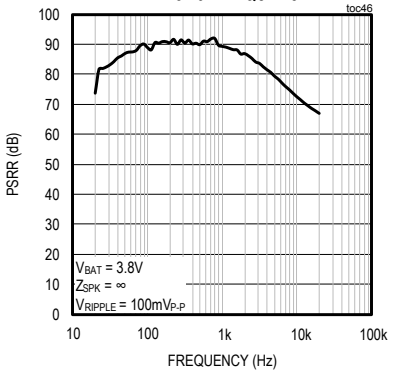
PVDD POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



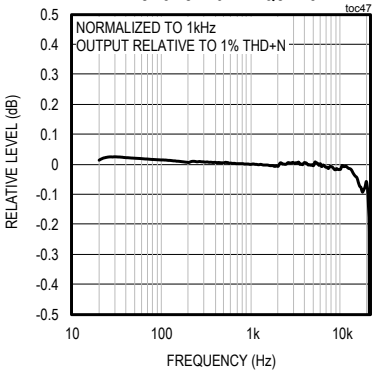
Typical Operating Characteristics (continued)

(V_{VBAT} = 3.8V, V_{DVDD} = 1.2V, $_{DVDDIO}$ = 1.2V, V_{AVDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, V_{PVDD} = 12V, C_{VBAT} = 10µF + 0.1µF , C_{PVDD} = 0.1µF + 10µF + 220µF, C_{DVDDIO} = 0.1µF, C_{DVDD} = 1µF, C_{VAVDD} = 1µF, C_{VREFC} = 1µF, A_V = 15dB, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, f_S = 48kHz, 24-bit data, f_{BCLK} = 3.072MHz. Typical values are at T_A = +25°C)

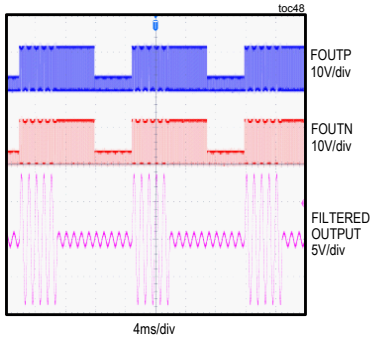
VBAT POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



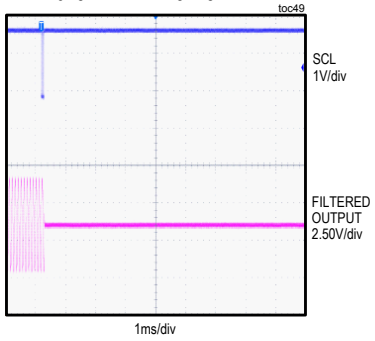
NORMALIZED SPEAKER OUTPUT RESPONSE vs. FREQUENCY



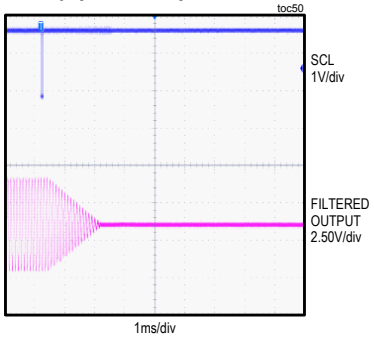
DG RESPONSE



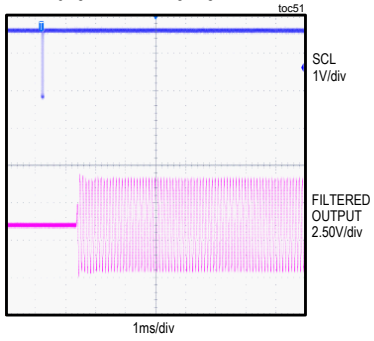
SOFTWARE DISABLE TURN-OFF RESPONSE VOLUME RAMPING DISABLED



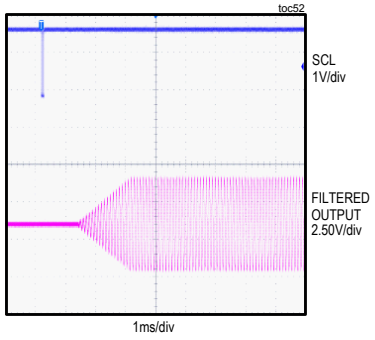
SOFTWARE DISABLE TURN-OFF RESPONSE VOLUME RAMPING ENABLED



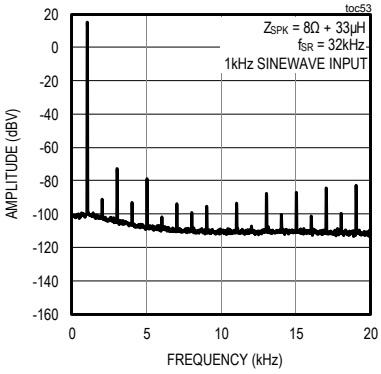
SOFTWARE ENABLE TURN-ON RESPONSE VOLUME RAMPING DISABLED



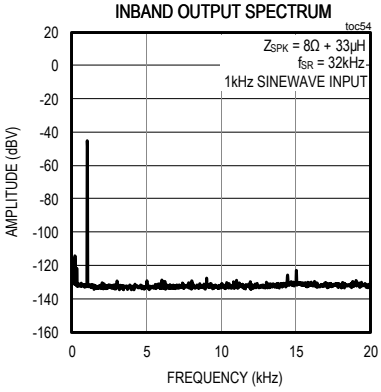
SOFTWARE ENABLE TURN-ON RESPONSE VOLUME RAMPING ENABLED



LARGE SIGNAL INBAND OUTPUT SPECTRUM



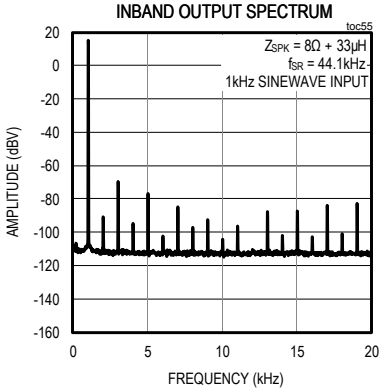
SMALL SIGNAL INBAND OUTPUT SPECTRUM



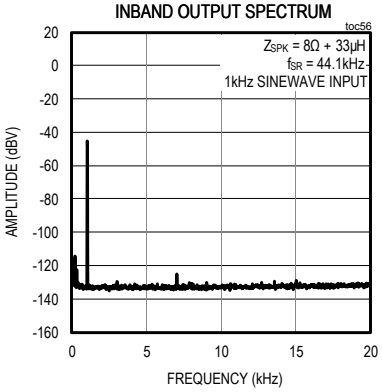
Typical Operating Characteristics (continued)

(V_{VBAT} = 3.8V, V_{DVDD} = 1.2V, $_{DVDDIO}$ = 1.2V, V_{AVDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, V_{PVDD} = 12V, C_{VBAT} = 10µF + 0.1µF , C_{PVDD} = 0.1µF + 10µF + 220µF, C_{DVDDIO} = 0.1µF, C_{DVDD} = 1µF, C_{VAVDD} = 1µF, C_{VREFC} = 1µF, A_V = 15dB, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, f_S = 48kHz, 24-bit data, f_{BCLK} = 3.072MHz. Typical values are at T_A = +25°C)

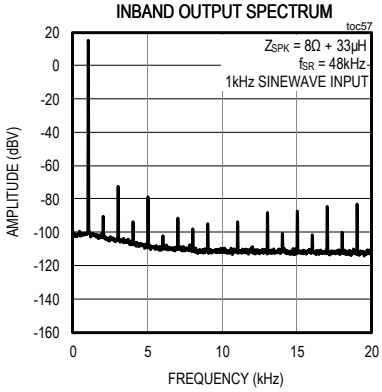
LARGE SIGNAL INBAND OUTPUT SPECTRUM



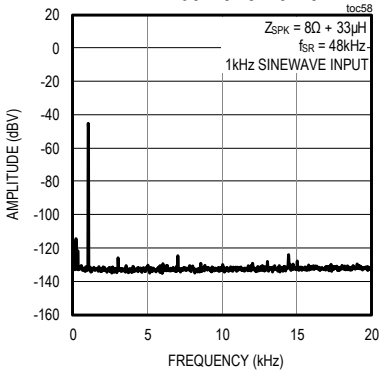
SMALL SIGNAL INBAND OUTPUT SPECTRUM



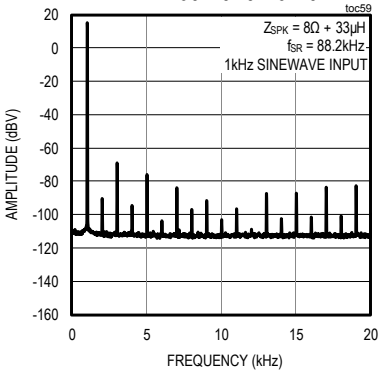
LARGE SIGNAL INBAND OUTPUT SPECTRUM



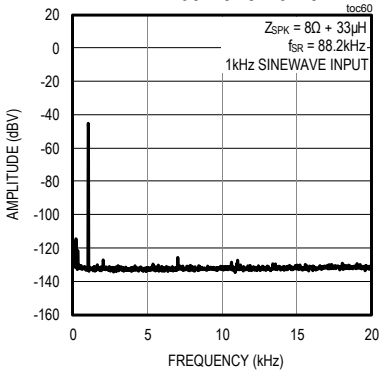
SMALL SIGNAL INBAND OUTPUT SPECTRUM



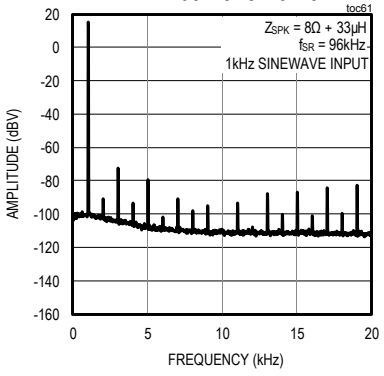
LARGE SIGNAL INBAND OUTPUT SPECTRUM



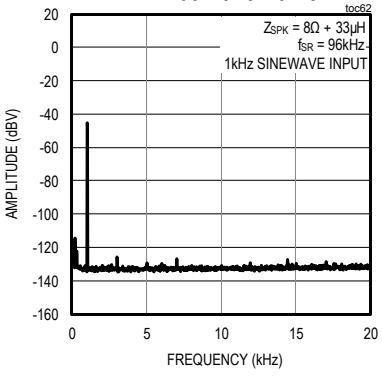
SMALL SIGNAL INBAND OUTPUT SPECTRUM



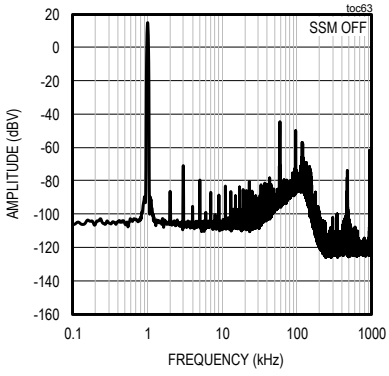
LARGE SIGNAL INBAND OUTPUT SPECTRUM



SMALL SIGNAL INBAND OUTPUT SPECTRUM



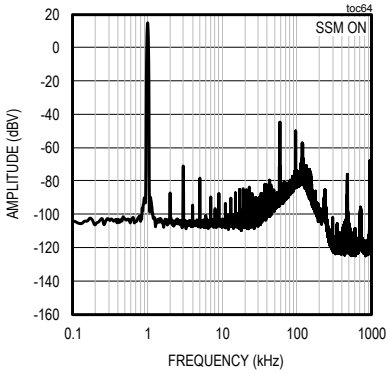
WIDEBAND OUTPUT SPECTRUM



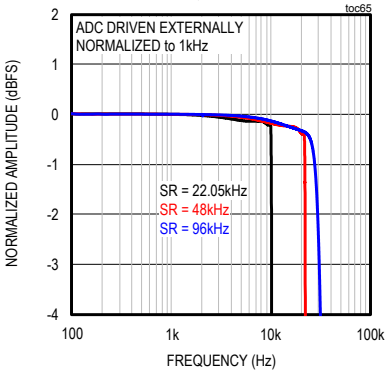
Typical Operating Characteristics (continued)

(V_{VBAT} = 3.8V, V_{DVDD} = 1.2V, $_{DVDDIO}$ = 1.2V, V_{AVDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, V_{PVDD} = 12V, C_{VBAT} = 10µF + 0.1µF , C_{PVDD} = 0.1µF + 10µF + 220µF, C_{DVDDIO} = 0.1µF, C_{DVDD} = 1µF, C_{VAVDD} = 1µF, C_{VREFC} = 1µF, A_V = 15dB, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, f_S = 48kHz, 24-bit data, f_{BCLK} = 3.072MHz. Typical values are at T_A = +25°C)

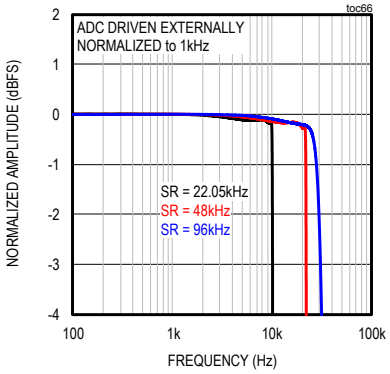
WIDEBAND OUTPUT SPECTRUM



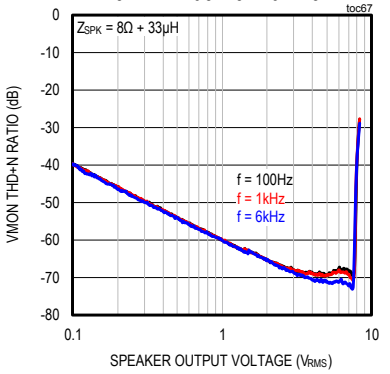
VMON FREQUENCY RESPONSE



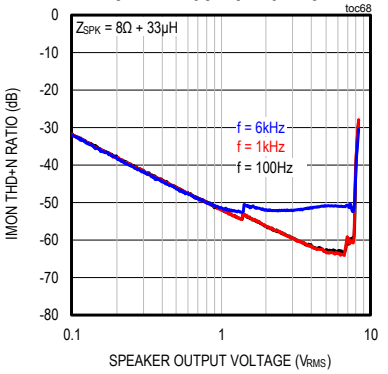
IMON FREQUENCY RESPONSE



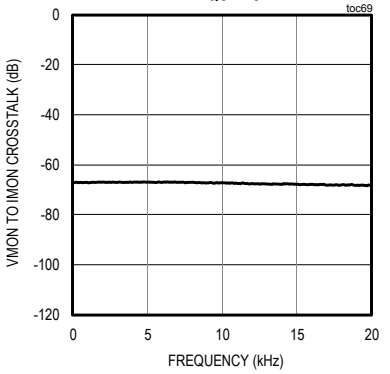
VMON TOTAL HARMONIC DISTORTION PLUS NOISE vs. SPEAKER OUTPUT VOLTAGE



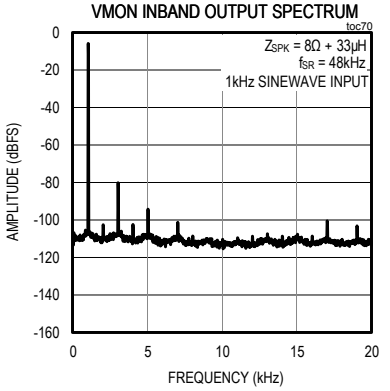
IMON TOTAL HARMONIC DISTORTION PLUS NOISE vs. SPEAKER OUTPUT VOLTAGE



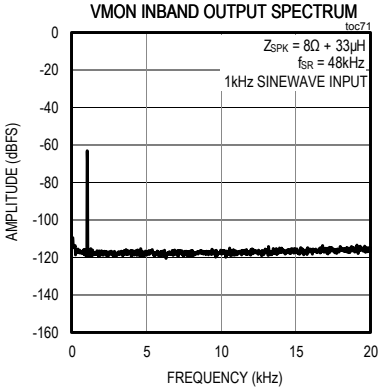
PCM VMON TO IMON CROSSTALK vs. FREQUENCY



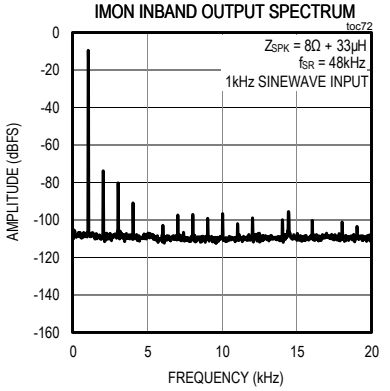
LARGE SIGNAL VMON INBAND OUTPUT SPECTRUM



SMALL SIGNAL VMON INBAND OUTPUT SPECTRUM



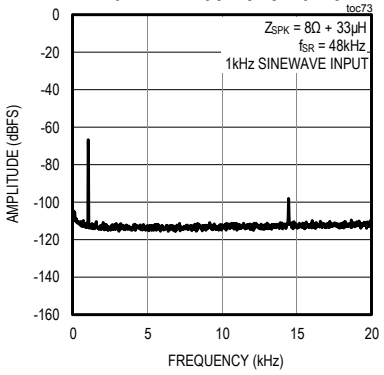
LARGE SIGNAL IMON INBAND OUTPUT SPECTRUM



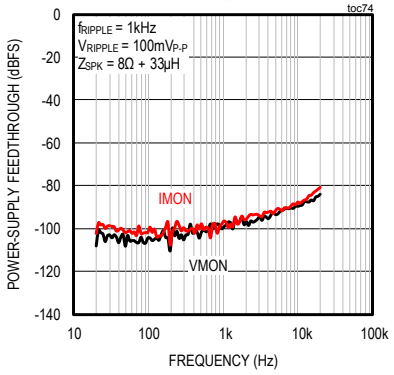
Typical Operating Characteristics (continued)

(V_{VBAT} = 3.8V, V_{DVDD} = 1.2V, $_{DVDDIO}$ = 1.2V, V_{AVDD} = 1.8V, V_{GND} = 0V, V_{PGND} = 0V, V_{PVDD} = 12V, C_{VBAT} = 10µF + 0.1µF , C_{PVDD} = 0.1µF + 10µF + 220µF, C_{DVDDIO} = 0.1µF, C_{DVDD} = 1µF, C_{VAVDD} = 1µF, C_{VREFC} = 1µF, A_V = 15dB, Z_{SPK} = ∞ between OUTP and OUTN, AC Measurement Bandwidth = 20Hz to 20kHz, f_S = 48kHz, 24-bit data, f_{BCLK} = 3.072MHz. Typical values are at T_A = +25°C)

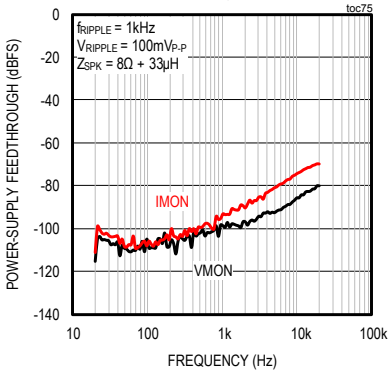
SMALL SIGNAL
IMON INBAND OUTPUT SPECTRUM



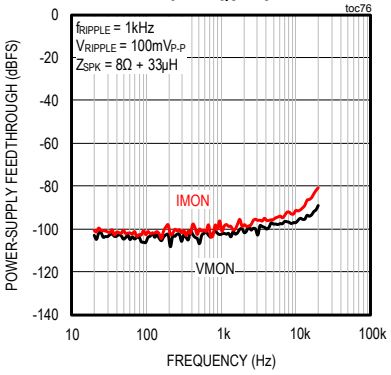
PVDD TO RECORD PATH
POWER-SUPPLY FEEDTHROUGH
vs. FREQUENCY



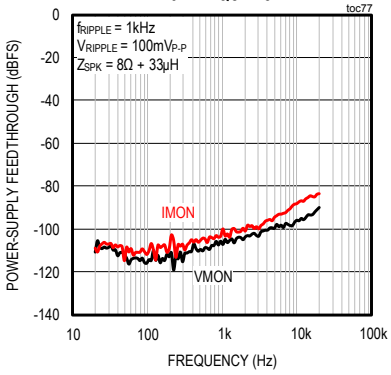
VBAT TO RECORD PATH
POWER-SUPPLY FEEDTHROUGH
vs. FREQUENCY



AVDD TO RECORD PATH
POWER-SUPPLY FEEDTHROUGH
vs. FREQUENCY

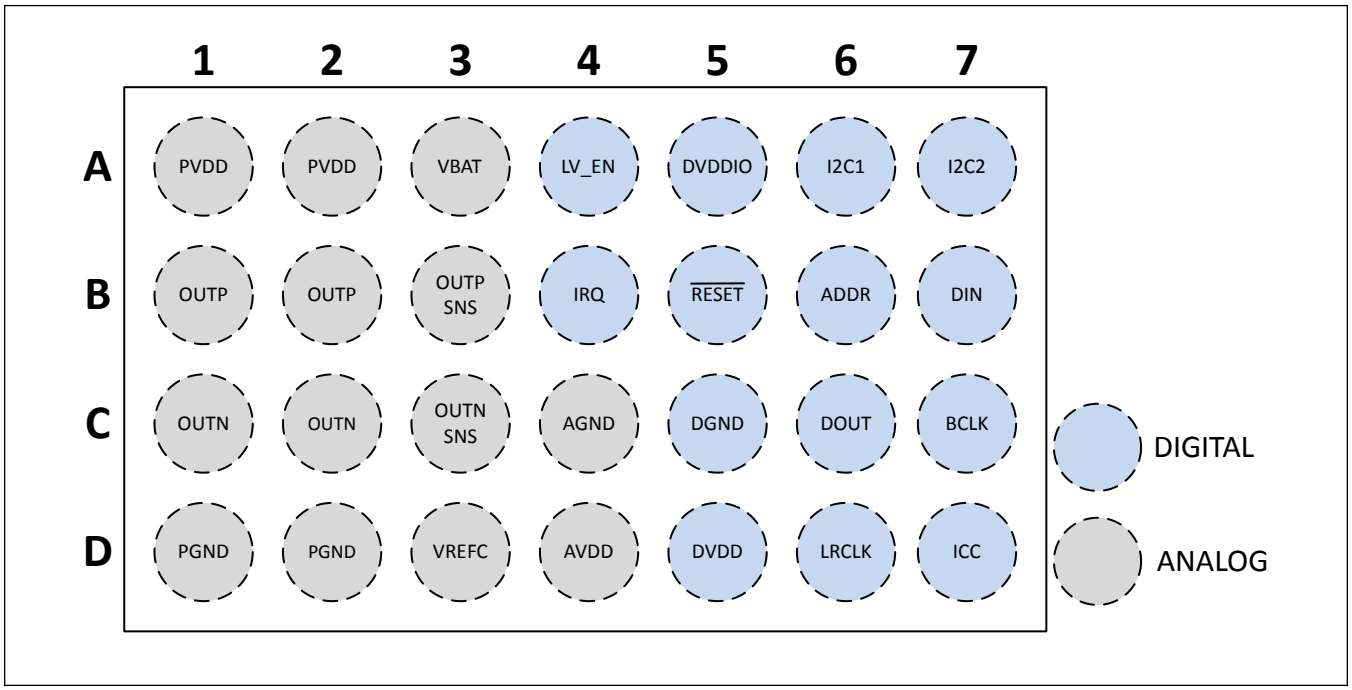


DVDD TO RECORD PATH
POWER-SUPPLY FEEDTHROUGH
vs. FREQUENCY



Bump Configuration

MAX98395



Bump Descriptions

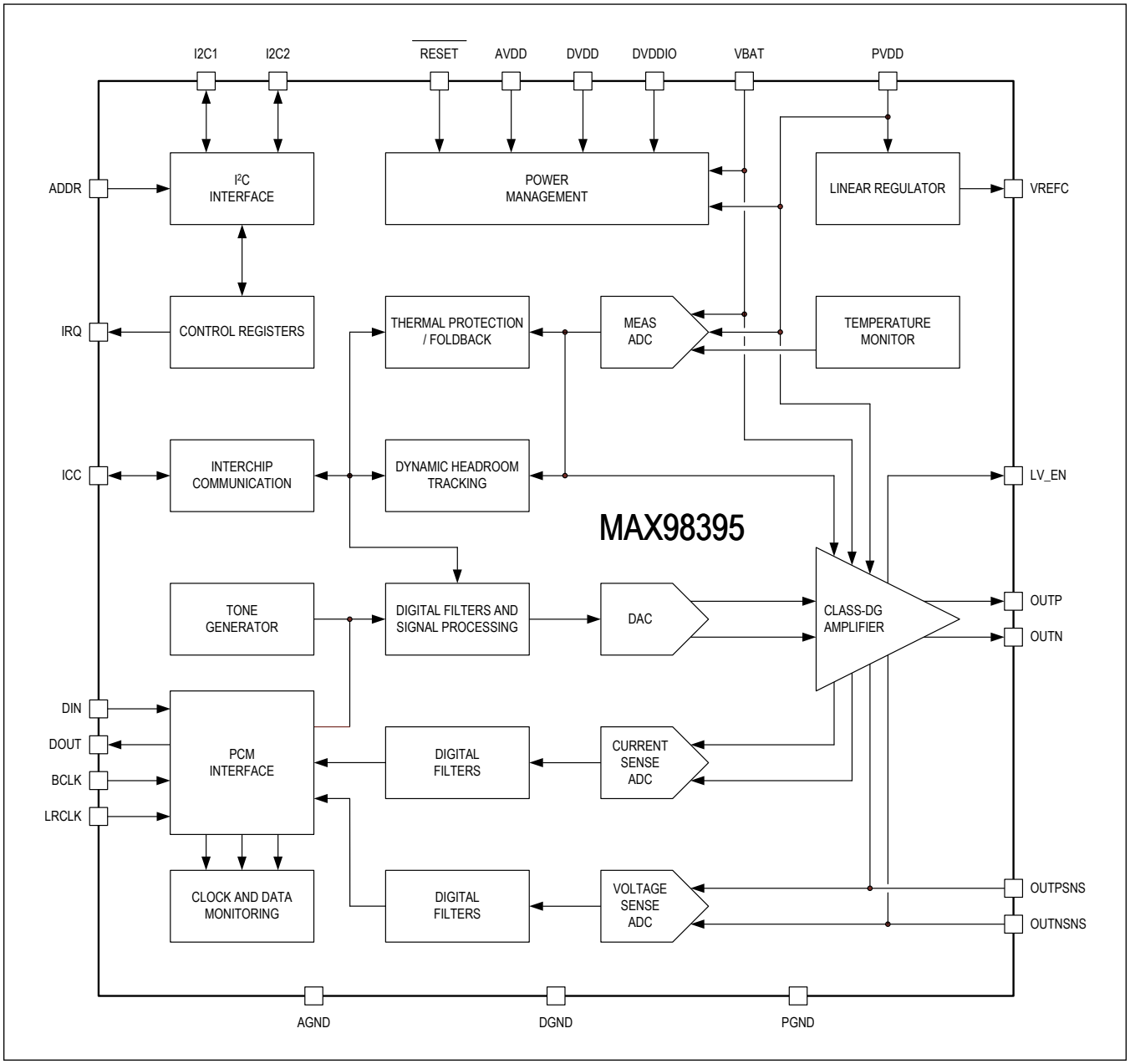
PIN	NAME	FUNCTION	REF SUPPLY	TYPE
D5	DVDD	Digital Core Power-Supply. Bypass to GND with a 1µF capacitor.		Supply
A5	DVDDIO	Digital Core and Interface Power-Supply. Bypass to DGND with a 0.1µF capacitor.		Supply
C5	DGND	Digital Ground		Supply
A1, A2	PVDD	Speaker Amplifier Power-Supply. Bypass each bump to PGND with a 0.1µF and 10µF capacitor placed as close as possible. Bypass the supply bus to PGND with a single 220µF bulk capacitor per device.		Supply
D1, D2	PGND	Speaker Amplifier Ground		Supply
A3	VBAT	Battery Power-Supply. Bypass to PGND with a 0.1µF and 10µF capacitor placed as close as possible.		Supply
D4	AVDD	Analog Power-Supply. Bypass to GND with a 1µF capacitor placed as close as possible.		Supply
C4	AGND	Analog Ground. Connect to the common ground plane of the application.		Supply
D3	VREFC	Internal Bias. Bypass to GND with a 1µF capacitor.	PVDD	
B5	/RESET	Hardware enable (active-low). Resets all digital portions of the device and all registers to default PoR settings.	DVDDIO	Digital Input
B1, B2	OUTP	Positive Speaker Amplifier Output	PVDD	Analog Output

Bump Descriptions (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
B3	OUTPSNS	Voltage Sense and Speaker Amplifier Feedback Positive Input. Connect as close as possible to the positive terminal of the loudspeaker. This pin must form a complete loop with OUTP.	PVDD	Analog Output
C1, C2	OUTN	Negative Speaker Amplifier Output	PVDD	Analog Output
C3	OUTNSNS	Voltage Sense and Speaker Amplifier Feedback Negative Input. Connect as close as possible to the negative terminal of the loudspeaker. This pin must form a complete loop with OUTN.	PVDD	Analog Output
A6	I2C1	I^2C-Compatible Serial-Data/Clock 1. This pin can be configured as either a SDA or SCL. Connect a 1.5kΩ pullup resistor to DVDDIO for full logic level swing.	DVDDIO	Digital I/O (Open drain)
A7	I2C2	I^2C-Compatible Serial-Data/Clock 2. This pin can be configured as either a SDA or SCL. Connect a 1.5kΩ pullup resistor to DVDDIO for full logic level swing.	DVDDIO	Digital I/O (Open Drain)
B6	ADDR	I^2C Address Select. Selects one of eight I^2C slave addresses in conjunction with I2C1 and I2C2 pins.	DVDDIO	Digital Input
B4	IRQ	Hardware Interrupt Output. Interrupt polarity and pin drive mode are configurable. Connect a 10kΩ pullup resistor to DVDDIO for full logic level swing in open-drain mode.	DVDDIO	Digital Output
C7	BCLK	PCM Interface BCLK Input. Internally pulled down to DGND through R_{PD}.	DVDDIO	Digital Input
D6	LRCLK	PCM Interface Frame Clock Input/Output. LRCLK frequency matches the PCM interface sample rate. Internally pulled down to DGND through R_{PD}.	DVDDIO	Digital Input
B7	DIN	PCM Interface Data Input. Internally pulled down to DGND through R_{PD}.	DVDDIO	Digital Input
C6	DOUT	PCM Interface Data Output	DVDDIO	Digital Output
A4	LV_EN	Low voltage enable output signals an external boost the active power-supply used by the amplifier output stage. The pin is asserted when the amplifier uses VBAT as the supply for the output stage.	DVDDIO	Digital Ouput (Open Drain)
D7	ICC	Interchip Communication Data Bus. Optionally allows multiple devices to be grouped up to communicate with each other. Internally pulled down to DGND through R_{PD}.	DVDDIO	Digital I/O

Functional Diagrams

Detailed Block Diagram



Detailed Description

Device State Control

The device has three distinct power states: the hardware shutdown state, software shutdown state, and active state. When transitioning between states, the device always moves from the hardware shutdown state to the software shutdown state to the active state (or the reverse) based on the state transition requirements. Normal transitions between the software shutdown state and active state are reversible without waiting for an in progress transition to be completed. State transitions due to device faults, supply removal, and reset conditions are not reversible and are always completed (once initiated) to protect the device.

Hardware Shutdown State

When the device is first powered up or after a hardware reset event, the device always initializes into the hardware shutdown state. In hardware shutdown, the device is configured to its lowest power state. Upon entering hardware shutdown, the device is globally placed into a reset condition. As a result, the I^2C control interface is disabled and all device registers are returned to their PoR states. When exiting hardware shutdown, the device initializes and then transitions into the software shutdown state. During this transition (as part of initialization), the OTP register trim settings are loaded. If the OTP load routine fails to complete successfully, an OTP_FAIL_* interrupt is generated once the device reaches the software shutdown state.

When the hardware reset input ($\overline{RESET}$) is asserted low, the device enters (or remains in) hardware shutdown. The device is also placed into hardware shutdown anytime the AVDD, DVDD, or DVDDIO supplies drop below their respective UVLO thresholds.

The device only exits hardware shutdown when the AVDD, DVDD, and DVDDIO supplies are all above their respective UVLO thresholds, and the hardware reset input ($\overline{RESET}$) is asserted high. Once all of these conditions are met, the device automatically exits hardware shutdown, and transitions into software shutdown.

Software Shutdown State

The device enters the software shutdown state after it transitions out of hardware shutdown state and when exiting the active state. In the software shutdown state, all blocks are automatically disabled except for the I^2C control interface. In the software shutdown state, all device registers can be programmed without restriction and all programmed register states are retained.

The global enable bit (*EN*) is used to transition the device into and out of software shutdown. When global enable (EN) is set high, the device transitions to the active state and a power-up done (PWRUP_DONE_*) interrupt is generated. When the device is in the active state and global enable (EN) is set low, the device transitions to the software shutdown state and a power-down done (PWRDN_DONE_*) interrupt is generated. Additionally, the device is reset and enters software shutdown anytime the software reset bit (RST) is written with a 1.

While in the software shutdown state, the PVDD and VBAT supplies can be powered down safely. Regardless of the state of the global enable bit, the device cannot transition from the software shutdown state to the active state until PVDD, and VBAT are all above their UVLO thresholds. If PVDD, or VBAT supplies drop below their UVLO levels while the device is in the active state, the device is forced back into the software shutdown state.

Recovery from Software Shutdown due to Supply Faults

The device provides two forms of fault recovery in the event that either VBAT or PVDD drop below their UVLO thresholds while the device is in its active state. Based on the setting of the VBAT_AUTORESTART and PVDD_AUTORESTART bits, the individual supply fault recovery is either in manual mode or auto restart mode.

If the bit is set low, then the supply UVLO fault recovery is in manual mode. In manual mode, when the supply drops below its UVLO threshold the device transitions into the software shutdown state (sets EN = 0), and generates the appropriate UVLO fault shutdown interrupt (VBAT_UVLO_SHUTDOWN_* or PVDD_UVLO_SHUTDOWN_* respectively). Even once the supply recovers (voltage levels exceed the UVLO thresholds), the device remains in the software shutdown state until the global enable bit (EN) is set high by the host software.

If the bit is instead set high, then the supply UVLO fault recovery is in auto restart mode. In auto restart mode, when the supply drops below its UVLO threshold the device is internally forced into software shutdown (EN state is preserved and remains high), and generates the appropriate UVLO fault shutdown interrupt (VBAT_UVLO_SHUTDOWN_* or PVDD_UVLO_SHUTDOWN_* respectively). Once the supply recovers (voltage levels exceed the UVLO thresholds), the device is no longer held in software shutdown and (if all other conditions are met) automatically restarts back into the active state. These recovery modes do not apply when the AVDD, DVDD, or DVDDIO supplies cause a UVLO fault while the device is in the active state. If AVDD, DVDD, or DVDDIO drop below their UVLO thresholds, the device is reset and is placed into hardware shutdown.

Active State

The device always enters the active state through a transition from the software shutdown state. In the active state, all enabled device blocks are active and speaker amplifier playback is possible. In the active state, only dynamic register settings (or those restricted to disabled blocks) can be programmed safely.

The only non-fault state transitions to or from the active state are those initiated through the global enable bit (EN). All other transitions to or from the active state are the result of fault events, and may result in audible glitches if they occur during active playback.

Device Sequencing

Table 1 and Table 2 show the recommended typical device power-up/down sequences.

Table 1. Typical Power-Up Sequence

STEP	ACTION	DETAILED DESCRIPTION
1	Power-Up Core Supplies	Power the DVDD, DVDDIO, and AVDD supplies above their UVLO thresholds.
2	Exit Hardware Shutdown State	Assert the hardware reset input ($\overline{RESET}$) to a logic high level. If $\overline{RESET}$ is tied to the DVDD/DVDDIO supply, this step is combined with step 1.
3	Enter Software Shutdown State	The device finishes the transition and enters the software shutdown state after the release from reset time ($t_{I^2C\_READY}$) elapses.
4	Program the Device Registers/ Enable the External Clocks	The I^2C interface is active, and all register can be freely configured. Ensure the PVDD and VBAT supplies are above their UVLO thresholds. Start both external clocks before exiting the software shutdown state.
5	Setup the PCM Interface Data Format, Clocking, and Sample Rate	By default the device PCM interface is configured to receive and transmit 32 bit, 48kHz, I^2S data where the falling LRCLK edge starts a new frame. The device PCM interface is also configured by default to accept 64 BCLKs per LRCLK and the input data is captured and the output data valid on rising BCLK edge. Registers 0x2040 to 0x2043 can be written to modify this default configuration.
6	Setup the Receive and Transmit Data Slot Source	By default the device is only setup to receive I^2S channel data slot is 0. Write 0x01 to 0x2046 to configure VMON and IMON data to channel 0 and channel 1 respectively. To change the default device receive and transmit source configurations write to registers 0x2044 and 0x2045-0x204B, 0x205D.
7	Enable the Device PCM Interface Receive Channel	Write 0x01 to register 0x205E.
8	Enable the Device PCM Interface Transmit Channel	Write 0x01 to register 0x205F.

Table 1. Typical Power-Up Sequence (continued)

STEP	ACTION	DETAILED DESCRIPTION
9	Disable Speaker-Safe Mode	By default, the speaker-safe mode is enabled and this applies a -18dB attenuation to the input signal. In normal operation, disable the speaker-safe mode by writing 0x02 to register 0x2092.
10	Enable Speaker Amplifier	Write 0x01 to register 0x20AF
11	Enable Current and Voltage sense ADC's	Write 0x03 to register 0x20E7
12	Exit Software Shutdown State	By default volume ramping on power-up is enabled. If volume ramping is disabled, the input audio data should be silent. Set the global enable to a logic high (EN = 1).
13	Enter the Active State	Device enters the active state after the turn-on time (t_{ON}) elapses.
14	Active State/ Audio Playback	Dynamic bits (and those restricted to disabled blocks) can be programmed. The device is capable of audio playback in the active state.

Table 2. Typical Power-Down Sequence

STEP	ACTION	DETAILED DESCRIPTION
1	Exit the Active State	By default, volume ramping on power-down is enabled. If volume ramping is disabled, the input audio data should be silent. Set the global enable bit to a logic low (EN = 0).
2	Enter the Software Shutdown State	Device enters the software shutdown state after the turn-off time (t_{OFF}) elapses.
3	Reprogram Device Registers/Disable the External Clocks	The device is fully programmable, and can idle in the software shutdown state. The external clocks and the AVDD/PVDD/VBAT supplies can be disabled To return to the active state, resume the power-up sequence from step 4.
4	Enter Hardware Shutdown State	For full hardware shutdown, disable the external clocks first. Assert the reset input ($\overline{RESET}$) to ground or power-down DVDD/DVDDIO.

PCM Interface

The flexible PCM slave interface supports common audio playback sample rates from 16kHz to 96kHz and I/V sense ADC sample rates from 8kHz to 96kHz. The PCM interface also supports standard I^2S, left-justified, and TDM data formats. The PCM interface is disabled and powered down when both the PCM data input (DIN) and PCM data output (DOUT) are disabled.

PCM Clock Configuration

The PCM slave interface requires the host to supply both BCLK and LRCLK. To configure the PCM interface clock inputs, the host must program both the device interface sample rate (*PCM_SR*) and BCLK to LRCLK (*PCM_BSEL*) ratio. The PCM interface sample rate must be configured to match the frequency of the frame clock (LRCLK) using the *PCM_SR* registers. The speaker path sample rate is also set by the *PCM_SR* setting. However, the I/V sense ADC path sample rate (*IVADC_SR*) can be set to the same rate or a lower rate than the speaker path sample rate (*PCM_SR*) according to the restrictions in Table 3. When the I/V sense ADC path is set to a lower rate than the speaker amplifier path, the output data contains repeated samples.

Table 3. Sample Rate Selection For I/V Sense

N/A = Not Available N/S = Not Supported		I/V SENSE ADC SAMPLE RATE (kHz)										
		96	88.2	48	44.1	32	24	22.05	16	12	11.025	8
PCM Interface and Speaker Path Sample Rate (kHz)	96	1	N/S	2	N/S	3	4	N/S	6	8	N/S	12
	88.2	N/A	1	N/S	2	N/S	N/S	4	N/S	N/S	8	N/S
	48	N/A	N/A	1	N/S	N/S	2	N/S	3	4	N/S	6
	44.1	N/A	N/A	N/A	1	N/S	N/S	2	N/S	N/S	4	N/S
	32	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S	N/S	4
	24	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S	3
	22.05	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S
	16	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2

The device supports a range of BCLK to LRCLK clock ratios (*PCM_BSEL*) ranging from 32 to 512. However, based on the selected PCM interface sample rate (LRCLK frequency) the configured clock ratio cannot result in a BLCK frequency that exceeds 24.576MHz.

PCM Data Format Configuration

The device supports the standard I²S, left-justified, and TDM data formats. The operating mode is configured using the *PCM_FORMAT* bit field.

I²S/Left-Justified Mode

I²S and left-justified formats support two channels that can be 16-, 24-, or 32-bits in length. The BCLK to LRCLK ratio (*PCM_BSEL*) must be configured to be twice the desired channel length. The audio data word size is configurable to 16-, 24-, or 32-bits in length (*PCM_CHANSZ*), but must be programmed to be less than or equal to the channel length. If the resulting channel length exceeds the configured data word size then the data input LSBs are truncated and the data output LSBs are padded with either zero or Hi-Z data based on the *PCM_TX_EXTRA_HIZ* register bit setting.

Table 4. Supported I²S/Left-Justified Mode Configurations

CHANNELS	CHANNEL LENGTH	BCLK TO LRCLK RATIO (*PCM_BSEL*)	SUPPORTED DATA WORD SIZES (*PCM_CHANSZ*)
2	16	32	16
	24	48	16, 24
	32	64	16, 24, 32

With the default PCM settings, falling LRCLK indicates the start of a new frame and the left channel data (channel 0), while rising LRCLK indicates the right channel data (channel 1). In I²S mode, the MSB of the audio word is latched on the second active BCLK edge after an LRCLK transition. In left-justified mode, the MSB of the audio word is latched on the first active BCLK edge after an LRCLK transition.

The *PCM_BCLKEDGE* register bit selects either the rising or falling edge of BCLK as the active edge that is used for data capture (DIN) and data output (DOUT). The *PCM_CHANSEL* bit configures which LRCLK edge indicates the start of a new frame (channel 0), and LRCLK transitions always align with the inactive BCLK edge. The data output is valid on the same active BCLK edge as the data input. The data output also transitions on the same edge as the data input.

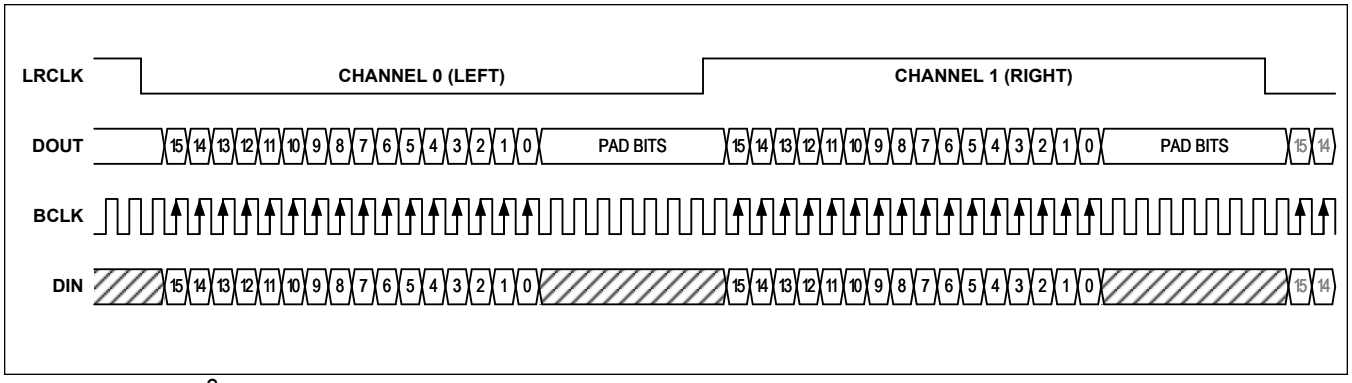


Figure 1. Standard I^2S Mode

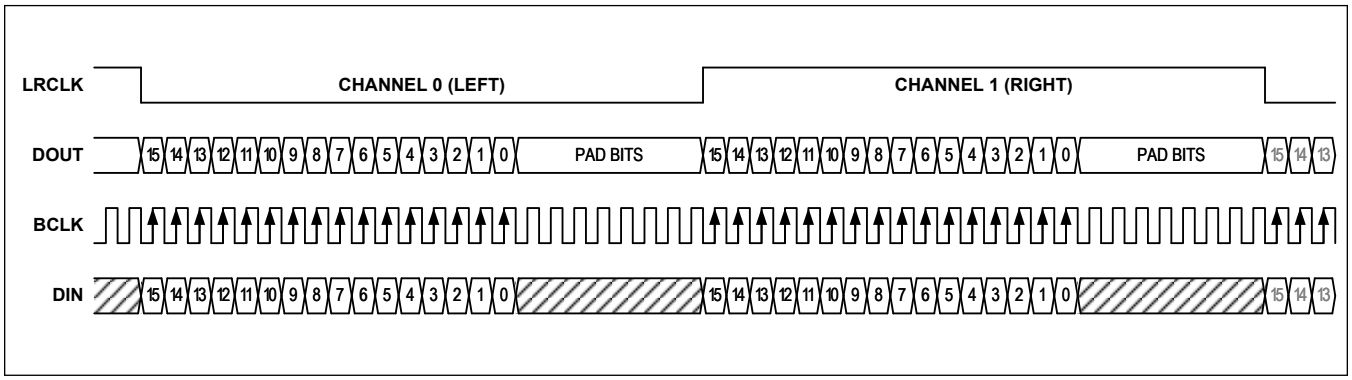


Figure 2. Left-Justified Mode

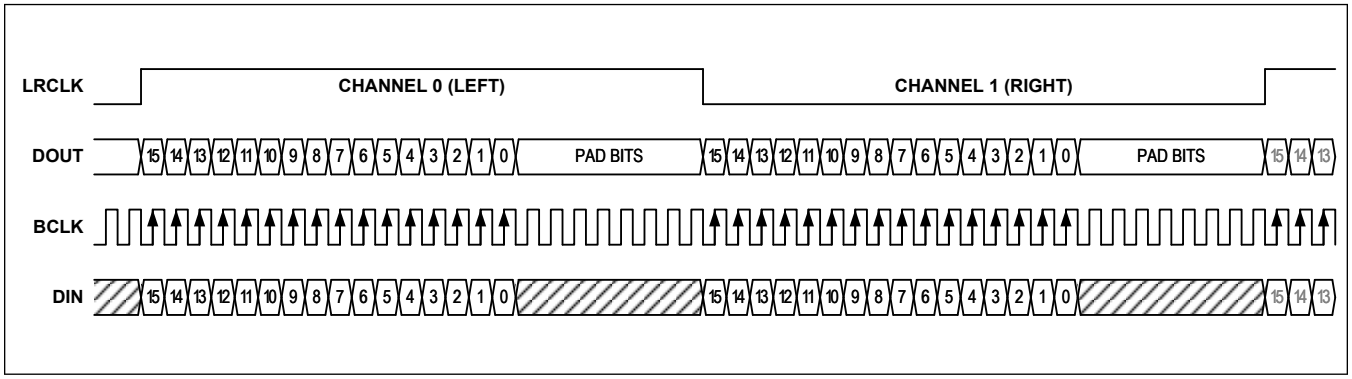


Figure 3. Left-Justified Mode (LRCLK Inverted)

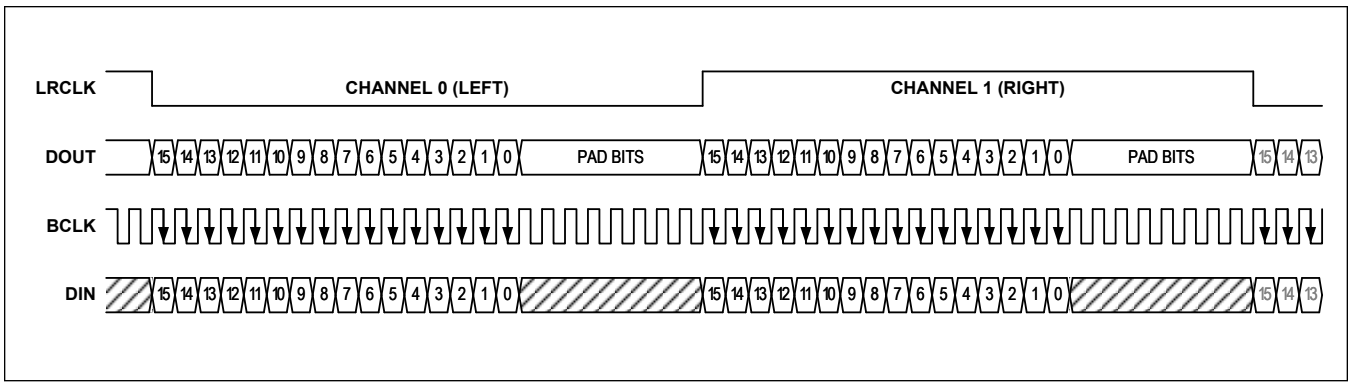


Figure 4. Left-Justified Mode (BCLK Inverted)

TDM Modes

The provided TDM modes supports timing for up to 16 digital audio input channels (from DIN) each containing 16-, 24-, or 32-bits of data. The digital audio output (to DOUT) is structured into 8-bit slots, and the timing can support up to a maximum of 64 data output slots. The number of TDM input channels and output slots is determined by both the selected BCLK to LRCLK ratio (*PCM_BSEL*) and the selected data word and channel length (*PCM_CHANSZ*).

For a given valid configuration, the number of available data input channels per frame is calculated as follows:

Number of Available Data Input Channels = BCLK to LRCLK Ratio/Channel Length

For a given valid configuration, the number of available 8-bit data output slots per frame is calculated as follows:

Number of Available Data Output Slots = BCLK to LRCLK Ratio/8

Table 5 shows the supported TDM mode configurations for each combination of input data channels and output data slots. In some configurations, the maximum PCM interface and speaker amplifier playback sample rate is limited to less than 96kHz to avoid violating the BCLK frequency limit of 24.576MHz.

Table 5. Supported TDM Mode Configurations

INPUT DATA CHANNELS	OUTPUT DATA SLOTS	DATA WORD SIZES (PCM_DATA_WIDTH)	BCLK TO LRCLK RATIO (PCM_BSEL)	MAXIMUM SPEAKER PLAYBACK SAMPLE RATE (FLRCLK)
2	4	16	32	96kHz
	6	24	48	
	8	32	64	
4	8	16	64	
	12	24	96	
	16	32	128	
8	16	16	128	
	24	24	192	
	32	32	256	
10	40	32	320	48kHz
16	32	16	256	96kHz
	48	24	384	48kHz
	64	32	512	

With the default PCM interface settings, in TDM mode a rising frame clock (LRCLK) edge acts as the frame sync pulse and indicates the start of a new frame. The frame sync pulse width must be equal to at least one bit clock period, however, the falling edge can occur at any time as long as it does not violate the setup time of the next frame sync pulse rising

edge. The *PCM_CHANSEL* bit can be used to invert the LRCLK edges (sync pulse) used to start a TDM frame.

In TDM mode, the MSB of the first audio word can be latched on the first (TDM mode 0), second (TDM mode 1), or third (TDM mode 2) active BCLK edge after the sync pulse and is programmed by the *PCM_FORMAT* bits. Additionally, the *PCM_BCLKEDGE* register bit allows for programmability of the BCLK edge that is used for data capture and data output. The data output is valid on the same active BCLK edge as the data input. The data output also transitions on the same edge as data input.

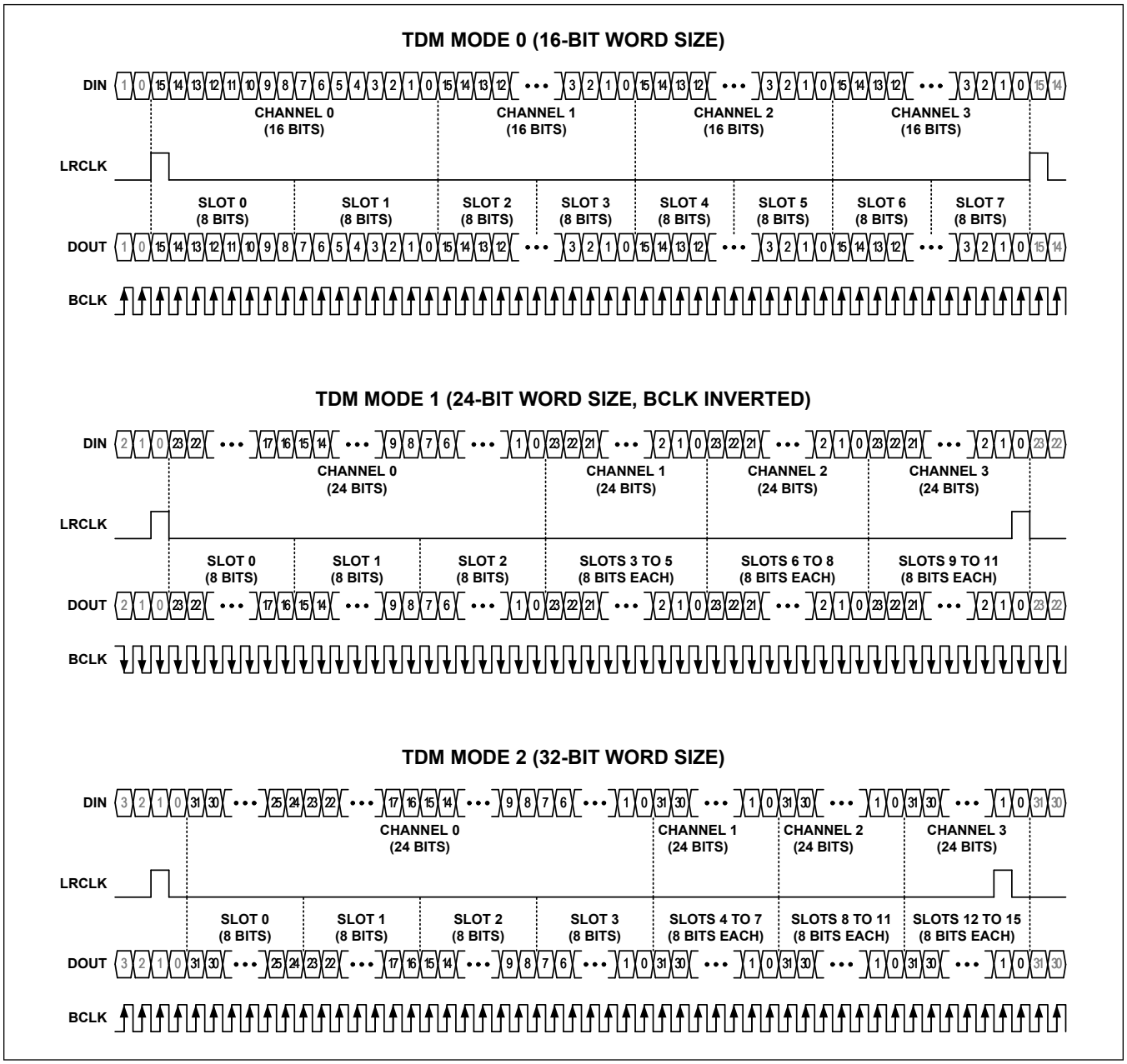


Figure 5. TDM Modes

PCM Data Path Configuration

The PCM interface data input (DIN) receives the source data for the speaker amplifier path, while the data output (DOUT) transmits the data from the I/V sense ADC path. In addition, the PCM data output can also transmit internal diagnostic data such as the speaker DSP monitor path, supply measurement ADC results, device status reporting, and the DHT attenuation level.

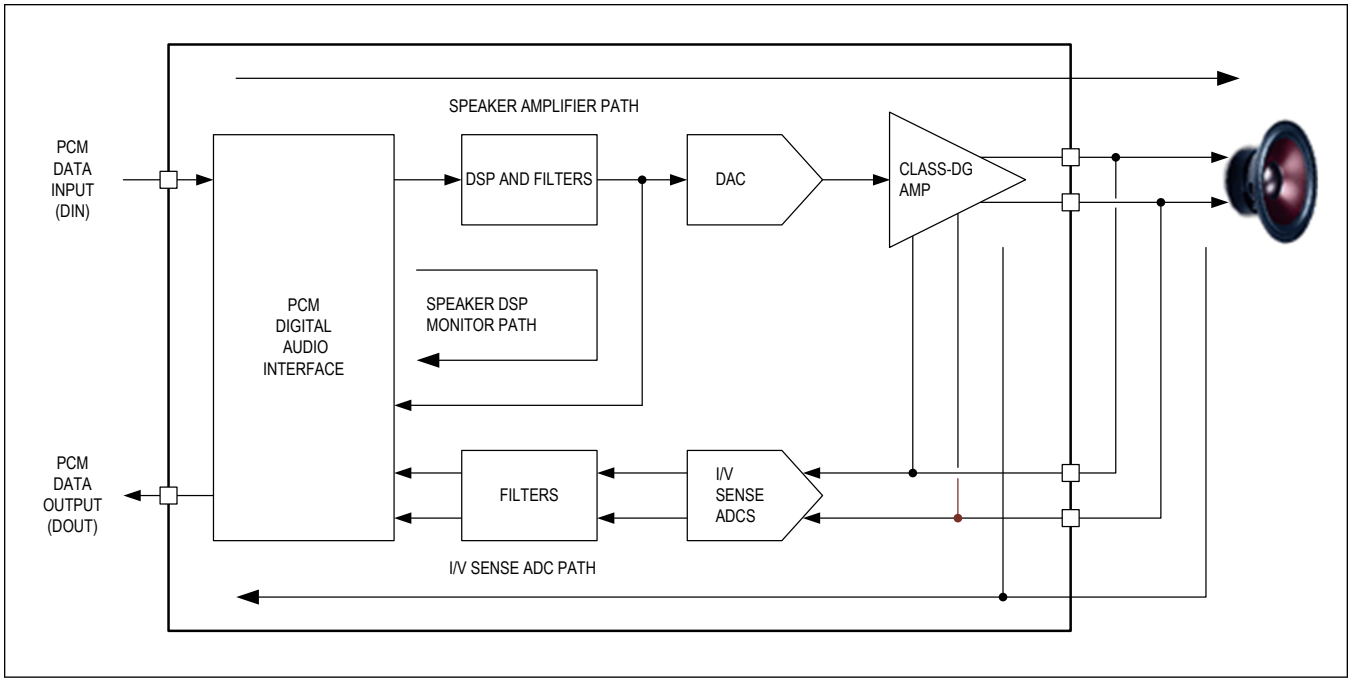


Figure 6. Device Audio Signal Path Diagram

PCM Data Input

The PCM interface data input (DIN) is enabled with the *PCM_RX_EN* bit and can accept data from any valid input data channel. The PCM interface data input should be enabled by setting *PCM_RX_EN* bit to 1 before entering device active state (*EN* = 1). The PCM interface data input (DIN) channel for the speaker playback path is selected with the *PCM_DAC_SOURCE* bit field. In I^2S and left-justified modes, only 2 input data channels are available, while in TDM mode, up to 16 channels of input data can be available. If the PCM data input is disabled (*PCM_RX_EN* = 0), a zero code value is driven into the speaker amplifier path.

PCM Data Output

The PCM interface data output (DOUT) is enabled by the *PCM_TX_EN* bit field, and can transmit any output data type onto any valid output channel or slot. In I^2S and left-justified mode, only 2 data output channels are available in each output transmit frame (channel 0 and 1). In TDM mode, each output transmit frame can contain up to 64 sequential 8-bit data output slots, each of which is numbered from 0 up to a maximum of 63.

The PCM data output can transmit several different output data types. In I^2S and left-justified modes, only the speaker amplifier output voltage sense, output current sense, and DSP monitor output data types are available for data output transmit. If the word size of the data output type is longer than the output channel data word (*PCM_CHANSZ*), the lowest trailing bits are truncated.

In TDM mode, all output data types are available and are individually assigned to data output slots. The output data types vary in word size from 8-bits to 32-bits, and as a result, in TDM mode require from 1 to 4 data output slots to transmit. Table 6 shows the supported output data types, and the parameters of each data type.

Table 6. Supported PCM Data Output Types

OUTPUT DATA TYPE	SYMBOL	DATA WORD SIZE	NUMBER OF TDM SLOTS	ENABLE/SLOT ASSIGNMENT
Speaker Amplifier Output Voltage Sense	VMON	16-bits	2	PCM_VMON_EN/ PCM_VMON_SLOT
Speaker Amplifier Output Current Sense	IMON	16-bits	2	PCM_IMON_EN/ PCM_IMON_SLOT
Speaker Amplifier DSP Monitor	DSPMON	32-bits	4	PCM_DSP_MONITOR_EN/ PCM_DSP_MONITOR_SLOT
Applied DHT Attenuation	DHT_ATN	16-bits	2	PCM_DHT_ATN_EN/ PCM_DHT_ATN_SLOT
Battery Voltage (V_{VBAT})	VBAT	16-bits	2	PCM_VBAT_EN/ PCM_VBAT_SLOT
PVDD Voltage (V_{PVDD})	PVDD	16-bits	2	PCM_PVDD_EN/ PCM_PVDD_SLOT
Device Status Flags	FLAG	8-bits	1	PCM_STATUS_EN/ PCM_STATUS_SLOT

An individual enable and slot assignment bit field is provided for each output data type. In I^2S and left-justified modes, use output slot 0 to assign data to channel 0 and output slot 1 to assign data to channel 1. In TDM mode, for data output types requiring more than 1 slot to transmit, the slot assignment selects the slot where the output data type transmit begins (for example, a 2 slot data type assigned to slot 6 would occupy slots 6 and 7).

In TDM mode, each data type can be assigned to any valid data output slot (or series of slots) with some restrictions. First, it is invalid for data types to be assigned such that the data word extends beyond the end of the data output frame. For example, data types that require 2 slots to transmit cannot be assigned to the last slot of the frame. Next, it is also invalid to assign a data output type to any slot that overlaps with the slot assignment of another data type (this also applies to channels in I^2S and left-justified modes). Finally, it is invalid to assign a data type to any slots that do not exist in the frame structure of the current PCM interface configuration.

Any data output (DOUT) slots that exist in the current frame structure but have no output data type assigned to them are either Hi-Z or driven with a 0 code (as set by the *PCM_TX_SLOT_HIZ* bit field). Likewise, if a data output type is disabled, then the assigned data output slot(s) are also either Hi-Z or driven with a 0 code (as set by the *PCM_TX_SLOT_HIZ* bit field).

Data Output Channel—Interleaved I/V Sense Data

In I^2S and left-justified use cases, the PCM interface limits the number of available data output channels to 2 making it impossible to fit amplifier output current and voltage sense data from stereo devices on a single shared data output (DOUT) line. For these cases, the data output can be configured to allow the current and voltage sense data types from a single device to share a single data output channel. To enable channel-interleaved mode, set the *PCM_TX_INTERLEAVE* bit high. Then assign the current and voltage sense data types to the same valid data channel (using *PCM_VMON_SLOT* and *PCM_IMON_SLOT*).

In this configuration, the current and voltage sense data types are frame interleaved on the assigned data output channel. The current and voltage sense data words are both 16-bits in length, and as a result, if the channel length is longer than 16-bits, the trailing padding bits are set to either Hi-Z or 0 code depending on the state of the *PCM_TX_EXTRA_HIZ* bit field.

To identify the data type in channel-interleaved mode, the LSB of the 16-bit data word is dropped (truncated). The data word is then right shifted by a single bit, and the now vacant MSB is replaced with either a 0 to indicate voltage sense data or a 1 to indicate current sense data. For phase alignment, the voltage sense data for a single sampling instant is always transmitted in the assigned channel on the first frame, followed by the current sense data on the second frame. The MSB value and the transmission order allow the host to identify and phase-align the output data across frames.

Since the I/V sense data is frame interleaved, the sample rate for the PCM interface must be greater than that of the I/V sense ADCs by an integer ratio of 2. The example below shows a basic case where the sample rate of the PCM interface is twice that of the I/V sense ADCs.

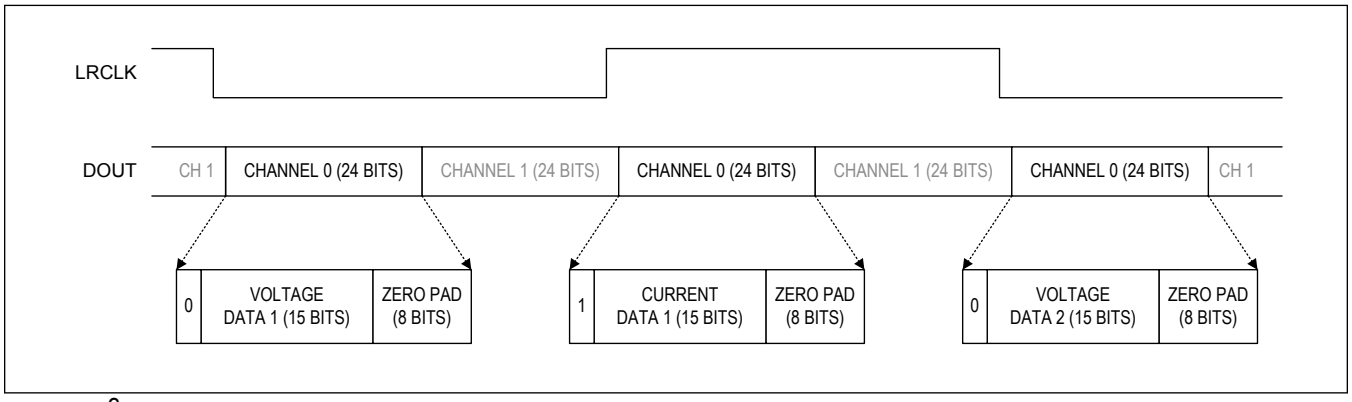


Figure 7. I²S Mode with Interleaved Voltage and Current Data , Channel Length = 24 Bits, Zero Padding

Data Output Shared Channel—I/V Sense Data

In I²S and left-justified use cases, the PCM interface limits the number of available data output channels to 2 making it impossible to fit amplifier output current and voltage sense data from stereo devices on a single shared data output (DOUT) line. For these cases, the data output can be configured to allow the current and voltage sense data types from a single device to share a single data output channel. To enable channel-shared mode, assign the current and voltage sense data types to the same valid data channel (using *PCM_VMON_SLOT* = *PCM_IMON_SLOT*). The voltage sense data is always transmitted first followed by the current sense data in the same assigned channel.

In this configuration, the BCLK/LRCLK ratio has to be configured for 64 or higher as the current and voltage sense data words are both 16-bits in length. If the BCLK/LRCLK ratio is less than 64, the current and voltage sense data do not decode properly.

Status Byte

The following interrupt information is reported in the status byte:

Bit 7 - Thermal warning begin

Bit 6 - Thermal warning end

Bit 5 - Thermal foldback begin

Bit 4 - Thermal foldback end

Bit 3 - DHT active end

Bit 2 - DHT active begin

Bit 1 - Speaker overcurrent

Bit 0 - Power-up done

PCM Interface Timing

Figure 8 and Figure 9 shows timing for BCLK, LRCLK, DIN, and DOUT. See the *Electrical Characteristics* table for more details.

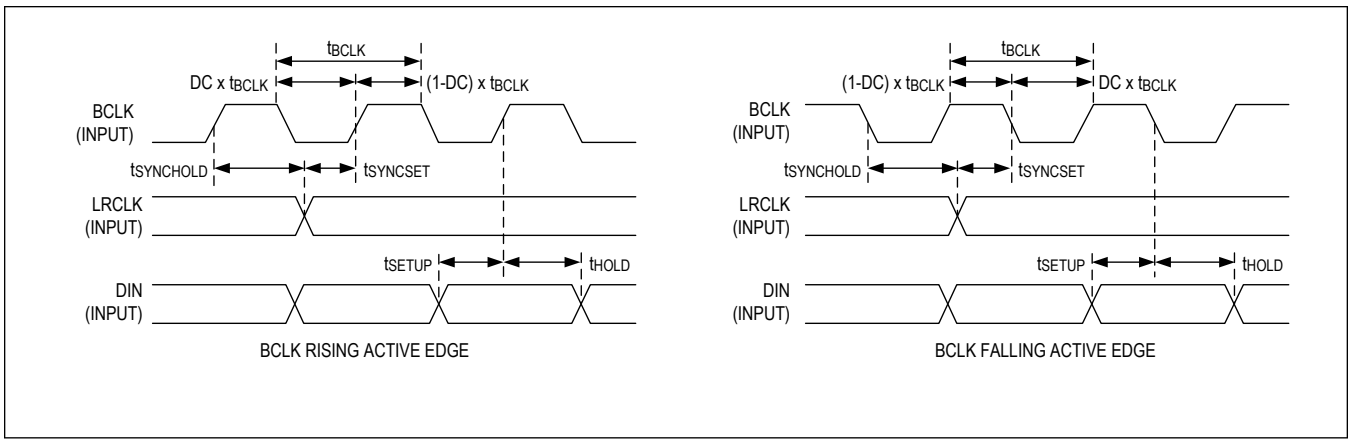


Figure 8. PCM Interface Timing/Slave Mode—LRCLK, BCLK, DIN Timing Diagram

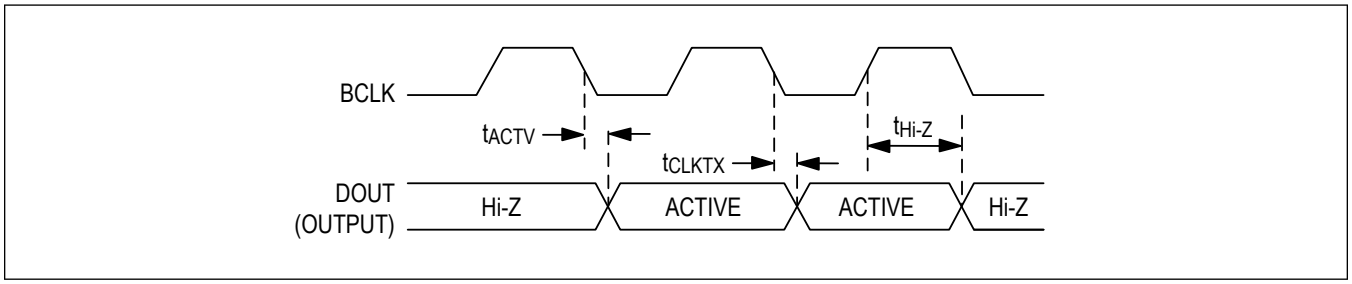


Figure 9. PCM Interface Timing/DOUT Timing Diagram

Interrupts

The device supports individually enabled status interrupts for sending feedback to the host about events that have occurred on-chip. When enabled, interrupts are transmitted on the IRQ output.

Interrupt Bit Field Composition

Each interrupt source has five individual bit field components. The function of each component is detailed below and the corresponding bit fields for each source can be identified by the appended suffix (shown in parentheses).

Raw Status (RAW): Each interrupt source has a read only bit to indicate the real-time raw status of the interrupt source.

State (STATE): Each interrupt source has a read only state bit that is set whenever a rising edge occurs on the associated raw status bit. The state bit is set regardless of the setting of the source enable bit.

Flag (FLAG): Each interrupt source has a read only flag bit. If the source enable bit is set, then the flag bit is set and an interrupt can be generated whenever the source state bit is set.

Enable (EN): Each interrupt source has a dynamic read/write enable bit. When the enable bit is set, the associated flag bit is set and an interrupt can be generated whenever the source state bit is set.

Clear (CLR): Each interrupt source has a dynamic write only clear bit. Writing a 1 to a clear bit resets the associated state and flag bits to 0. Writing a 0 to a clear bit has no effect. In I^2C control mode, the IRQ output is deasserted if all flag bits are 0.

Interrupt Output Configuration

The device allows the user to configure the drive mode, drive strength, and polarity of the IRQ output. The *IRQ_MODE* bit controls the drive mode. If *IRQ_MODE* is 0, the pin is configured as an open-drained output and requires an external pullup resistor. If *IRQ_MODE* is 1, then IRQ is configured as a push-pull CMOS output.

Additionally, when IRQ is configured as a push-pull CMOS output, the drive strength control (*IRQ_DRV*) bits set the drive strength of the IRQ output. Four different CMOS drive strengths are available.

The *IRQ_POL* bit controls the polarity of the IRQ bus. Interrupt events (a flag bit is set high) assert the IRQ bus low if IRQ_POL = 0 and high if IRQ_POL = 1. The IRQ bus deasserts if all flag bits are cleared (set low).

Interrupt Sources

Table 7. Interrupt Sources

INTERRUPT SOURCES	BIT FIELD	DESCRIPTION
Thermal Shutdown Begin Event	THERMSHDN_BGN_*	Indicates when the thermal-shutdown threshold has been exceeded.
Thermal Shutdown End Event	THERMSHDN_END_*	Indicates that the die temperature was previously above the thermal-shutdown threshold and has now dropped below the threshold.
Thermal Warning Begin Event	THERMWARN_BGN_*	Indicates when the thermal-warning threshold has been exceeded.
Thermal Warning End Event	THERMWARN_END_*	Indicates that the die temperature was previously above the thermal-warning threshold and has now dropped below the threshold.
Thermal Foldback Begin Event	THERMFB_BGN_*	Indicates die temperature is above the thermal-warning threshold and the device is attenuating the output.
Thermal Foldback End Event	THERMFB_END_*	Indicates die temperature is below the thermal-warning threshold and the device has stopped attenuating the output.
OTP Load Fail Event	OTP_FAIL_*	Indicates when the OTP load routine that runs when exiting hardware shutdown has failed to complete successfully. If the OTP load routine fails, the device is held in software shutdown.
Speaker Over Current Event	SPK_OVC_*	Indicates that the speaker amplifier current limit has been exceeded.
Internal CLK Error	INT_CLK_ERR_*	Indicates a clock stop error in the internal clocks of the device.
Internal Data Error	INT_SPKMON_ERR_*	Indicates a data error in the internal datapath of the device.
External CLK (BCLK/LRCLK) Error	CLK_ERR_*	Indicates a frequency or framing error in the input BCLK or LRCLK.
External CLK (BCLK/LRCLK) Recover	CLK_RECOVER_*	Indicates that the input BCLK or LRCLK has recovered after an error event.
External Data (DIN) Error	DMON_ERR_*	Indicates a data stuck or data magnitude error at the PCM data input (DIN).
Power-Up Done Event	PWRUP_DONE_*	Indicates when the device has entered the active state and the device is ready to play audio.
Power-Down Done Event	PWRDN_DONE_*	Indicates when the device has entered the software shutdown state.
PVDD UVLO Shutdown Event	PVDD_UVLO_SHDN_*	Indicates that PVDD is below the minimum allowed voltage when the device is in active state.

Table 7. Interrupt Sources (continued)

VBAT UVLO Shutdown Event	VBAT_UVLO_SHDN_*	Indicates that VBAT is below the minimum allowed voltage when the device is in active state.
DHT Active Begin Event	DHT_ACTIVE_BGN_*	Indicates that the DHT circuit is active and is applying attenuation to the signal.
DHT Active End Event	DHT_ACTIVE_END_*	Indicates that the DHT circuit has stopped applying attenuation to the signal.
NOTE: The bit fields are shown without the component suffixes. For example, OTP_FAIL_* refers to OTP_FAIL_RAW, OTP_FAIL_STATE, OTP_FAIL_FLAG, OTP_FAIL_EN, and OTP_FAIL_CLR. All Interrupt sources have these 5 component bit fields.		

Speaker Path

The source input data to the speaker amplifier path is routed from either the PCM interface or the tone generator. The data is then routed through digital filters, signal processing, and volume/gain control blocks before reaching the Class-DG speaker amplifier.

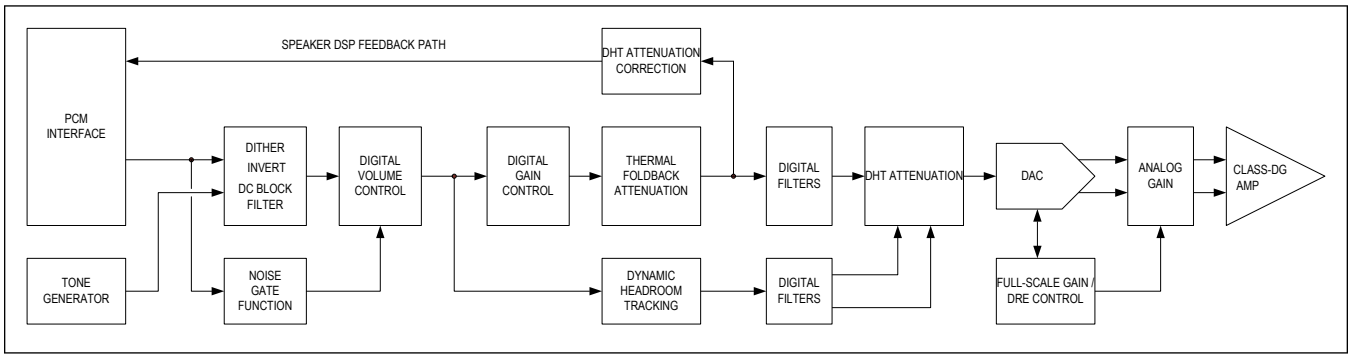


Figure 10. Speaker Signal Path Diagram

Speaker Path Noise Gate

The speaker path noise gate function is enabled when the device is in the active state and the noise gate enable (*NG_EN*) is set to 1. The noise gate enable can be programmed dynamically. However, if the noise gate function is disabled (*NG_EN* is set to 0) while the noise gate is active (speaker path actively muted), the noise gate function remains active until after it deactivates normally (unmutes the speaker path).

When the noise gate is enabled, the noise gate activates whenever the amplitude of the input audio data to the speaker path (from the PCM interface) is below the configured mute threshold (*NG_MUTE_THRESH*) for more than 1024 consecutive data samples. When the noise gate is active, the amplifier path is muted, the current and voltage sense ADC paths output zero code data, and the device idles in a reduced power state.

The noise gate deactivates immediately if the amplitude of a single sample from the input audio data exceeds the configured unmute threshold (*NG_UNMUTE_THRESH)*. When the noise gate deactivates, the speaker path is unmuted and returns to normal operation before the input audio data (that triggered deactivation) reaches the speaker output. Once noise gate deactivation is completed, the current and voltage sense ADC paths resume operation and output data normally.

The noise gate mute and unmute threshold settings are selected in terms of the number of bits (starting from the LSB) that must be toggling (or active) in order for the input signal amplitude to exceed the thresholds. It is invalid to set the noise gate unmute threshold (*NG_UNMUTE_THRESH*) such that it is less than the configured mute threshold (*NG_MUTE_THRESH*). The location of the audio data LSB within the PCM input data channel is determined by the configured PCM data word size (*PCM_CHANSZ*). The supported combinations are shown in Table 8.

Table 8. Noise Gate Threshold LSB Location by Input Data Configuration

INPUT DATA WORD SIZE (*PCM_CHANSZ*)	NOISE GATE FUNCTION LSB LOCATION
16	16
24	24
32	

It is not valid to enable the speaker path noise gate function when the tone generator is enabled.

Speaker Path Dither

The input data to the speaker path can optionally have dither (±1LSB peak-to-peak) applied if *SPK_DITH_EN* is set to 1. No dither is applied when *SPK_DITH_EN* is set to 0.

Speaker Path Data Inversion

The input data to the speaker path can optionally be inverted by setting the *SPK_INVERT* bit is set to 1.

Speaker Path DC Blocking Filter

A DC blocking filter can be enabled on the speaker path by setting the *SPK_DCBLK_EN* bit to 1.

Speaker Path Digital Volume Control

The device provides a dynamically programmable speaker path digital volume control. The digital volume control provides an attenuation range of 0dB to -63dB in 0.5dB steps that is configured with the *SPK_VOL* bit field. A digital mute is also provided, and is enabled when *SPK_VOL* is set to 0x7F.

Digital volume ramping during speaker path start up, speaker path shutdown, and digital mute (*SPK_VOL* = 0x7F) is disabled by default. However, both the volume ramp up and ramp down can be individually enabled with the *SPK_VOL_RMPUP_BYPASS* and *SPK_VOL_RMPDN_BYPASS* bit fields respectively. When volume ramp up or ramp down is enabled, the device turn-on and turn-off times are longer.

Speaker Path Digital Gain Control

The device provides a programmable speaker path digital gain control. The digital gain control provides a range of 0dB to +6dB in 0.5dB steps that is configured with the *SPK_GAIN* bit field. Unlike the digital volume control, the digital gain setting cannot be dynamically changed.

Speaker Path DSP Data Feedback Path

The speaker path DSP data can be routed from just before the DAC input back to the PCM interface, and can be assigned to any valid data output channel. The speaker path DSP data feedback path is enabled with the *SPK_FB_EN* bit.

Speaker Safe Mode

The device provides a safe mode bit (SPK_SAFE_EN), which when set to 1, applies a -18dB attenuation to the input signal. By default, speaker safe mode is enabled to protect any speaker connected to the device on power up when the off-chip speaker protection algorithm is still initializing. While speaker safe mode is enabled, the digital volume control (*SPK_VOL*) and speaker digital gain control (*SPK_GAIN*) settings are ignored.

Speaker Path Maximum Peak Output Voltage Scaling

The device operates over a large PVDD supply voltage range, and as a result, the full-scale speaker amplifier output amplitude level is configurable to allow it to be scaled. As a baseline, the full-scale output of the speaker path DAC is 3.68dBV (typical). The speaker path no-load maximum peak output voltage level (V_{MPO}) is then programmable relative to this baseline level. The peak output scaling range is from +4dB to +18dB, and is set with the *SPK_GAIN_MAX* bit field.

The speaker output signal level (in dBV) for a given digital input signal level (in dBFS) is calculated as follows:

Output Signal Level (dBV) = Input Signal Level (dBFS) + 3.68 (dBV) + SPK_GAIN_MAX (dB)

(0dBFS is referenced to 0dBV)

The peak output voltage scaling is applied to the signal path using a combination of digital gain and analog gain adjustments.

Dynamic Headroom Tracking (DHT)

The device features DHT that can preserve consistent signal distortion and listening levels in the presence of a varying supply level. The DHT block provides both a dynamic range compressor (DRC) and limiter. The limiter can operate as either a signal distortion limiter (SDL) or standard signal level limiter (SLL). Each of these three functions can be used independently (modes 1 through 3), and the SLL and DRC can be used simultaneously (mode 4).

The DHT block is enabled with the *DHT_EN* bit. Prior to enabling the DHT, the measurement ADC PVDD and VBAT channels should be configured and enabled as required based on the amplifier mode of operation. The DHT block uses the measured supply levels and the current signal level to calculate the attenuation (if any) that is applied to the signal path. Also, the DHT block should not be disabled by setting the DHT_EN bit to 0 when the DHT is active (i.e., attenuation is being applied).

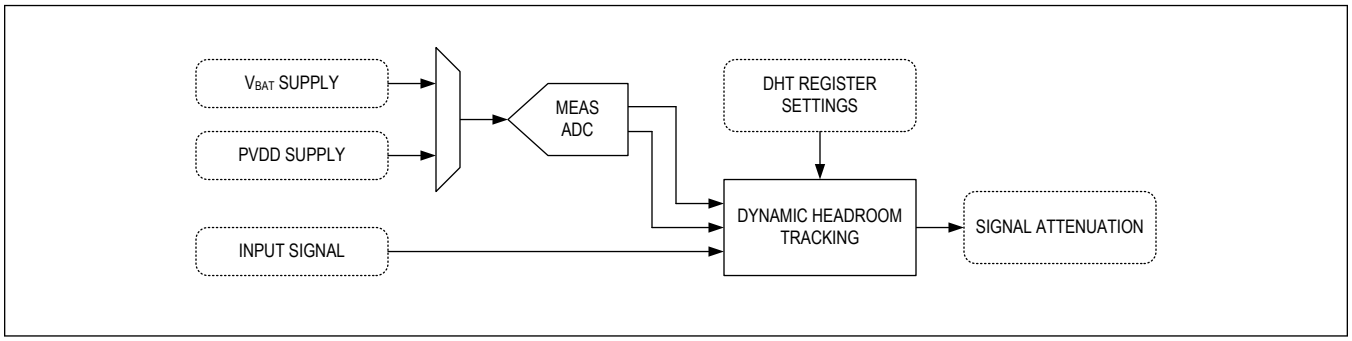


Figure 11. Simplified Dynamic Headroom Tracking System Block Diagram

DHT Supply Tracking and Headroom

The DHT block uses three parameters to track the target peak output level (V_{TPO}) relative to the maximum peak output voltage (V_{MPO}) as the active speaker amplifier supply level varies.

The first is the speaker amplifier full-scale gain setting (*SPK_GAIN_MAX* bit field). This control selects the maximum (no-load) peak output voltage level (V_{MPO}) that is output by the Class-DG amplifier with a full-scale input signal (0dBFS). Most DHT thresholds and parameters are calculated relative to the full-scale V_{MPO}. The DHT block uses a maximum gain of 16dB for calculating the maximum (no-load) peak output voltage level and so for gain settings above 16dB set by *SPK_GAIN_MAX* = 0x0D(17dB) and 0xOE(18dB) the DHT block underestimates the gain by 2dB.

The second parameter is the measured speaker amplifier supply voltage level (V_{SUP}). The measurement ADC provides the DHT block with the current supply voltage levels (V_{PVDD} and V_{VBAT}). The DHT block decides which supply voltage to use for calculations based on the currently active speaker amplifier supply.

The third parameter is the speaker amplifier supply headroom (SUP_{HR}). The supply headroom is a positive or negative percentage offset relative to the measured V_{SUP} conversion result. It is configured using the *DHT_HR* bit field, and can be set from +20% to -20% of V_{SUP} in 2.5% step sizes.

The DHT target peak output voltage level (V_{TPO}) is equal to the measured supply voltage (V_{SUP}) scaled to include the selected supply headroom percentage, and is actively calculated with the following equation:

$$V_{TPO} = V_{SUP} \times (100\% – SUP_{HR})$$

The target peak output attenuation (or ratio) from V_{TPO} to V_{MPO} is calculated as follows:

$$A_{TPO} = 20 \times \log (V_{TPO}/V_{MPO})$$

If A_{TPO} exceeds 0dB (V_{SUP} with headroom > V_{MPO}), then the DHT block assumes that there is sufficient supply voltage to reproduce the audio signals as configured without attenuation. In this case, A_{TPO} = 0dB is used for all further calculations. This is important as the DHT functions only apply attenuation, and never apply positive gain. Once the calculated V_{TPO} drops below V_{MPO}, the calculated target peak output attenuation (A_{TPO}) is less than 0dB, and the DHT functions are applied appropriately as the input signal level changes.

For example, if V_{MPO} = 13.63V, V_{SUP} = 8.04V, and SUP_{HR} = -20%, then solving for V_{TPO} yields a target peak output level of ~9.65V. Next, solving for the target peak output attenuation (A_{TPO}) yields approximately -3dB.

Figure 12 shows the default transfer function (with no DHT attenuation applied), where the current target peak output level (V_{TPO}) is based on the current V_{SUP}, and the supply headroom settings. The tracked V_{TPO} and the resulting peak output attenuation (A_{TPO}) are then used in the attenuation calculations for the DHT functions. Note that this and all subsequent figures are not drawn to precise scale, and that the x-axis input signal level (dBFS) is on a linear scale, while the y-axis peak output voltage level is on a log scale.

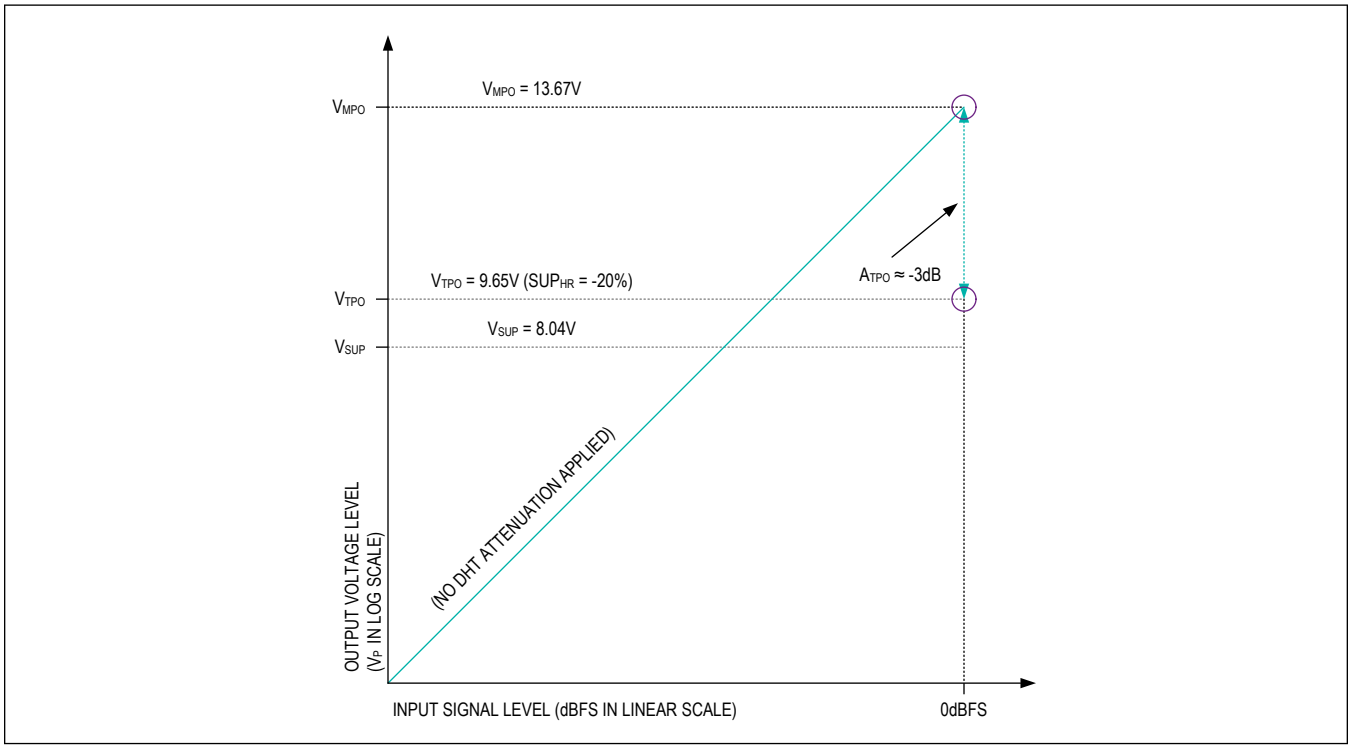


Figure 12. V_{TPO} and A_{TPO} Calculation Example

DHT Mode 1—Signal Distortion Limiter (SDL)

The DHT signal distortion limiter (SDL) maintains a consistent level of signal distortion at the amplifier output as the supply voltage (V_{SUP}) changes. To use DHT mode 1 (just the signal distortion limiter active), set the *DHT_LIM_MODE* bit low (default) to place the limiter function in supply tracking mode (SDL), and set the dynamic range compressor rotation point (*DHT_VROT_PNT*) to 0dBFS (effectively disabling the DRC). The signal distortion limiter function is a compressor with a ratio of infinity to 1 that actively sets its threshold (V_{SDL} in voltage) equal to the calculated target peak output voltage level (V_{TPO}). The output referred SDL threshold (SDL_{THR}) and the input referred SDL knee or rotation point (SDL_{RP}) are equal in mode 1, and can be calculated relative to full-scale (in dBFS) as a ratio of V_{TPO} to V_{MPO}:

$$SDL_{RP} = SDL_{THR} = 20 \times \log (A_{TPO}) = 20 \times \log (V_{TPO}/V_{MPO})$$

The transfer function for input signal levels below the SDL rotation point (SDL_{RP}) is unchanged. When the input signal level exceeds SDL_{RP}, the signal distortion limiter function is applied to the signal path. As the input signal level increases, the distortion limiter attenuation continues to increase as well and can be calculated for a given input signal level (A_{INPUT} in dBFS) as follows:

$$SDL\ ATTENUATION = SDL_{RP} - A_{INPUT}$$

By actively recalculating SDL_{RP} (or SDL_{THR}) as the target peak output level (V_{TPO}) changes, the DHT SDL maintains a consistent limit and level of amplifier output distortion relative to available supply voltage (V_{SUP}).

When the target peak output voltage (V_{TPO}) exceeds the amplifier maximum peak output voltage (V_{MPO}), there is sufficient headroom and no SDL attenuation is applied. However, as soon as V_{TPO} falls below V_{MPO}, it is possible for the input signal amplitude to exceed the calculated SDL_{RP}. The following examples show the transfer function when $V_{SUP} \geq V_{MPO}$ with the minimum (-20%), no (0%), and maximum (+20%) supply headroom (SUP_{HR}) settings. Note that in the case with positive headroom (+20%), the SDL_{RP} falls below the input signal full-scale level even though $V_{SUP} = V_{MPO}$.

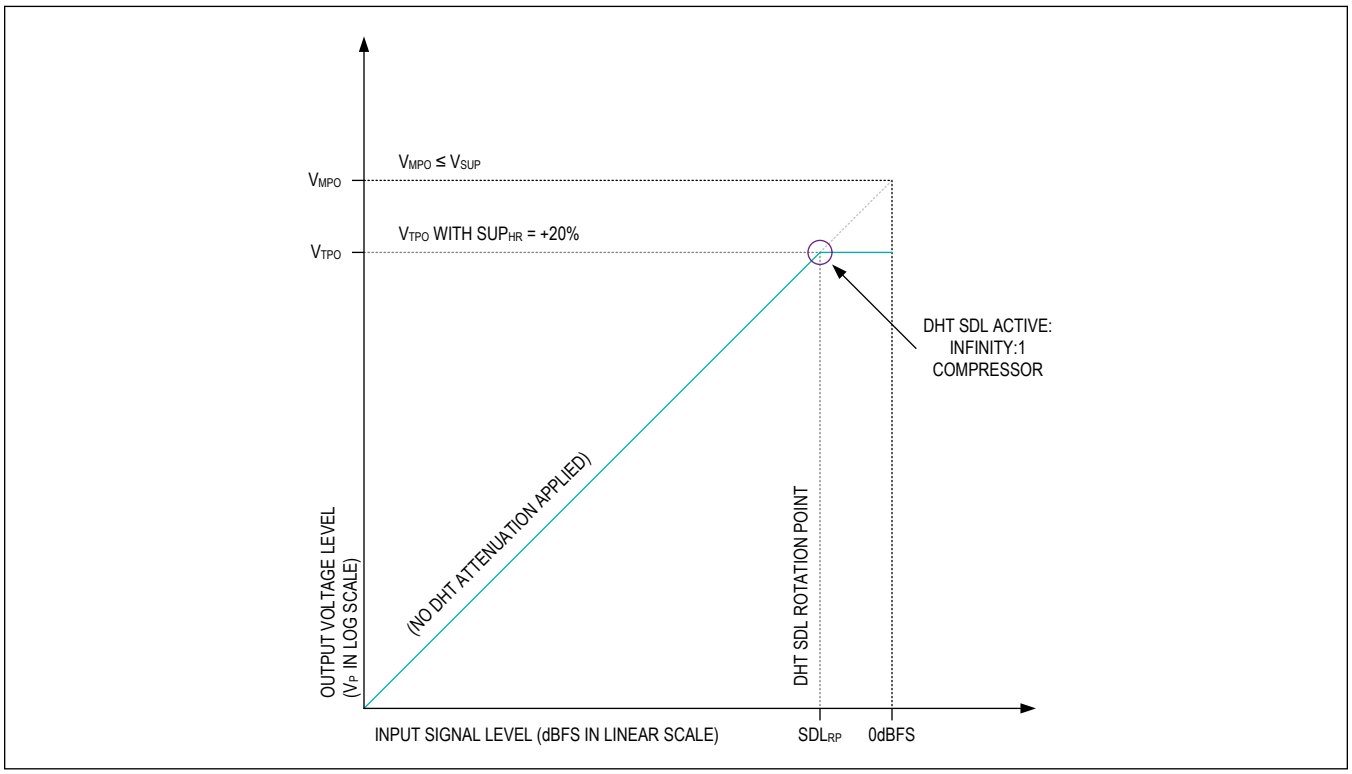


Figure 13. Signal Distortion Limiter with $V_{MPO} \leq V_{SUP}$ and +20% Headroom (SUP_{HR})

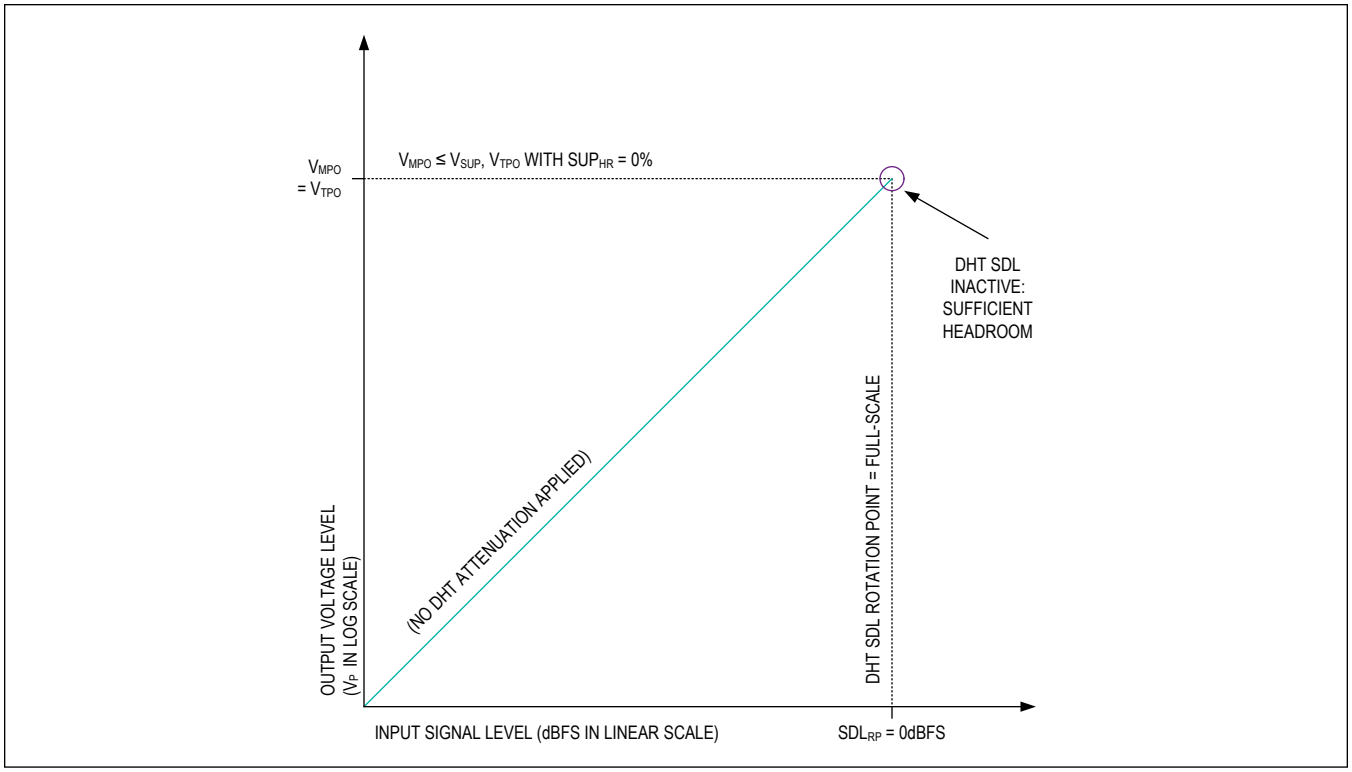


Figure 14. Signal Distortion Limiter with $V_{MPO} \le V_{SUP}$ and 0% Headroom (SUP_{HR})

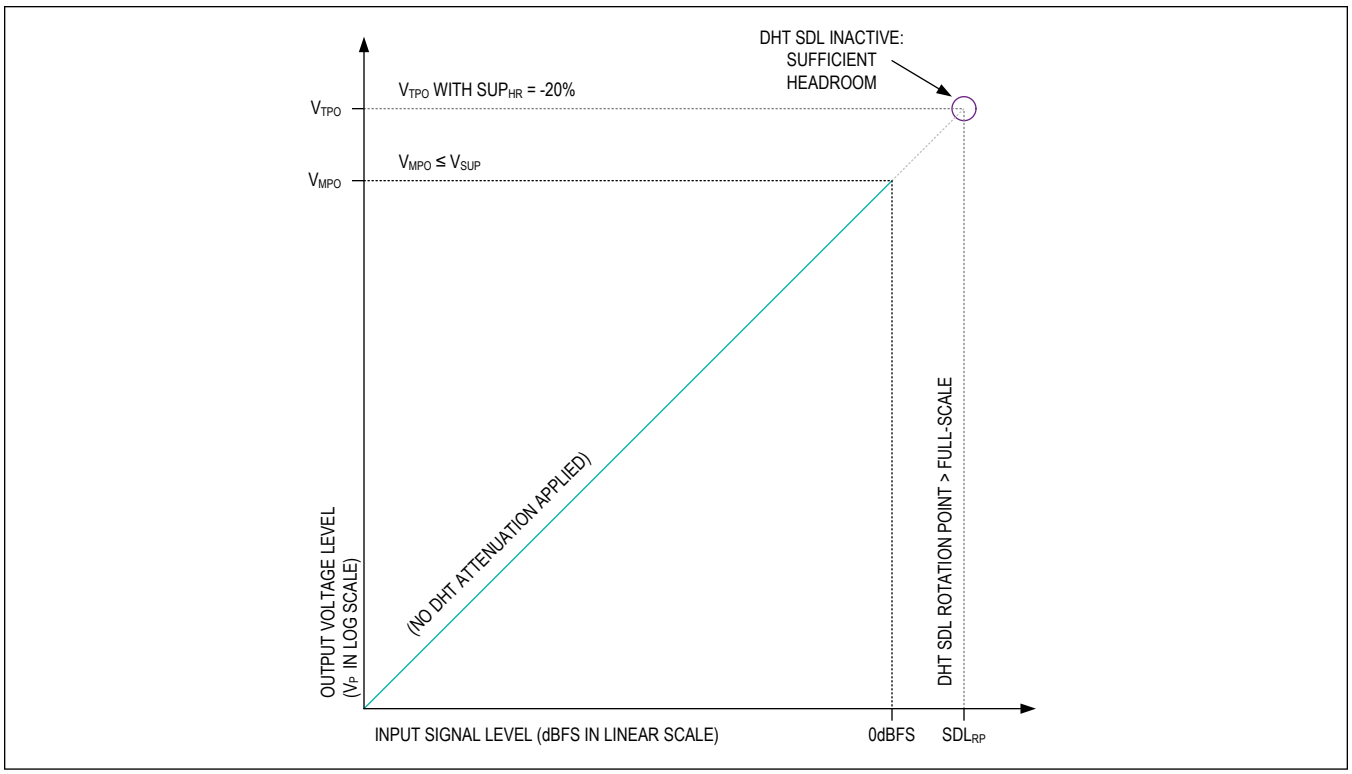


Figure 15. Signal Distortion Limiter with $V_{MPO} \leq V_{SUP}$ and -20% Headroom (SUP_{HR})

As the supply voltage (V_{SUP}) drops further below the maximum peak output voltage (V_{MPO}), the DHT target peak output voltage (V_{TPO}) proportionally scales down. In cases with zero or positive amplifier supply headroom settings (+20% ≥ SUP_{HR} ≥ 0%), the input signal level can exceed the SDL rotation point (SDL_{RP}) before the peak output exceeds V_{SUP}. In this case, amplifier output clipping can be prevented.

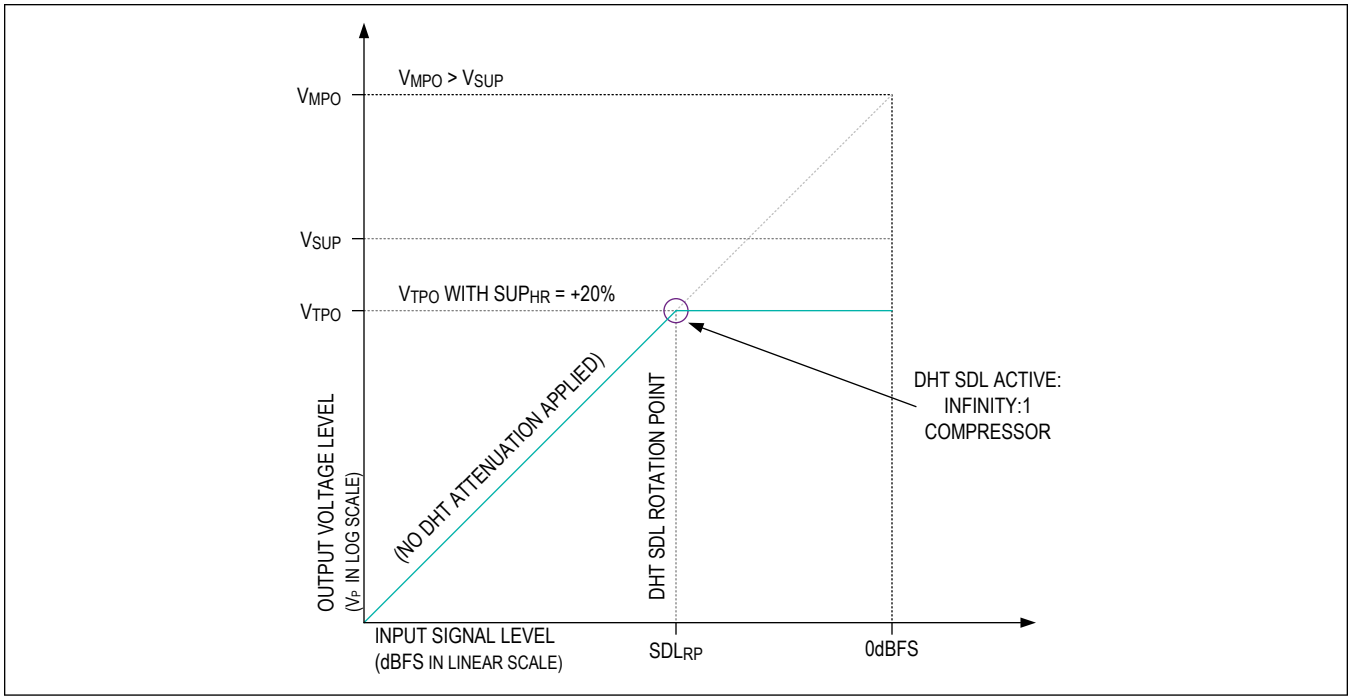


Figure 16. Signal Distortion Limiter with V_{MPO} > V_{SUP} and +20% Headroom (SUP_{HR})

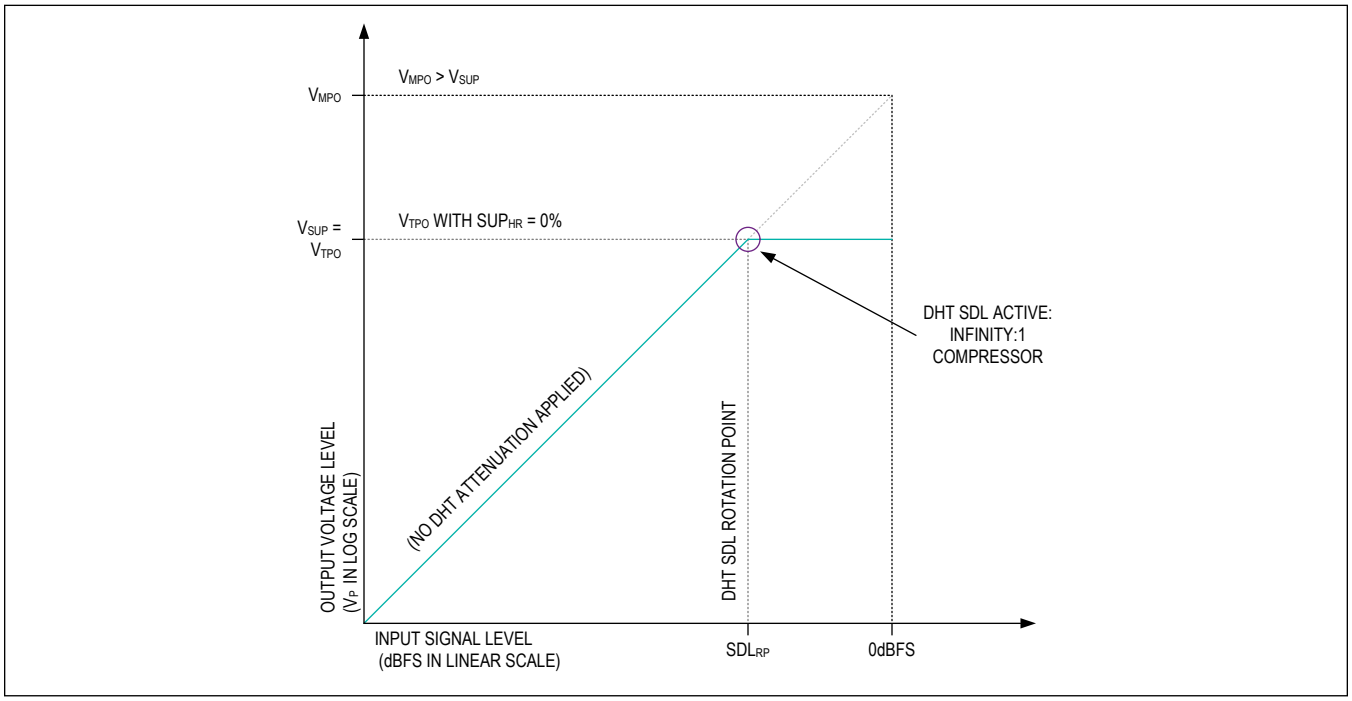


Figure 17. Signal Distortion Limiter with V_{MPO} > V_{SUP} and 0% Headroom (SUP_{HR})

In cases with a negative supply headroom setting (0% > SUP_{HR} ≥ -20%), the input signal does not exceed the SDL_{RP} until after the peak output reaches V_{SUP}. As a result, clipping occurs at the amplifier output. However, once the input signal level exceeds the SDL_{RP}, the audio signal level is digitally limited by the SDL preventing the amplifier output clipping from worsening further.

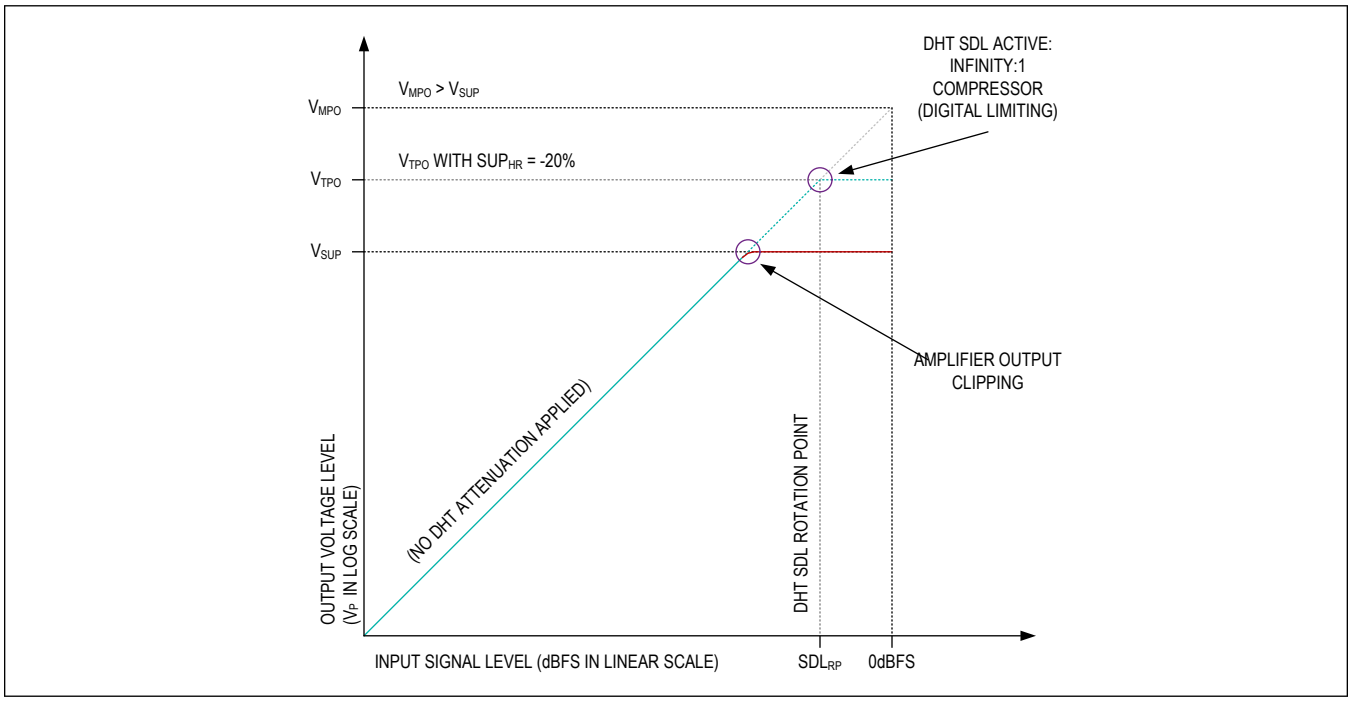


Figure 18. Signal Distortion Limiter with V_{MPO} > V_{SUP} and -20% Headroom (SUPHR)

DHT Mode 2—Signal Level Limiter (SLL)

In DHT mode 2, the limiter is configured as a fixed threshold signal level limiter (SLL). Set the *DHT_LIM_MODE* bit high to place the limiter function in SLL mode, and set the dynamic range compressor rotation point to 0dBFS (effectively disabling the DRC).

Like the signal distortion limiter, the signal level limiter function is a compressor with a ratio of infinity to 1. However, unlike the SDL, the SLL output referred threshold (SLL_{THR}) is configured to a set level. The SLL_{THR} is selected with the *DHT_LIM_THRES* bit field from a range of 0dBFS to -15dBFS. The SLL threshold can also be expressed as an input referred knee or rotation point (SLL_{RP}) which is equal to SLL_{THR} in mode 2. The SLL amplifier peak output voltage limit (V_{SLL}) is calculated from the selected SLL threshold (SLL_{THR}) and maximum peak output voltage (V_{MPO}) with the following equation:

$$\text{SLL PEAK OUTPUT VOLTAGE LIMIT} = V_{SLL} = V_{MPO} \times 10\ \text{^}(SLL_{THR}/20)$$

The transfer function for signal levels below the SLL threshold (SLL_{THR}) is unchanged. When the signal level exceeds the SLL_{THR}, the signal level limiter function is applied to the signal path. As the input signal level increases, the limiter attenuation continues to increase as well and can be calculated for a given input signal level (A_{INPUT} in dBFS) relative to SLL_{RP} (= SLL_{THR}) as follows:

$$\text{SLL ATTENUATION} = SLL_{RP} - A_{INPUT}$$

When V_{TPO} is greater than V_{SLL}, the amplifier peak output level is limited to V_{SLL} whenever the signal amplitude exceeds the SLL threshold (SLL_{THR}). As a result of the fixed SLL threshold and rotation point, the transfer function is identical for any V_{SUP} level and corresponding V_{TPO} that is greater than V_{SLL}.

This is illustrated in Figure 19 for decreasing V_{SUP} and V_{TPO} levels. As V_{SUP} decreases, V_{TPO} is recalculated and decreases as well. Three different, progressively lower V_{TPO} levels are shown (V_{TPO1}, V_{TPO2}, and V_{TPO3}). Due to the fixed SLL threshold, V_{SLL} is the same in all three cases. Since all three V_{TPO} values are greater than V_{SLL}, the transfer function for each case is identical and is limited at V_{SLL}.

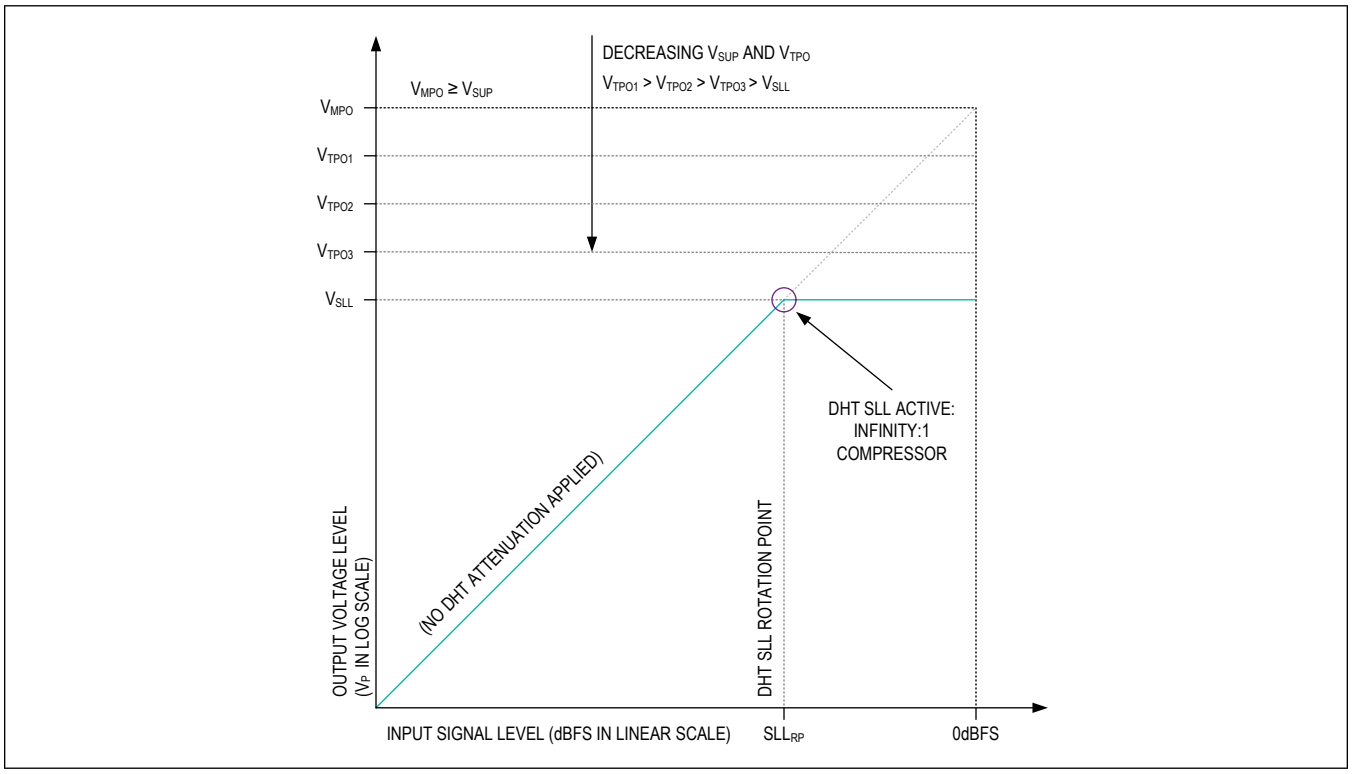


Figure 19. Signal Level Limiter with V_{TPO} > V_{SLL} as V_{SUP} Decreases

When the V_{TPO} is less than V_{SLL}, the amplifier output can clip before the input signal amplitude exceeds the SLL rotation point (SLL_{RP} = SLL_{THR}). As the input signal level continues to increase, once it exceeds SLL_{RP} the signal level is digitally limited preventing the amplifier output clipping from worsening further. Because both the SLL threshold and rotation point are fixed relative to full-scale, as V_{SUP} continues to decrease, the clipping at the amplifier output grows progressively worse prior to the input signal exceeding SLL_{RP} (= SLL_{THR}).

Figure 20 has the same SLL settings as Figure 19 (same SLL_{THR}). For simplicity, V_{TPO} = V_{SUP} (SUP_{HR} = 0%) and V_{TPO} has decreased further and is now less than V_{SLL}. As a result, the amplifier output clips before the SLL digitally limits the signal level.

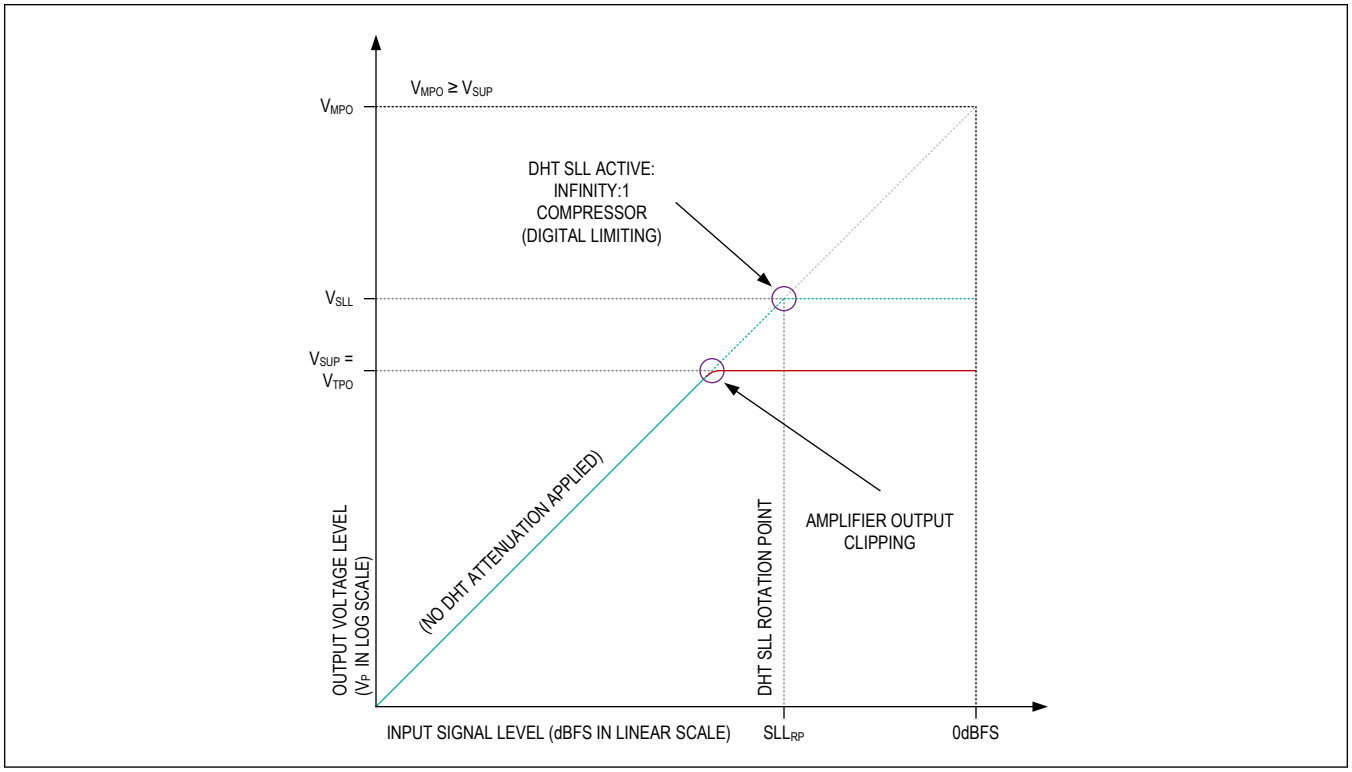


Figure 20. Signal Level Limiter with V_{TPO} < V_{SLL} Showing Amplifier Output Clipping

DHT Mode 3—Dynamic Range Compressor (DRC)

The DHT dynamic range compressor (DRC) is configured by setting the input referred rotation point (DRC_{RP} in dBFS). The DRC_{RP} can be selected from a 0dBFS to -15dBFS range with the *DHT_VROT_PNT* bit field. To calculate the DRC output referred voltage threshold (V_{DRC}), use the following equation:

$$V_{DRC} = V_{MPO} \times 10 \text{ ^ } (DRC_{RP}/20)$$

For mode 3 operation, set the DRC rotation point (DRC_{RP}) to any level lower than 0dBFS. Next, to disable limiter functions, place it into signal level limiter mode (*DHT_LIM_MODE* = 1), and set the fixed SLL threshold (SLL_{THR}) to 0dBFS (using the *DHT_LIM_THRES* bit field).

Once configured, the dynamic range compressor rotation point (DRC_{RP}) is fixed at the selected level (or ratio) relative to input full-scale. As V_{SUP} and V_{TPO} change, the DRC compression ratio for input signals exceeding DRC_{RP} changes as well. The transfer function, however, for input signals below DRC_{RP} remains unchanged.

DHT tracks the target peak output voltage (V_{TPO}) and attenuation (A_{TPO}). As they change, the adaptive DRC compression ratio smoothly scales the listening level of the amplifier (for any input signals that exceed DRC_{RP}). The DRC compression ratio is actively calculated with the following formula:

$$\text{DRC COMPRESSION RATIO} = DRC_{RP}/(A_{TPO}–DRC_{RP})$$

The DRC attenuation for a given input signal level (A_{INPUT} in dBFS) is calculated as follows:

$$\text{DRC ATTENUATION} = \text{ATPO–AINPUT x (ATPO/DRCRP)}$$

The following example shows the DRC transfer function with SUP_{HR} ≥ 0% as V_{SUP} (and thus V_{TPO}) decreases. As the V_{TPO} level decreases (from V_{TPO1} to V_{TPO2} to V_{TPO3}), the DRC compression ratio increases.

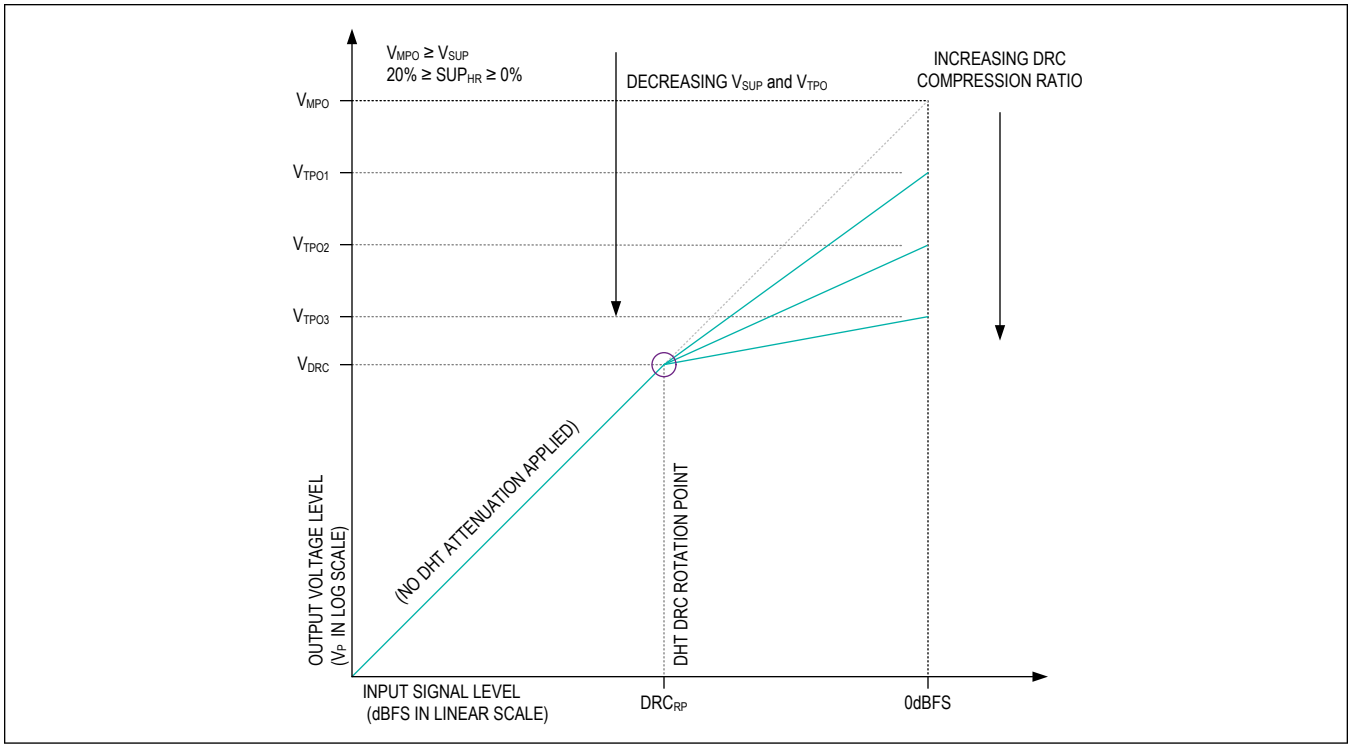


Figure 21. Dynamic Range Compression with Decreasing V_{SUP} and SUP_{HR} ≥ 0%

Figure 22 shows the DRC transfer function with SUP_{HR} < 0%. Due to the negative supply headroom, V_{TPO} is greater than V_{SUP} and the amplifier output clips before the input signal reaches full-scale.

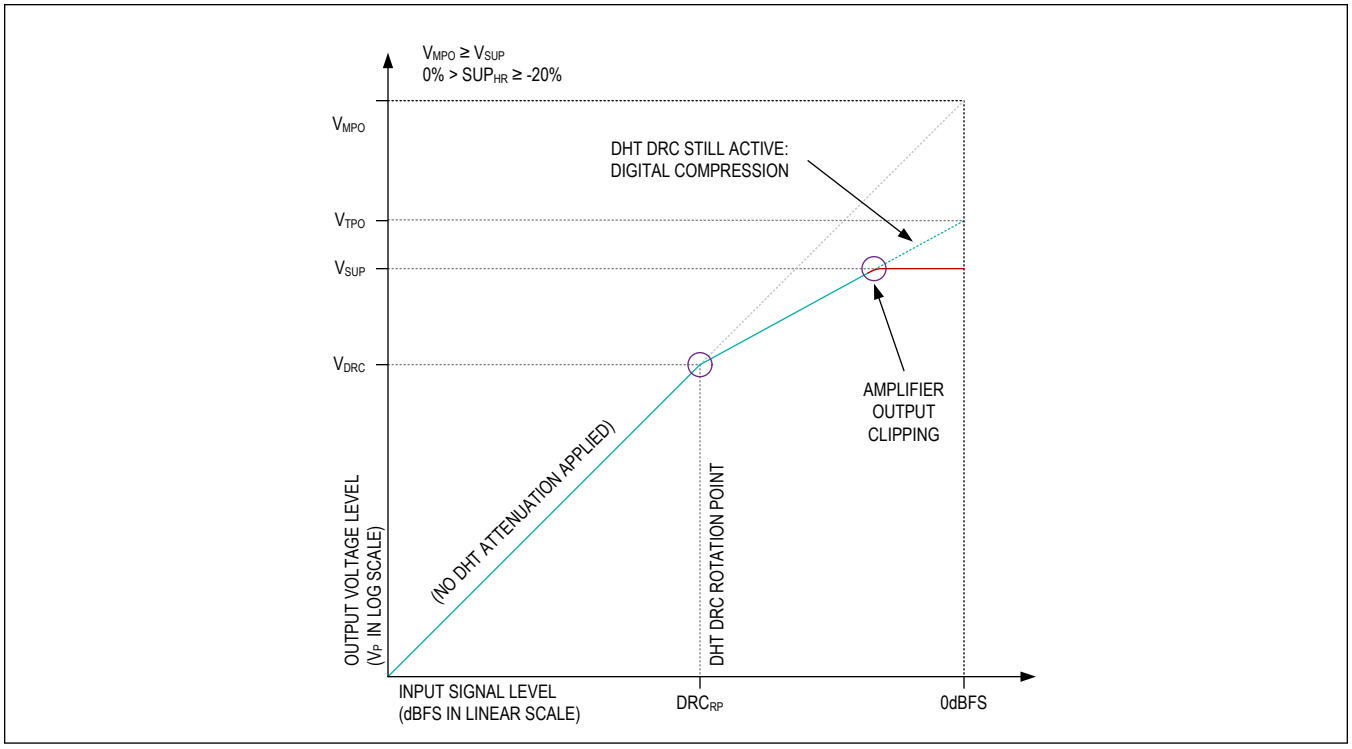


Figure 22. Dynamic Range Compressor with SUP_{HR} < 0% and Output Clipping

DHT Mode 4—Dynamic Range Compressor (DRC) with Signal Level Limiter (SLL)

In DHT mode 4, the dynamic range compressor (DRC) and signal level limiter (SLL) are both enabled. To allow mode 4, the DRC rotation point (DRC_{RP}) must be less than 0dBFS. In addition, the DHT limiter function must be configured for SLL mode (*DHT_LIM_MODE* = 1) with an SLL threshold (SLL_{THR}) less than 0dBFS. Finally, to create a DHT response curve with both DRC and SLL inflection points, the SLL threshold (V_{SLL}) must be greater than the DRC voltage threshold (V_{DRC}). This insures that the resulting SLL_{RP} is always greater than the DRC_{RP} (otherwise, the SLL limits the signal level before the DRC rotation point is ever reached).

Figure 23 shows three mode 4 transfer functions for three progressively lower V_{SUP} levels. The supply headroom is configured for SUP_{HR} > 0% (positive supply headroom), and the calculated V_{TPO} value is falling (such that V_{TPO1} > V_{TPO2} > V_{TPO3}). The DRC rotation point and SLL threshold are constant in all three cases, and SLL_{THR} is selected such that as V_{TPO} falls the SLL knee (SLL_{RP}) is greater than the DRC_{RP}.

In the first two cases (for V_{TPO1} and V_{TPO2}), the calculated SLL output voltage limit (V_{SLL}) is less than V_{TPO}. As the signal level increases, it is first compressed (by the DRC function), and then limited once the output level reaches V_{SLL}. In the third case, V_{SLL} is greater than V_{TPO3} and the signal level (while still compressed by the DRC) reaches full-scale before exceeding V_{SLL}, and the SLL limiter function is never applied.

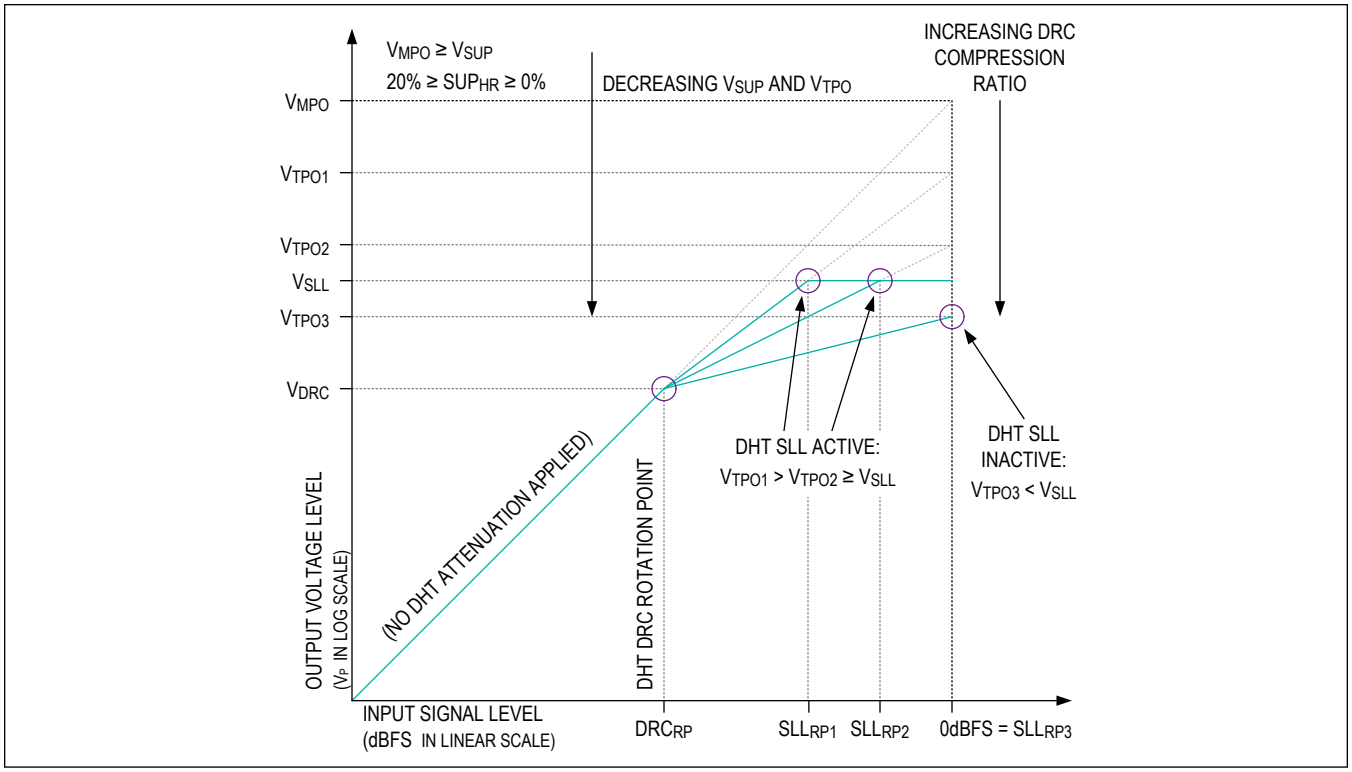


Figure 23. DHT DRC and SLL with Decreasing V_{SUP}(V_{TPO}), and SUP_{HR} ≥ 0%

Figure 24 shows a mode 4 transfer function where the supply headroom is negative (SUP_{HR} < 0%). As before, the SLL threshold (SLL_{THR}) is programmed so that the resulting SLL_{RP} is greater than the DRC_{RP}. This also insures that the resulting V_{SLL} is greater than V_{DRC} and less than V_{TPO}. As the audio signal level increases, it is first compressed (by the DRC function), and then limited once the digital output signal level reaches V_{SLL}. However, due to the negative headroom, the amplifier output clips before the SLL function digitally limits the signal level.

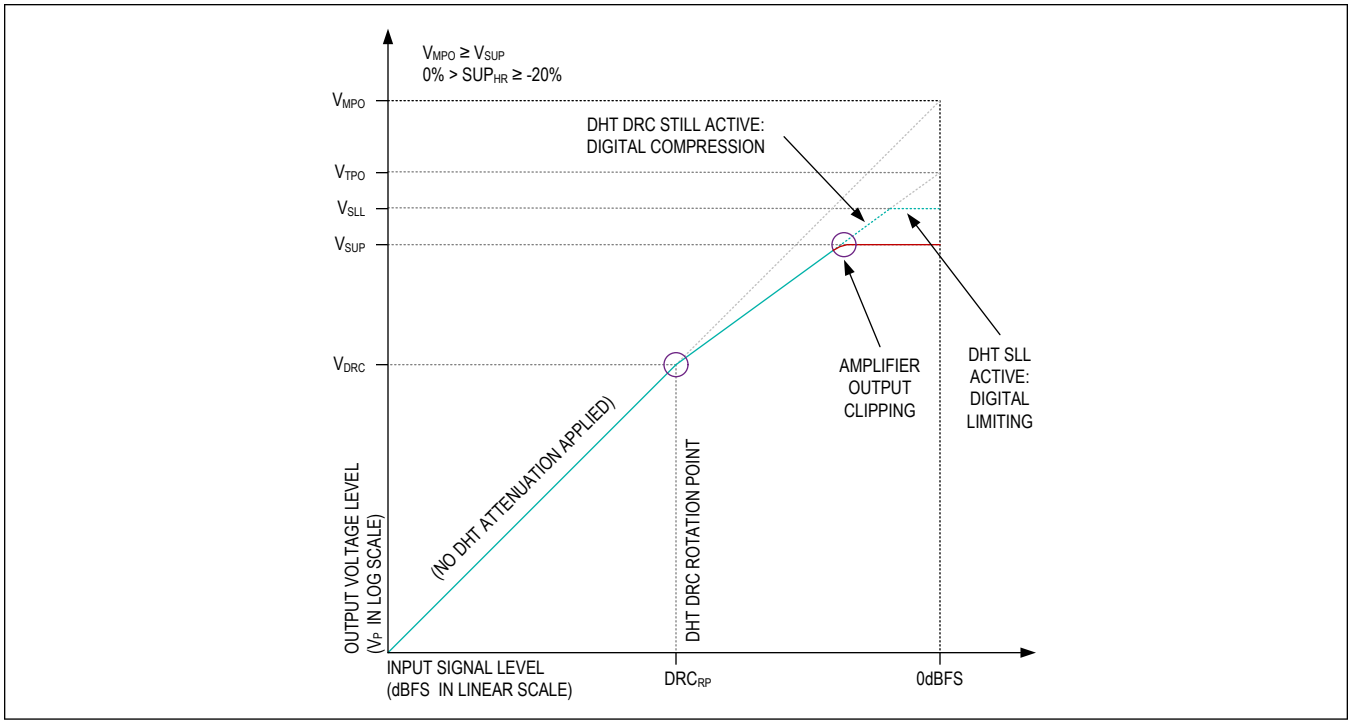


Figure 24. DHT DRC and SLL with Decreasing V_{SUP}(V_{TPO}), and SUP_{HR} < 0%

DHT Attenuation

When the DHT block first applies attenuation, an interrupt is generated (DHT_ACTIVE_BGN_*). When the DHT block fully releases all applied attenuation (i.e., DHT is inactive), an interrupt is generated (DHT_ACTIVE_END_*). Interrupts are not generated when DHT is actively adjusting the level of attenuation.

The maximum attenuation (A_{MAX}) applied to the audio signal by the DHT functions is selected with the *DHT_MAX_ATN* bit field. The maximum attenuation can be set from -1dB to -15dB with a 1dB step size. The configured DHT functions stop further attenuation of the audio signal once the calculated attenuation (relative to the unattenuated input signal level) reaches the selected maximum attenuation (A_{MAX}). If the calculated attenuation (based on input signal level and measured V_{SUP}) exceeds the selected maximum attenuation (A_{MAX}), the applied attenuation is set equal to (limited at) A_{MAX}. This can occur anytime the target peak output (V_{TPO}) to maximum peak output (V_{MPO}) ratio or peak output attenuation (denoted A_{TPO}) is less than (or has a larger absolute value than) A_{MAX}.

All previous examples show cases where the peak output attenuation (A_{TPO}) did not exceed the selected maximum attenuation (A_{MAX}). The following figures show signal distortion limiter use cases where V_{SUP} has decreased until A_{TPO} < A_{MAX} (the DHT DRC function DRC_{RP} is set to 0dbFS as in use case 1).

In Figure 25, the SUP_{HR} is set to -20%. Since A_{TPO} < A_{MAX}, the attenuation applied by the distortion limiter reaches the programmed maximum attenuation level before the input signal reaches full-scale. For input signals past the point where calculated attenuation is equal to A_{MAX}, the attenuation stops increasing and is now fixed at A_{MAX}. As a result, past this point the audio signal (in the digital domain) begins to increase. This results in the distortion increasing at the amplifier output (which was already clipping at the limited level of distortion).

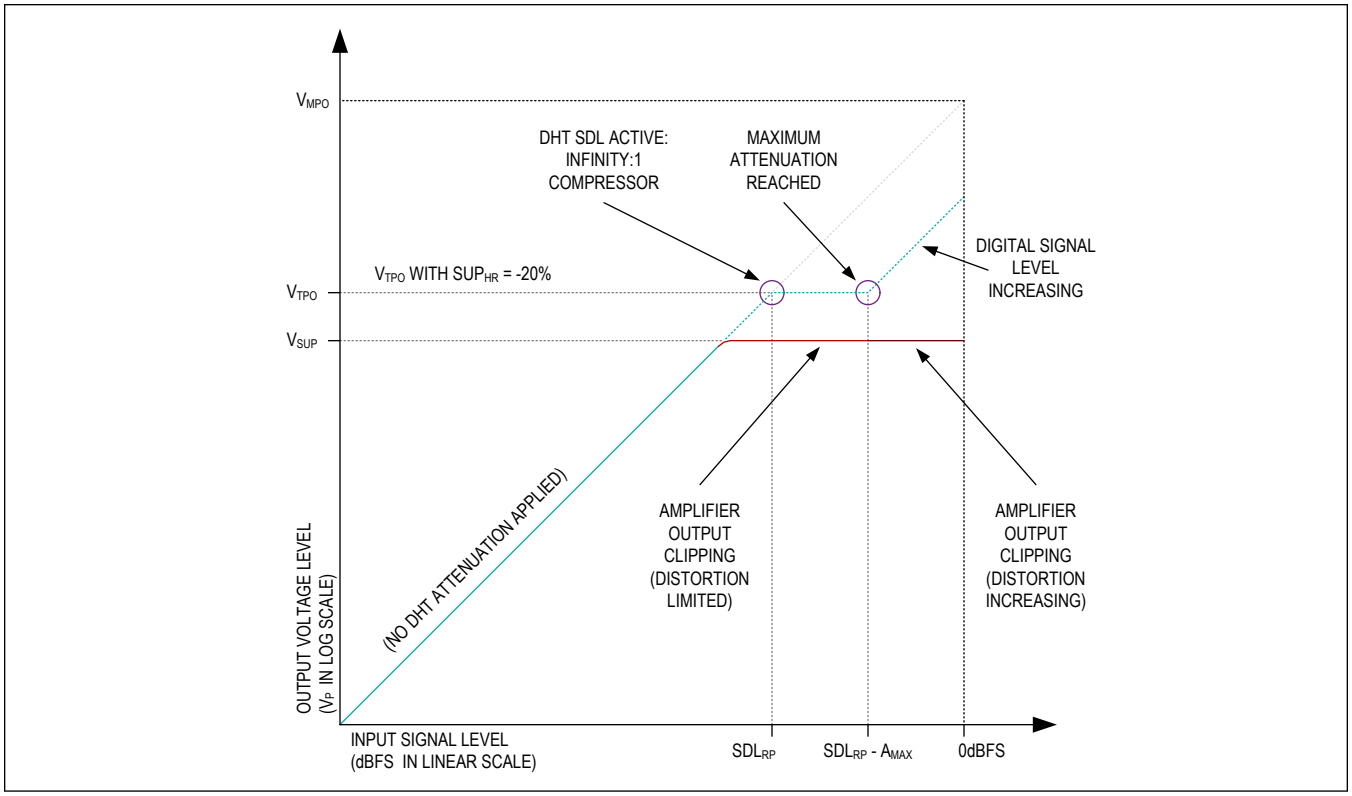


Figure 25. Distortion Limiter Case with -20% Headroom and A_{MAX} Exceeded

In Figure 26, the supply headroom is set to +20%. As before, the attenuation applied by the SDL reaches the selected maximum attenuation (A_{MAX}) before the input signal reaches full-scale. Past this point, the audio signal (in the digital domain) begins increasing and the signal level (and any distortion) at the amplifier output increases as well. In this case, the amplifier output was not clipping until after A_{MAX} was exceeded.

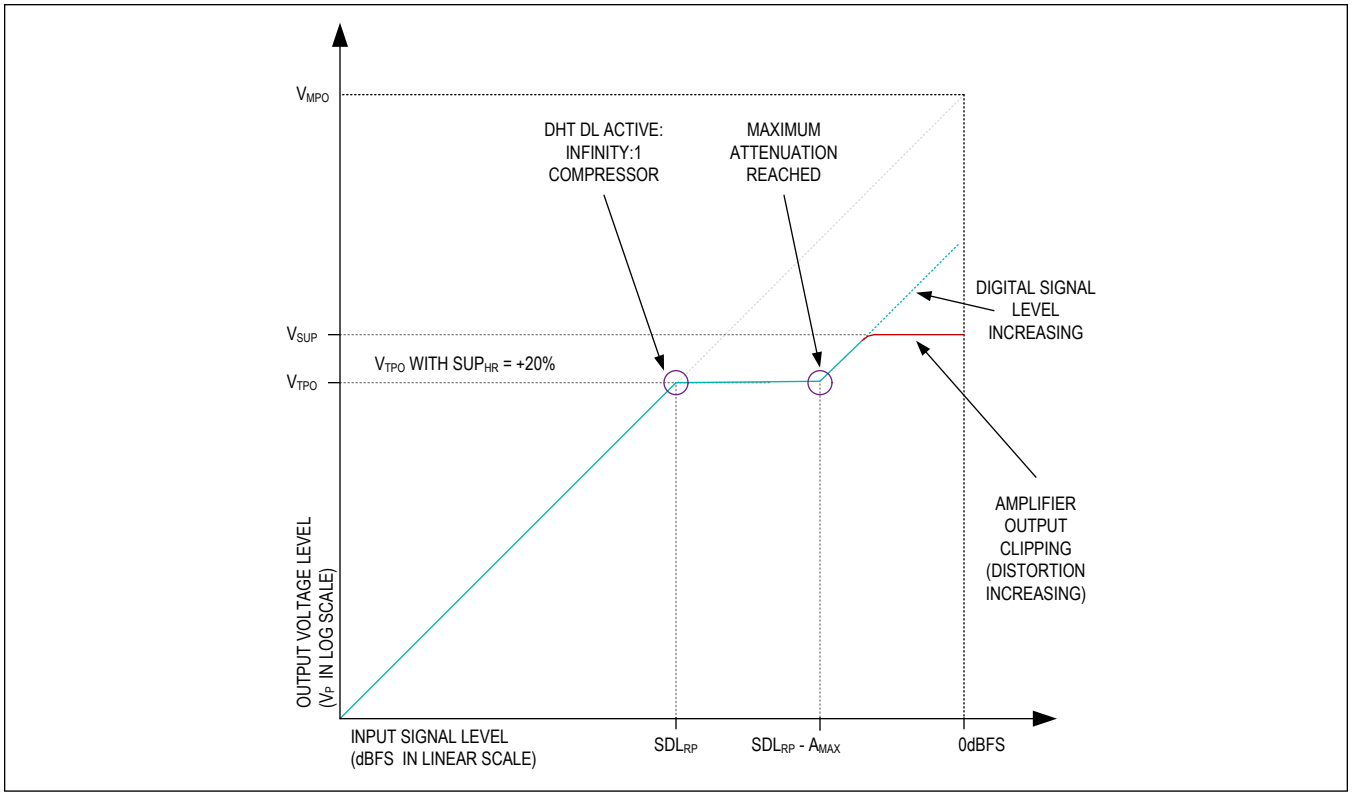


Figure 26. Distortion Limiter Case with +20% Headroom and A_{MAX} Exceeded

DHT Attenuation Reporting

In TDM mode, the current level of DHT attenuation is reported on the PCM data output (DOUT) when the DHT attenuation transmit enable bit is set high (*PCM_DHT_ATN_EN* = 1). The DHT attenuation level output is transmitted as a 14-bit unsigned binary attenuation level.

DOUT CURRENT DHT ATTENUATION (dB) = 20 x log(14-bit DOUT Value /16383)

If enabled, the DHT attenuation target (in dB) is also shared between devices on the inter chip communication (ICC) bus. In this case, the DHT attenuation level output is transmitted as a 10-bit unsigned binary attenuation level (DHT_ATN) followed by 6 bits of zero padding.

The current DHT attenuation (in dB) is calculated from the 10-bit value (DHT_ATN) with the following equation:

ICC CURRENT DHT ATTENUATION (dB) = - (DHT_ATN[9:0] x 0.015625dB)

The current DHT attenuation level cannot exceed the selected DHT maximum attenuation (A_{MAX}). Additionally, when the DHT is inactive, the reported attenuation is 0x0.

DHT Ballistics

When the signal level exceeds the rotation point or threshold for a configured DHT function (SDL, SLL, and/or DRC), or continues to increase beyond this point, the appropriate level of attenuation is applied to the signal level at the programmed attack rate. The DHT attack rate is selected with the *DHT_ATK_RATE* bit field.

The change in input signal level is detected by a peak detect circuit which has a fixed 3.5ms release time. When the signal level decreases or drops below the rotation point or threshold for a configured DHT function (SDL, SLL, and/or DRC), the appropriate level of applied attenuation is released. The DHT release rate is selected with the *DHT_RLS_RATE* bit field. However, due to the 3.5ms/dB peak detector, the 2ms/dB release rate is effectively 3.5ms/dB. All other release rates have a fixed delta of 3.5ms compared to the programmed release rate.

The attack-and-release behavior is a bit different when triggered by a change in active amplifier supply level. When the supply level decreases and triggers a DHT function attack, the attenuation is applied quickly at the configured attack rate. Likewise, as the supply level increases, the attenuation is released at the configured release rate. However, if DHT supply hysteresis is enabled (*DHT_SUPPLY_HYST_EN* = 1), then as the supply increases the applied DHT function does not release attenuation until the increase in the supply level exceeds the programmed DHT supply hysteresis level (*DHT_SUPPLY_HYST*). Once the supply increase exceeds the hysteresis, the appropriate level of applied attenuation is released at the configured release rate.

Speaker Amplifier

The device features a Class-DG speaker amplifier output stage. The speaker amplifier playback path is enabled and disabled using the *SPK_EN* bit. The *SPK_EN* bit is restricted on the *PCM_TX_EN* (i.e., the *SPK_EN* bit can only be changed after *PCM_TX_EN* bit is set to zero). The Class-DG multilevel amplifier generates a rail-to-rail output, pulse-width modulated (PWM) signal. By varying the PWM duty cycle the amplifier modulates the output with the audio input signal. Because the switching frequency of the amplifier is 472kHz (typical) when the output signal is filtered by the speaker, only the audio component remains. Rail-to-rail operation ensures that power dissipation at the output is dominated by the on resistance (R_{ON}) of the power output MOSFETs brief saturation current draw as the output switches, and the current draw necessary to charge the output stage gates.

In addition, the amplifier's output MOSFETs are segmented, and to save power they are automatically scaled based on the selected operating mode, input signal level, and configured gain structure.

Speaker Amplifier Operating Modes

The speaker amplifier can operate both in Class-DG and standard Class-D modes. In Class-DG mode, the amplifier output supply rail is switched between V_{PVDD} and V_{VBAT} based on the signal level. If Class-DG operation is disabled, the amplifier operates as a fixed supply Class-D amplifier and can be configured to use either V_{PVDD} or V_{VBAT} as the output supply rail. The speaker amplifier operating mode is selected with the *SPK_MODE* bit field.

Class-DG Mode Enabled

Class-DG is the default speaker amplifier mode of operation (*SPK_MODE* = 0x0). In this mode, the amplifier switches the supply rail between PVDD and VBAT as needed to efficiently supply the required output power.

Additionally, if V_{VBAT} drops below a programmed threshold level *VBATLOW_OK_LVL* bit field, the amplifier operates from PVDD supply rail regardless of signal level.

The Class-DG signal level threshold (VDG_THR) at which the amplifier switches between the supply rails is programmable. The method used to program the signal level threshold is selected with the *SPK_DG_SEL* bit field. When *SPK_DG_SEL* is set to 0x0, the threshold (VDG_THR) is set to a fixed peak voltage level with the *SPK_DG_THRES* bit field. When *SPK_DG_SEL* is set to 0x1 (default), the threshold (VDG_THR) is variable relative to the current VBAT voltage (measurement ADC result). The peak voltage headroom relative to V_{VBAT} is configured with the *SPK_DG_HEADROOM* bit field. Finally, if *SPK_DG_SEL* is set to 0x2, the threshold (VDG_THR) is set based on whichever setting (*SPK_DG_THRES* and *SPK_DG_HEADROOM*) results in the lowest threshold for the current V_{VBAT} voltage level. As a result, as V_{VBAT} decreases, VDG_THR can transition from a fixed threshold to a lower V_{VBAT} headroom based variable threshold.

The Class-DG mode hold time is configured with the *SPK_DG_HOLD_TIME* bit field. To save power, when the signal level drops below the threshold for longer than hold time, VBAT is selected as the active amplifier supply. The amplifier switches to the VBAT supply only at signal zero cross, so the measured hold time is the register configured hold time plus the time taken for a zero cross event to occur. When VBAT is the active amplifier output supply, the LV_EN output asserts high. When the signal level rises above the threshold, the amplifier supply quickly switches to PVDD to provide higher output voltage swing and to avoid clipping. When PVDD is the active amplifier output supply, the LV_EN output asserts low.

Delay for DG Mode

When the amplifier is operating in the automatic Class-DG mode, to avoid the potential for clipping the output signal as the PVDD supply rises, there is a programmable delay in the signal path controlled by *SPK_DG_DELAY*. This allows the PVDD supply time to increase the output voltage before it is required to output larger signals.

Class-DG Mode Disabled

When Class-DG mode is disabled, the speaker amplifier operates in standard Class-D mode. In this case, the active amplifier output supply is configured to either PVDD (*SPK_MODE* = 0x1) or VBAT (*SPK_MODE* = 0x2).

If the active amplifier output supply is configured to VBAT (*SPK_MODE* = 0x2), the amplifier operates from VBAT regardless of signal level. In this mode, the LV_EN pin is asserted high.

When the active amplifier supply is set to PVDD, the amplifier always operates from PVDD regardless of the signal and supply levels. Furthermore, to save power PVDD can be actively regulated between any levels within its standard operating range (3V to 14V). In this mode, the LV_EN pin is always asserted low.

Speaker Amplifier Ultra-Low EMI Filterless Operation

Traditional Class-D amplifiers require the use of external LC filters, or shielding, to meet electromagnetic-interference (EMI) regulation standards. However, the device features emissions limiting circuitry that limits the output switching harmonics that can directly contribute to EMI and radiated emissions.

The programmable speaker amplifier edge rate control bits are used to adjust the switching edge rate to help tune EMI performance. As the edge rate increases, the efficiency improves slightly. While as the edge rate is decreased, the efficiency drops slightly. The speaker amplifier edge rate is configured with the *SPK_SL_RATE_GMODE*, *SPK_SL_RATE_LS*, and *SPK_SL_RATE_HS* bit fields.

The speaker amplifier output also supports spread-spectrum modulation (SSM). SSM is enabled by default and it optimizes the suppression and control of the output switching harmonics that can contribute to EMI and radiated emissions. The modulation index in spread-spectrum mode is controlled by the *SPK_SSM_MOD_INDEX* bit field, and the maximum modulation index (MMI) varies accordingly. Higher percentage settings of the modulation index results in the switching frequency of the amplifier being modulated by a wider range, spreading out-of-band energy across a wider bandwidth. Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

Speaker Amplifier Overcurrent Protection

The device features amplifier current limit protection that protects the amplifier output from both high current and short circuit events. If the *OVC_AUTORESTART_EN* bit is set to 1 and the speaker amplifier output current exceeds the current limit threshold (4.5A min.), the device generates an interrupt and disables the amplifier output. After ~20ms, the amplifier output is re-enabled. If the overcurrent condition still exists, the device continues to disable and re-enable the amplifier output automatically until the fault condition is removed.

If the *OVC_AUTORESTART_EN* bit is set to 0, when a speaker amplifier overcurrent event occurs, the device still generates an interrupt and disables the amplifier output. However, in this case, the device is placed into software shutdown and the software enable (*EN*) bit is set to 0. As a result, the host must manually re-enable the device after an overcurrent event.

Speaker Current and Voltage Sense ADC Path

The device provides two separate 16-bit ADCs to monitor the speaker amplifier output current and voltage (the I/V sense ADC path). The current and voltage ADC paths are independently enabled with the *IVADC_I_EN* and *IVADC_V_EN* bits respectively. Voltage and current ADC data is output through the PCM interface data output (DOUT) which is enabled by the *PCM_TX_EN* bit field.

For accurate voltage measurements, the OUTPSNS and OUTNSNS pins should be Kelvin connected as close as possible to the load connected between OUTP and OUTN. If a filter is installed between the speaker amplifier output pins and the load, then the sense lines should be connected close to the load and after the filter. The speaker amplifier current is measured internally and requires no external connections.

The voltage and current digital data output is routed to the host through the PCM interface. Both the current and voltage sense ADC output data can optionally have dither applied (±1 LSB peak-to-peak) by setting the *IVADC_DITH_EN* bit field to 1. No dither is applied when *IVADC_DITH_EN* is set to 0.

The I/V sense ADC path provides separate optional DC blocking filters (first-order highpass) in the current and voltage sense paths. The current and voltage path filters are enabled by setting the *IVADC_I_DCBLK_EN* and *IVADC_V_DCBLK_EN* bit fields to 1 respectively.

To ensure phase alignment, the current and voltage sense ADCs should be enabled either with a single write to the *IVADC_I_EN* and *IVADC_V_EN* bits (*EN* = 1) or by setting both bits high before exiting software shutdown.

Measurement ADC

The device features a configurable 9-bit measurement ADC. The measurement ADC has three channels, one for die temperature measurement (measurement ADC thermal channel), one for for PVDD supply voltage measurement (measurement ADC PVDD channel), and one channel for VBAT supply voltage measurement (measurement ADC VBAT channel). Enabled channels are measured sequentially and continuously. The programmable measurement ADC sample rate can be set independently for the three channels. Each channel separately provides an optional programmable lowpass IIR filter.

Measurement ADC Thermal Channel

When the device is clocked, in the active state (EN = 1) the measurement ADC thermal channel automatically activates. When active, it continuously measures and reports the device die temperature over the range from -29°C to +150°C.

The output of the thermal ADC channel can be readback through the *MEAS_ADC_THERM_DATA* bit field, and is the input to both the thermal protection and thermal foldback blocks. By default (*MEAS_ADC_THERM_RD_MODE* = 0), the thermal readback value is automatically updated after each conversion is completed. Setting *MEAS_ADC_THERM_RD_MODE* to 1 places thermal readback into manual mode. In manual mode, the thermal readback result is updated manually when a 1 is written to the *MEAS_ADC_THERM_RD_UPD* bit field. The ADC thermal channel data read back in manual mode and the data streamed through the PCM interface is 9 bits. In the automatic mode, since the 9 bit data readback is from two registers, the LSB register isn't guaranteed to be synchronous with the MSB register and can result in higher noise in automatic mode.

The thermal ADC channel also provides an optional lowpass IIR filter with a programmable bandwidth that scales relative to the measurement ADC sample rate. The filter is enabled with the *MEAS_ADC_TEMP_FILT_EN* bit field and the bandwidth is set with the *MEAS_ADC_TEMP_FILT_COEFF* bit field.

Measurement ADC PVDD Channel

When the device is clocked and in the active state (EN = 1), the measurement ADC PVDD channel can be enabled. The PVDD channel is manually enabled by setting the *MEAS_ADC_PVDD_EN* bit to 1 and must be manually enabled for the DHT to operate. When the channel is enabled, it continuously measures and reports the PVDD supply voltage level over the range of 2.5V to 14.5V.

The output of the measurement ADC PVDD channel can be readback through the *MEAS_ADC_PVDD_DATA* bit field, and is routed to the DHT. By default (*MEAS_ADC_PVDD_RD_MODE* = 0), the PVDD readback value is automatically updated after each conversion is completed. Setting *MEAS_ADC_PVDD_RD_MODE* to 1 places PVDD readback into manual mode. In manual mode, the readback result is updated when a 1 is written to the *MEAS_ADC_PVDD_RD_UPD* bit field. The ADC PVDD channel data read back in manual mode and the data streamed through the PCM interface is 9 bits. In the automatic mode, since the 9 bit data readback is from two registers, the LSB register is not guaranteed to be synchronous with the MSB register and can result in higher noise in automatic mode.

The lowest measured PVDD measurement result is readback through the *LOWEST_PVDD_DATA_MSB* and *LOWEST_PVDD_DATA_LSB* bit fields. These bit fields both automatically clear and are reset to the value of the current measurement result immediately after LSB readback is completed.

The PVDD channel also provides an optional lowpass IIR filter with a programmable bandwidth that scales relative to the measurement ADC sample rate. The filter is enabled with the MEAS_ADC_PVDD_FILT_EN bit and the bandwidth is set with the MEAS_ADC_PVDD_FILT_COEFF bit field.

Measurement ADC VBAT Channel

When the device is clocked, in the active state (EN = 1), the measurement ADC VBAT channel can be enabled. The VBAT channel is manually enabled by setting the MEAS_ADC_VBAT_EN bit to 1 and must be manually enabled for the DHT to operate. When the channel is enabled, it continuously measures and reports the VBAT supply voltage level over the range of 2.5V to 5.5V.

The output of the measurement ADC VBAT channel can be readback through the MEAS_ADC_VBAT_DATA bit field. By default (MEAS_ADC_VBAT_RD_MODE = 0), the VBAT readback value is automatically updated after each conversion is completed. Setting MEAS_ADC_VBAT_RD_MODE to 1 places VBAT readback into manual mode. In manual mode, the readback result is updated when a 1 is written to the MEAS_ADC_VBAT_RD_UPD bit field. The ADC VBAT channel data read back in manual mode and the data streamed via the PCM interface is 9 bits. In the automatic mode, since the 9 bit data readback is from two registers, the LSB register isn't guaranteed to be synchronous with the MSB register and can result in higher noise in automatic mode.

The lowest measured VBAT measurement result is readback through the LOWEST_VBAT_DATA_MSB and LOWEST_VBAT_DATA_LSB bit fields. These bit fields both automatically clear and are reset to the value of the current measurement result immediately after LSB readback is completed.

The VBAT channel also provides an optional lowpass IIR filter with a programmable bandwidth that scales relative to the measurement ADC sample rate. The filter is enabled with the MEAS_ADC_VBAT_FILT_EN bit and the bandwidth is set with the MEAS_ADC_VBAT_FILT_COEFF bit field.

Clock and Data Monitors

The device provides input data and external clock monitors that detect host and system level faults. The data monitor detects persistent stuck and high amplitude input signals, while the clock monitor detects external clock failures and invalid clock configurations. Upon fault detection, these monitors automatically place the device into software shutdown to stop glitches and unwanted signals at the amplifier output and speaker load.

Input Data Monitor

The device provides an optional input data monitor that is enabled by setting DMON_MAG_EN to 1 for the data magnitude monitor or DMON_STUCK_EN to 1 for the data stuck monitor. Once the data monitor is enabled, it actively monitors the selected input data (from DIN) to the speaker amplifier path anytime the device exits software shutdown (EN = 1) and the amplifier is enabled (SPK_EN = 1). When the tone generator is enabled, the data monitor is automatically disabled.

When active, the block monitors the selected input data for the enabled data error types (data magnitude, data stuck, or both). The DMON_DURATION bit field selects the duration that a data stuck or magnitude error must persist for before a data error is detected. Once a data error is detected, the data monitor automatically places the device into software shutdown (sets EN to 0) and generates a data monitor error interrupt (DMON_ERR_*).

A data stuck error is detected if the input signal repeats a fixed value with a magnitude (positive or negative) that is beyond the data stuck threshold (DMON_STUCK_THRES) for longer than the data error duration (set by DMON_DURATION). If the input signal repeats a fixed value for any duration with a magnitude that is within the data stuck threshold limits (such as a zero or near zero code), no data stuck error is detected.

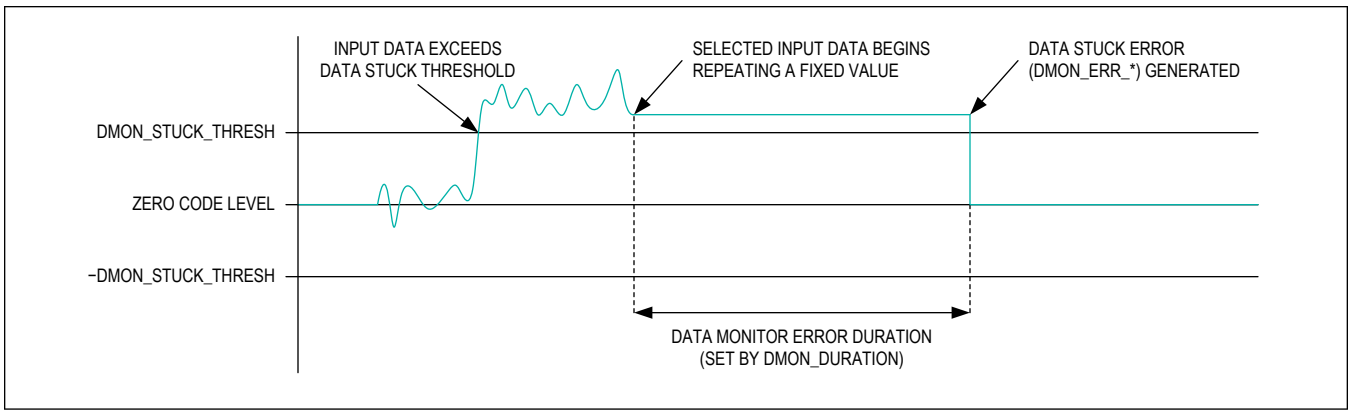


Figure 27. Data Monitor Error Generation due to Input Data Stuck Error Detection

A data magnitude error is detected if the input signal magnitude (positive or negative) is beyond the data magnitude threshold (set by *DMON_MAG_THRES*) for longer than the data error duration (set by *DMON_DURATION*).

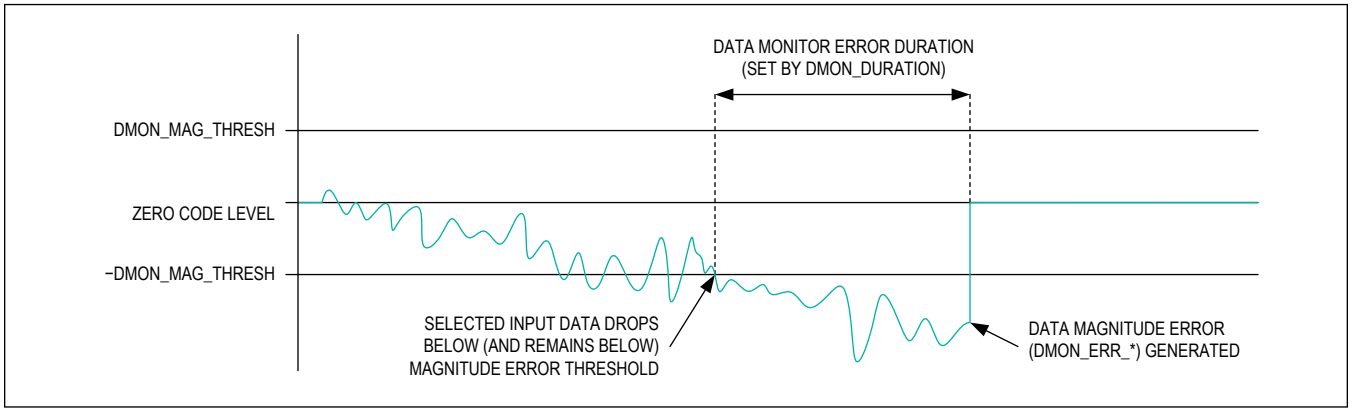


Figure 28. Monitor Error Generation due to Input Data Magnitude Error Detection

Clock Monitor

The device provides an optional clock monitor that is enabled by setting *CMON_EN* to 1. Once enabled, it actively monitors the input BCLK and LRCLK anytime the device exits software shutdown (*EN* = 1). When the tone generator is enabled, the clock monitor is automatically disabled. When active, the clock monitor detects clock activity, clock frequency, and frame timing (clock ratio). If faults are detected, the clock monitor automatically places the device into software shutdown and generates a clock error interrupt (*CLK_ERR_**).

The clock monitor operates in automatic mode when *CMON_AUTORESTART_EN* = 1, and manual mode when *CMON_AUTORESTART_EN* = 0. In automatic mode, when a clock error places the device into software shutdown, the global enable bit (*EN*) is not changed (remains 1), and the device automatically recovers from all clock errors. In automatic mode, both clock error (*CLK_ERR_**) and clock recovery (*CLK_RECOVER_**) interrupts are generated in pairs (a clock recovery interrupt is not possible until after a clock error has occurred).

In manual mode, when a clock error places the device into software shutdown, the global enable bit (*EN*) is set to 0. Clock recovery (*CLK_RECOVER_**) interrupts are never generated in manual mode, and the device remains in software shutdown until the host sets *EN* back to 1. Once the device is re-enabled (*EN* set to 1), the clock monitor is active and detects any new (or persisting) clock errors. If a clock error is detected, the device returns to software shutdown (*EN* = 0), and a new clock error interrupt (*CLK_ERR_**) is generated.

Clock errors are fault conditions, and audible glitches can occur on clock monitor based transitions into and out of software shutdown. When the clock monitor is enabled, no false clock error or clock recovery interrupts are generated when the host software transitions the device normally into and out of software shutdown.

Clock Activity and Frequency Detection

When the clock monitor is enabled, the bit clock (BCLK) and frame clock (LRCLK) frequencies are monitored. The expected LRCLK frequency is equal to the PCM sample rate (*PCM_SR*). The expected BCLK frequency is based on the BCLK to LRCLK ratio (*PCM_BSEL*) relative to the PCM sample rate (*PCM_SR*).

The current frequency of each clock is measured relative to (and once per interval of) the programmed frame period (as set by *PCM_SR*). A clock frequency error is detected when the measured clock frequencies differ from programmed clock frequencies (faster or slower) by more than the frequency error threshold (*45% typical)*. If either clock stops high or low, the frequency measurement result allows detection of the clock stop event.

The *CMON_ERRTOL* bit field sets the clock frequency error tolerance. The tolerance is the required number of consecutive frame clock periods (*PCM_SR*) with an incorrect clock frequency before a clock error is generated. If the error persists for the selected number of frame periods, a clock error interrupt (*CLK_ERR_**) is generated, and the device is placed into software shutdown.

In automatic mode, the *CMON_ERRTOL* bit field also sets the number of consecutive frame clock periods with no clock frequency errors (LRCLK or BCLK) that are required for automatic restart to occur. Once the selected number of consecutive error free frames are detected, a clock recovery interrupt (*CLK_RECOVER_**) is generated and the device automatically exits software shutdown.

In manual mode, no clock recovery interrupts are generated. The clock monitor remains disabled and the device remains in software shutdown until the host software sets *EN* back to 1.

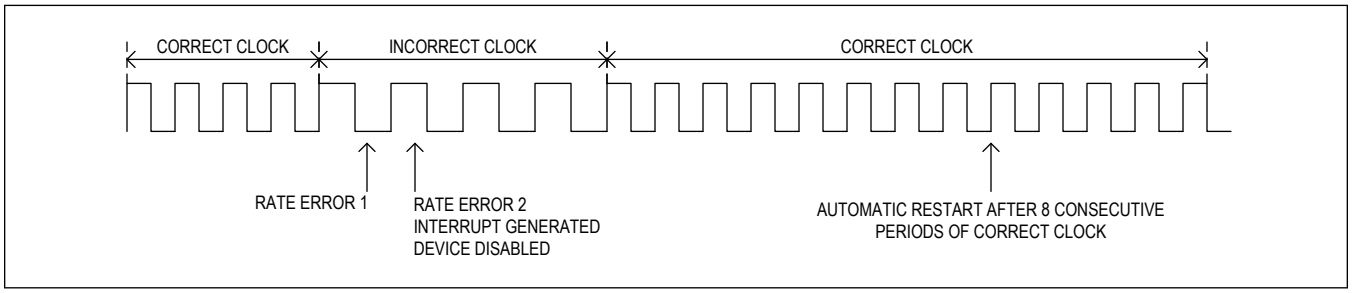


Figure 29. Clock Monitor LRCLK Rate Error Example with CMON_ERRTOL = 0x1

Clock Frame Error Detection

When the clock monitor is enabled, the bit clock (BCLK) to frame clock (LRCLK) ratio is monitored. The clock monitor counts the number of BCLK periods per frame (LRCLK period), and then compares the count to the configured clock ratio (*PCM_BSEL*). In addition, in I^2S and left-justified (LJ) modes, the clock monitor verifies the LRCLK duty cycle by checking that the number of BCLK periods per channel is equal. In TDM mode, data transport is synchronized to the active frame clock (LRCLK) edge, so no duty cycle restrictions are enforced.

A frame error is detected in each frame where the monitored clock ratio (and duty cycle in I^2S and LJ modes) differs from the configured settings. The *CMON_BSELTOL* bit field sets the number of consecutive frames with frame errors that are required before a clock error interrupt is generated (*CLK_ERR_**) and the device is placed into software shutdown.

In automatic mode, the *CMON_BSELTOL* bit field also sets the number of consecutive frames with no frame errors that are required for automatic restart to occur. Once the selected number of consecutive error free frames are detected, a clock recover interrupt (*CLK_RECOVER_**) is generated and the device automatically exits software shutdown.

In manual mode, no clock recovery interrupts are generated. The clock monitor remains disabled and the device remains in software shutdown until the host software sets *EN* back to 1.

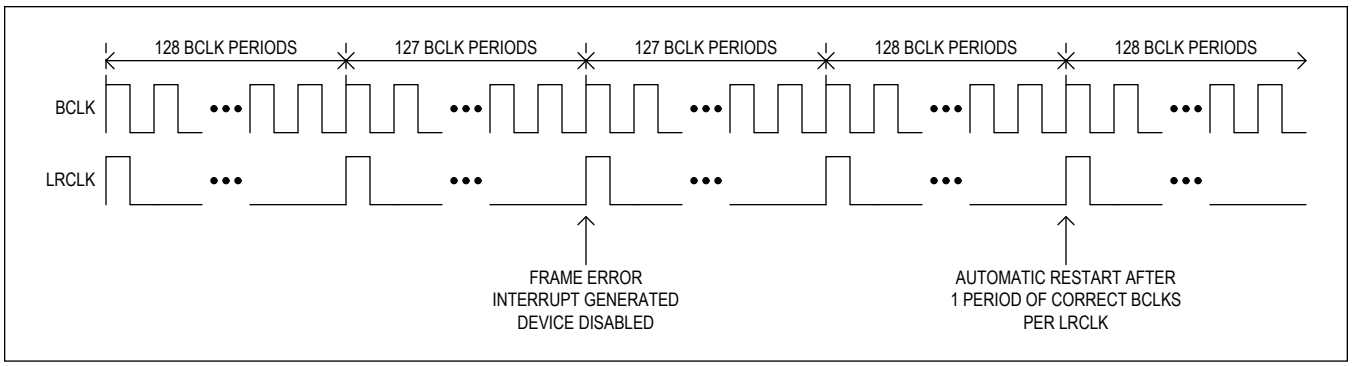


Figure 30. Clock Monitor Framing Error Example in TDM Mode with PCM_BSEL = 0x6 and CMON_BSELTOL = 0x0

Thermal Protection

When the device is active, the measurement ADC thermal channel is automatically enabled and monitors die temperature to ensure that it does not exceed the configured thermal thresholds. Interrupt registers are provided so that the device can notify the host when the die temperature crosses the thermal-warning threshold, the thermal-shutdown threshold, or when thermal foldback starts and stops.

Thermal Warning and Thermal Shutdown Configuration

The thermal-warning threshold is configured by the *THERMWARN_THRESH[5:0]* bit field and the thermal-shutdown threshold is configured by the *THERMSHDN_THRESH*[5:0] bit field. When die temperature is decreasing, hysteresis is applied to both thresholds. The temperature hysteresis is configured by the *THERM_HYST* bit field.

Thermal Shutdown Recovery Configuration

The device thermal-shutdown-recovery behavior is determined by the state of *THERM_AUTORESTART_EN* bit. When the *THERM_AUTORESTART_EN* bit is set to 0, the thermal-shutdown recovery is in manual mode. In manual mode, when the die temperature exceeds the thermal-shutdown threshold, an interrupt is generated and the amplifier output is automatically disabled. Once the die temperature drops below the thermal-shutdown minus the hysteresis, and warning thresholds minus the hysteresis, the appropriate interrupts are generated to notify the host. In addition, once the die temperature drops below the thermal-warning threshold minus the hysteresis, the device is placed into software shutdown (*EN* is set to 0) and remains in that state until the host manually re-enables the device.

When the *THERM_AUTORESTART_EN* bit is set to 1, the thermal-shutdown recovery is in automatic mode. In automatic mode, when the die temperature exceeds the thermal-shutdown threshold, an interrupt is generated and the amplifier is automatically disabled. Once the die temperature drops below the thermal-shutdown threshold minus the hysteresis, an interrupt is generated but the amplifier remains disabled. When the temperature drops below the thermal-warning threshold minus the hysteresis, another interrupt is generated and (unlike manual mode) the amplifier is then automatically re-enabled.

Thermal Foldback

The device features thermal foldback to allow for a smoother audio response to high temperature events. Thermal foldback is enabled by setting the *THERMFB_EN* bit to 1. Once enabled, when the die temperature exceeds the configured thermal-warning threshold (+120°C by default), an interrupt is generated (*THERMFB_BGN_**) and attenuation is applied to the speaker amplifier path. As the die temperature increases, the level of attenuation also increases proportionally up to a maximum level of -12dB (unless the thermal-shutdown threshold is exceeded first). Likewise, as die temperature decreases (including hysteresis and hold time), the applied attenuation also proportionally decreases. The slope of the thermal-foldback attenuation is programmed with the *THERMFB_SLOPE* bit field.

When thermal foldback is active, the attack time for a gain change can be a maximum of 2 samples. Additionally, there is up to a 7 sample delay in the signal path attenuation due to the group delay of the amplifier. The attenuation release rate (for decreasing temperature) is programmable and is configured with the *THERMFB_RLS* bit field. When the die

temperature starts to decrease and drops below the maximum temperature minus the programmed hysteresis level, the attenuation starts to release after the programmed hold time (set with the THERMFB_HOLD bit field, thermal foldback settings) and then the interrupt (THERMFB_END_*) is generated.

Tone Generator

The device includes a tone generator, which when enabled (using the TONE_EN bit field), replaces the PCM interface as the input source to the speaker playback path. When the tone generator is enabled, both it and the speaker playback path operates without the need for any external clocks.

The tone generator output is configured to generate sine wave or DC tones (using the TONE_CONFIG bit field).

The tone generator can create sine waves with either a 1kHz fixed frequency or a variable sample rate dependent frequency. When a sample rate based sinewave output is selected, the tone generator output frequency is set by the playback sample rate setting (PCM_SR) divided by the selected ratio (as set by TONE_CONFIG). For the playback sample rate of 44.1kHz and its multiples, the tone generator output frequency can vary by up to 9%. The tone generator supports all available sample rate settings (PCM_SR). The amplitude of the output sine wave relative to full-scale is selected with the TONE_AMPLITUDE bit field

The tone generator can output either a fixed or a programmable DC output level (as set by TONE_CONFIG). Fixed DC output levels of zero code, positive half-scale, and negative half-scale are provided for quick configuration. If the programmable DC output level is selected (TONE_CONFIG), the DC level is configured as a signed two's complement value with the TONE_DC bit field.

Interchip Communication

The device features an interchip communication (ICC) interface that uses a shared data bus to facilitate synchronized speaker amplifier path attenuation adjustments across groups of devices. Depending on the configuration, the ICC interface can synchronize DHT attenuation, thermal foldback, or both. Each device in a given group transmits one channel of data, and receives the data channels of all grouped devices. Grouped devices then apply (assuming both are enabled) the overall lowest DHT attenuation target and the highest measured temperature (for thermal foldback) reported by any device in the group.

ICC Operation and Data Format

The bidirectional ICC bus is used to synchronize the responses of grouped devices. To create the ICC bus, the ICC interface pins of each device are externally connected together (whether or not the devices are in the same group). The ICC bus operates with the same clock sources and data format configuration as the PCM interface data input (DIN), and can support a maximum of 16 channels. For a given valid PCM interface configuration, the number of available ICC data channels per frame is calculated as follows (based on the PCM_CHANSZ, PCM_BSEL, and PCM_FORMAT settings):

Number of Available Data Input Channels = BCLK to LRCLK Ratio/Channel Length

The ICC interface is disabled when both the ICC data transmit output (ICC_TX_EN) and the ICC data link (ICC_LINK_EN) is disabled. To enable the ICC interface, both ICC_TX_EN and ICC_LINK_EN must be set to 1. It is illegal to set these controls to different values, and both must always be set to the same state (either enabled or disabled). Once the ICC link and data transmit is enabled, the ICC data output channel is assigned with the ICC_TX_DEST bit field. The ICC pin is Hi-Z during all other data channels, and can be configured (with the ICC_RX_CHn_EN bits) to accept data from the output data channels of grouped devices.

The transmitted ICC data is always the same size as the configured PCM data input word size (as set by PCM_CHANSZ). When a 16-bit data word is selected, the ICC data word is not long enough to synchronize both DHT and thermal foldback. In this case, the ICC_DATA_SEL bit is used to choose whether the DHT function or thermal foldback function is synchronized. When a 24- or 32-bit data word size is selected, ICC can synchronize both DHT and thermal foldback across a given group. In these cases, the ICC_DATA_SEL bit has no effect. Active ICC data channels always contain ICC data words followed by zero padding bit up to the ICC data channel length (which is equal to PCM input data channel length). If DHT or thermal foldback is disabled for any given group, then the transmitted ICC data for the disabled function(s) is always zero code.

Multiamplifier Grouping

The ICC interface allows multiple devices to be grouped so that DHT, thermal foldback, or both can be synchronized. The receive channel enables (*ICC_RX_CHn_EN*) are used to define groups. A given device monitors all selected channels (when *ICC_RX_CHn_EN* = 1, and n denotes the channel number) on the ICC data bus. The configured set of receive channels must also include the assigned transmit channel (as set by *ICC_TX_DEST*) for any given device. Each device in a given group must have identical settings for all ICC receive channel enables (*ICC_RX_CHn_EN*). Furthermore, all devices in the same group must have identical DHT, thermal protection, and thermal foldback settings to achieve a synchronized response across the group. The behavior of a group as a whole is undefined if any given device in a group has different settings.

The ICC bus can support a maximum of 16 data channels. The minimum size of a group is two devices, and as a result, the maximum number of concurrent groups on a single ICC bus is eight. A group can contain as many as 16 devices, but then only a single group is possible on a single ICC bus.

ICC Multi-Group Example

Consider a system design that includes four devices that require DHT synchronization, and that two distinct groups of two devices each (with different DHT settings) must share a single ICC bus. The PCM interface (and thus ICC bus) is configured in TDM mode 1 with four 16-bit data channels available. One possible configuration (among many) is to assign devices 1 and 3 to the first group (denoted group A), and to assign devices 2 and 4 to a second group (denoted group B).

To configure group A, both devices 1 and 3 are set to monitor channels 0 and 2 by programming *ICC_RX_CH0_EN* = 1 and *ICC_RX_CH2_EN* = 1 on both devices (all other ICC receive bit fields are 0). Device 1 transmits on channel 0 (*ICC_TX_DEST* = 0x0) and device 3 transmits on channel 2 (*ICC_TX_DEST* = 0x2).

To configure group B, both devices 2 and 4 are set to monitor channels 1 and 3 by programming *ICC_RX_CH1_EN* = 1 and *ICC_RX_CH3_EN* = 1 on both devices (all other ICC receive bit fields are 0). Device 2 transmits on channel 1 (*ICC_TX_DEST* = 0x1) and device 4 transmits on channel 3 (*ICC_TX_DEST* = 0x3).

Since the ICC channel length and data word size is limited to 16-bits, the *ICC_DATA_SEL* bit field in all 4 devices must be set to 0 to select DHT target attenuation synchronization. Finally, on all 4 devices, set *ICC_LINK_EN* = 1 and *ICC_TX_EN* = 1 to enable the ICC interfaces.

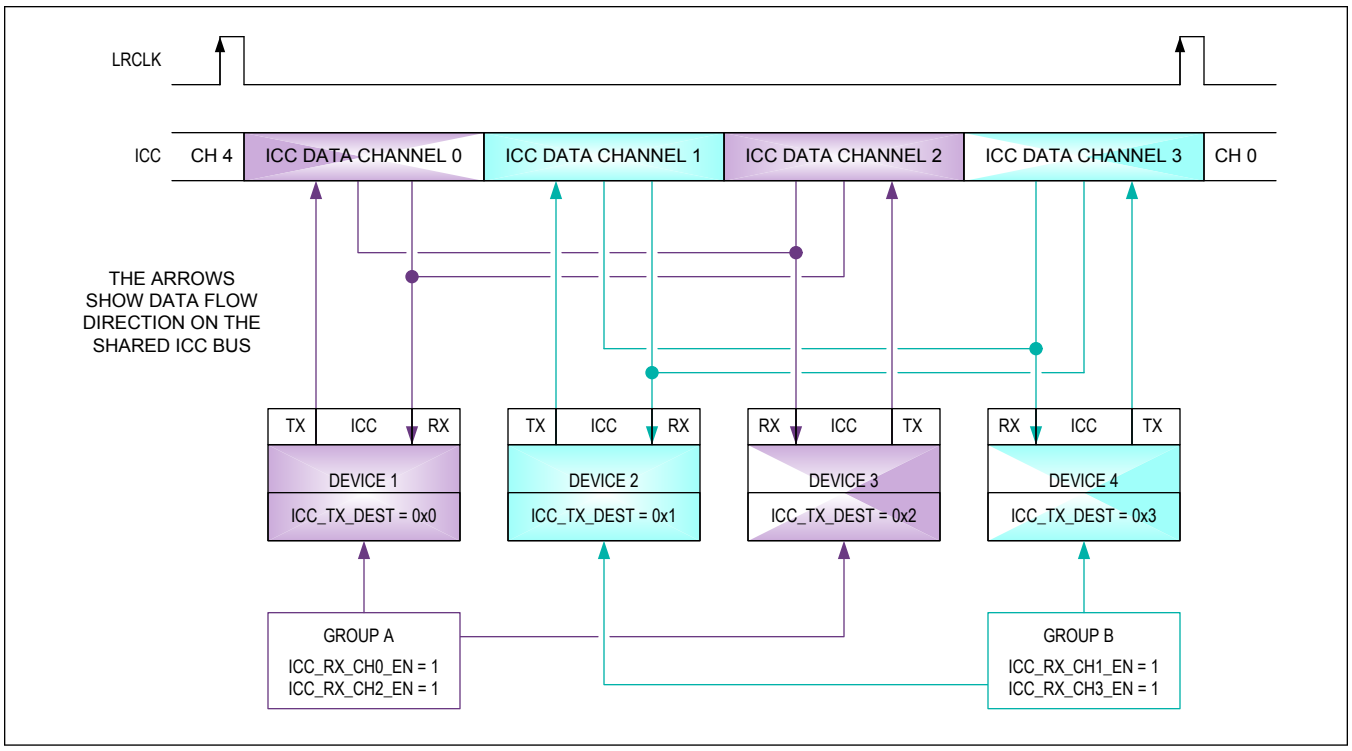


Figure 31. ICC Multi-Group Example with 2 Groups and 4 Total Devices

ICC Timing

Figure 32 shows timing for BCLK and ICC. See the *Electrical Characteristics* table for more details.

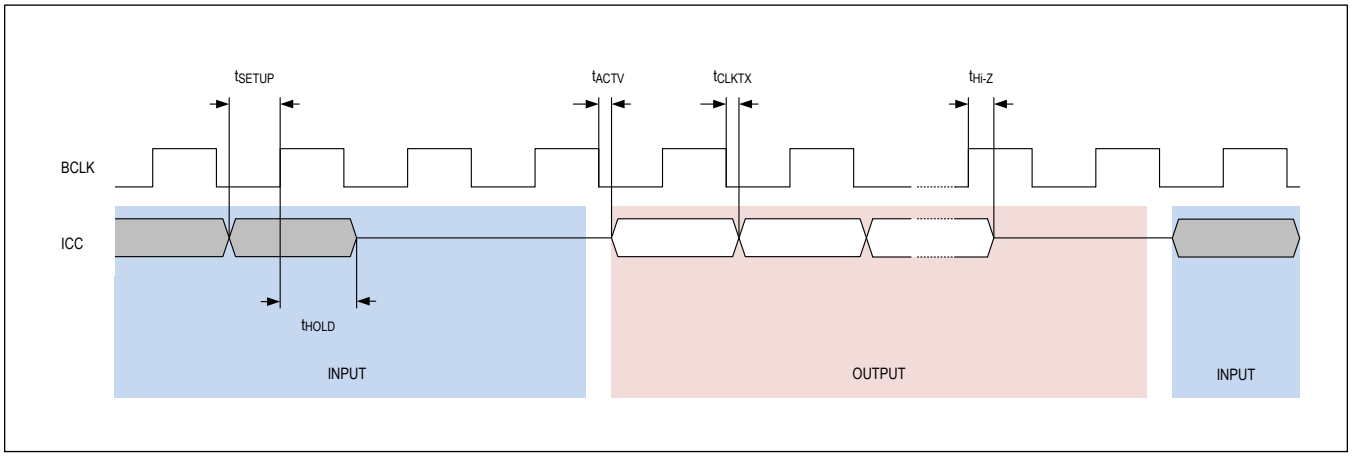


Figure 32. PCM Interface Timing/Interchip Communication—ICC Timing Diagram

I²C Serial Interface

The I²C serial control interface is activated when the device detects a valid I²C start condition at the I2C1 and I2C2 pins. The I2C1 and I2C2 pins can each act as either SCL or SDA respectively, and the start condition configures the device address and state of each pin. After the first I²C transaction, the I²C interface configuration should remain fixed.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. The seven most significant bits are programmable through the ADDR connection, and the required I2C1 and I2C2 connections for each address are shown. The device does not communicate if ADDR is unconnected. Setting the read/write bit to 1 configures the device for read mode. Setting the read/write bit to 0 configures the device for write mode. The address is the first byte of information sent to the IC after the START condition.

Table 9. I²C Slave Address

I2C1	I2C2	ADDR CONNECTION	I²C SLAVE ADDRESS (BINARY)	I²C WRITE ADDRESS (BINARY)	I²C READ ADDRESS (BINARY)
SDA	SCL	Connected to DVDDIO	0111000x	01110000	01110001
SDA	SCL	Connected to GND	0111001x	01110010	01110011
SDA	SCL	Connected to SDA	0111010x	01110100	01110101
SDA	SCL	Connected to SCL	0111011x	01110110	01110111
SCL	SDA	Connected to DVDDIO	0111100x	01111000	01111001
SCL	SDA	Connected to GND	0111101x	01111010	01111011
SCL	SDA	Connected to SDA	0111110x	01111100	01111101
SCL	SDA	Connected to SCL	0111111x	01111110	01111111

The IC features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 1MHz.

Figure 33 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the IC by transmitting the proper slave address followed by two register address bytes (most significant byte first) and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL pulses. The IC transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

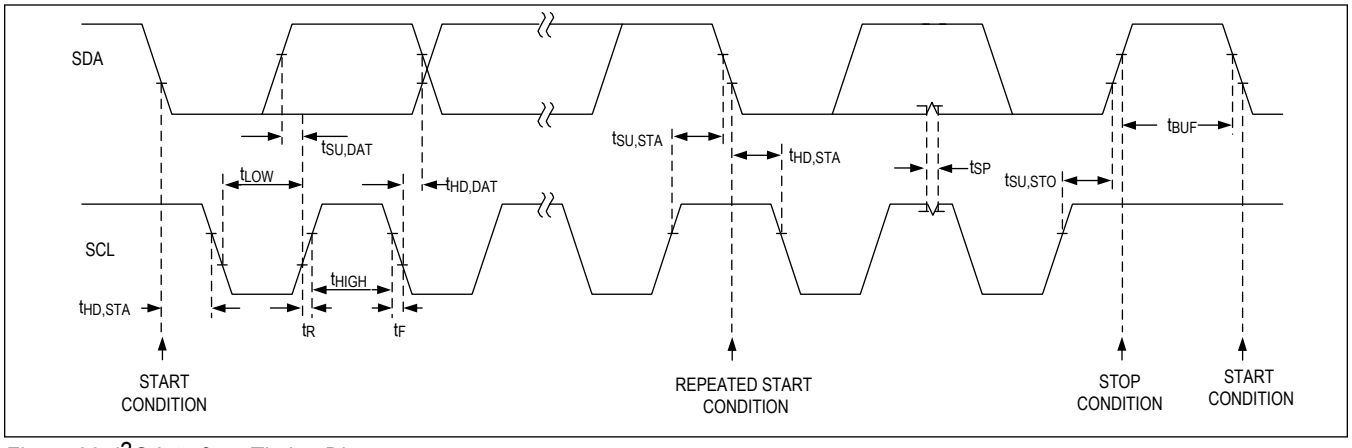


Figure 33. I²C Interface Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

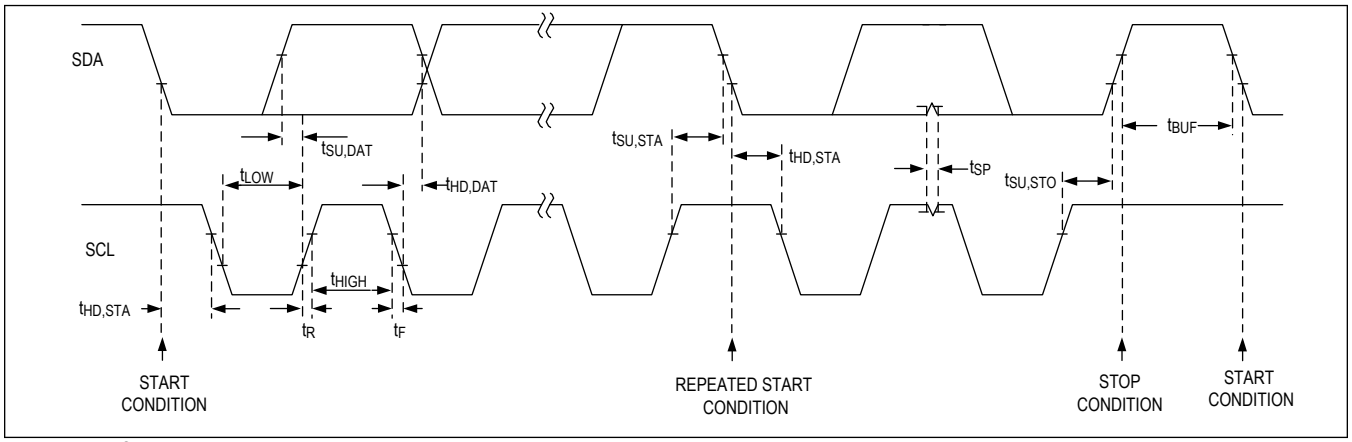


Figure 34. I²C START, STOP, and REPEATED START Conditions

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the IC uses to handshake receipt of each byte of data when in write mode. The IC pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

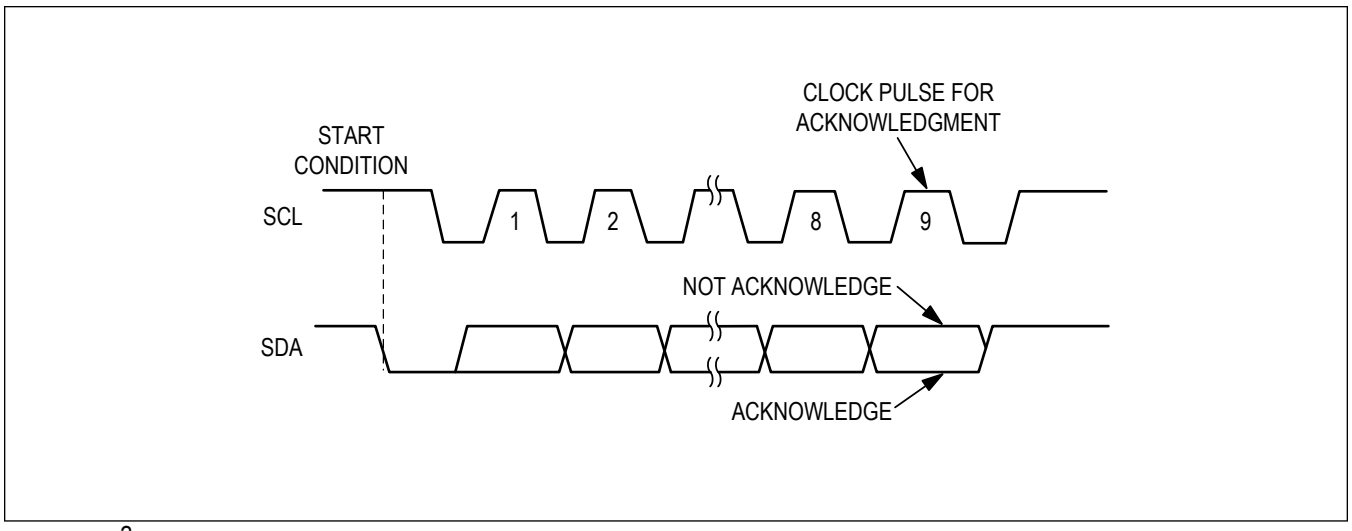


Figure 35. I²C Acknowledge

Write Data Format

A write to the IC includes transmission of a START condition, the slave address with the R/W bit set to 0, two bytes of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second and third bytes transmitted from the master configure the ICs internal register address pointer. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

The third byte sent to the IC contains the data that is written to the chosen register. An acknowledge pulse from the IC signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

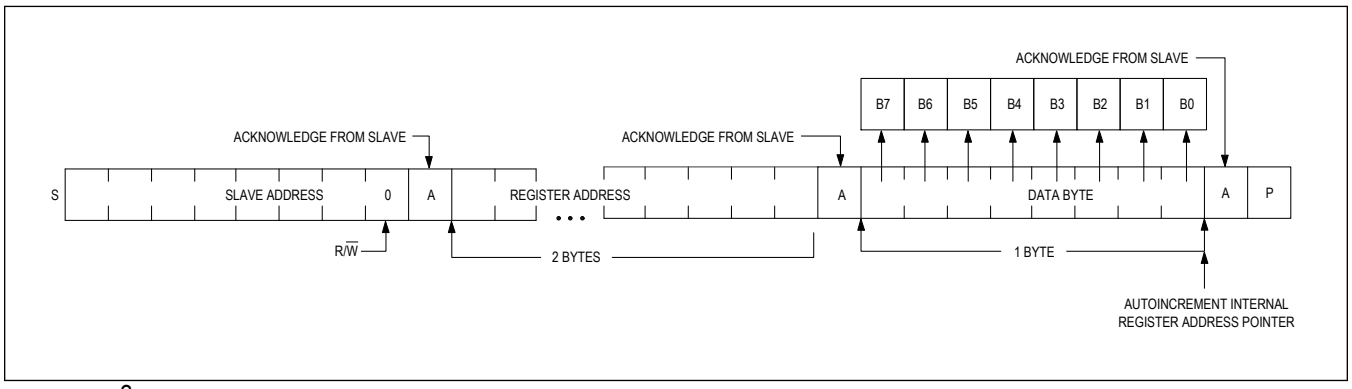


Figure 36. I²C Writing One Byte of Data to the Slave

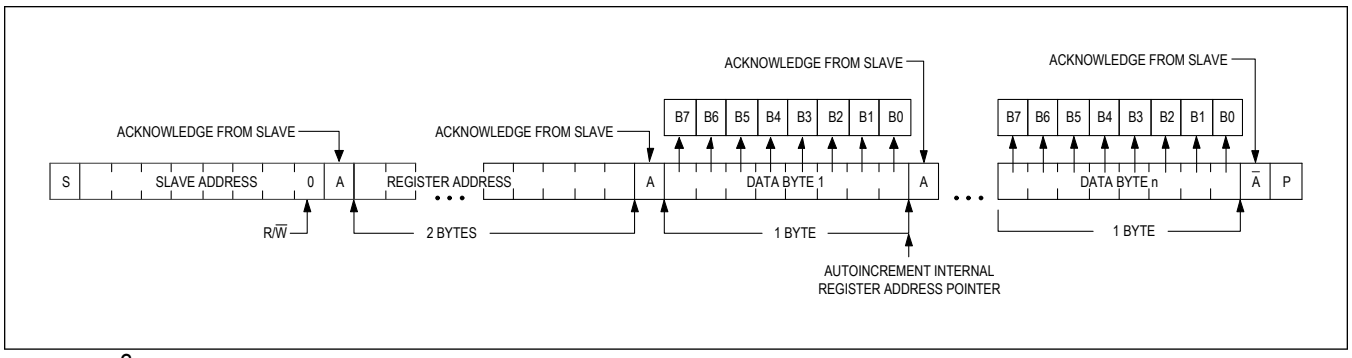


Figure 37. I²C Writing n-Bytes of Data to the Slave

Read Data Format

Sending the slave address with the R/W bit set to 1 to initiate a read operation. The IC acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x2000.

The first byte transmitted from the IC is the content of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the ICs slave address with the R/W bit set to 0 followed by the two byte register address. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The IC then transmits the contents of the specified register. The address pointer auto-increments after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition.

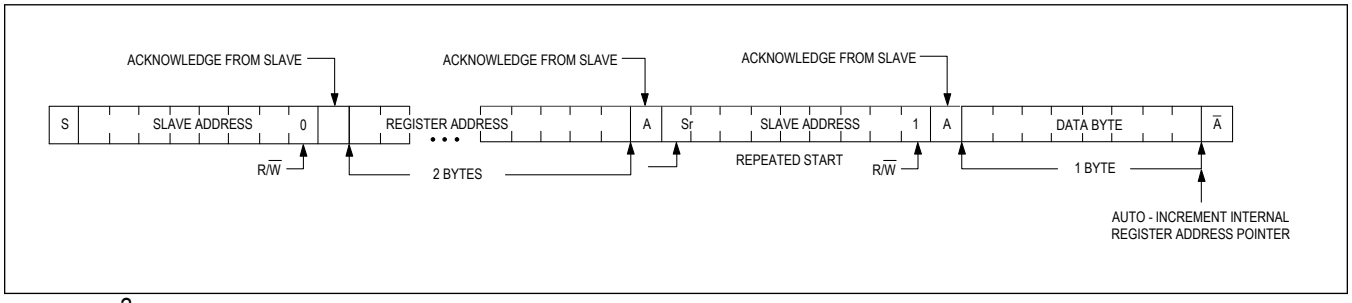


Figure 38. I²C Reading One Byte of Data from the Slave

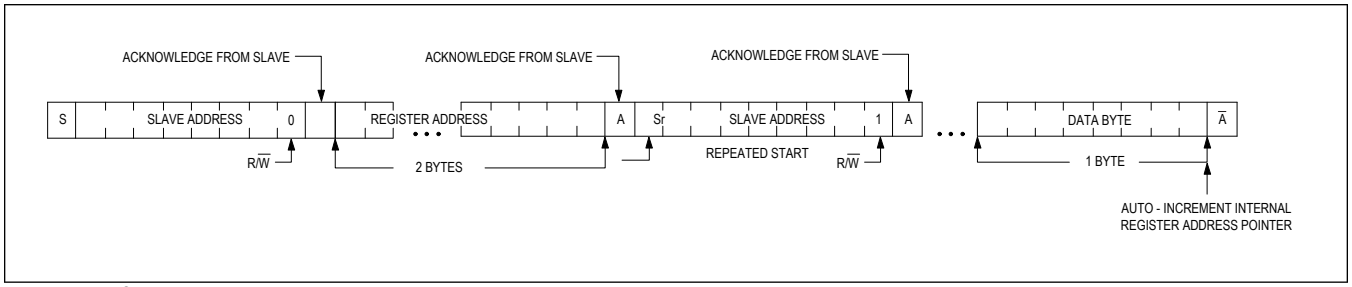


Figure 39. I²C Reading n-Bytes of Data from the Slave

I²C Register Map

Control Bit Field Types and Write Access Restrictions

The device control bit fields fall into one of three basic types: read, write, or read and write. There are no read restrictions, and any read enabled bit field can be read back anytime the I²C control interface is active. There are however write restrictions, and every write enabled bit field falls into one of two write access subtypes.

The first write access subtype is dynamic. Dynamic bit fields effectively have no write access restrictions, and can be safely changed (written) in any device state where the I²C control interface is active. The second bit field access subtype is restricted. Restricted bit fields should only be changed (written) when the related functional block (as shown in Table 10) is powered down.

If the write access is restricted to the global enable (restrictions EN and ENL), then the restricted bit field should only be changed (written) when the device is in software-shutdown. As a form of system protection, write access to some critical global enable restricted bit fields (ENL) is locked out by the hardware when the device is not in the software-shutdown state. Attempting to change (write to) these locked restricted bit fields when the device is not in the software-shutdown state has no effect (read-access is still allowed).

The bit field type and write access subtype is provided for every bit field in the detailed register description tables. For all bit fields with the restricted subtype, the dependency is also denoted in the "RES" column.

Table 10 provides a detailed description of all device register types, access subtypes, and restriction dependencies that are used by this device. The write access restrictions describe the specific device condition(s) that should be met (and the corresponding bit field settings) before the system attempts to change (write to) bit fields with that restriction type.

Table 10. Control Bit Types and Write Access Restrictions

BIT FIELD TYPE	WRITE ACCESS	WRITE ACCESS RESTRICTIONS		"RES" SYMBOL
		DESCRIPTION	CONDITION	
Read	Read Only	—	—	—
Write or Read/ Write	Dynamic	—	—	—
	Restricted	Device in Software Shutdown	EN = 0	**EN**
		Write Access Locked Out by Hardware Unless the Device is in Software Shutdown	EN = 0	**ENL**
		Speaker Amplifier Output and Feedback Disabled	SPK_EN = 0 and SPK_FB_EN = 0	**SPK**
		Voltage and Current Sense ADCs Disabled	IVADC_V_EN = 0 and IVADC_I_EN = 0	**IVS**
		Thermal Foldback Disabled	THERMFB_EN = 0	**TFB**
		Noise Gate Disabled	NOISEGATE_EN = 0	**NG**
		Dynamic Headroom Tracking Disabled	DHT_EN = 0	**DHT**
		PCM Interface Data Input and Output Disabled	PCM_RX_EN = 0 and PCM_TX_EN = 0	**PCM**
		PCM Data Output Disabled	PCM_TX_EN = 0	**TXEN**
		IRQ Bus Output Disabled	IRQ_EN = 0	**IRQ**
		Interchip Communication (ICC) Interface Disabled	ICC_LINK_EN = 0 and ICC_TX_EN = 0	**ICC**

Register Map

MAX98395 Register Map

ADDRESS	NAME	MSB							LSB
Reset									
0x2000	Software Reset[7:0]	–	–	–	–	–	–	–	RST
Interrupts									
0x2001	Interrupt Raw 1[7:0]	THERMSHDN_BGN_RAW	THERMSHDN_END_RAW	THERMWARN_BGN_RAW	THERMWARN_END_RAW	THERMFB_BGN_RAW	THERMFB_END_RAW	OTP_FAIL_RAW	SPK_OVC_RAW
0x2002	Interrupt Raw 2[7:0]	–	–	INT_SPKMON_ERR_RAW	INT_CLK_ERR_RAW	–	CLK_RECOVER_RAW	CLK_ER R_RAW	DMON_ERR_RAW
0x2003	Interrupt Raw 3[7:0]	–	–	PWRUP_DONE_RAW	PWRDN_DONE_RAW	PVDD_UVLO_SHDN_RAW	VBAT_UVLO_SHDN_RAW	DHT_ACTIVE_BGN_RAW	DHT_ACTIVE_END_RAW
0x2006	Interrupt State 1[7:0]	THERMSHDN_BGN_STATE	THERMSHDN_END_STATE	THERMWARN_BGN_STATE	THERMWARN_END_STATE	THERMFB_BGN_STATE	THERMFB_END_STATE	OTP_FAIL_STATE	SPK_OVC_STATE
0x2007	Interrupt State 2[7:0]	–	–	INT_SPKMON_ERR_STATE	INT_CLK_ERR_STATE	–	CLK_RECOVER_STATE	CLK_ER R_STATE	DMON_ERR_STATE
0x2008	Interrupt State 3[7:0]	–	–	PWRUP_DONE_STATE	PWRDN_DONE_STATE	PVDD_UVLO_SHDN_STATE	VBAT_UVLO_SHDN_STATE	DHT_ACTIVE_BGN_STATE	DHT_ACTIVE_END_STATE
0x200B	Interrupt Flag 1[7:0]	THERMSHDN_BGN_FLAG	THERMSHDN_END_FLAG	THERMWARN_BGN_FLAG	THERMWARN_END_FLAG	THERMFB_BGN_FLAG	THERMFB_END_FLAG	OTP_FAIL_FLAG	SPK_OVC_FLAG
0x200C	Interrupt Flag 2[7:0]	–	–	INT_SPKMON_ERR_FLAG	INT_CLK_ERR_FLAG	–	CLK_RECOVER_FLAG	CLK_ER R_FLAG	DMON_ERR_FLAG
0x200D	Interrupt Flag 3[7:0]	–	–	PWRUP_DONE_FLAG	PWRDN_DONE_FLAG	PVDD_UVLO_SHDN_FLAG	VBAT_UVLO_SHDN_FLAG	DHT_ACTIVE_BGN_FLAG	DHT_ACTIVE_END_FLAG
0x2010	Interrupt Enable 1[7:0]	THERMSHDN_BGN_EN	THERMSHDN_END_EN	THERMWARN_BGN_EN	THERMWARN_END_EN	THERMFB_BGN_EN	THERMFB_END_EN	OTP_FAIL_EN	SPK_OVC_EN
0x2011	Interrupt Enable 2[7:0]	–	–	INT_SPKMON_ERR_EN	INT_CLK_ERR_EN	–	CLK_RECOVER_EN	CLK_ER R_EN	DMON_ERR_EN

ADDRESS	NAME	MSB							LSB
0x2012	Interrupt Enable 3[7:0]	–	–	PWRUP_DONE_EN	PWRDN_DONE_EN	PVDD_UVLO_SHDN_EN	VBAT_UVLO_SHDN_EN	DHT_ACTIVE_BGN_EN	DHT_ACTIVE_END_EN
0x2015	Interrupt Flag Clear 1[7:0]	THERMSHDN_BGN_CLR	THERMSHDN_END_CLR	THERMWARN_BGN_CLR	THERMWARN_END_CLR	THERMFB_BGN_CLR	THERMFB_END_CLR	OTP_FAIL_CLR	SPK_OVC_CLR
0x2016	Interrupt Flag Clear 2[7:0]	–	–	INT_SPKMON_ERR_CLR	INT_CLK_ERR_CLR	–	CLK_RECOVER_CLR	CLK_ERR_CLR	DMON_ERR_CLR
0x2017	Interrupt Flag Clear 3[7:0]	–	–	PWRUP_DONE_CLR	PWRDN_DONE_CLR	PVDD_UVLO_SHDN_CLR	VBAT_UVLO_SHDN_CLR	DHT_ACTIVE_BGN_CLR	DHT_ACTIVE_END_CLR
0x201F	IRQ Control[7:0]	–	–	–	–	–	IRQ_MODE	IRQ_POL	IRQ_EN
Thermal Protection									
0x2020	Thermal Warning Threshhold[7:0]	–	–	THERMWARN_THRESH[5:0]					
0x2021	Thermal Shutdown Threshold[7:0]	–	–	THERMSHDN_THRESH[5:0]					
0x2022	Thermal Hysteresis[7:0]	–	–	–	–	–	–	THERM_HYST[1:0]	
0x2023	Thermal Foldback Settings[7:0]	–	–	THERMFB_HOLD[1:0]		THERMFB_RLS[1:0]		THERMFB_SLOPE[1:0]	
0x2027	Thermal Foldback Enable[7:0]	–	–	–	–	–	–	–	THERMFB_EN
Noise Gate									
0x2030	Noise Gate Control[7:0]	NG_UNMUTE_THRESH[3:0]				NG_MUTE_THRESH[3:0]			
0x2033	Noise Gate Enables[7:0]	–	–	–	–	–	–	–	NOISEGATE_EN
Clock and Data Monitor Control									
0x2038	Clock Monitor Control[7:0]	–	CMON_BSELTOL[2:0]			CMON_ERRTOL[2:0]			CMON_AUTORESTART_EN
0x2039	Data Monitor Control[7:0]	–	–	DMON_MAG_THRES[1:0]		DMON_STUCK_THRES[1:0]		DMON_DURATION[1:0]	
0x203F	Enable Controls[7:0]	–	–	–	–	SPKMON_EN	DMON_MAG_EN	DMON_STUCK_EN	CMON_EN
PCM Registers									
0x2040	Pin Config[7:0]	LV_EN_DRV[1:0]		ICC_DRV[1:0]		IRQ_DRV[1:0]		DOUT_DRV[1:0]	
0x2041	PCM Mode Config[7:0]	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]			PCM_TX_INTERLEAVE	PCM_CHANSEL	PCM_TX_EXTRA_HIZ
0x2042	PCM Clock Setup[7:0]	–	–	–	PCM_BCLKEDGE	PCM_BSEL[3:0]			
0x2043	PCM Sample Rate Setup 1[7:0]	IVADC_SR[3:0]				PCM_SR[3:0]			

ADDRESS	NAME	MSB							LSB
0x2044	PCM RX Source[7:0]	–	–	–	–	PCM_DAC_SOURCE[3:0]			
0x2045	PCM TX Control 1[7:0]	–	–	PCM_VMON_SLOT[5:0]					
0x2046	PCM TX Control 2[7:0]	–	–	PCM_IMON_SLOT[5:0]					
0x2047	PCM TX Control 3[7:0]	–	–	PCM_PVDD_SLOT[5:0]					
0x2048	PCM TX Control 4[7:0]	–	–	PCM_VBAT_SLOT[5:0]					
0x2049	PCM TX Control 5[7:0]	–	–	PCM_DHT_ATN_SLOT[5:0]					
0x204A	PCM TX Control 6[7:0]	–	–	PCM_STATUS_SLOT[5:0]					
0x204B	PCM TX Control 7[7:0]	–	–	PCM_DSP_MONITOR_SLOT[5:0]					
0x204C	PCM Tx HiZ Control 1[7:0]	PCM_TX_SLOT_HIZ[63:56]							
0x204D	PCM Tx HiZ Control 2[7:0]	PCM_TX_SLOT_HIZ[55:48]							
0x204E	PCM Tx HiZ Control 3[7:0]	PCM_TX_SLOT_HIZ[47:40]							
0x204F	PCM Tx HiZ Control 4[7:0]	PCM_TX_SLOT_HIZ[39:32]							
0x2050	PCM Tx HiZ Control 5[7:0]	PCM_TX_SLOT_HIZ[31:24]							
0x2051	PCM Tx HiZ Control6[7:0]	PCM_TX_SLOT_HIZ[23:16]							
0x2052	PCM Tx HiZ Control 7[7:0]	PCM_TX_SLOT_HIZ[15:8]							
0x2053	PCM Tx HiZ Control 8[7:0]	PCM_TX_SLOT_HIZ[7:0]							
0x205D	PCM TX Source Enables[7:0]	–	PCM_STATUS_EN	PCM_DHT_ATN_EN	PCM_VBAT_EN	PCM_PVDD_EN	PCM_DSPMONITOR_EN	PCM_IMON_EN	PCM_VMON_EN
0x205E	PCM Rx Enables[7:0]	–	–	–	–	–	–	–	PCM_RX_EN
0x205F	PCM Tx Enables[7:0]	–	–	–	–	–	–	–	PCM_TX_EN
Interchip Communication									
0x2070	ICC Rx Enables A[7:0]	ICC_RX_CH7_EN	ICC_RX_CH6_EN	ICC_RX_CH5_EN	ICC_RX_CH4_EN	ICC_RX_CH3_EN	ICC_RX_CH2_EN	ICC_RX_CH1_EN	ICC_RX_CH0_EN
0x2071	ICC Rx Enables B[7:0]	ICC_RX_CH15_EN	ICC_RX_CH14_EN	ICC_RX_CH13_EN	ICC_RX_CH12_EN	ICC_RX_CH11_EN	ICC_RX_CH10_EN	ICC_RX_CH9_EN	ICC_RX_CH8_EN
0x2072	ICC Tx Control[7:0]	–	–	–	ICC_DATA_SEL	ICC_TX_DEST[3:0]			
0x207F	ICC Enables[7:0]	–	–	–	–	–	–	ICC_LINK_EN	ICC_TX_EN
Tone Generator Control									
0x2083	Tone Generator and DC Config[7:0]	–	–	TONE_AMPLITUDE[1:0]		TONE_CONFIG[3:0]			
0x2084	Tone Generator DC Level 1[7:0]	TONE_DC[23:16]							

ADDRESS	NAME	MSB							LSB
0x2085	Tone Generator DC Level 2[7:0]	TONE_DC[15:8]							
0x2086	Tone Generator DC Level 3[7:0]	TONE_DC[7:0]							
0x2087	Tone Generator Clock Control[7:0]	–	–	–	–	–	–	–	REF_CLK_SEL
0x208F	Tone Generator Enable[7:0]	–	–	–	–	–	–	–	TONE_EN
Speaker Path Control									
0x2090	AMP volume control[7:0]	–	SPK_VOL[6:0]						
0x2091	AMP Path Gain[7:0]	SPK_GAIN[3:0]				SPK_GAIN_MAX[3:0]			
0x2092	AMP DSP Config[7:0]	–	–	SPK_SAFE_EN	SPK_VOL_RMPDN_BYPASS	SPK_VOL_RMPUP_BYPASS	SPK_INVERT	SPK_DITH_EN	SPK_DCBLK_EN
0x2093	SSM Configuration[7:0]	–	–	–	–	SPK_SSM_EN	SPK_SSM_MOD_INDEX[2:0]		
0x2094	SPK Class DG Threshold[7:0]	–	–	–	SPK_DG_THRES[4:0]				
0x2095	SPK Class DG Headroom[7:0]	–	–	SPK_DG_SEL[1:0]		SPK_DG_HEADROOM[3:0]			
0x2096	SPK Class DG Hold Time[7:0]	–	–	–	–	SPK_DG_HOLD_TIME[3:0]			
0x2097	SPK Class DG Delay[7:0]	–	–	SPK_DG_DELAY[5:0]					
0x2098	SPK Class DG Mode[7:0]	–	–	–	–	–	–	SPK_MODE[1:0]	
0x2099	SPK Class DG VBAT Level[7:0]	–	–	–	–	–	VBATLOW_OK_LVL[2:0]		
0x209C	SPK Edge Control 1[7:0]	–	–	–	–	SPK_SL_RATE_GMODE[3:0]			
0x209D	SPK Edge Control 2[7:0]	SPK_SL_RATE_LS[3:0]				SPK_SL_RATE_HS[3:0]			
0x20AF	AMP enables[7:0]	–	–	–	–	–	–	SPK_FB_EN	SPK_EN
Meas ADC									
0x20B0	Meas ADC Sample Rate[7:0]	–	–	MEAS_ADC_TEMP_SR[1:0]		MEAS_ADC_PVDD_SR[1:0]		MEAS_ADC_VBAT_SR[1:0]	
0x20B1	Meas ADC PVDD Config[7:0]	–	–	–	MEAS_ADC_PVDD_FILT_EN	MEAS_ADC_PVDD_FILT_COEFF[3:0]			
0x20B2	Meas ADC VBAT Config[7:0]	–	–	–	MEAS_ADC_VBAT_FILT_EN	MEAS_ADC_VBAT_FILT_COEFF[3:0]			

ADDRESS	NAME	MSB							LSB
0x20B3	Meas ADC Thermal Config[7:0]	–	–	–	MEAS_ADC_TEMP_FILT_EN	MEAS_ADC_TEMP_FILT_COEFF[3:0]			
0x20B4	Meas ADC Readback Control 1[7:0]	–	–	–	–	–	MEAS_ADC_THERM_RD_MODE	MEAS_ADC_VBAT_RD_MODE	MEAS_ADC_PVDD_RD_MODE
0x20B5	Meas ADC Readback Control 2[7:0]	–	–	–	–	–	MEAS_ADC_THERM_RD_UPD	MEAS_ADC_VBAT_RD_UPD	MEAS_ADC_PVDD_RD_UPD
0x20B6	Meas ADC PVDD Readback MSB[7:0]	MEAS_ADC_PVDD_DATA[8:1]							
0x20B7	Meas ADC PVDD Readback LSB[7:0]	–	–	–	–	–	–	–	MEAS_ADC_PVDD_DATA[0]
0x20B8	Meas ADC VBAT Readback MSB[7:0]	MEAS_ADC_VBAT_DATA[8:1]							
0x20B9	Meas ADC VBAT Readback LSB[7:0]	–	–	–	–	–	–	–	MEAS_ADC_VBAT_DATA[0]
0x20BA	Meas ADC Temp Readback MSB[7:0]	MEAS_ADC_THERM_DATA[8:1]							
0x20BB	Meas ADC Temp Readback LSB[7:0]	–	–	–	–	–	–	–	MEAS_ADC_THERM_DATA[0]
0x20BC	Meas ADC Lowest PVDD Readback MSB[7:0]	LOWEST_PVDD_DATA[8:1]							
0x20BD	Meas ADC Lowest PVDD Readback LSB[7:0]	–	–	–	–	–	–	–	LOWEST_PVDD_DATA[0]
0x20BE	Meas ADC Lowest VBAT Readback MSB[7:0]	LOWEST_VBAT_DATA[8:1]							
0x20BF	Meas ADC Lowest VBAT Readback LSB[7:0]	–	–	–	–	–	–	–	LOWEST_VBAT_DATA[0]
0x20C7	Meas ADC Config[7:0]	–	–	–	–	–	–	MEAS_ADC_VBAT_EN	MEAS_ADC_PVDD_EN
Dynamic Headroom Tracking									
0x20D0	DHT Configuration 1[7:0]	–	–	–	–	DHT_VROT_PNT[3:0]			

ADDRESS	NAME	MSB							LSB
0x20D1	Limiter Configuration 1[7:0]	–	–	–	DHT_HR[4:0]				
0x20D2	Limiter Configuration 2[7:0]	–	–	DHT_LIM_THRESH[4:0]					DHT_LIM_MODE
0x20D3	DHT Configuration 2[7:0]	–	–	–	–	DHT_MAX_ATN[3:0]			
0x20D4	DHT Configuration 3[7:0]	–	–	–	–	DHT_ATK_RATE[3:0]			
0x20D5	DHT Configuration 4[7:0]	–	–	–	–	DHT_RLS_RATE[3:0]			
0x20D6	DHT Supply Hysteresis Configuration[7:0]	–	–	–	–	DHT_SUPPLY_HYST[2:0]			DHT_SUPPLY_HYST_EN
0x20DF	DHT Enable[7:0]	–	–	–	–	–	–	–	DHT_EN
I_V Sense Path Control									
0x20E0	Measurement DSP Config[7:0]	–	–	–	–	–	IVADC_DITH_EN	IVADC_I_DCBLK_EN	IVADC_V_DCBLK_EN
0x20E7	Measurement enables[7:0]	–	–	–	–	–	–	IVADC_I_EN	IVADC_V_EN
System Configuration									
0x20FE	Auto-Restart Behavior[7:0]	–	–	–	–	OVC_AUTORESTART_EN	THERM_AUTORESTART_EN	VBAT_AUTORESTART_EN	PVDD_AUTORESTART_EN
0x20FF	Global Enable[7:0]	–	–	–	–	–	–	–	EN
Device and Revision ID									
0x21FF	Revision ID[7:0]	REV_ID[7:0]							

Register Details

Software Reset (0x2000)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	RST
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
RST	0	This bit field is used to trigger a software reset event. Writing a 1 resets the device and returns the control registers to their power-on reset states. Writing a 0 has no effect, and readback always returns 0.	0: No action. 1: Triggers a software reset event.

Interrupt Raw 1 (0x2001)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_BGN_RAW	THERMSHDN_END_RAW	THERMWARN_BGN_RAW	THERMWARN_END_RAW	THERMFB_BGN_RAW	THERMFB_END_RAW	OTP_FAIL_RAW	SPK_OVC_RAW
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_BGN_RAW	7	Raw value of thermal shutdown begin indicator.	0: Die temperature below thermal warning limit. 1: Die temperature above thermal warning limit.
THERMSHDN_END_RAW	6	Raw value of thermal shutdown end indicator.	0: Die temperature above thermal shutdown limit. 1: Die temperature has dropped below thermal shutdown limit.
THERMWARN_BGN_RAW	5	Raw value of thermal warning begin indicator.	0: Die temperature below thermal warning limit. 1: Die temperature above thermal warning limit.
THERMWARN_END_RAW	4	Raw value of thermal warning end indicator.	0: Die temperature above thermal warning limit. 1: Die temperature has dropped below thermal warning limit.
THERMFB_BGN_RAW	3	Raw value of thermal foldback begin.	0: The thermal foldback is not active. 1: Thermal foldback is active.
THERMFB_END_RAW	2	Raw value of thermal foldback end.	0: The thermal foldback is active. 1: Thermal foldback has ended.
OTP_FAIL_RAW	1	Raw status of OTP load fail.	0: No OTP load failure. 1: The OTP load routine did not complete succesfully.
SPK_OVC_RAW	0	Raw value of speaker overcurrent limit.	0: Speaker overcurrent limit inactive. 1: Speaker overcurrent limit active.

Interrupt Raw 2 (0x2002)

BIT	7	6	5	4	3	2	1	0
Field	–	–	INT_SPKMON_ERR_RAW	INT_CLK_ERR_RAW	–	CLK_RECOVER_RAW	CLK_ERR_RAW	DMON_ERR_RAW
Reset	–	–	0b0	0x0	–	0x0	0x0	0b0
Access Type	–	–	Read Only	Read Only	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
INT_SPKMON_ERR_RAW	5	Raw value of the internal speaker monitor status indicator.	0: Internal speaker monitor not reporting data error. 1: Internal speaker monitor reporting data error.
INT_CLK_ERR_RAW	4	Raw value of internal clock error indicator.	0: Internal clock monitor not reporting clock error. 1: Internal clock monitor reporting clock error.
CLK_RECOVER_RAW	2	Raw value of the external clock monitor error recovery indicator.	0: Clock monitor not reporting clock error recovery. 1: Clock monitor reporting clock error recovery.
CLK_ERR_RAW	1	Raw value of the external clock monitor error indicator.	0: No external clock error detected. 1: Clock monitor reporting clock error.

BITFIELD	BITS	DESCRIPTION	DECODE
DMON_ERR_RAW	0	Raw value of external data monitor error indicator.	0: No external data error detected. 1: Data monitor reporting data error.

Interrupt Raw 3 (0x2003)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PWRUP_DONE_RAW	PWRDN_DONE_RAW	PVDD_UVLO_SHDN_RAW	VBAT_UVLO_SHDN_RAW	DHT_ACTIVE_BGN_RAW	DHT_ACTIVE_END_RAW
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PWRUP_DONE_RAW	5	Raw value of power-up done.	0: Device is not reporting a power-up event. 1: Device is reporting a power-up into the active state with the speaker amplifier enabled.
PWRDN_DONE_RAW	4	Raw value of power-down done.	0: Device is not reporting a power-down into software shutdown event. 1: Device is reporting a power-down into software shutdown event.
PVDD_UVLO_SHDN_RAW	3	Raw value of PVDD UVLO error indicator.	0: No PVDD UVLO error. 1: PVDD below UVLO threshold in the active state.
VBAT_UVLO_SHDN_RAW	2	Raw value of VBAT UVLO error indicator.	0: No VBAT UVLO error. 1: VBAT below UVLO threshold in the active state.
DHT_ACTIVE_BGN_RAW	1	Raw value of DHT active begin.	0: DHT is not active. 1: DHT is active.
DHT_ACTIVE_END_RAW	0	Raw value of DHT active end.	0: DHT is currently active or has not yet applied attenuation. 1: DHT activity has ended.

Interrupt State 1 (0x2006)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_BGN_STATE	THERMSHDN_END_STATE	THERMWARN_BGN_STATE	THERMWARN_END_STATE	THERMFB_BGN_STATE	THERMFB_END_STATE	OTP_FAIL_STATE	SPK_OVC_STATE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_BGN_STATE	7	Unmaskable interrupt state, cleared by THERMSHDN_BGN_CLR.	0: No rising edge of THERMSHDN_BGN_RAW since last THERMSHDN_BGN_CLR. 1: Rising edge of THERMSHDN_BGN_RAW since last THERMSHDN_BGN_CLR.

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_END_STATE	6	Unmaskable interrupt state, cleared by THERMSHDN_END_CLR.	0: No rising edge of THERMSHDN_END_RAW since last THERMSHDN_END_CLR. 1: Rising edge of THERMSHDN_END_RAW since last THERMSHDN_END_CLR.
THERMWARN_BGN_STATE	5	Unmaskable interrupt state, cleared by THERMWARN_BGN_CLR.	0: No rising edge of THERMWARN_BGN_RAW since last THERMWARN_BGN_CLR. 1: Rising edge of THERMWARN_BGN_RAW since last THERMWARN_BGN_CLR.
THERMWARN_END_STATE	4	Unmaskable interrupt state, cleared by THERMWARN_END_CLR.	0: No rising edge of THERMWARN_END_RAW since last THERMWARN_END_CLR. 1: Rising edge of THERMWARN_END_RAW since last THERMWARN_END_CLR.
THERMFB_BGN_STATE	3	Unmaskable interrupt state, cleared by THERMFB_BGN_CLR.	0: No rising edge of THERMFB_BGN_RAW since last THERMFB_BGN_CLR. 1: Rising edge of THERMFB_BGN_RAW since last THERMFB_BGN_CLR.
THERMFB_END_STATE	2	Unmaskable interrupt state, cleared by THERMFB_END_CLR.	0: No rising edge of THERMFB_END_RAW since last THERMFB_END_CLR. 1: Rising edge of THERMFB_END_RAW since last THERMFB_END_CLR.
OTP_FAIL_STATE	1	Unmaskable interrupt state, cleared by OTP_FAIL_CLR.	0: No rising edge of OTP_FAIL_RAW since last OTP_FAIL_CLR. 1: Rising edge of OTP_FAIL_RAW since last OTP_FAIL_CLR.
SPK_OVC_STATE	0	Unmaskable interrupt state, cleared by SPK_OVC_CLR.	0: No rising edge of SPK_OVC_RAW since last SPK_OVC_CLR. 1: Rising edge of SPK_OVC_RAW since last SPK_OVC_CLR.

Interrupt State 2 (0x2007)

BIT	7	6	5	4	3	2	1	0
Field	–	–	INT_SPKMON_ERR_STATE	INT_CLK_ERR_STATE	–	CLK_RECOVER_STATE	CLK_ERR_STATE	DMON_ERR_STATE
Reset	–	–	0b0	0x0	–	0x0	0x0	0b0
Access Type	–	–	Read Only	Read Only	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
INT_SPKMON_ERR_STATE	5	Unmaskable interrupt state, cleared by INT_SPKMON_ERR_CLR.	0: No rising edge of INT_SPKMON_ERR_RAW since last INT_SPKMON_ERR_CLR. 1: Rising edge of INT_SPKMON_ERR_RAW since last INT_SPKMON_ERR_CLR.
INT_CLK_ERR_STATE	4	Unmaskable interrupt state, cleared by INT_CLK_ERR_CLR.	0: No rising edge of INT_CLK_ERR_RAW since last INT_CLK_ERR_CLR. 1: Rising edge of INT_CLK_ERR_RAW since last INT_CLK_ERR_CLR.
CLK_RECOVER_STATE	2	Unmaskable interrupt state, cleared by CLK_RECOVER_CLR.	0: No rising edge of CLK_RECOVER_RAW since last CLK_RECOVER_CLR. 1: Rising edge of CLK_RECOVER_RAW since last CLK_RECOVER_CLR.

BITFIELD	BITS	DESCRIPTION	DECODE
CLK_ERR_STATE	1	Unmaskable interrupt state, cleared by CLK_ERR_CLR.	0: No rising edge of CLK_ERR_RAW since last CLK_ERR_CLR. 1: Rising edge of CLK_ERR_RAW since last CLK_ERR_CLR.
DMON_ERR_STATE	0	Unmaskable interrupt state, cleared by DMON_ERR_CLR.	0: No rising edge of DMON_ERR_RAW since last DMON_ERR_CLR. 1: Rising edge of DMON_ERR_RAW since last DMON_ERR_CLR.

Interrupt State 3 (0x2008)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PWRUP_DONE_STATE	PWRDN_DONE_STATE	PVDD_UVLO_SHDN_STATE	VBAT_UVLO_SHDN_STATE	DHT_ACTIVE_BGN_STATE	DHT_ACTIVE_END_STATE
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PWRUP_DONE_STATE	5	Unmaskable interrupt state, cleared by PWRUP_DONE_CLR.	0: No rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR. 1: Rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR.
PWRDN_DONE_STATE	4	Unmaskable interrupt state, cleared by PWRDN_DONE_CLR.	0: No rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR. 1: Rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR.
PVDD_UVLO_SHDN_STATE	3	Unmaskable interrupt state, cleared by PVDD_UVLO_SHDN_CLR.	0: No rising edge of PVDD_UVLO_SHDN_RAW since last PVDD_UVLO_SHDN_CLR. 1: Rising edge of PVDD_UVLO_SHDN_RAW since last PVDD_UVLO_SHDN_CLR.
VBAT_UVLO_SHDN_STATE	2	Unmaskable interrupt state, cleared by VBAT_UVLO_SHDN_CLR.	0: No rising edge of VBAT_UVLO_SHDN_RAW since last VBAT_UVLO_SHDN_CLR. 1: Rising edge of VBAT_UVLO_SHDN_RAW since last VBAT_UVLO_SHDN_CLR.
DHT_ACTIVE_BGN_STATE	1	Unmaskable interrupt state, cleared by DHT_ACTIVE_BGN_CLR.	0: No rising edge of DHT_ACTIVE_BGN_RAW since last DHT_ACTIVE_BGN_CLR. 1: Rising edge of DHT_ACTIVE_BGN_RAW since last DHT_ACTIVE_BGN_CLR.
DHT_ACTIVE_END_STATE	0	Unmaskable interrupt state, cleared by DHT_ACTIVE_END_CLR.	0: No rising edge of DHT_ACTIVE_END_RAW since last DHT_ACTIVE_END_CLR. 1: Rising edge of DHT_ACTIVE_END_RAW since last DHT_ACTIVE_END_CLR.

Interrupt Flag 1 (0x200B)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_BGN_FLAG	THERMSHDN_END_FLAG	THERMWARN_BGN_FLAG	THERMWARN_END_FLAG	THERMFB_BGN_FLAG	THERMFB_END_FLAG	OTP_FAIL_FLAG	SPK_OVC_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_BGN_FLAG	7	Masked by THERMSHDN_BGN_EN and cleared by THERMSHDN_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of THERMSHDN_BGN_RAW since last THERMSHDN_BGN_CLR or THERMSHDN_BGN_EN is low. 1: THERMSHDN_BGN_EN is high and rising edge of THERMSHDN_BGN_RAW since last THERMSHDN_BGN_CLR.
THERMSHDN_END_FLAG	6	Masked by THERMSHDN_END_EN and cleared by THERMSHDN_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of THERMSHDN_END_RAW since last THERMSHDN_END_CLR or THERMSHDN_END_EN is low. 1: THERMSHDN_END_EN is high and rising edge of THERMSHDN_END_RAW since last THERMSHDN_END_CLR.
THERMWARN_BGN_FLAG	5	Masked by THERMWARN_BGN_EN and cleared by THERMWARN_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of THERMWARN_BGN_RAW since last THERMWARN_BGN_CLR or THERMWARN_BGN_EN is low. 1: THERMWARN_BGN_EN is high and rising edge of THERMWARN_BGN_RAW since last THERMWARN_BGN_CLR.
THERMWARN_END_FLAG	4	Masked by THERMWARN_END_EN and cleared by THERMWARN_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of THERMWARN_END_RAW since last THERMWARN_END_CLR or THERMWARN_END_EN is low. 1: THERMWARN_END_EN is high and rising edge of THERMWARN_END_RAW since last THERMWARN_END_CLR.
THERMFB_BGN_FLAG	3	Masked by THERMFB_BGN_EN and cleared by THERMFB_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of THERMFB_BGN_RAW since last THERMFB_BGN_CLR or THERMFB_BGN_EN is low. 1: THERMFB_BGN_EN is high and rising edge of THERMFB_BGN_RAW since last THERMFB_BGN_CLR.
THERMFB_END_FLAG	2	Masked by THERMFB_END_EN and cleared by THERMFB_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of THERMFB_END_RAW since last THERMFB_END_CLR or THERMFB_END_EN is low. 1: THERMFB_END_EN is high and rising edge of THERMFB_END_RAW since last THERMFB_END_CLR.
OTP_FAIL_FLAG	1	Masked by OTP_FAIL_EN and cleared by OTP_FAIL_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of OTP_FAIL_RAW since last OTP_FAIL_CLR or OTP_FAIL_EN is low. 1: OTP_FAIL_EN is high and rising edge of OTP_FAIL_RAW since last OTP_FAIL_CLR.
SPK_OVC_FLAG	0	Masked by SPK_OVC_EN and cleared by SPK_OVC_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of SPK_OVC_RAW since last SPK_OVC_CLR or SPK_OVC_EN is low. 1: SPK_OVC_EN is high and rising edge of SPK_OVC_RAW since last SPK_OVC_CLR.

Interrupt Flag 2 (0x200C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	INT_SPKMON_ERR_FLAG	INT_CLK_ERR_FLAG	–	CLK_RECOVER_FLAG	CLK_ERR_FLAG	DMON_ERR_FLAG
Reset	–	–	0b0	0x0	–	0x0	0x0	0b0
Access Type	–	–	Read Only	Read Only	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
INT_SPKMON_ERR_FLAG	5	Masked by INT_SPKMON_ERR_EN and cleared by INT_SPKMON_ERR_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of INT_SPKMON_ERR_RAW since last INT_SPKMON_ERR_CLR or INT_SPKMON_ERR_EN is low. 1: INT_SPKMON_ERR_EN high and rising edge of INT_SPKMON_ERR_RAW since last INT_SPKMON_ERR_CLR.
INT_CLK_ERR_FLAG	4	Masked by INT_CLK_ERR_EN and cleared by INT_CLK_ERR_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of INT_CLK_ERR_RAW since last INT_CLK_ERR_CLR or INT_CLK_ERR_EN is low. 1: INT_CLK_ERR_EN high and rising edge of INT_CLK_ERR_RAW since last INT_CLK_ERR_CLR.
CLK_RECOVER_FLAG	2	Masked by CLK_RECOVER_EN and cleared by CLK_RECOVER_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of CLK_RECOVER_RAW since last CLK_RECOVER_CLR or CLK_RECOVER_EN is low. 1: BCLK_RECOVER_EN high and rising edge of BCLK_RECOVER_RAW since last BCLK_RECOVER_CLR.
CLK_ERR_FLAG	1	Masked by CLK_ERR_EN and cleared by CLK_ERR_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of CLK_ERR_RAW since last CLK_ERR_CLR or CLK_ERR_EN is low. 1: CLK_ERR_EN high and rising edge of CLK_ERR_RAW since last CLK_ERR_CLR.
DMON_ERR_FLAG	0	Masked by DMON_ERR_EN and cleared by DMON_ERR_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of DMON_ERR_RAW since last DMON_ERR_CLR or DMON_ERR_EN is low. 1: DMON_ERR_EN high and rising edge of DMON_ERR_RAW since last DMON_ERR_CLR.

Interrupt Flag 3 (0x200D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PWRUP_DONE_FLAG	PWRDN_DONE_FLAG	PVDD_UVLO_SHDN_FLAG	VBAT_UVLO_SHDN_FLAG	DHT_ACTIVE_BGN_FLAG	DHT_ACTIVE_END_FLAG
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PWRUP_DONE_FLAG	5	Masked by PWRUP_DONE_EN and cleared by PWRUP_DONE_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR or PWRUP_DONE_EN is low. 1: PWRUP_DONE_EN is high and rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR.

BITFIELD	BITS	DESCRIPTION	DECODE
PWRDN_DONE_FLAG	4	Masked by PWRDN_DONE_EN and cleared by PWRDN_DONE_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR or PWRDN_DONE_EN is low. 1: PWRDN_DONE_EN is high and rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR.
PVDD_UVLO_SHDN_FLAG	3	Masked by PVDD_UVLO_SHDN_EN and cleared by PVDD_UVLO_SHDN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of PVDD_UVLO_SHDN_RAW since last PVDD_UVLO_SHDN_CLR or PVDD_UVLO_SHDN_EN is low. 1: PVDD_UVLO_SHDN_EN is high and rising edge of PVDD_UVLO_SHDN_RAW since last PVDD_UVLO_SHDN_CLR.
VBAT_UVLO_SHDN_FLAG	2	Masked by VBAT_UVLO_SHDN_EN and cleared by VBAT_UVLO_SHDN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of VBAT_UVLO_SHDN_RAW since last VBAT_UVLO_SHDN_CLR or VBAT_UVLO_SHDN_EN is low. 1: VBAT_UVLO_SHDN_EN is high and rising edge of VBAT_UVLO_SHDN_RAW since last VBAT_UVLO_SHDN_CLR.
DHT_ACTIVE_BGN_FLAG	1	Masked by DHT_ACTIVE_BGN_EN and cleared by DHT_ACTIVE_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of DHT_ACTIVE_BGN_RAW since last DHT_ACTIVE_BGN_CLR or DHT_ACTIVE_BGN_EN is low. 1: DHT_ACTIVE_BGN_EN is high and rising edge of DHT_ACTIVE_BGN_RAW since last DHT_ACTIVE_BGN_CLR.
DHT_ACTIVE_END_FLAG	0	Masked by DHT_ACTIVE_END_EN and cleared by DHT_ACTIVE_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of DHT_ACTIVE_END_RAW since last DHT_ACTIVE_END_CLR or DHT_ACTIVE_END_EN is low. 1: DHT_ACTIVE_END_EN is high and rising edge of DHT_ACTIVE_END_RAW since last DHT_ACTIVE_END_CLR.

Interrupt Enable 1 (0x2010)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_BGN_EN	THERMSHDN_END_EN	THERMWARN_BGN_EN	THERMWARN_END_EN	THERMFB_BGN_EN	THERMFB_END_EN	OTP_FAIL_EN	SPK_OVC_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_BGN_EN	7	Enable (unmask) control for THERMSHDN_BGN_FLAG.	0: THERMSHDN_BGN_FLAG cannot go high. 1: THERMSHDN_BGN_FLAG goes high if there is a rising edge on THERMSHDN_BGN_RAW since last THERMSHDN_BGN_CLR.
THERMSHDN_END_EN	6	Enable (unmask) control for THERMSHDN_END_FLAG.	0: THERMSHDN_END_FLAG cannot go high. 1: THERMSHDN_END_FLAG goes high if there is a rising edge on THERMSHDN_END_RAW since last THERMSHDN_END_CLR.

BITFIELD	BITS	DESCRIPTION	DECODE
THERMWARN_BGN_EN	5	Enable (unmask) control for THERMWARN_BGN_FLAG.	0: THERMWARN_BGN_FLAG cannot go high. 1: THERMWARN_BGN_FLAG goes high if there is a rising edge on THERMWARN_BGN_RAW since last THERMWARN_BGN_CLR.
THERMWARN_END_EN	4	Enable (unmask) control for THERMWARN_END_FLAG.	0: THERMWARN_END_FLAG cannot go high. 1: THERMWARN_END_FLAG goes high if there is a rising edge on THERMWARN_END_RAW since last THERMWARN_END_CLR.
THERMFB_BGN_EN	3	Enable (unmask) control for THERMFB_BGN_FLAG.	0: THERMFB_BGN_FLAG cannot go high. 1: THERMFB_BGN_FLAG goes high if there is a rising edge on THERMFB_BGN_RAW since last THERMFB_BGN_CLR.
THERMFB_END_EN	2	Enable (unmask) control for THERMFB_END_FLAG.	0: THERMFB_END_FLAG cannot go high. 1: THERMFB_END_FLAG goes high if there is a rising edge on THERMFB_END_RAW since last THERMFB_END_CLR.
OTP_FAIL_EN	1	Enable (unmask) control for OTP_FAIL_FLAG.	0: OTP_FAIL_FLAG cannot go high. 1: OTP_FAIL_FLAG goes high if there is a rising edge on OTP_FAIL_RAW since last OTP_FAIL_CLR.
SPK_OVC_EN	0	Enable (unmask) control for SPK_OVC_FLAG.	0: SPK_OVC_FLAG cannot go high. 1: SPK_OVC_FLAG goes high if there is a rising edge on SPK_OVC_RAW since last SPK_OVC_CLR.

Interrupt Enable 2 (0x2011)

BIT	7	6	5	4	3	2	1	0
Field	–	–	INT_SPKMON_ERR_EN	INT_CLK_ERR_EN	–	CLK_RECOVER_EN	CLK_ERR_EN	DMON_ERR_EN
Reset	–	–	0b0	0x0	–	0x0	0x0	0b0
Access Type	–	–	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
INT_SPKMON_ERR_EN	5	Enable (unmask) control for INT_SPKMON_ERR_FLAG.	0: INT_SPKMON_ERR_FLAG cannot go high. 1: INT_SPKMON_ERR_FLAG goes high if there is a rising edge on INT_SPKMON_ERR_RAW since last INT_SPKMON_ERR_CLR.
INT_CLK_ERR_EN	4	Enable (unmask) control for INT_CLK_ERR_FLAG.	0: INT_CLK_ERR_FLAG cannot go high. 1: INT_CLK_ERR_FLAG goes high if there is a rising edge on INT_CLK_ERR_RAW since last INT_CLK_ERR_CLR.
CLK_RECOVER_EN	2	Enable (unmask) control for CLK_RECOVER_FLAG.	0: CLK_RECOVER_FLAG cannot go high. 1: CLK_RECOVER_FLAG goes high if there is a rising edge on CLK_RECOVER_RAW since last CLK_RECOVER_CLR.
CLK_ERR_EN	1	Enable (unmask) control for CLK_ERR_FLAG.	0: CLK_ERR_FLAG cannot go high. 1: CLK_ERR_FLAG goes high if there is a rising edge on CLK_ERR_RAW since last CLK_ERR_CLR.

BITFIELD	BITS	DESCRIPTION	DECODE
DMON_ERR_EN	0	Enable (unmask) control for DMON_ERR_FLAG.	0: DMON_ERR_FLAG cannot go high. 1: DMON_ERR_FLAG goes high if there is a rising edge on DMON_ERR_RAW since last DMON_ERR_CLR.

Interrupt Enable 3 (0x2012)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PWRUP_DONE_EN	PWRDN_DONE_EN	PVDD_UVLO_SHDN_EN	VBAT_UVLO_SHDN_EN	DHT_ACTIVE_BGN_EN	DHT_ACTIVE_END_EN
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PWRUP_DONE_EN	5	Enable (unmask) control for PWRUP_DONE_FLAG.	0: PWRUP_DONE_FLAG cannot go high. 1: PWRUP_DONE_FLAG goes high if there is a rising edge on PWRUP_DONE_RAW since last PWRUP_DONE_CLR.
PWRDN_DONE_EN	4	Enable (unmask) control for PWRDN_DONE_FLAG.	0: PWRDN_DONE_FLAG cannot go high. 1: PWRDN_DONE_FLAG goes high if there is a rising edge on PWRDN_DONE_RAW since last PWRDN_DONE_CLR.
PVDD_UVLO_SHDN_EN	3	Enable (unmask) control for PVDD_UVLO_SHDN_FLAG.	0: PVDD_UVLO_SHDN_FLAG cannot go high. 1: PVDD_UVLO_SHDN_FLAG goes high if there is a rising edge on PVDD_UVLO_SHDN_RAW since last PVDD_UVLO_SHDN_CLR.
VBAT_UVLO_SHDN_EN	2	Enable (unmask) control for VBAT_UVLO_SHDN_FLAG.	0: VBAT_UVLO_SHDN_FLAG cannot go high. 1: VBAT_UVLO_SHDN_FLAG goes high if there is a rising edge on VBAT_UVLO_SHDN_RAW since last VBAT_UVLO_SHDN_CLR.
DHT_ACTIVE_BGN_EN	1	Enable (unmask) control for DHT_ACTIVE_BGN_FLAG.	0: DHT_ACTIVE_BGN_FLAG cannot go high. 1: DHT_ACTIVE_BGN_FLAG goes high if there is a rising edge on DHT_ACTIVE_BGN_RAW since last DHT_ACTIVE_BGN_CLR.
DHT_ACTIVE_END_EN	0	Enable (unmask) control for DHT_ACTIVE_END_FLAG.	0: DHT_ACTIVE_END_FLAG cannot go high. 1: DHT_ACTIVE_END_FLAG goes high if there is a rising edge on DHT_ACTIVE_END_RAW since last DHT_ACTIVE_END_CLR.

Interrupt Flag Clear 1 (0x2015)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_BGN_CLR	THERMSHDN_END_CLR	THERMWARN_BGN_CLR	THERMWARN_END_CLR	THERMFB_BGN_CLR	THERMFB_END_CLR	OTP_FAIL_CLR	SPK_OVC_CLR
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_BGN_CLR	7	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears THERMSHDN_BGN_STATE and THERMSHDN_BGN_FLAG to zero.
THERMSHDN_END_CLR	6	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears THERMSHDN_END_STATE and THERMSHDN_END_FLAG to zero.
THERMWARN_BGN_CLR	5	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears THERMWARN_BGN_STATE and THERMWARN_BGN_FLAG to zero.
THERMWARN_END_CLR	4	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears THERMWARN_END_STATE and THERMWARN_END_FLAG to zero.
THERMFB_BGN_CLR	3	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears THERMFB_BGN_STATE and THERMFB_BGN_FLAG to zero.
THERMFB_END_CLR	2	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears THERMFB_END_STATE and THERMFB_END_FLAG to zero.
OTP_FAIL_CLR	1	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears OTP_FAIL_STATE and OTP_FAIL_FLAG to zero.
SPK_OVC_CLR	0	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears SPK_OVC_STATE and SPK_OVC_FLAG to zero.

Interrupt Flag Clear 2 (0x2016)

BIT	7	6	5	4	3	2	1	0
Field	–	–	INT_SPKMON_ERR_CLR	INT_CLK_ERR_CLR	–	CLK_RECOVER_CLR	CLK_ERR_CLR	DMON_ERR_CLR
Reset	–	–	0b0	0x0	–	0x0	0x0	0b0
Access Type	–	–	Write Only	Write Only	–	Write Only	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
INT_SPKMON_ERR_CLR	5	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears INT_SPKMON_ERR_STATE and INT_SPKMON_ERR_FLAG to zero.
INT_CLK_ERR_CLR	4	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears INT_CLK_ERR_STATE and INT_CLK_ERR_FLAG to zero.
CLK_RECOVER_CLR	2	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears CLK_RECOVER_STATE and CLK_RECOVER_FLAG to zero.
CLK_ERR_CLR	1	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears CLK_ERR_STATE and CLK_ERR_FLAG to zero.
DMON_ERR_CLR	0	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears DMON_ERR_STATE and DMON_ERR_FLAG to zero.

Interrupt Flag Clear 3 (0x2017)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PWRUP_DONE_CLR	PWRDN_DONE_CLR	PVDD_UVLO_SHDN_CLR	VBAT_UVLO_SHDN_CLR	DHT_ACTIVE_BGN_CLR	DHT_ACTIVE_END_CLR
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
PWRUP_DONE_CLR	5	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears PWRUP_DONE_STATE and PWRUP_DONE_FLAG to zero.
PWRDN_DONE_CLR	4	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears PWRDN_DONE_STATE and PWRDN_DONE_FLAG to zero.
PVDD_UVLO_SHDN_CLR	3	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears PVDD_UVLO_SHDN_STATE and PVDD_UVLO_SHDN_FLAG to zero.
VBAT_UVLO_SHDN_CLR	2	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears VBAT_UVLO_SHDN_STATE and VBAT_UVLO_SHDN_FLAG to zero.
DHT_ACTIVE_BGN_CLR	1	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears DHT_ACTIVE_BGN_STATE and DHT_ACTIVE_BGN_FLAG to zero.
DHT_ACTIVE_END_CLR	0	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears DHT_ACTIVE_END_STATE and DHT_ACTIVE_END_FLAG to zero.

IRQ Control (0x201F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	IRQ_MODE	IRQ_POL	IRQ_EN
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_MODE	2	Controls the drive mode of the IRQ output.	0: Open-drain output (an external pull-up resistor is required) 1: CMOS push-pull output
IRQ_POL	1	Controls the IRQ output assert polarity.	
IRQ_EN	0	Enables the IRQ output.	0: IRQ output is disabled and is Hi-Z 1: IRQ output is enabled and controlled by the interrupt controller

Thermal Warning Threshhold (0x2020)

BIT	7	6	5	4	3	2	1	0
Field	–	–	THERMWARN_THRESH[5:0]					
Reset	–	–	0x14					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
THERMWARN_THRESH	5:0	Sets the thermal-warning threshold temperature.	0x00: 100°C 0x01: 101°C 0x02: 102°C ...: ... 0x30: 148°C 0x31: 149°C 0x32-0x3F: 150°C

Thermal Shutdown Threshold (0x2021)

BIT	7	6	5	4	3	2	1	0
Field	–	–	THERMSHDN_THRESH[5:0]					
Reset	–	–	0x32					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_THRESH	5:0	Sets the thermal-shutdown threshold temperature.	0x00: 100°C 0x01: 101°C 0x02: 102°C ...: ... 0x30: 148°C 0x31: 149°C 0x32 to 0x3F: 150°C

Thermal Hysteresis (0x2022)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	THERM_HYST[1:0]	
Reset	–	–	–	–	–	–	0x2	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
THERM_HYST	1:0	Controls the amount of hysteresis applied to the thermal threshold measurements.	0x0: 2°C 0x1: 5°C 0x2: 7°C 0x3: 10°C

Thermal Foldback Settings (0x2023)

BIT	7	6	5	4	3	2	1	0
Field	–	–	THERMFB_HOLD[1:0]		THERMFB_RLS[1:0]		THERMFB_SLOPE[1:0]	
Reset	–	–	0x3		0x0		0x0	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
THERMFB_HOLD	5:4	The thermal foldback hold time controls how long the device temperature must remain below the configured thermal threshold hysteresis before thermal foldback release begins.	0x0: 0ms 0x1: 20ms 0x2: 40ms 0x3: 80ms
THERMFB_RLS	3:2	This sets the release rate of the thermal foldback attenuation.	0x0: 3ms/dB 0x1: 10ms/dB 0x2: 100ms/dB 0x3: 300ms/dB
THERMFB_SLOPE	1:0	This sets the slope of the thermal foldback attenuation.	00: 0.5 dB/°C 01: 1.0 dB/°C 10: 2.0 dB/°C 11: Reserved

Thermal Foldback Enable (0x2027)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	THERMFB_EN
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
THERMFB_EN	0	Enables thermal foldback.	0: Thermal foldback disabled 1: Thermal foldback enabled

Noise Gate Control (0x2030)

BIT	7	6	5	4	3	2	1	0
Field	NG_UNMUTE_THRESH[3:0]				NG_MUTE_THRESH[3:0]			
Reset	0x3				0x2			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
NG_UNMUTE_THRESH	7:4	Sets the threshold (number of LSBs toggling) at which the noise gate block deactivates.	0x0: 1 LSB 0x1: 2 LSBs 0x2: 3 LSBs 0x3: 4 LSBs 0x4: 5 LSBs 0x5: 6 LSBs 0x6: 7 LSBs 0x7: 8 LSBs 0x8: 9 LSBs 0x9: 10 LSBs 0xA to 0xF: Reserved
NG_MUTE_THRESH	3:0	Sets the threshold (number of LSBs toggling) at which the noise gate block is activated.	0x0: 1 LSB 0x1: 2 LSBs 0x2: 3 LSBs 0x3: 4 LSBs 0x4: 5 LSBs 0x5: 6 LSBs 0x6: 7 LSBs 0x7: 8 LSBs 0x8: 9 LSBs 0x9: 10 LSBs 0xA to 0xF: Reserved

Noise Gate Enables (0x2033)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	NOISEGATE_EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
NOISEGATE_EN	0	Enables the noise gate.	0: Noise gate disabled. 1: Noise gate enabled.

Clock Monitor Control (0x2038)

BIT	7	6	5	4	3	2	1	0
Field	–	CMON_BSELTOL[2:0]			CMON_ERRTOL[2:0]			CMON_AUTORESTART_EN
Reset	–	0b0			0x0			0x0
Access Type	–	Write, Read			Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CMON_BSELTOL	6:4	The number of frames of incorrect or correct clock ratio (BCLKs per LRCLK) needed to trigger or recover from a framing error.	0x0: Trigger after 1 incorrect LRCLK frame, recover after 1 correct LRCLK frame. 0x1: Trigger after 2 incorrect LRCLK frames, recover after 16 correct LRCLK frames. 0x2: Trigger after 3 incorrect LRCLK frames, recover after 24 correct LRCLK frame. 0x3: Trigger after 4 incorrect LRCLK frames, recover after 32 correct LRCLK frames. 0x4: Trigger after 5 incorrect LRCLK frames, recover after 40 correct LRCLK frames. 0x5: Trigger after 6 incorrect LRCLK frames, recover after 48 correct LRCLK frames. 0x6: Trigger after 7 incorrect LRCLK frames, recover after 56 correct LRCLK frames. 0x7: Trigger after 8 incorrect LRCLK frames, recover after 64 correct LRCLK frames.
CMON_ERRTOL	3:1	Selects the number of incorrect or correct LRCLK periods needed to trigger or recover from a frame clock rate error.	0x0: Trigger after 1 incorrect LRCLK frame, recover after 1 correct LRCLK frame. 0x1: Trigger after 2 incorrect LRCLK frames, recover after 16 correct LRCLK frames. 0x2: Trigger after 3 incorrect LRCLK frames, recover after 24 correct LRCLK frame. 0x3: Trigger after 4 incorrect LRCLK frames, recover after 32 correct LRCLK frames. 0x4: Trigger after 5 incorrect LRCLK frames, recover after 40 correct LRCLK frames. 0x5: Trigger after 6 incorrect LRCLK frames, recover after 48 correct LRCLK frames. 0x6: Trigger after 7 incorrect LRCLK frames, recover after 56 correct LRCLK frames. 0x7: Trigger after 8 incorrect LRCLK frames, recover after 64 correct LRCLK frames.
CMON_AUTORESTART_EN	0	Controls whether or not the device automatically resumes playback when the clocks become valid after the device is disabled due to a clock monitor error.	0: Device does not automatically restart after valid clocks are reapplied. 1: Device automatically restarts after valid clocks are reapplied.

Data Monitor Control (0x2039)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DMON_MAG_THRES[1:0]		DMON_STUCK_THRES[1:0]		DMON_DURATION[1:0]	
Reset	–	–	0x0		0x0		0x0	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DMON_MAG_THRES	5:4	Sets the data magnitude error threshold that the input PCM amplitude level is compared against. If the input signal is above this threshold for longer than the DMON_DURATION, data monitor error is asserted.	0x0: -30.1030dB (5 bits) 0x1: -24.0824dB (4 bits) 0x2: -18.0618dB (3 bits) 0x3: -12.0412dB (2 bits)

BITFIELD	BITS	DESCRIPTION	DECODE
DMON_STUCK_THRES	3:2	Sets the data stuck error threshold that the input PCM amplitude level is compared against. If the input signal is stuck at the same value above this threshold for longer than the DMON_DURATION, data monitor error is asserted.	0x0: 15 bits (-90.3090 dBFS) 0x1: 13 bits (-78.2678 dBFS) 0x2: 11 bits (-66.2266 dBFS) 0x3: 9 bits (-54.1854 dBFS)
DMON_DURATION	1:0	Sets the time duration over which the data monitor must consecutively detect erroneous input PCM data before asserting a data monitor error.	0x0: 64ms 0x1: 256ms 0x2: 1024ms 0x3: 4096ms

Enable Controls (0x203F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPKMON_EN	DMON_MAG_EN	DMON_STUCK_EN	CMON_EN
Reset	–	–	–	–	0x1	0x1	0x1	0x1
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPKMON_EN	3	Enable speaker protection monitor.	0x0: Disable 0x1: Enable
DMON_MAG_EN	2	Enables the data monitor circuit to monitor PCM input data for large magnitude (DC) audio.	0: Data magnitude check disabled. 1: Data magnitude check enabled.
DMON_STUCK_EN	1	Enables the data monitor circuit to monitor PCM input for stuck data.	0: Data stuck monitor disabled. 1: Data stuck monitor enabled.
CMON_EN	0	Enables the clock monitor.	0: Clock monitor disabled. 1: Clock monitor enabled.

Pin Config (0x2040)

BIT	7	6	5	4	3	2	1	0
Field	LV_EN_DRV[1:0]		ICC_DRV[1:0]		IRQ_DRV[1:0]		DOUT_DRV[1:0]	
Reset	0x1		0x1		0x1		0x1	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
LV_EN_DRV	7:6	Configures the output drive strength of LV_EN.	0x0: Reduced drive mode 0x1: Normal drive mode 0x2: High drive mode 0x3: Maximum drive mode
ICC_DRV	5:4	Configures the output drive strength of ICC.	00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Maximum drive mode
IRQ_DRV	3:2	Configures the output drive strength of IRQ.	00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Maximum drive mode

BITFIELD	BITS	DESCRIPTION	DECODE
DOUT_DRV	1:0	Configures the output drive strength of DOUT.	00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Maximum drive mode

PCM Mode Config (0x2041)

BIT	7	6	5	4	3	2	1	0
Field	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]			PCM_TX_INTERLEAVE	PCM_CHANSEL	PCM_TX_EXTRA_HIZ
Reset	0x3		0x0			0x0	0b0	0b0
Access Type	Write, Read		Write, Read			Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_CHANSZ	7:6	Configures the PCM data word size for each channel.	00: Reserved 01: 16-bit 10: 24-bit 11: 32-bit
PCM_FORMAT	5:3	Selects the PCM data format.	0x0: I^2S Mode 0x1: Left-justified 0x2: Reserved 0x3: TDM Mode 0 (0 BCLK delay from LRCLK) 0x4: TDM Mode 1 (1 BCLK delay from LRCLK) 0x5: TDM Mode 2 (2 BCLK delay from LRCLK) 0x6 to 0x7: Reserved
PCM_TX_INTERLEAVE	2	Controls whether or not I/V sense data assigned to the same channel is frame interleaved on the PCM data output (DOUT).	0: Disable interleave mode. 1: Enable interleave mode.
PCM_CHANSEL	1	Selects which LRCK edge starts a new frame (channel 0 or slot 0).	0: I^2S and LJ mode: Falling LRCLK edge starts a new frame. In TDM modes: Rising LRCLK edge starts a new frame. 1: In I^2S and LJ mode: Rising LRCLK edge starts a new frame. In TDM modes: Falling LRCLK edge starts a new frame.
PCM_TX_EXTRA_HIZ	0	Select whether DOUT is driven to zero or Hi-Z during extra BCLK cycles.	0: Drive DOUT to zero for extra BCLK cycles 1: Drive DOUT to Hi-Z for extra BCLK cycles

PCM Clock Setup (0x2042)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PCM_BCLKEDGE	PCM_BSEL[3:0]			
Reset	–	–	–	0b0	0x4			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_BCLKEDGE	4	Selects the active BCLK edge.	0: Input data captured and output data valid on rising edge of BCLK. 1: Input data captured and output data valid on falling edge of BCLK.
PCM_BSEL	3:0	Selects the number of BCLKs per LRCLK expected by the PCM interface.	0x0 to 0x1: Reserved 0x2: 32 0x3: 48 0x4: 64 0x5: 96 0x6: 128 0x7: 192 0x8: 256 0x9: 384 0xA: 512 0xB: 320 0xC to 0xF: Reserved

PCM Sample Rate Setup 1 (0x2043)

BIT	7	6	5	4	3	2	1	0
Field	IVADC_SR[3:0]				PCM_SR[3:0]			
Reset	0x8				0x8			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
IVADC_SR	7:4	Sets the sample rate of the I/V sense ADC path.	0x0: 8kHz 0x1: 11.025kHz 0x2: 12kHz 0x3: 16kHz 0x4: 22.05kHz 0x5: 24kHz 0x6: 32kHz 0x7: 44.1kHz 0x8: 48kHz 0x9: 88.2kHz 0xA: 96kHz 0xB to 0xF: Reserved
PCM_SR	3:0	Sets the sample rate of the PCM interface. This corresponds to the expected LRCLK frequency.	0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: 16kHz 0x4: 22.05kHz 0x5: 24kHz 0x6: 32kHz 0x7: 44.1kHz 0x8: 48kHz 0x9: 88.2kHz 0xA: 96kHz 0xB to 0xF: Reserved

PCM RX Source (0x2044)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PCM_DAC_SOURCE[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_DAC_SOURCE	3:0	Selects the PCM data input channel that is routed to the speaker amplifier path.	0x0: PCM Input Channel 0 0x1: PCM Input Channel 1 0x2: PCM Input Channel 2 ...: ... 0xE: PCM Input Channel 14 0xF: PCM Input Channel 15

PCM TX Control 1 (0x2045)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_VMON_SLOT[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_VMON_SLOT	5:0	VMON Data Output Slot Select. VMON data requires 2 slots. In non-TDM mode only, slot 0 and slot 1 are valid.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 2 (0x2046)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_IMON_SLOT[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_IMON_SLOT	5:0	IMON Data Output Slot Select. IMON data requires two slots. In non-TDM mode only, Slot 0 and Slot 1 are valid.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 3 (0x2047)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_PVDD_SLOT[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_PVDD_SLOT	5:0	PVDD Data (ADC) Output Slot Select. PVDD data requires two slots.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 4 (0x2048)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_VBAT_SLOT[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_VBAT_SLOT	5:0	VBAT Data (ADC) Output Slot Select. VBAT data requires two slots.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 5 (0x2049)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_DHT_ATN_SLOT[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_DHT_ATN_SLOT	5:0	DHT Attenuation Data Output Slot Select. DHT attenuation data requires two slots.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 6 (0x204A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_STATUS_SLOT[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_STATUS_SLOT	5:0	Chip Satus Byte Data Output Slot Select.	0x00: Slot 00 0x01: Slot 01 0x02 to 0x3D: .... 0x3E: SLOT 62 0x3F: SLOT 63

PCM TX Control 7 (0x204B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_DSP_MONITOR_SLOT[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_DSP_MONITOR_SLOT	5:0	DSP Monitor Data Output Slot Select. DSP montior data requires 4 slots.	0x0: Slot 00/01/02/03 0x1: Slot 01/02/03/04 0x2: Slot 02/03/04/05 0x3 to 0x3B: .... 0x3C: Slot 60/61/62/63 0x3D: Reserved 0x3E: Reserved 0x3F: Reserved

PCM Tx HiZ Control 1 (0x204C)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[63:56]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	Configures the unused PCM data output slots to transmit either Hi-Z or 0.	Value: Decode 0: Output 0 on idle slots from 63 to 56 1: Output Hi-Z on slots from 63 to 56

PCM Tx HiZ Control 2 (0x204D)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[55:48]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	Configures the unused PCM slots to set them to Hi-Z or 0.	0: Output 0 on idle slots from 55 to 48 1: Output Hi-Z on slots from 55 to 48

PCM Tx HiZ Control 3 (0x204E)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[47:40]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	Configures the unused PCM slots to set them all to Hi-Z or 0.	0: Output 0 on idle slots from 47 to 40 1: Output Hi-Z on slots from 47 to 40

PCM Tx HiZ Control 4 (0x204F)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[39:32]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	Configures the unused PCM slots to set them all to Hi-Z or 0.	0: Output 0 on idle slots from 39 to 32 1: Output Hi-Z on slots from 39 to 32

PCM Tx HiZ Control 5 (0x2050)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[31:24]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	Configures the unused PCM slots to set them all to Hi-Z or 0.	0: Output 0 on slots from 31 to 24 1: Output Hi-Z on idle slots from 31 to 24

PCM Tx HiZ Control6 (0x2051)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[23:16]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	Configures the unused PCM slots to set them all to Hi-Z or 0.	0: Output 0 on idle slots from 23 to 16 1: Output Hi-Z on slots from 23 to 16

PCM Tx HiZ Control 7 (0x2052)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[15:8]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	Configures the unused PCM slots to set them all to Hi-Z or 0.	0: Output 0 on slots from 15 to 8 1: Output Hi-Z on idle slots from 15 to 8

PCM Tx HiZ Control 8 (0x2053)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	Configures the unused PCM slots to set them all to Hi-Z or 0.	0: Output 0 on idle slots from 7 to 0 1: Output Hi-Z on slots from 7 to 0

PCM TX Source Enables (0x205D)

BIT	7	6	5	4	3	2	1	0
Field	–	PCM_STATUS_EN	PCM_DHT_ATN_EN	PCM_VBAT_EN	PCM_PVDD_EN	PCM_DSPMONITOR_EN	PCM_IMON_EN	PCM_VMON_EN
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_STATUS_EN	6	Enables transmit of the device status byte on the assigned data output (DOUT) slot. This output data can be transmitted only in TDM mode.	0: Disable device status byte transmit 1: Enable device status byte transmit
PCM_DHT_ATN_EN	5	Enables transmit of the applied DHT attenuation on the assigned data output (DOUT) slot. This output data can be transmitted only in TDM mode.	0: Disable DHT attenuation data transmit 1: Enable DHT attenuation data transmit
PCM_VBAT_EN	4	Enables transmit of the measured VBAT supply voltage on the assigned data output (DOUT) slot. This output data can be transmitted only in TDM mode.	0: Disable VBAT supply voltage data transmit 1: Enable VBAT supply voltage data transmit

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_PVDD_EN	3	Enables transmit of the measured PVDD supply voltage on the assigned data output (DOUT) slot. This output data can be transmitted only in TDM mode.	0: Disable PVDD supply voltage data transmit 1: Enable PVDD supply voltage data transmit
PCM_DSPMONITOR_EN	2	Enables transmit of the playback path DSP output data on the assigned data output (DOUT) slot.	0: Disable playback path data transmit 1: Enable playback path data transmit
PCM_IMON_EN	1	Enables transmit of the current sense output data on the assigned data output (DOUT) slot.	0: Disable current sense data transmit 1: Enable current sense data transmit
PCM_VMON_EN	0	Enables transmit of the voltage sense output data on the assigned data output (DOUT) slot.	0: Disable voltage sense data transmit 1: Enable voltage sense data transmit

PCM Rx Enables (0x205E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PCM_RX_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_RX_EN	0	Enables the data input (DIN) of the PCM interface.	0: PCM data input disabled 1: PCM data input enabled

PCM Tx Enables (0x205F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PCM_TX_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PCM_TX_EN	0	Enables the data output (DOUT) of the PCM interface.	0: PCM data output disabled 1: PCM data output enabled

ICC Rx Enables A (0x2070)

BIT	7	6	5	4	3	2	1	0
Field	ICC_RX_CH7_EN	ICC_RX_CH6_EN	ICC_RX_CH5_EN	ICC_RX_CH4_EN	ICC_RX_CH3_EN	ICC_RX_CH2_EN	ICC_RX_CH1_EN	ICC_RX_CH0_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ICC_RX_CH7_EN	7	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 7 is disabled. 1: ICC receive channel 7 is enabled.

BITFIELD	BITS	DESCRIPTION	DECODE
ICC_RX_CH 6_EN	6	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 6 is disabled. 1: ICC receive channel 6 is enabled.
ICC_RX_CH 5_EN	5	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 5 is disabled. 1: ICC receive channel 5 is enabled.
ICC_RX_CH 4_EN	4	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 4 is disabled. 1: ICC receive channel 4 is enabled.
ICC_RX_CH 3_EN	3	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 3 is disabled. 1: ICC receive channel 3 is enabled.
ICC_RX_CH 2_EN	2	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 2 is disabled. 1: ICC receive channel 2 is enabled.
ICC_RX_CH 1_EN	1	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 1 is disabled. 1: ICC receive channel 1 is enabled.
ICC_RX_CH 0_EN	0	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 0 is disabled. 1: ICC receive channel 0 is enabled.

ICC Rx Enables B (0x2071)

BIT	7	6	5	4	3	2	1	0
Field	ICC_RX_CH15_EN	ICC_RX_CH14_EN	ICC_RX_CH13_EN	ICC_RX_CH12_EN	ICC_RX_CH11_EN	ICC_RX_CH10_EN	ICC_RX_CH9_EN	ICC_RX_CH8_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ICC_RX_CH 15_EN	7	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 15 is disabled 1: ICC receive channel 15 is enabled
ICC_RX_CH 14_EN	6	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 14 is disabled 1: ICC receive channel 14 is enabled
ICC_RX_CH 13_EN	5	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 13 is disabled 1: ICC receive channel 13 is enabled
ICC_RX_CH 12_EN	4	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 12 is disabled 1: ICC receive channel 12 is enabled
ICC_RX_CH 11_EN	3	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 11 is disabled 1: ICC receive channel 11 is enabled
ICC_RX_CH 10_EN	2	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 10 is disabled 1: ICC receive channel 10 is enabled
ICC_RX_CH 9_EN	1	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 9 is disabled 1: ICC receive channel 9 is enabled
ICC_RX_CH 8_EN	0	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 8 is disabled 1: ICC receive channel 8 is enabled

ICC Tx Control (0x2072)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ICC_DATA_SEL	ICC_TX_DEST[3:0]			
Reset	–	–	–	0x0	0x0			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ICC_DATA_SEL	4	Select whether the ICC pin transmits DHT or thermal foldback data when PCM data word size (data width) is only 16-bits. This has no effect when the data word size is 24- or 32-bits.	0: ICC transmits DHT data. 1: ICC transmits thernmal foldback data.
ICC_TX_DEST	3:0	Selects the device transmit channel for ICC data.	0x0: ICC Channel 0 0x1: ICC Channel 1 ....: ... 0xE: ICC Channel 14 0xF: ICC Channel 15

ICC Enables (0x207F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	ICC_LINK_EN	ICC_TX_EN
Reset	–	–	–	–	–	–	0b0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ICC_LINK_EN	1	Enables ICC link between devices.	0: ICC thermal link disabled 1: ICC thermal link enabled
ICC_TX_EN	0	Select whether the ICC pin transmitter is enabled/disabled.	0: ICC transmit disabled 1: ICC transmit enabled

Tone Generator and DC Config (0x2083)

BIT	7	6	5	4	3	2	1	0
Field	–	–	TONE_AMPLITUDE[1:0]		TONE_CONFIG[3:0]			
Reset	–	–	0x0		0x4			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TONE_AMPLITUDE	5:4	Sets the sine wave amplitude. This register is not used when programming the tone generator to output DC signals.	0x0: -6dBFS 0x1: -4.8dBFS 0x2: 0dBFS 0x3: Reserved
TONE_CONFIG	3:0	Configures the output of the tone generator. For signal output, the frequency is a division of the sample rate (f_S).	0x0: DC value programmed by TONE_DC[23:0] 0x1: DC = 0x0000 = 0 0x2: DC = +FullScale/2 0x3: DC = -FullScale/2 0x4: 1 KHz tone at all sample rates 0x5: fs/4 0x6: fs/6 0xE to 0xF: Reserved

Tone Generator DC Level 1 (0x2084)

BIT	7	6	5	4	3	2	1	0
Field	TONE_DC[23:16]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TONE_DC	7:0	Sets the tone generator DC output level as a signed binary relative to full-scale.

Tone Generator DC Level 2 (0x2085)

BIT	7	6	5	4	3	2	1	0
Field	TONE_DC[15:8]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TONE_DC	7:0	Sets the tone generator DC output level as a signed binary relative to full-scale.

Tone Generator DC Level 3 (0x2086)

BIT	7	6	5	4	3	2	1	0
Field	TONE_DC[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TONE_DC	7:0	Sets the tone generator DC output level as a signed binary relative to full-scale.

Tone Generator Clock Control (0x2087)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	REF_CLK_SEL
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
REF_CLK_SEL	0	Selects the tone generator clock source.	0: Internal OCS_CLK 1: External BCLK

Tone Generator Enable (0x208F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	TONE_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TONE_EN	0	Enables the tone generator. When enabled, it replaces the PCM interface as the input to the speaker amplifier path.	0: Tone generator disabled. 1: Tone generate enabled.

AMP volume control (0x2090)

BIT	7	6	5	4	3	2	1	0
Field	–	SPK_VOL[6:0]						
Reset	–	0x0						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_VOL	6:0	Sets the digital volume level of the speaker amplifier path.	0x00: 0dB 0x01: -0.5dB 0x02: -1.0dB ...: (-0.5dB steps) 0x7C: -62.0dB 0x7D: -62.5dB 0x7E: -63dB 0x7F: Mute

AMP Path Gain (0x2091)

BIT	7	6	5	4	3	2	1	0
Field	SPK_GAIN[3:0]				SPK_GAIN_MAX[3:0]			
Reset	0x0				0xB			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_GAIN	7:4	Sets the digital gain level of the speaker amplifier path.	0x00: 0dB 0x01: 0.5dB 0x02: 1.0dB 0x03: 1.5dB 0x04: 2.0dB 0x05: 2.5dB 0x06: 3.0dB 0x07: 3.5dB 0x08: 4.0dB 0x09: 5.0dB 0x0A: 6.0dB 0x0B to 0x0F: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_GAIN_MAX	3:0	Sets the maximum peak output voltage level (V_{MPO}) for the speaker path (no-load). Values in dB are relative to the baseline speaker path DAC full-scale output level of 3.68dBV.	0x00: 3.43V_P (4dB) 0x01: 3.84V_P (5dB) 0x02: 4.31V_P (6dB) 0x03: 4.84V_P (7dB) 0x04: 5.43V_P (8dB) 0x05: 6.09V_P (9dB) 0x06: 6.84V_P (10dB) 0x07: 7.67V_P (11dB) 0x08: 8.61V_P (12dB) 0x09: 9.66V_P (13dB) 0x0A: 10.84V_P (14dB) 0x0B: 12.16V_P (15dB) 0x0C: 13.64V_P (16dB) 0x0D: 15.31V_P (17dB) 0x0E: 17.17V_P (18dB) 0x0F: Reserved

AMP DSP Config (0x2092)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SPK_SAFE_EN	SPK_VOL_RMPDN_BYPASS	SPK_VOL_RMPUP_BYPASS	SPK_INVERT	SPK_DITH_EN	SPK_DCBLK_EN
Reset	–	–	0x1	0b0	0b0	0b0	0b1	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_SAFE_EN	5	The safe mode bit protects any speaker connected to the device on power up. When this setting is enabled, the amplifier output is set to -18dBFS or less.	0: Speaker safe mode disabled. 1: Speaker safe mode enabled.
SPK_VOL_RMPDN_BYPASS	4	Controls whether the speaker amplifier path volume is internally ramped down during shutdown and during volume changes.	0: Volume ramp enabled. 1: Volume ramp bypassed.
SPK_VOL_RMPUP_BYPASS	3	Controls whether the speaker amplifier path volume is internally ramped up during startup and during volume changes.	0: Volume ramp enabled. 1: Volume ramp bypassed.
SPK_INVERT	2	Inverts the speaker amplifier path output.	0: Output is normal. 1: Output is inverted.
SPK_DITH_EN	1	Selects whether or not dither is applied data in the speaker amplifier path.	0: Dither disabled. 1: Dither enabled.
SPK_DCBLK_EN	0	Controls the DC blocking filter in the speaker amplifier path.	0: DC blocking filter disabled. 1: DC blocking filter enabled.

SSM Configuration (0x2093)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPK_SSM_EN	SPK_SSM_MOD_INDEX[2:0]		
Reset	–	–	–	–	0x0	0x5		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_SSM_EN	3	Enables spread-spectrum clocking.	0: Spread-spectrum clocking is disabled. 1: Spread-spectrum clocking is enabled.
SPK_SSM_MOD_INDEX	2:0	Selects the modulation index for the Class-D amplifier spread-spectrum clocks. The modulation index can be varied as follows:	0x0: MMI 0x1: MMI * 5/6 0x2: MMI * 4/6 0x3: MMI * 3/6 0x4: MMI * 2/6 0x5: MMI * 1/6 0x6 to 0x7: Reserved

SPK Class DG Threshold (0x2094)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	SPK_DG_THRES[4:0]				
Reset	–	–	–	0x12				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_DG_THRES	4:0	Sets the DG mode fixed peak signal level threshold (active when SPK_DG_SEL = 0x0 or 0x2).	0x00: 3.8V 0x01: 3.7V 0x02: 3.6V 0x03 to 0x1D: ... (0.1V steps) 0x1E: 0.6V 0x1F: 0.7V

SPK Class DG Headroom (0x2095)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SPK_DG_SEL[1:0]		SPK_DG_HEADROOM[3:0]			
Reset	–	–	0x1		0x7			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_DG_SEL	5:4	Selects the method used for speaker amplifier DG mode operation.	0x0: Class-DG mode uses a fixed peak signal level threshold (SPK_DG_THRES). 0x1: Class-DG mode uses supply headroom relative to measured VBAT voltage (SPK_DG_HEADROOM). 0x2: Class-DG mode uses the lower of fixed peak signal level threshold (SPK_DG_THRES) and VBAT supply headroom (SPK_DG_HEADROOM). 0x3: Reserved
SPK_DG_HEADROOM	3:0	Sets the DG mode headroom relative to the measured V_{VBAT} supply level (active when SPK_DG_SEL = 0x1 or 0x2).	0x0: 0V 0x1: 0.25V 0x2: 0.5V 0x3 to 0xD: ... (0.25V steps) 0xE: 3.5V 0xF: 3.75V

SPK Class DG Hold Time (0x2096)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPK_DG_HOLD_TIME[3:0]			
Reset	–	–	–	–	0x7			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_DG_HOLD_TIME	3:0	Sets the speaker amplifier DG mode hold time. When the peak signal level falls below the DG mode threshold for longer than this time, VBAT is selected as the active amplifier supply.	0x0: 0.15ms 0x1: 0.25ms 0x2: 0.5ms 0x3: 1.0ms 0x4: 2.5ms 0x5: 5.0ms 0x6: 10ms 0x7: 20ms 0x8: 30ms 0x9: 40ms 0xA: 50ms 0xB: 125ms 0xC: 250ms 0xD: 500ms 0xE: 750ms 0xF: 1.0s

SPK Class DG Delay (0x2097)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SPK_DG_DELAY[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_DG_DELAY	5:0	Selects the speaker amplifier path signal delay for DG mode operation. Delays the audio output by N samples (N x f_S).	0x0: No Delay 0x1: Delay 1 sample 0x2: Delay 2 samples 0x3 to 0x1D: ... (1 sample step) 0x1E: Delay 30 samples 0x1F: Delay 31 samples

SPK Class DG Mode (0x2098)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SPK_MODE[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_MODE	1:0	Selects the speaker amplifier operating mode.	0x0: DG mode is enabled. 0x1: DG mode is disabled and amplifier is always supplied from PVDD pin. 0x2: DG mode is disabled and amplifier is supplied from VBAT pin when supply conditions are met. 0x3: Reserved

SPK Class DG VBAT Level (0x2099)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	VBATLOW_OK_LVL[2:0]		
Reset	–	–	–	–	–	0x3		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VBATLOW_OK_LVL	2:0	Sets the threshold for VBAT level below which the amplifier is forced to operate in PVDD mode only (i.e., the active amplifier supply is PVDD only).	0x0: 2.5V 0x1: 2.6V 0x2: 2.7V 0x3: 2.8V 0x4: 2.9V 0x5: 3.0V 0x6: Reserved 0x7: Reserved

SPK Edge Control 1 (0x209C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPK_SL_RATE_GMODE[3:0]			
Reset	–	–	–	–	0xA			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_SL_RATE_GMODE	3:0	These bits control the rise time PMOS power FET connected to the VBAT supply pin. This in effect controls the rise time at OUTx nodes	0000: Slowest rise time. 0001: Slower than default rise time. 1010: Default 1111: Faster than default rise time.

SPK Edge Control 2 (0x209D)

BIT	7	6	5	4	3	2	1	0
Field	SPK_SL_RATE_LS[3:0]				SPK_SL_RATE_HS[3:0]			
Reset	0xA				0xA			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_SL_RATE_LS	7:4	.These bits control the fall time of the NMOS power FET. This in effect controls fall time at OUTx nodes.	0000: Fastest Fall time. 0001: Faster fall time than default. 1010: Default fall time. 1111: Slower fall time than default.
SPK_SL_RATE_HS	3:0	These bits control the rise time PMOS power FET connected to the PVDD supply pin. This in effect controls rise time at OUTx nodes.	0000: Fastest rise time. 0001: Faster rise time than default. 1010: Default rise time. 1111: Slower rise time than default.

AMP enables (0x20AF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SPK_FB_EN	SPK_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_FB_EN	1	Enables PCM data output from the end of the speaker amplifier path DSP.	0: Speaker amplifier path DSP feedback disabled. 1: Speaker amplifier path DSP feedback enabled.
SPK_EN	0	Enables the speaker amplifier path.	0: Speaker amplifier is disabled 1: Speaker amplifier is enabled

Meas ADC Sample Rate (0x20B0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	MEAS_ADC_TEMP_SR[1:0]		MEAS_ADC_PVDD_SR[1:0]		MEAS_ADC_VBAT_SR[1:0]	
Reset	–	–	0x3		0x0		0x0	
Access Type	–	–	Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_TEMP_SR	5:4	Configures the sample rate of the thermal channel of the measurement ADC.	0x0: 300kHz 0x1: 150kHz 0x2: 75kHz 0x3: 37.5kHz
MEAS_ADC_PVDD_SR	3:2	Configures the sample rate of the PVDD channel of the measurement ADC.	00: 300kHz 01: 150kHz 10: 75kHz 11: 37.5kHz
MEAS_ADC_VBAT_SR	1:0	Configures the sample rate of the VBAT channel of the measurement ADC.	0x0: 300kHz 0x1: 150kHz 0x2: 75kHz 0x3: 37.5kHz

Meas ADC PVDD Config (0x20B1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEAS_ADC_PVDD_FILT_EN	MEAS_ADC_PVDD_FILT_COEFF[3:0]			
Reset	–	–	–	0x0	0x0			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_PVDD_FILT_EN	4	Controls whether filtering is applied to the PVDD channel output.	0: Filter is bypassed 1: Filter is applied
MEAS_ADC_PVDD_FILT_COEFF	3:0	Sets the PVDD channel lowpass filter bandwidth.	Value: Measurement ADC channel sample rate 0x5 to 0xF: Reserved

Meas ADC VBAT Config (0x20B2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEAS_ADC_VBAT_FILT_EN	MEAS_ADC_VBAT_FILT_COEFF[3:0]			
Reset	–	–	–	0x0	0x00			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_VBAT_FILT_EN	4	Controls whether filtering is applied to the VBAT channel output.	0: Filter is bypassed 1: Filter is applied
MEAS_ADC_VBAT_FILT_COEFF	3:0	Sets the VBAT channel lowpass filter bandwidth.	Value: Measurement ADC channel sample rate 0x5 to 0xF: Reserved

Meas ADC Thermal Config (0x20B3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEAS_ADC_TEMP_FILT_EN	MEAS_ADC_TEMP_FILT_COEFF[3:0]			
Reset	–	–	–	0x0	0x00			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_TEMP_FILT_EN	4	Controls whether filtering is applied to the thermal channel output.	0: Filter is bypassed 1: Filter is applied
MEAS_ADC_TEMP_FILT_COEFF	3:0	Sets the thermal channel lowpass filter bandwidth.	Value: Measurement ADC channel sample rate 0x5 to 0xF: Reserved

Meas ADC Readback Control 1 (0x20B4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MEAS_ADC_THERM_RD_MODE	MEAS_ADC_VBAT_RD_MODE	MEAS_ADC_PVDD_RD_MODE
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_THERM_RD_MODE	2		0: Measurement ADC channel readback data is automatically updated. 1: Inititates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_VBAT_RD_MODE	1		0: Measurement ADC channel readback data is automatically updated. 1: Inititates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_PVDD_RD_MODE	0		0: Measurement ADC channel readback data is automatically updated. 1: Inititates a measurement and locks the result into the measurement ADC channel readback register.

Meas ADC Readback Control 2 (0x20B5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MEAS_ADC_THERM_RD_UPD	MEAS_ADC_VBAT_RD_UPD	MEAS_ADC_PVDD_RD_UPD
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write Only	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_THERM_RD_UPD	2	Write 1 to inititate a measurement and locks the result into the measurement ADC channel readback register.	0: No effect 1: Inititates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_VBAT_RD_UPD	1	Write 1 to inititate a measurement and locks the result into the measurement ADC channel readback register.	0: No effect 1: Inititates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_PVDD_RD_UPD	0	Write 1 to inititate a measurement and locks the result into the measurement ADC channel readback register.	0: No effect 1: Inititates a measurement and locks the result into the measurement ADC channel readback register.

Meas ADC PVDD Readback MSB (0x20B6)

BIT	7	6	5	4	3	2	1	0
Field	MEAS_ADC_PVDD_DATA[8:1]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MEAS_ADC_PVDD_DATA	7:0	Provides the measured PVDD value. To convert the 9-bit code into a real voltage, use the following: Measured V_{PVDD} (V) = 2.5V + MEAS_ADC_PVDD_DATA[8:0] x 0.0234375V

Meas ADC PVDD Readback LSB (0x20B7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_PVDD_DATA[0]
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
MEAS_ADC_PVDD_DATA	0	Provides the measured PVDD value. To convert the 9-bit code into a real voltage, use the following: Measured V_{PVDD} (V) = 2.5V + MEAS_ADC_PVDD_DATA[8:0] x 0.0234375V

Meas ADC VBAT Readback MSB (0x20B8)

BIT	7	6	5	4	3	2	1	0
Field	MEAS_ADC_VBAT_DATA[8:1]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MEAS_ADC_VBAT_DATA	7:0	Provides the measured VBAT value. To convert the 9-bit code into a real voltage, use the following: Measured VVBAT (V) = 2.5V + MEAS_ADC_VBAT_DATA[8:0] x 0.0234375V

Meas ADC VBAT Readback LSB (0x20B9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_VBAT_DATA[0]
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
MEAS_ADC_VBAT_DATA	0	Provides the measured VBAT value. To convert the 9-bit code into a real voltage, use the following: Measured VVBAT (V) = 2.5V + MEAS_ADC_VBAT_DATA[8:0] x 0.0234375V

Meas ADC Temp Readback MSB (0x20BA)

BIT	7	6	5	4	3	2	1	0
Field	MEAS_ADC_THERM_DATA[8:1]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
MEAS_ADC_THERM_DATA	7:0	Provides the measured temperature value. To convert the 9-bit code into a real temperature, use the following: Measured Temperature (°C) = (MEAS_ADC_THERM_DATA[8:0] x 1.0°C) - 167°C

Meas ADC Temp Readback LSB (0x20BB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_THERM_DATA[0]
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
MEAS_ADC_THERM_DATA	0	Provides the measured temperature value. To convert the 9-bit code into a real temperature, use the following: Measured Temperature (°C) = (MEAS_ADC_THERM_DATA[8:0] x 1.0°C) - 167°C

Meas ADC Lowest PVDD Readback MSB (0x20BC)

BIT	7	6	5	4	3	2	1	0
Field	LOWEST_PVDD_DATA[8:1]							
Reset	0xFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
LOWEST_PVDD_DATA	7:0	Provides the lowest measured PVDD value. To convert the 9-bit code into a real voltage, use the following: Measured V_{PVDD} (V) = 2.5V + MEAS_ADC_PVDD_DATA[8:0] x 0.0234375V

Meas ADC Lowest PVDD Readback LSB (0x20BD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOWEST_PVDD_DATA[0]
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Read, Ext

BITFIELD	BITS	DESCRIPTION
LOWEST_PVDD_DATA	0	Provides the lowest measured PVDD value. To convert the 9-bit code into a real voltage, use the following: Measured V_{PVDD} (V) = 2.5V + MEAS_ADC_PVDD_DATA[8:0] x 0.0234375V

Meas ADC Lowest VBAT Readback MSB (0x20BE)

BIT	7	6	5	4	3	2	1	0
Field	LOWEST_VBAT_DATA[8:1]							
Reset	0xFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
LOWEST_VBAT_DATA	7:0	Provides the measured VBAT value. To convert the 9-bit code into a real voltage, use the following: Measured V_{VBAT} (V) = 2.5V + MEAS_ADC_VBAT_DATA[8:0] x 0.0234375V

Meas ADC Lowest VBAT Readback LSB (0x20BF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOWEST_VBAT_DATA[0]
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Read, Ext

BITFIELD	BITS	DESCRIPTION
LOWEST_VBAT_DATA	0	Provides the measured VBAT value. To convert the 9-bit code into a real voltage, use the following: Measured VVBAT (V) = 2.5V + MEAS_ADC_VBAT_DATA[8:0] x 0.0234375V

Meas ADC Config (0x20C7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MEAS_ADC_VBAT_EN	MEAS_ADC_PVDD_EN
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEAS_ADC_VBAT_EN	1	Manually enables the measurement ADC VBAT channel.	0: Do not manually enable the measurement ADC channel (may be automatically enabled). 1: Manually force the measurement ADC channel to be enabled anytime the device is in the active state.
MEAS_ADC_PVDD_EN	0	Manually enables the measurement ADC PVDD channel.	0: Do not manually enable the measurement ADC channel (may be automatically enabled). 1: Manually force the measurement ADC channel to be enabled anytime the device is in the active state.

DHT Configuration 1 (0x20D0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_VROT_PNT[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_VROT_PNT	3:0	Sets the DRC rotation point.	0x0: 0dBFS 0x1: -1dBFS 0x2: -2dBFS 0x3: -3dBFS 0x4: -4dBFS 0x5: -5dBFS 0x6: -6dBFS 0x7: -8dBFS 0x8: -10dBFS 0x9: -12dBFS 0xA: -15dBFS 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

Limiter Configuration 1 (0x20D1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DHT_HR[4:0]				
Reset	–	–	–	0x8				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_HR	4:0	Selects the DHT supply headroom for the DRC and limiter functions.	0x0: -20% 0x1: -17.5% 0x2: -15% 0x3: -12.5% 0x4: -10% 0x5: -7.5% 0x6: -5.0% 0x7: -2.5% 0x8: 0% 0x9: +2.5% 0xA: +5.0% 0xB: +7.5% 0xC: +10% 0xD: +12.5% 0xE: +15% 0xF: +17.5% 010: +20%

Limiter Configuration 2 (0x20D2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DHT_LIM_THRESH[4:0]					DHT_LIM_MODE
Reset	–	–	0x0					0x0
Access Type	–	–	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_LIM_THRESH	5:1	Selects the fixed threshold level for signal level limiter mode (SLL). Has no effect in signal distortion limiter mode (SDL).	00000: 0dBFS 00001: -1dBFS 00010: -2dBFS ...: (-1dBFS steps) 01110: -14dBFS 01111: -15dBFS 10000 to 11111: Reserved
DHT_LIM_MODE	0	Selects whether the DHT limiter is in signal distortion or signal level limiter mode.	0: Signal distortion limiter mode where limiter threshold tracks supply. 1: Signal level limiter mode where limiter uses fixed thresholds.

DHT Configuration 2 (0x20D3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_MAX_ATN[3:0]			
Reset	–	–	–	–	0xF			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_MAX_ATN	3:0	Selects the maximum attenuation that can be applied to the audio signal by the DHT.	0x0: Reserved 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4: -4dB 0x5: -5dB 0x6: -6dB 0x7: -7dB 0x8: -8dB 0x9: -9dB 0xA: -10dB 0xB: -11dB 0xC: -12dB 0xD: -13dB 0xE: -14dB 0xF: -15dB

DHT Configuration 3 (0x20D4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_ATK_RATE[3:0]			
Reset	–	–	–	–	0x2			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_ATK_RATE	3:0	Selects the DHT attack rate.	0x0: 20µs/dB 0x1: 40µs/dB 0x2: 80µs/dB 0x3: 160µs/dB 0x4: 320µs/dB 0x5: 640µs/dB 0x6: 1.28ms/dB 0x7: 2.56ms/dB 0x8: 5.12ms/dB 0x9: 10.24ms/dB 0xA: 20.48ms/dB 0xB: 40.96ms/dB 0xC: 81.92ms/dB 0xD: 163.84ms/dB 0xE: Reserved 0xF: Reserved

DHT Configuration 4 (0x20D5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_RLS_RATE[3:0]			
Reset	–	–	–	–	0x4			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_RLS_RATE	3:0	Selects the DHT release rate.	0x0: 2ms/dB 0x1: 4ms/dB 0x2: 8ms/dB 0x3: 16ms/dB 0x4: 32ms/dB 0x5: 64ms/dB 0x6: 128ms/dB 0x7: 256ms/dB 0x8: 512ms/dB 0x9: 1.024s/dB 0xA: 2.048s/dB 0xB: 4.096s/dB 0xC: 8.192s/dB 0xD: 16.384s/dB 0xE: Reserved 0xF: Reserved

DHT Supply Hysteresis Configuration (0x20D6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_SUPPLY_HYST[2:0]			DHT_SUPPLY_HYST_EN
Reset	–	–	–	–	0x3			0x1
Access Type	–	–	–	–	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_SUPPLY_HYST	3:1	Selects the supply hysteresis for DHT attenuation release when supply increases.	0x0: 1 LSB 0x1: 2 LSB 0x2: 3 LSB 0x3: 4 LSB 0x4: 6 LSB 0x5: 8 LSB 0x6: 10 LSB 0x7: 12 LSB 0x8: Reserved
DHT_SUPPLY_HYST_EN	0	Select whether PVDD DHT hysteresis is enabled or disabled.	0: PVDD hysteresis is disabled. 1: PVDD hysteresis is enabled.

DHT Enable (0x20DF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DHT_EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DHT_EN	0	Select whether DHT is enabled or disabled.	0: DHT is disabled 1: DHT is enabled

Measurement DSP Config (0x20E0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	IVADC_DITH_EN	IVADC_I_DCBLK_EN	IVADC_V_DCBLK_EN
Reset	–	–	–	–	–	0b1	0b0	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IVADC_DITH_EN	2	Select whether or not dither is applied to the I/V sense ADC path.	0: Dither disabled. 1: Dither enabled.
IVADC_I_DCBLK_EN	1	Enables the DC blocking filter in the current sense ADC path.	0: DC blocker disabled. 1: DC blocker enabled.
IVADC_V_DCBLK_EN	0	Enables the DC blocking filter in the voltage sense ADC path.	0: DC blocker disabled. 1: DC blocker enabled.

Measurement enables (0x20E7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	IVADC_I_EN	IVADC_V_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IVADC_I_EN	1	Enables the speaker current sense ADC path. When this bit is set to 1, the current sense ADC path is powered up if the device is in the active state (EN = 1).	0: Speaker current sense ADC path disabled. 1: Speaker current sense ADC path enabled.
IVADC_V_EN	0	Enables the speaker voltage sense ADC path. When this bit is set to 1, the voltage sense ADC path is powered up if the device is in the active state (EN = 1).	0: Speaker voltage sense ADC path disabled. 1: Speaker voltage sense ADC path enabled.

Auto-Restart Behavior (0x20FE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OVC_AUTORESTART_EN	THERM_AUTORESTART_EN	VBAT_AUTORESTART_EN	PVDD_AUTORESTART_EN
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OVC_AUTORESTART_EN	3	Controls whether or not the speaker amplifier is automatically reenabled after an overcurrent fault condition.	0: Overcurrent recovery is in manual mode 1: Overcurrent recovery is in auto mode

BITFIELD	BITS	DESCRIPTION	DECODE
THERM_AUTORESTART_EN	2	Controls whether or not the device automatically returns to the active state when the die temperature recovers from thermal shutdown.	0: Thermal shutdown recovery is in manual mode. 1: Thermal shutdown recovery is in auto mode.
VBAT_AUTORESTART_EN	1	Controls whether or not the device automatically returns to the active state when VBAT recovers from UVLO event.	0: VBAT UVLO recovery is in manual mode. 1: VBAT UVLO recovery is in auto mode.
PVDD_AUTORESTART_EN	0	Controls whether or not the device automatically returns to the active state when PVDD recovers from UVLO event.	0: PVDD UVLO recovery is in manual mode. 1: PVDD UVLO recovery is in auto mode.

Global Enable (0x20FF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
EN	0	Disable or enable all blocks and reset all logic except the I^2C interface and control registers.	0: Device in software shutdown. 1: Device enabled.

Revision ID (0x21FF)

BIT	7	6	5	4	3	2	1	0
Field	REV_ID[7:0]							
Reset	0x41							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
REV_ID	7:0	Revision of the device. Updated at every device revision.	0x41: Device revision

Applications Information

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Use at least four PCB layers, and add thermal vias to the ground/power plane close to the device to ensure good thermal performance and high-end output power. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal. Ground the power signals and the analog signals of the IC separately at the system ground plane, to prevent switching interference from corrupting sensitive analog signals. Place the recommended supply decoupling capacitors as close as possible to the IC. The PVDD to PGND connection must be kept short and should have minimum trace length and loop area to ensure optimal performance. Use wide, low-resistance output, supply and ground traces. As load impedance decreases, the current drawn from the device outputs increase. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the speaker output to a 4Ω load through a 100mΩ trace, 49mW is consumed in the trace. If power is delivered through a 10mΩ trace, only 5mW is consumed in the trace. Wide output, supply, and ground traces also improve the power dissipation of the device. The device is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on the top and bottom PCB planes. It is advisable to follow the layout of the MAX98395 EV kit as closely as possible in the application. Thermal and performance measurements shown in this data sheet were measured with a 6-layer board with 2 signal layers and 4 ground layers. As a result, the EV kit performance is likely better than what can be achieved with a JEDEC standard board.

Recommended External Components

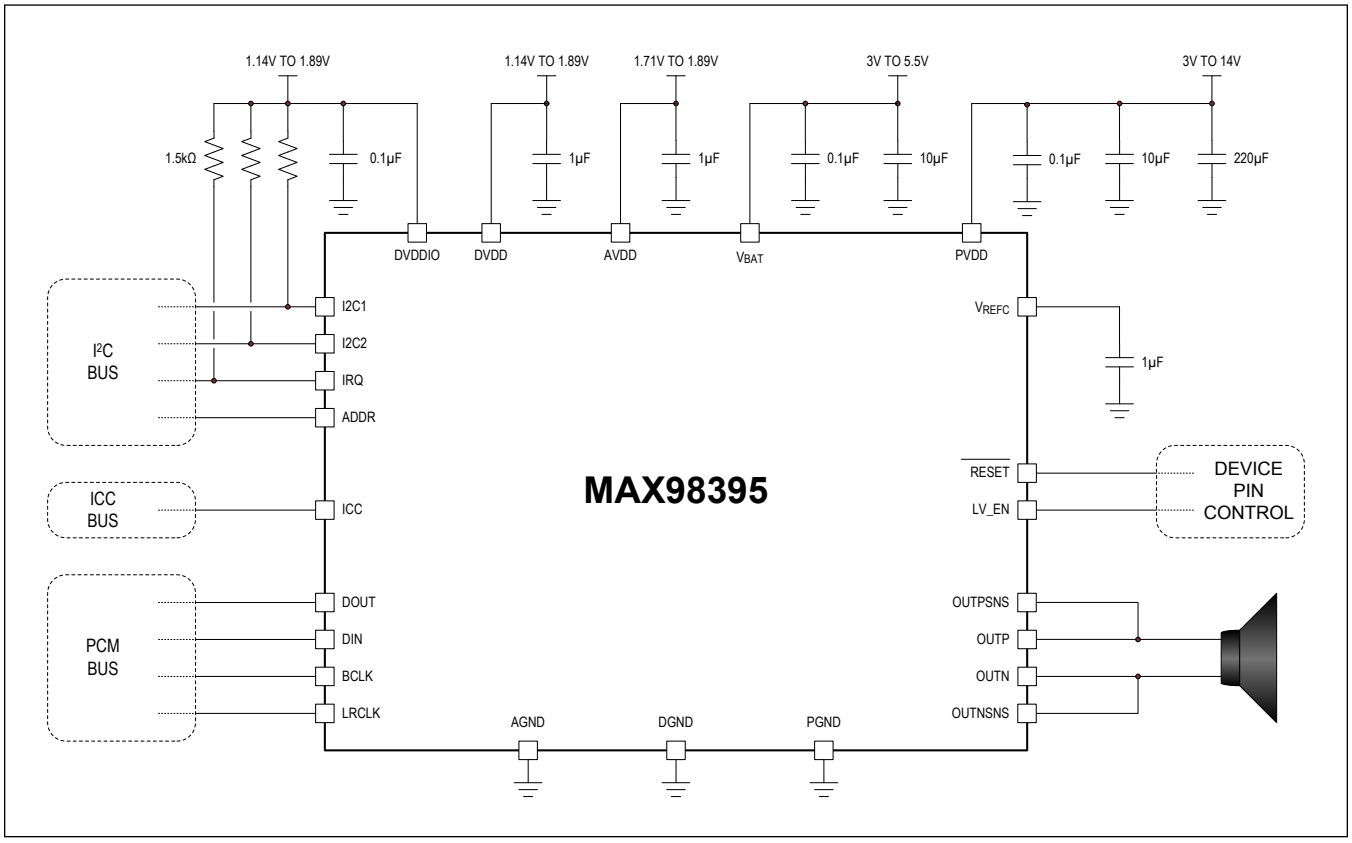
Table 11 shows the recommended external components. See the *Typical Application Circuits* for more details.

Table 11. Component List

BUMP	VALUE	SIZE	VOLTAGE RATING (V)	DIELECTRIC
PVDD	220µF ± 20%	—	35	Alum-Elec
PVDD	10µF ± 20%	0603	25	X5R
PVDD	0.1µF ± 10%	0402	25	X5R
VBAT	1µF	0201	16	X5R
VBAT	10µF	0603	25	X5R
VREFC	1µF ± 20%	0201	6.3	X5R
DVDD	1µF ± 20%	0201	6.3	X5R
DVDDIO	1µF ± 20%	0201	6.3	X5R
AVDD	1µF ± 20%	0201	6.3	X5R

Typical Application Circuits

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX98395EWI+	-40°C to +85°C	28 WLP
MAX98395EWI+ T	-40°C to +85°C	28 WLP

+Denotes a lead(Pb)-free/RoHA-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/19	Initial release	—