

74AVC16374

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

Rev. 3 — 16 August 2013

Product data sheet

1. General description

The 74AVC16374 is a 16-bit edge triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. The 74AVC16374 consist of 2 sections of 8 edge-triggered flip-flops. A clock input (CP) and an output enable ($\overline{OE}$) are provided per 8-bit section.

The 74AVC16374 is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power-up or power-down, $\overline{nOE}$ should be tied to VCC through a pull-up resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient (see [Figure 5](#) and [Figure 6](#)).

2. Features and benefits

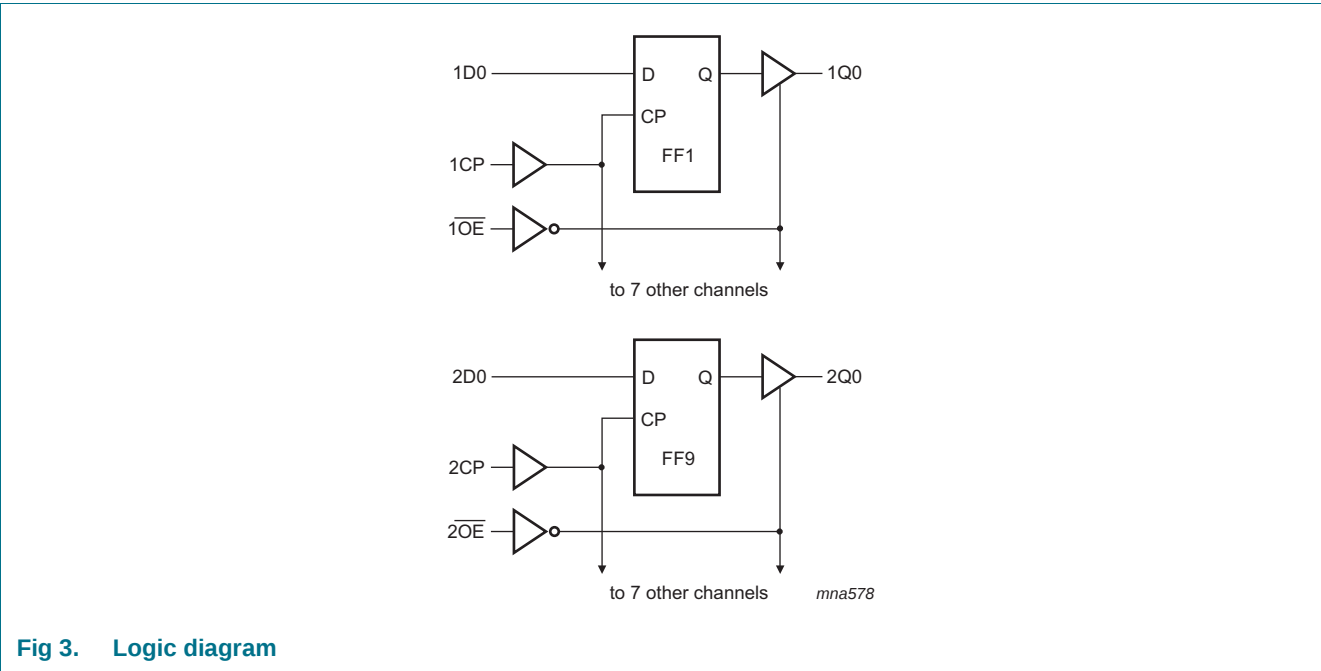
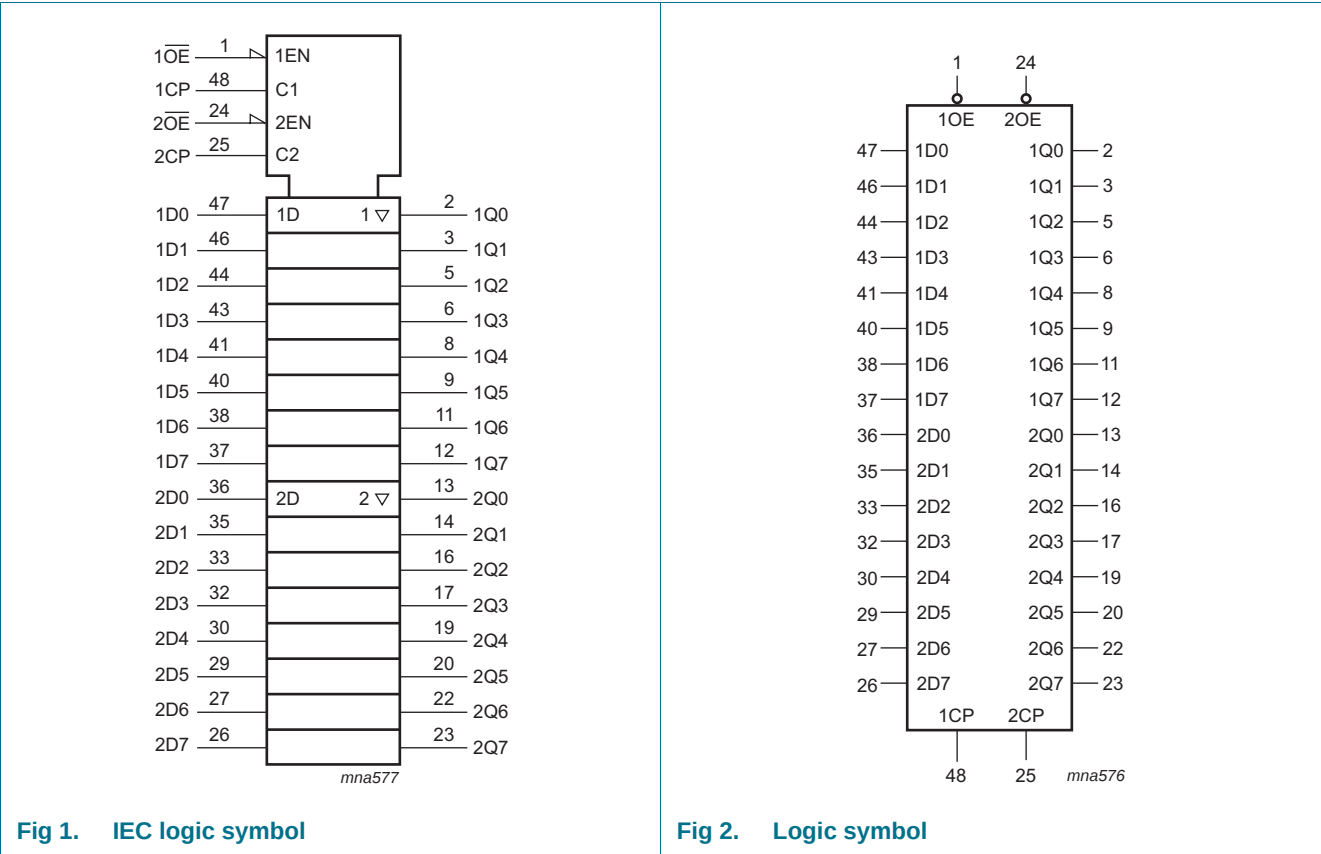
- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standards:
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8-1A (2.7 V to 3.6 V)
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Dynamic Controlled Output (DCO) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple V_{CC} and GND pins to minimize noise and ground bounce
- Supports Live Insertion

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC16374DGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram



5. Pinning information

5.1 Pinning

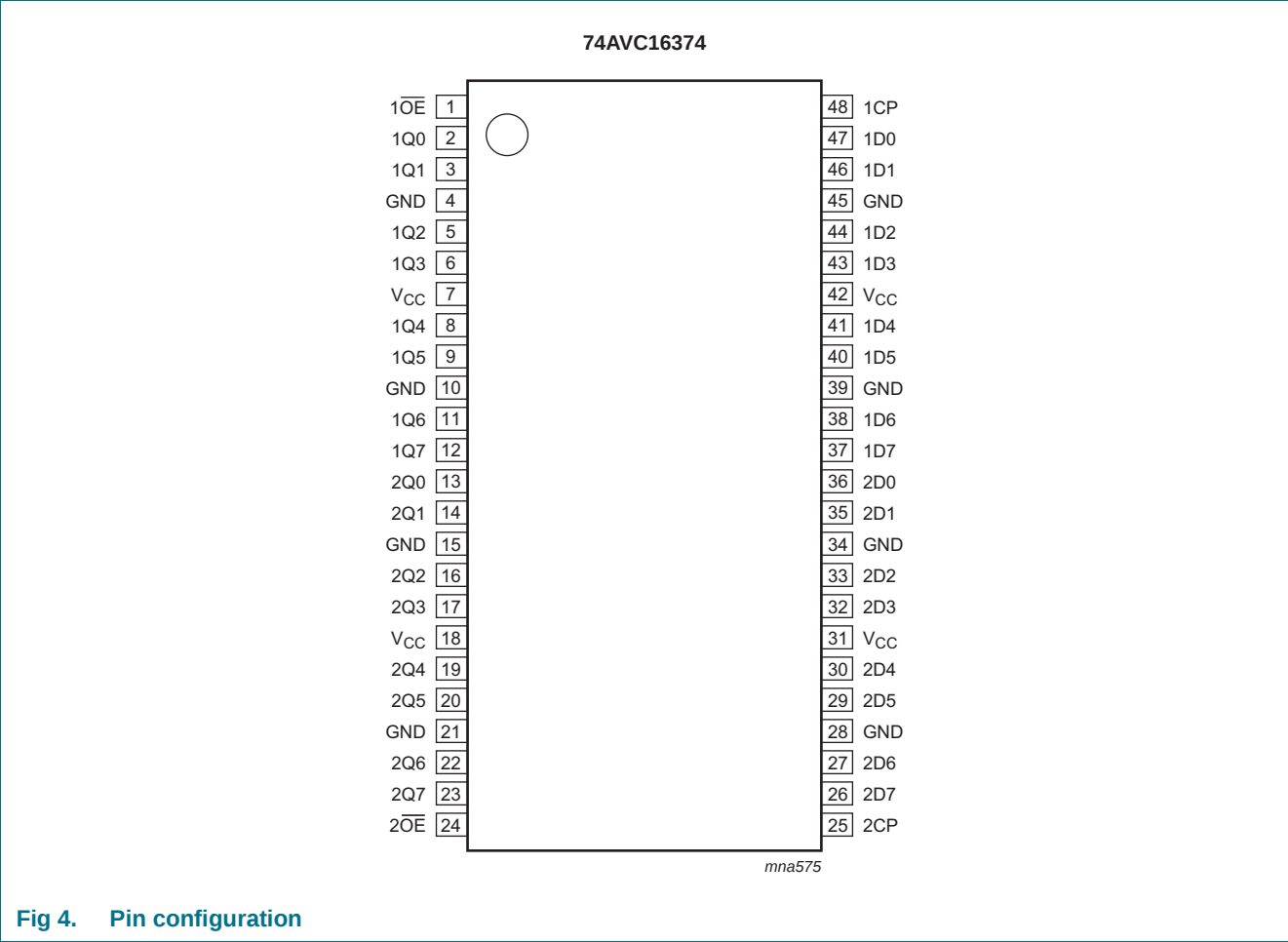


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1OE}$	1	output enable input (active LOW)
1Q0 to 1Q7	2, 3, 5, 6, 8, 9, 11, 12	3-state flip-flop outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	supply voltage
2Q0 to 2Q7	13, 14, 16, 17, 19, 20, 22, 23	3-state flip-flop outputs
$\overline{2OE}$	24	output enable input (active LOW)
2CP	25	clock input
2D0 to 2D7	36, 35, 33, 32, 30, 29, 27, 26	data input/output
1D0 to 1D7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
1CP	48	clock input

6. Functional description

Table 3. Function table^[1]

Operating modes	Inputs			Internal flip-flops	Outputs
	$\overline{nOE}$	nCp	nDn		nQn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

[1] H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high-impedance OFF-state

↑ = LOW-to-HIGH CP transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA
V_I	input voltage		[1] -0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	output HIGH or LOW	[1] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[1] -0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 60 °C, the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	according to JEDEC Low Voltage Standards	1.4	-	1.6	V
			1.65	-	1.95	V
			2.3	-	2.7	V
			3.0	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	3.6	V
V_O	output voltage	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	3.6	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.4$ V to 1.6 V	0	-	40	ns/V
		$V_{CC} = 1.65$ V to 2.3 V	0	-	30	ns/V
		$V_{CC} = 2.3$ V to 3.0 V	0	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	0	-	10	ns/V

9. Static characteristics

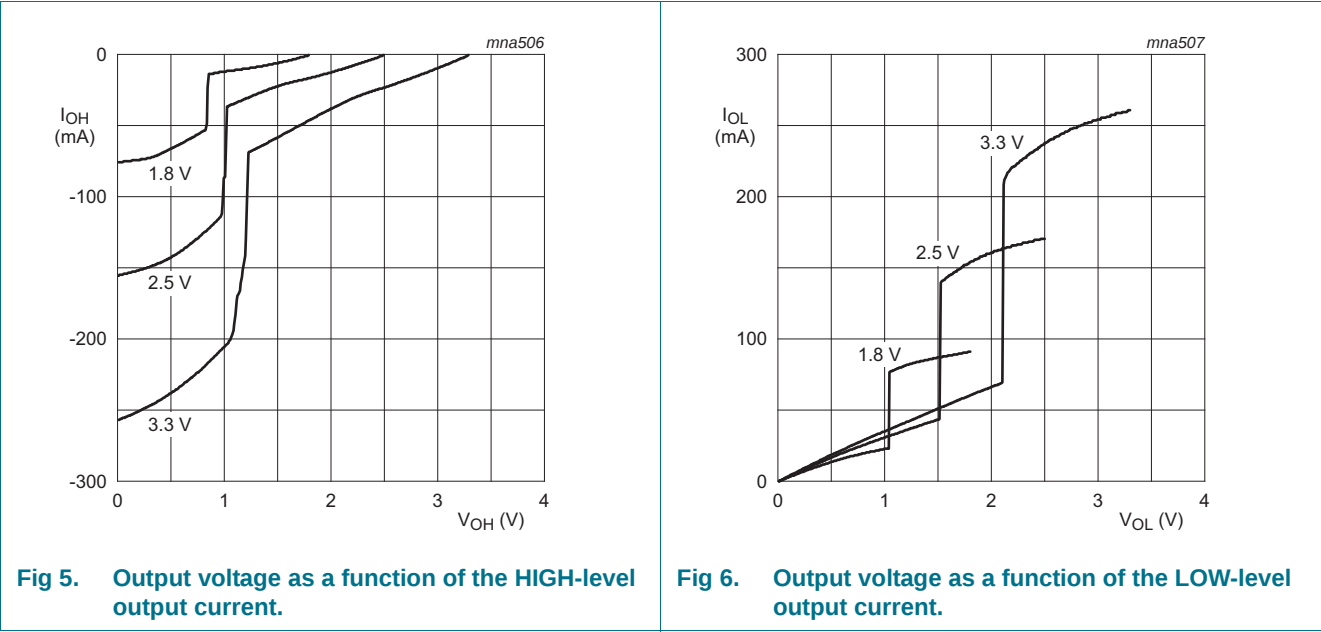
Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = –40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	V _{CC}	-	-	V
		V _{CC} = 1.4 V to 1.6 V	0.65 × V _{CC}	0.9	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	0.9	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	1.5	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	GND	V
		V _{CC} = 1.4 V to 1.6 V	-	0.9	0.35 × V _{CC}	V
		V _{CC} = 1.65 V to 1.95 V	-	0.9	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	1.5	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = –100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} – 0.20	V _{CC}	-	V
		I _O = –3 mA; V _{CC} = 1.4 V	V _{CC} – 0.35	V _{CC} – 0.23	-	V
		I _O = –4 mA; V _{CC} = 1.65 V	V _{CC} – 0.45	V _{CC} – 0.25	-	V
		I _O = –8 mA; V _{CC} = 2.3 V	V _{CC} – 0.55	V _{CC} – 0.38	-	V
		I _O = –12 mA; V _{CC} = 3.0 V	V _{CC} – 0.70	V _{CC} – 0.48	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	GND	0.20	V
		I _O = 3 mA; V _{CC} = 1.4 V	-	0.10	0.35	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	0.10	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	0.26	0.55	V
		I _O = 12 mA; V _{CC} = 3.0 V	-	0.36	0.70	V
I _I	input leakage current	per pin; V _I = V _{CC} or GND; V _{CC} = 1.4 V to 3.6 V	-	0.1	2.5	µA
I _{OFF}	power-off leakage current	V _I or V _O = 3.6 V; V _{CC} = 0.0 V	-	±0.1	±10	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND				
		V _{CC} = 1.4 V to 2.7 V	-	0.1	5	µA
		V _{CC} = 3.0 V to 3.6 V	-	0.1	10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A				
		V _{CC} = 1.4 V to 2.7 V	-	0.1	20	µA
		V _{CC} = 3.0 V to 3.6 V	-	0.2	40	µA
C _I	input capacitance		-	5	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

9.1 Graphs



10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). $t_r = t_f \leq 2$ ns. For test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit
			Min	Typ ^[2]	Max	
t_{pd}	propagation delay	nCP to nQn; see Figure 7 ^[1]				
		$V_{CC} = 1.2$ V	-	3.1	-	ns
		$V_{CC} = 1.4$ V to 1.6 V	1.2	2.4	8.4	ns
		$V_{CC} = 1.65$ V to 1.95 V	1.0	2.0	6.7	ns
		$V_{CC} = 2.3$ V to 2.7 V	0.8	1.5	4.1	ns
		$V_{CC} = 3.0$ V to 3.6 V	0.7	1.3	3.3	ns
t_{en}	enable time	nOE to nQn, nBn; see Figure 8 ^[1]				
		$V_{CC} = 1.2$ V	-	5.4	-	ns
		$V_{CC} = 1.4$ V to 1.6 V	1.6	3.9	8.5	ns
		$V_{CC} = 1.65$ V to 1.95 V	2.3	3.3	6.7	ns
		$V_{CC} = 2.3$ V to 2.7 V	0.9	2.3	4.3	ns
		$V_{CC} = 3.0$ V to 3.6 V	0.7	2.0	3.4	ns
t_{dis}	disable time	nOE to nQn; see Figure 8 ^[1]				
		$V_{CC} = 1.2$ V	-	5.6	-	ns
		$V_{CC} = 1.4$ V to 1.6 V	2.5	4.5	9.4	ns
		$V_{CC} = 1.65$ V to 1.95 V	1.8	3.3	7.8	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.0	1.8	4.2	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.2	2.0	3.9	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). $t_r = t_f \leq 2$ ns. For test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit
			Min	Typ ^[2]	Max	
t_w	pulse width	HIGH; nCP; see Figure 7				
		$V_{CC} = 1.2$ V	-	0.8	-	ns
		$V_{CC} = 1.4$ V to 1.6 V	-	0.5	-	ns
		$V_{CC} = 1.65$ V to 1.95 V	3.1	0.3	-	ns
		$V_{CC} = 2.3$ V to 2.7 V	2.5	0.2	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	2.5	0.2	-	ns
t_{su}	set-up time	nDn to nCP; see Figure 8				
		$V_{CC} = 1.2$ V	-	–0.6	-	ns
		$V_{CC} = 1.4$ V to 1.6 V	2.7	–0.3	-	ns
		$V_{CC} = 1.65$ V to 1.95 V	1.9	–0.3	-	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.4	–0.2	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.4	–0.1	-	ns
t_h	hold time	nDn to nCP; see Figure 8				
		$V_{CC} = 1.2$ V	-	0.8	-	ns
		$V_{CC} = 1.4$ V to 1.6 V	1.3	0.7	-	ns
		$V_{CC} = 1.65$ V to 1.95 V	1.2	0.6	-	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.1	0.5	-	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.1	0.4	-	ns
f_{max}	maximum frequency	see Figure 8				
		$V_{CC} = 1.2$ V	-	250	-	MHz
		$V_{CC} = 1.4$ V to 1.6 V	-	300	-	MHz
		$V_{CC} = 1.65$ V to 1.95 V	160	320	-	MHz
		$V_{CC} = 2.3$ V to 2.7 V	200	350	-	MHz
		$V_{CC} = 3.0$ V to 3.6 V	200	350	-	MHz
C_{PD}	power dissipation capacitance	per input; $V_I = \text{GND to } V_{CC}$ [3]				
		outputs enabled	-	66	-	pF
		outputs disabled	-	1	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[2] Typical values are measured at $T_{amb} = 25$ °C and $V_{CC} = 1.2$ V, 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

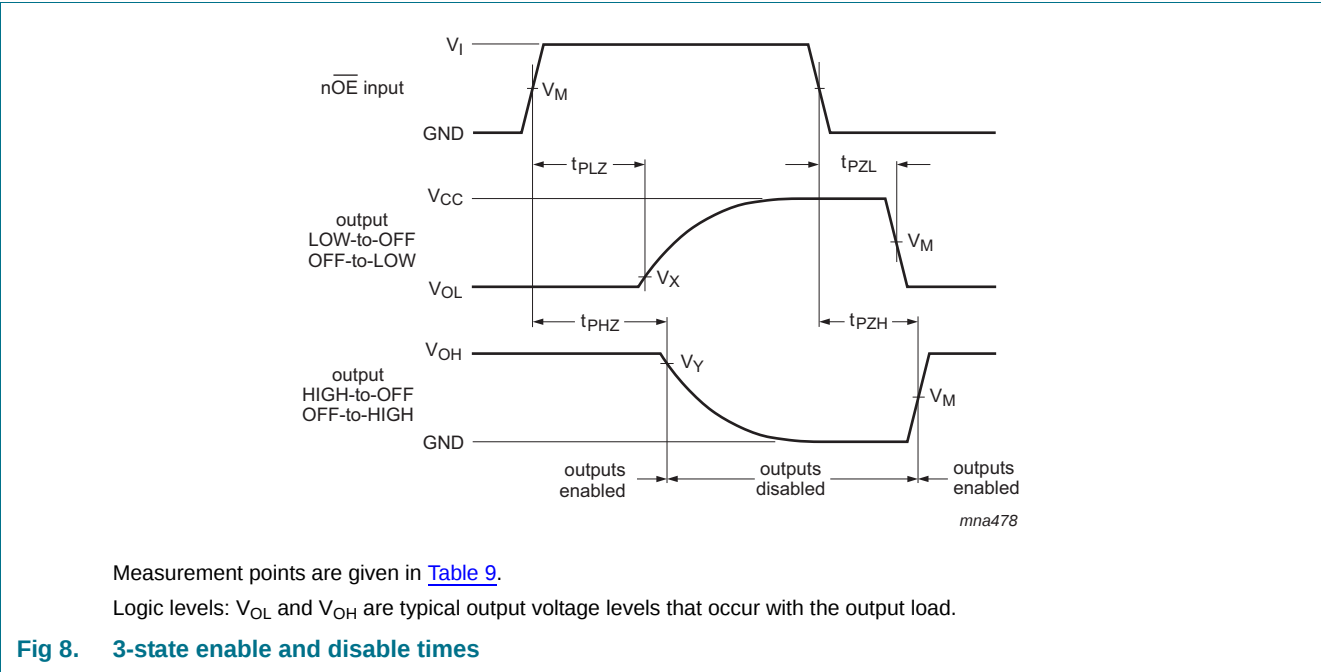
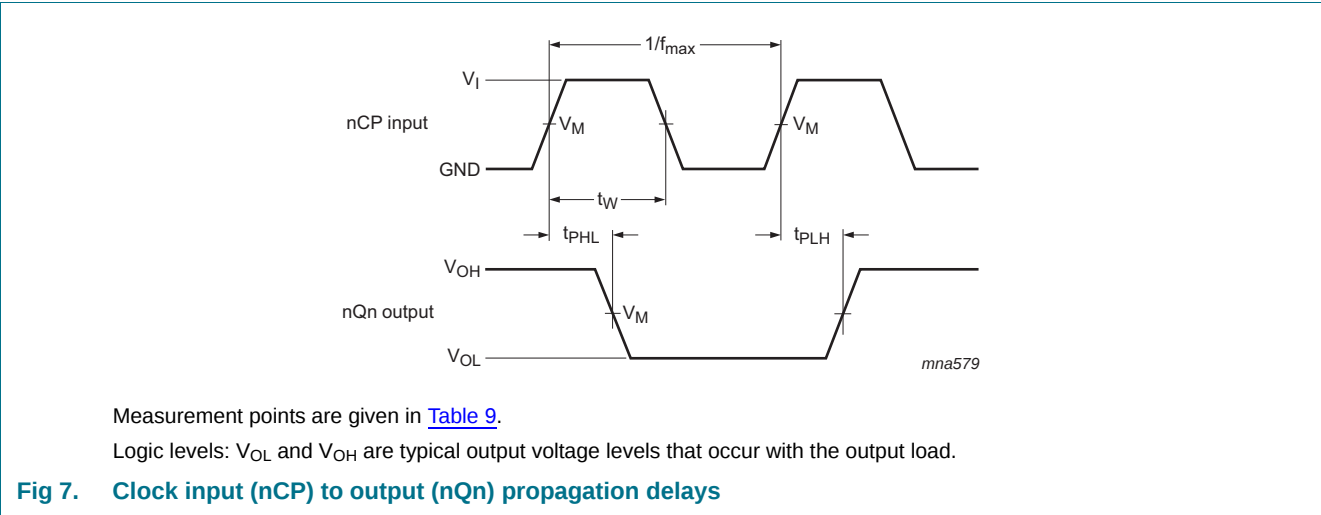
C_L = output load capacitance in pF

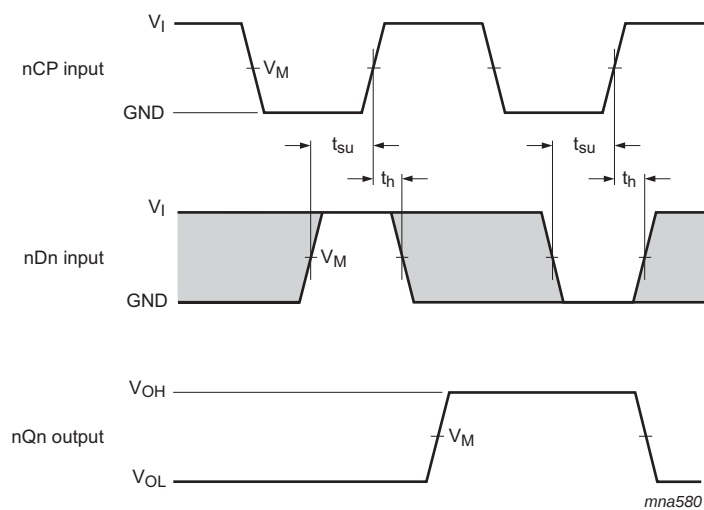
V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms



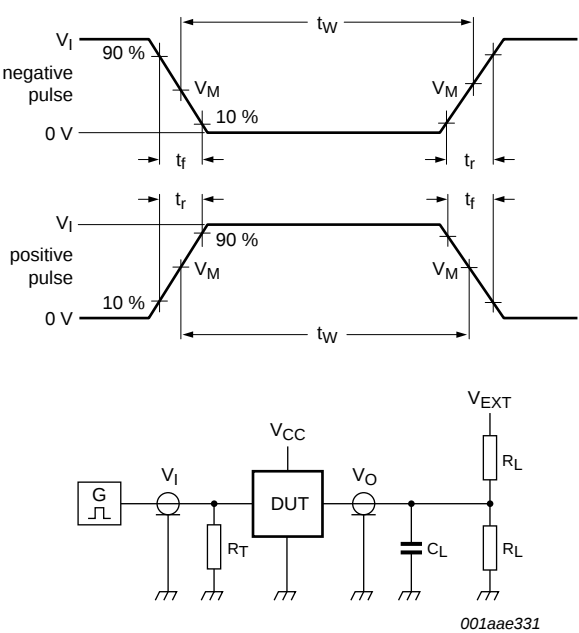


Measurement points are given in [Table 9](#).
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Data set-up and hold times for nDn input to nCP input

Table 8. Measurement points

Supply voltage	V_M	Input			
V_{CC}		V_I	$t_r = t_f$	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.4 V to 1.6 V	$0.5 \times V_{CC}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
3.0 V to 3.6 V	$0.5 \times V_{CC}$	V_{CC}	$\leq 2 \text{ ns}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	15 pF	2 k Ω	open	$2 \times V_{CC}$	GND
1.4 V to 1.6 V	V_{CC}	≤ 2 ns	15 pF	2 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1

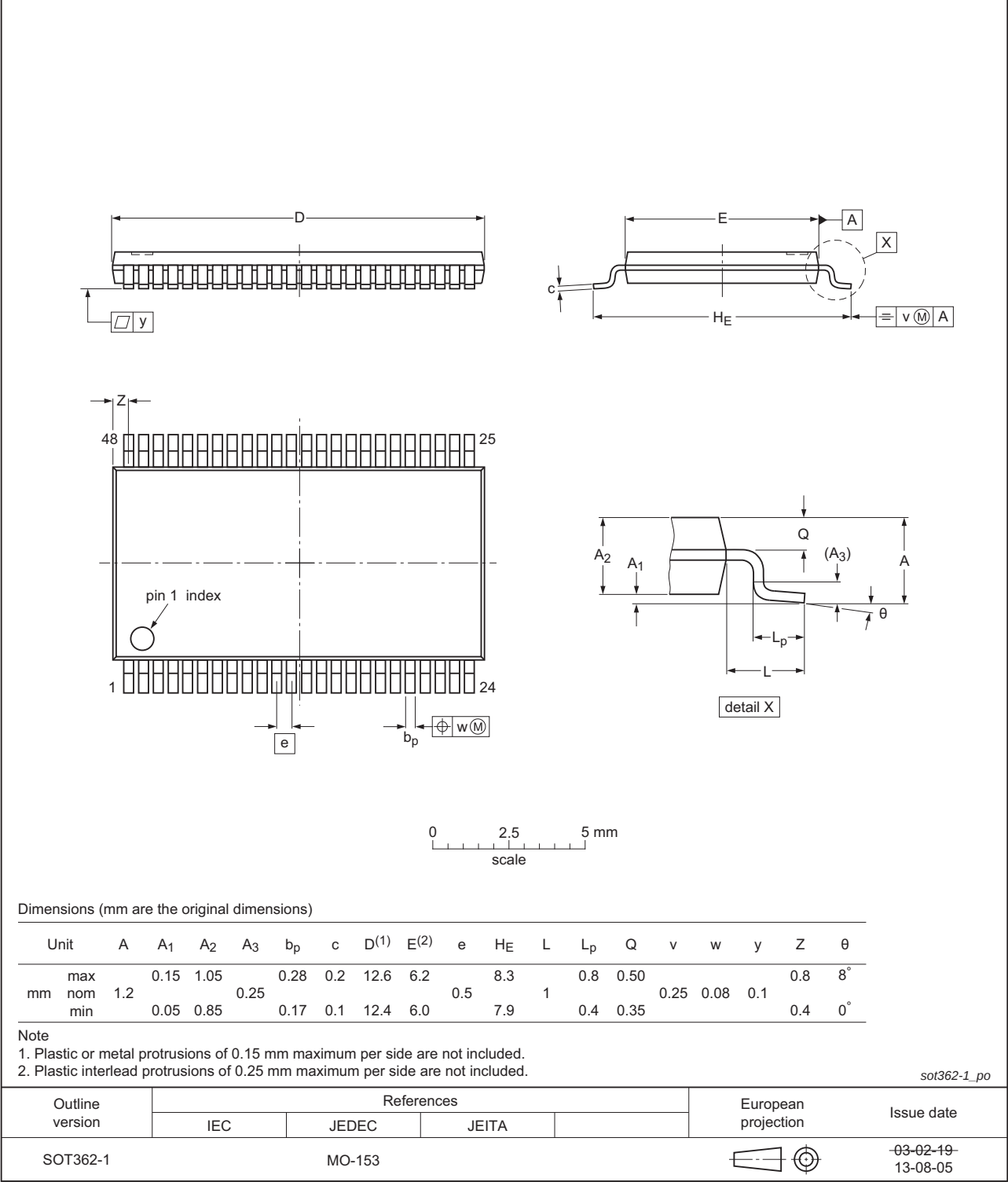


Fig 11. Package outline SOT362-1 (TSSOP48)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74AVC16374 v.3	20130816	Product data sheet	-	-	74AVC16374 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.				
74AVC16374 v.2	20000309	Product specification	-	-	74AVC16374 v.1
74AVC16374 v.1	19981211	Product specification	-	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

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