ZARLINK SEMICONDUCTOR

ISO CMOS ST-BUS™ Family MT8977
T1/ESF Framer Circuit (ACCUNET® T1.5)

Data Sheet

Features

- D3/D4 or ESF framing and SLC-96 compatible
- Two frame elastic buffer with jitter tolerance improved to 156 UI
- Insertion and detection of A, B, C, D bits, signalling freeze, optional debounce
- Selectable B8ZS, jammed bit (ZCS) or no zero code suppression
- Yellow alarm and blue alarm signal capabilities
- Bipolar violation count, F_T error count, CRC error count
- Selectable robbed bit signalling
- Frame and superframe sync. signals, Tx and Rx
- AMI encoding and decoding
- Per channel, overall, and remote loop around
- Digital phase detector between T1 line and ST-BUS
- One uncommitted scan point and drive point
- Pin compatible with MT8976 and MT8979
- ST-BUS compatible

September 2005

Ordering Information

MT8977AE	28 Pin PDIP	Tubes
MT8977AP	44 Pin PLCC	Tubes
MT8977APR	44 Pin PLCC	Tape & Reel
MT8977AP1	44 Pin PLCC*	Tubes
MT8977APR1	44 Pin PLCC*	Tape & Reel
MT8977AE1	28 Pin PDIP*	Tubes

*Pb Free Matte Tin

-40°C to +85°C

Applications

- DS1/ESF digital trunk interfaces
- Computer to PBX interfaces (DMI and CPI)
- High speed computer to computer data links

Description

The MT8977 is a variant of the MT8976 framer, which has been enhanced to meet ACCUNET T1.5 wander tolerance (138 UI).

The MT8977 meets ESF and D3/D4 formats, and is compatible with SLC-96 systems.

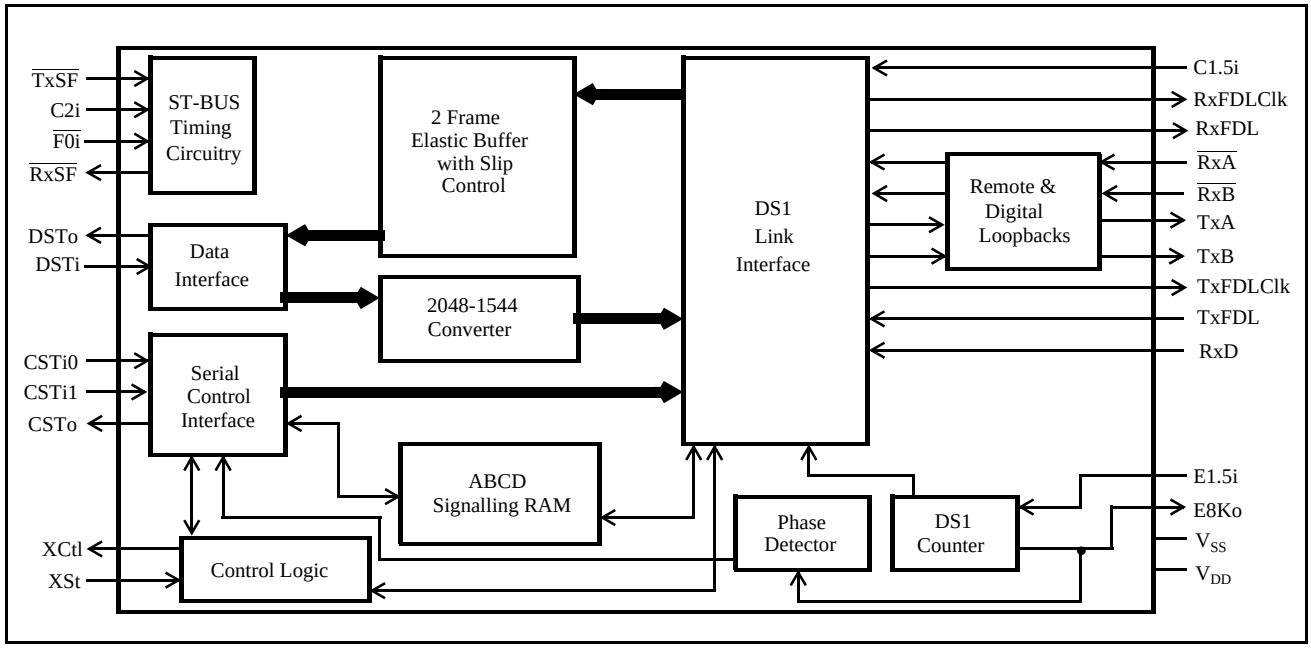

Figure 1 - Functional Block Diagram

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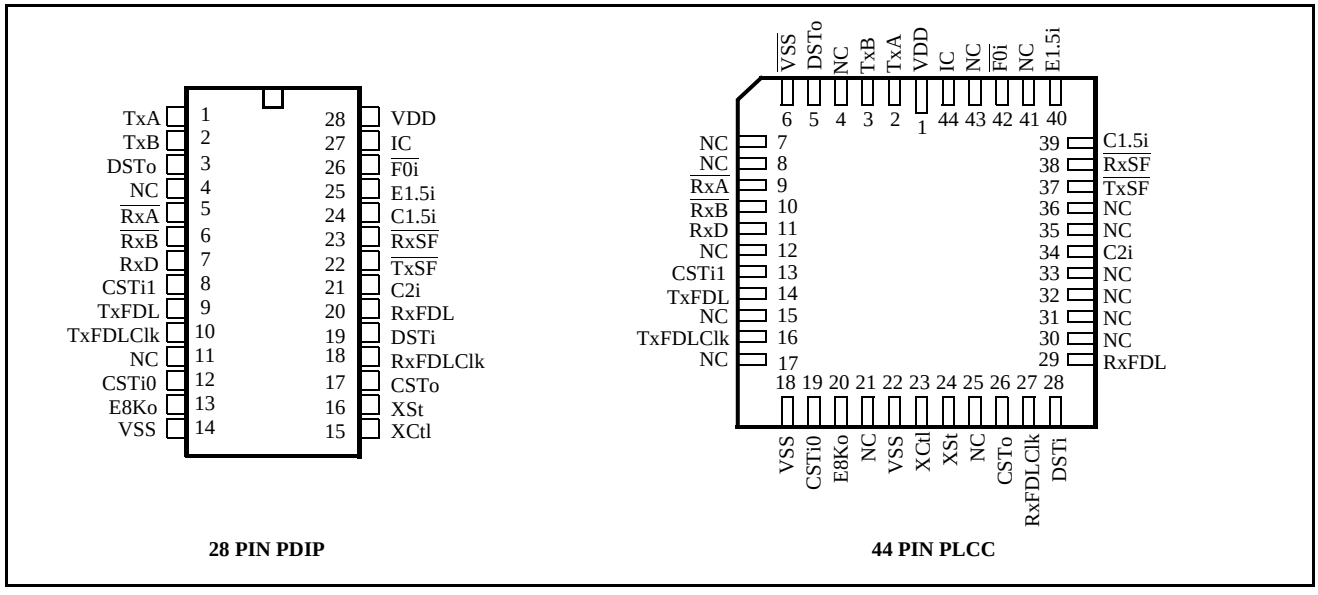


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
DIP	PLCC		
1	2	TxA	**Transmit A Output.** Unipolar output that can be used in conjunction with TxB and external line driver circuitry to generate the bipolar DS1 signal.
2	3	TxB	**Transmit B Output.** Unipolar output that can be used in conjunction with TxA and external line driver circuitry to generate the bipolar DS1 signal.
3	5	DSTo	**Data ST-BUS Output.** A 2048 kbit/s serial output stream which contains the 24 PCM or data channels received from the DS1 line.
4	4	NC	**No Connection.**
5	9	$\overline{\text{RxA}}$	**Receive A Complementary Input.** Accepts a unipolar split phase signal decoded externally from the received DS1 bipolar signal. This input, in conjunction with $\overline{\text{RxB}}$, detects bipolar violations in the received signal.
6	10	$\overline{\text{RxB}}$	**Receive B Complementary Input.** Accepts a unipolar split phase signal decoded externally from the received DS1 bipolar signal. This input, in conjunction with $\overline{\text{RxA}}$, detects bipolar violations in the received signal.
7	11	RxD	**Receive Data Input.** Unipolar RZ data signal decoded from the received DS1 signal. Generally the signals input at $\overline{\text{RxA}}$ and $\overline{\text{RxB}}$ are combined externally with a NAND gate and the resulting composite signal is input at this pin.
8	13	CSTi1	**Control ST-BUS Input #1.** A 2048 kbit/s serial control stream which carries 24 per-channel control words.
9	14	TxFDL	**Transmit Facility Data Link (Input).** A 4 kHz serial input stream that is multiplexed into the FDL position in the ESF mode, or the F_S pattern when in SLC-96 mode. It is clocked in on the rising edge of TxFDLClk.

Pin Description (continued)

Pin #		Name	Description
DIP	PLCC		
10	16	TxFDLClk	**Transmit Facility Data Link Clock (Output).** A 4 kHz clock used to clock in the FDL data.
11		NC	**No connection.**
12	19	CSTi0	**Control ST-BUS Input #0.** A 2048 kbit/s serial control stream that contains 24 per channel control words and two master control words.
13	20	E8Ko	**Extracted 8 kHz Output.** The E1.5i clock is internally divided by 193 to produce an 8 kHz clock which is aligned with the received DS1 frame and output at this pin. The 8 kHz signal is derived from C1.5 in Digital Loopback mode.
14	6, 18, 22	V_{SS}	**System Ground.**
15	23	XCtl	**External Control (Output).** This is an uncommitted external output pin which is set or reset via bit 3 in Master Control Word 1 on CSTi0. The state of XCtl is updated once per frame.
16	24	XSt	**External Status (Schmitt Trigger Input).** The state of this pin is sampled once per frame and the status is reported in bit 5 of Master Status Word 2 on CSTo.
17	26	CSTo	**Control ST-BUS Output.** This is a 2048 kbit/s serial control stream which provides the 24 per-channel status words, and two master status words.
18	27	RxFDLClk	**Receive Facility Data Link Clock (Output).** A 4 kHz clock signal used to clock out FDL information. The data is clocked out on the rising edge of RxFDLClk.
19	28	DSTi	**Data ST-BUS Input.** This pin accepts a 2048 kbit/s serial stream which contains the 24 PCM or data channels to be transmitted on the T1 trunk.
20	29	RxFDL	**Received Facility Data Link (Output).** A 4 kHz serial output stream that is demultiplexed from the FDL in ESF mode, or the received Fs bit pattern in SLC-96 mode. It is clocked out on the rising edge of RxFDLClk.
21	34	C2i	**2.048 MHz Clock Input.** This is the master clock used for clocking serial data into DSTi, CSTi0 and CSTi1. It is also used to clock serial data out of CSTo and DSTo.
22	37	$\overline{\text{TxSF}}$	**Transmit Superframe Pulse Input.** A low going pulse applied at this pin will make the next transmit frame the first frame of a superframe. The device will free run if this pin is held high.
23	38	$\overline{\text{RxSF}}$	**Received Superframe Pulse Output.** A pulse output on this pin designates that the next frame of data on the ST-BUS is from frame 1 of the received superframe. The period is 12 frames long in D3/D4 modes and 24 frames in ESF mode. Pulses are output only when the device is synchronized to the received DS1 signal.
24	39	C1.5i	**1.544 MHz Clock Input**. This is the DS1 transmit clock and is used to output data on TxA and TxB. It must be phase-locked to C2i. Data is clocked out on the rising edge of C1.5i.
25	40	E1.5i	**1.544 MHz Extracted Clock (Input).** This clock which is extracted from the received data is used to clock in data at $\overline{\text{RxA}}$, $\overline{\text{RxB}}$ and RxD. The falling edge of the clock is nominally aligned with the center of the received bit on RxD, $\overline{\text{RxA}}$ and $\overline{\text{RxB}}$.
26	42	$\overline{\text{F0i}}$	**Frame Pulse Input.** This is the frame synchronization signal which defines the beginning of the 32 channel ST-BUS frame.
27	44	IC	**Internal Connection.** Tied to V_{SS} for normal operation.

Pin Description (continued)

Pin #		Name	Description
DIP	PLCC		
28	1	V_{DD}	**Positive Power Supply Input.** +5V ±5%.

Functional Timing Diagrams

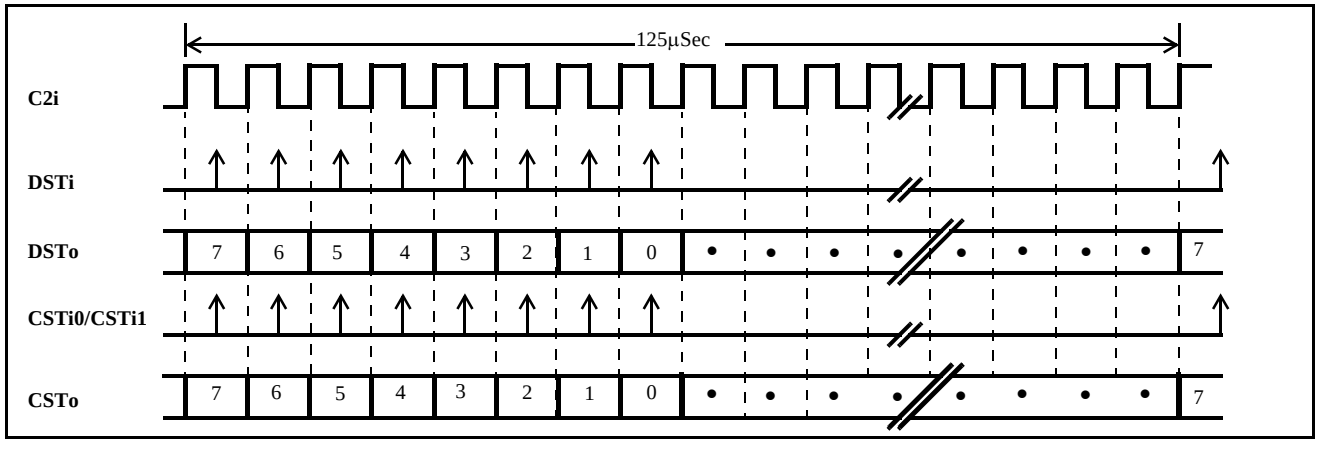


Figure 3 - ST-BUS Timing

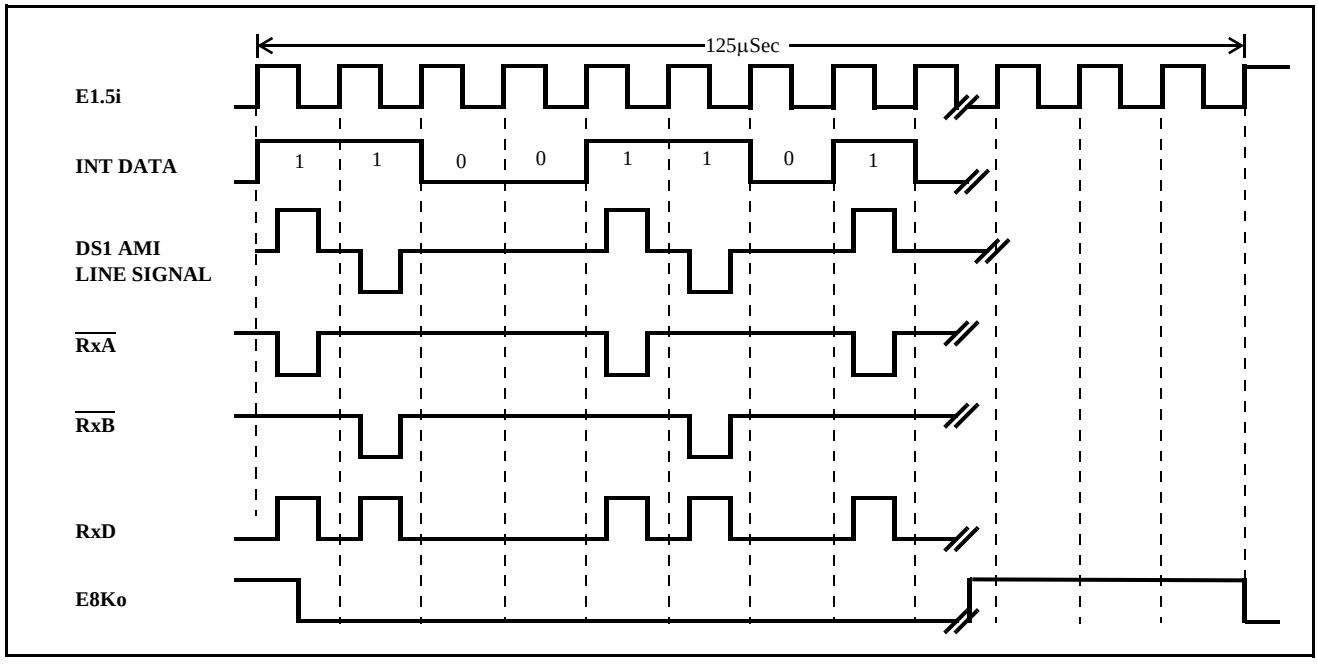


Figure 4 - FiDS1 Receive Timing

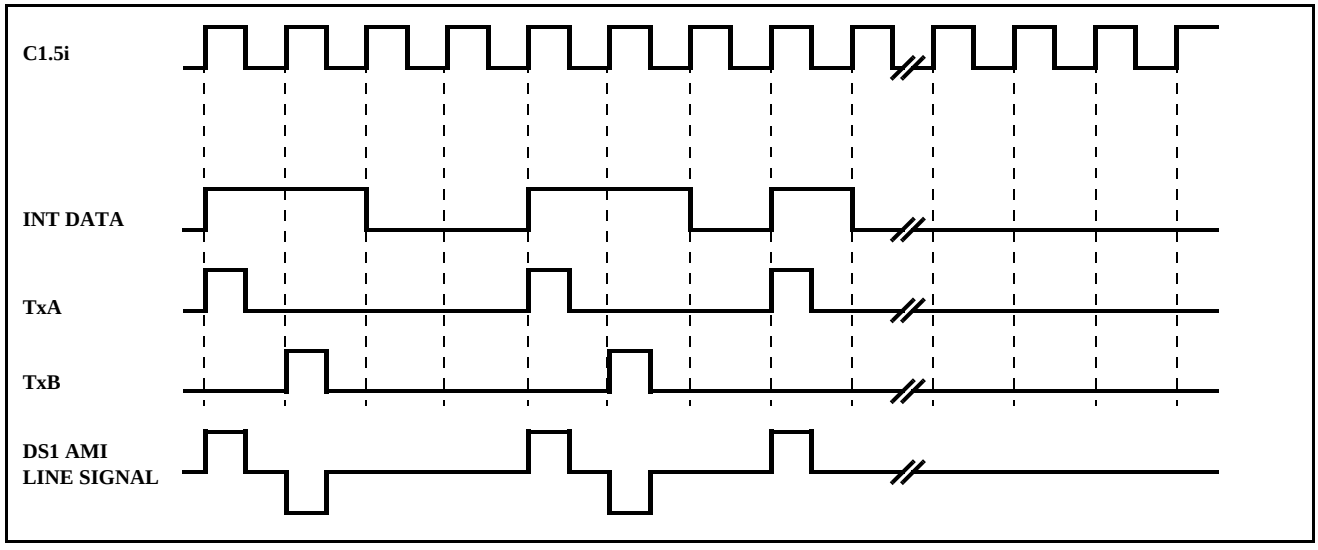


Figure 5 - DS1 Transmit Timing

DSTi	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

ST-BUS CHANNEL VERSUS DS1 CHANNEL TRANSMITTED

DSTo	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
DS1		1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24

ST-BUS CHANNEL VERSUS DS1 CHANNEL RECEIVED

CSTi0	0 PCCW1	1 PCCW1	2 PCCW1	3 X	4 PCCW1	5 PCCW1	6 PCCW1	7 X	8 PCCW1	9 PCCW1	10 PCCW1	11 X	12 PCCW1	13 PCCW1	14 PCCW1	15 MCW1	16 PCCW1	17 PCCW1	18 PCCW1	19 X	20 PCCW1	21 PCCW1	22 PCCW1	23 X	24 PCCW1	25 PCCW1	26 PCCW1	27 X	28 PCCW1	29 PCCW1	30 PCCW1	31 MCW2
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

PCCW = Per Channel Control Word
MCW1/2 =Master Control Word 1/2

ST-BUS CHANNEL VERSUS DS1 CHANNEL CONTROLLED

CSTi1	0 PCCW2	1 PCCW2	2 PCCW2	3 X	4 PCCW2	5 PCCW2	6 PCCW2	7 X	8 PCCW2	9 PCCW2	10 PCCW2	11 X	12 PCCW2	13 PCCW2	14 PCCW2	15 X	16 PCCW2	17 PCCW2	18 PCCW2	19 X	20 PCCW2	21 PCCW2	22 PCCW2	23 X	24 PCCW2	25 PCCW2	26 PCCW2	27 X	28 PCCW2	29 PCCW2	30 PCCW2	31 X
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

PCCW = Per Channel Control Word

ST-BUS CHANNEL VERSUS DS1 CHANNEL CONTROLLED

CSTo	0 PCSW	1 PCSW	2 PCSW	3 PSW	4 PCSW	5 PCSW	6 PCSW	7 X	8 PCSW	9 PCSW	10 PCSW	11 X	12 PCSW	13 PCSW	14 PCSW	15 MSW1	16 PCSW	17 PCSW	18 PCSW	19 X	20 PCSW	21 PCSW	22 PCSW	23 X	24 PCSW	25 PCSW	26 PCSW	27 X	28 PCSW	29 PCSW	30 PCSW	31 MSW2
DS1	1	2	3		4	5	6		7	8	9		10	11	12		13	14	15		16	17	18		19	20	21		22	23	24	

PCSW =Per Channel Status Word
PSW = Phase Status Word
MSW =Master Status Word

ST-BUS VERSUS DS1 CHANNEL STATUS

Figure 6 - ST-BUS Channel Allocations

Functional Description

The MT8977 provides a simple interface to a bidirectional DS1 link. All of the formatting and signalling insertion and detection is done by the device. Various programmable options in the device include: ESF, D3/D4, or SLC-96 mode, common channel or robbed bit signalling, zero code suppression, alarms, and local and remote loop back. All data and control information is communicated to the MT8977 via 2048 kbit/s serial streams conforming to Zarlink's ST-BUS format.

The ST-BUS is a TDM serial bus that operates at 2048 kbits/s. The serial streams are divided into 125 μsec frames that are made up of 32 8 bit channels. A serial stream that is made up of these 32 8 bit channels is known as an ST-BUS stream, and one of these 64 kbit/s channels is known as an ST-BUS channel.

The system side of the MT8977 is made up of ST-BUS inputs and outputs, i.e. control inputs and outputs (CSTi/o) and data inputs and outputs (DSTi/o). These signals are functionally represented in Figure 3. The line side of the device is made up of the split phase inputs and outputs that can be interfaced to an external bipolar receiver and transmitter. Functional transmit and receive timing is shown in Figures 4 and 5.

Data for transmission on the DS1 line is clocked serially into the device at the DSTi pin. The DSTi pin accepts a 32 channel time division multiplexed ST-BUS stream. Data is clocked in with the falling edge of the C2i clock. ST-BUS frame boundaries are defined by the frame pulse applied at the F0i pin. Only 24 of the available 32 channels on the ST-BUS serial stream are actually transmitted on the DS1 side. The unused 8 channels are ignored by the device.

Data received from the DS1 line is clocked out of the device in a similar manner at the DSTo pin. Data is clocked out on the rising edge of the C2i clock. Only 24 of the 32 channels output by the device contain the information from the DS1 line. The DSTo pin is, however, actively driven during the unused channel timeslots. Figure 6 shows the correspondence between the DS1 channels and the ST-BUS channels.

All control and monitoring of the device is accomplished through two ST-BUS serial control inputs and one serial control output. Control ST-BUS input number 0 (CSTi0) accepts an ST-BUS serial stream which contains the 24 per channel control words and two master control words. The per channel control words relate directly to the 24 information channels output on the DS1 side. The master control words affect operation of the whole device. Control ST-BUS input number 1 (CSTi1) accepts an ST-BUS stream containing the A, B, C and D signalling bits. The relationship between the CSTi channels and the controlled DS0 channels is shown in Figure 6. Status and signalling information is received from the device via the control ST-BUS output (CSTo). This serial output stream contains two master status words, 24 per channel status words and one Phase Status Word. Figure 6 shows the correspondence between the received DS1 channels and the status words. Detailed information on the operation of the control interface is presented below.

Programmable Features

The main features in the device are programmed through two master control words which occupy channels 15 and 31 in Control ST-BUS input stream number 0 (CSTi0). These two eight bit words are used to:

- Select the different operating modes of the device ESF, D3/D4 or SLC-96.
- Activate the features that are needed in a certain application; common channel signalling, zero code suppression, signalling debounce, etc.
- Turn on in service alarms, diagnostic loop arounds, and the external control function.

Tables 1 and 2 contain a complete explanation of the function of the different bits in Master Control Words 1 and 2.

Bit	Name	Description
7	Debounce	When set the received A, B, C and D signalling bits are reported directly in the per channel status words output at CSTo. When clear, the signalling bits are debounced for 6 to 9 ms before they are placed on CSTo.
6	TSPZCS	**Transparent Zero Code Suppression.** When this bit is set, no zero code suppression is implemented.
5	B8ZS	**Binary Eight Zero Suppression.** When this bit is set, B8ZS zero code suppression is enabled. When clear, bit 7 in data channels containing all zeros is forced high before being transmitted on the DS1 side. This bit is inactive if the TSPZCS bit is set.
4	8KHSel	**8 kHz Output Select.** When set, the E8Ko pin is held high. When clear, the E8Ko generates an 8 kHz output derived from the E1.5i or C1.5 clock (see Pin Description for E8Ko).
3	XCtl	**External Control Pin.** When set, the XCtl pin is held high. When clear, XCtl is held low.
2	ESFYLW	**ESF Yellow Alarm.** Valid only in ESF mode. When set, a sequence of eight 1's followed by eight 0's is sent in the FDL bit positions. When clear, the FDL bit contains data input at the TxFDL pin.
1	Robbed bit	When this bit is set, robbed bit signalling is disabled on all DS0 transmit channels. When clear, A, B, C and D signalling bit insertion in bit 8 for all DS0 transmit channels in every 6^{th} frame is enabled.
0	YLALR	**Yellow Alarm.** When set, bit 2 of all DS1 channels is set low. When clear, bit 2 operates normally.

Table 1 - Master Control Word 1 (Channel 15, CSTi0)

Bit	Name	Description
7	RMLOOP	**Remote Loopback.** When set, the data received at $\overline{RxA}$ and $\overline{RxB}$ is looped back to TxB and TxA respectively. The data is clocked into the device with E1.5i. The device still monitors the received data and outputs it at DSTo. The device operates normally when the bit is clear.
6	DGLOOP	**Digital Loopback.** When set, the data input on DSTi is looped around to DSTo. The normal received data on $\overline{RxA}$, $\overline{RxB}$ and RxD is ignored. However, the data input at DSTi is still transmitted on TxA and TxB. The device frames up on the looped data using the C1.5i clock.
5	ALL1'S	**All One's Alarm.** When set, the chip transmits an unframed all 1's signal on TxA and TxB.
4	ESF/D4	**ESF/D4 Select.** When set, the device is in ESF mode. When clear, the device is in D3/D4 mode.
3	ReFR	**Reframe.** If set for at least one frame and then cleared, the chip will begin to search for a new frame position. Only the change from high to low will cause a reframe, not a continuous low level.
2	SLC-96	**SLC-96 Mode Select.** The chip is in SLC-96 mode when this bit is set. This enables input and output of the F_S bit pattern using the same pins as the facility data link in ESF mode. The chip will use the same framing algorithm as D3/D4 mode. The user must insert the valid F_S bits in 2 out of 6 superframes to allow the receiver to find superframe sync, and the transmitter to insert A and B bits in every 6^{th} frame. The SLC-96 FDL completely replaces the F_S pattern in the outgoing S bit position. Inactive in ESF mode.
1	CRC/MIMIC	In ESF mode, when set, the chip disregards the CRC calculation during synchronization. When clear, the device will check for a correct CRC before going into synchronization. In D3/D4 mode, when set, the device will synchronize on the first correct S-bit pattern detected. When this bit is clear, the device will not synchronize if it has detected more than one candidate for the frame alignment pattern (i.e., a mimic).
0	Maint.	**Maintenance Mode.** When set, the device will declare itself out-of-sync if 4 out of 12 consecutive F_T bits are in error. When clear, the out-of-sync threshold is 2 errors in 4 F_T bits. In this mode, four consecutive bits following an errored F_T bit are examined.

Table 2 - Master Control Word 2 (Channel 31, CSTi0)

Major Operating Modes

The major operating modes of the device are enabled by bits 2 and 4 of Master Control Word 2. The Extended Superframe (ESF) mode is enabled when bit 4 is set high. Bit 2 has no effect in this mode. The ESF mode enables the transmission of the S bit pattern shown in Table 3. This includes the frame/superframe pattern, the CRC-6, and the Facility Data Link (FDL). The device generates the frame/multiframe pattern and calculates the CRC for each superframe. The data clocked into the device on the TxFDL pin is incorporated into the FDL. ESF mode will also insert A, B, C and D signalling bits into the 24 frame multiframe. The DS1 frame begins after approximately 25 periods of the C1.5i clock from the $\overline{F0i}$ frame pulse.

During synchronization the receiver locks to the incoming frame, calculates the CRC and compares it to the CRC received in the next multiframe. The device will not declare itself to be in synchronization unless a valid framing pattern in the S-bit is detected and a correct CRC is received. The CRC check in this case provides protection against false framing. The CRC check can be turned off by setting bit 1 in Master Control Word 2.

The device can be forced to resynchronize itself. If Bit 3 in Master Control Word 2 is set for one frame and then subsequently reset, the device will start to search for a new frame position. The decision to reframe is made by the user's system processor on the basis of the status conditions detected in the received master status words. This may include consideration of the number of errors in the received CRC in conjunction with an indication of the presence of a mimic. When the device attains synchronization the mimic bit in Master Status Word 1 is set if the device found another possible candidate when it was searching for the framing pattern.

Note that the device will resynchronize automatically if the errors in the terminal framing pattern (F_T or FPS) exceed the threshold set with bit 0 in Master Control Word 2.

Standard D3/D4 framing is enabled when bit 4 of Master Control Word 2 is reset (logic 0). In this mode the device searches for and inserts the framing pattern shown in Table 4. This mode only supports AB bit signalling, and does not contain a CRC check.

The CRC/MIMIC bit in Master Control Word 2, when set high, allows the device to synchronize in the presence of a mimic. If this bit is reset, the device will not synchronize in the presence of a mimic (Also, refer to section on Framing algorithm).

In the D3/D4 mode the device can also be made compatible with SLC-96 by setting bit two of Master Control Word 2. This allows the user to insert and extract the signalling framing pattern on the DS1 bit stream using the FDL input and output pins. The user must format this 4 kbits of information externally to meet all of the requirements of the SLC-96 specification (see Table 5). The device multiplexes and demultiplexes this information into the proper position. This mode of operation can also be used for any other application that uses all or part of the signalling framing pattern. As long as the serial stream clocked into the TxFDL contains two proper sets of consecutive synchronization bits (as shown in Table 5 for frames 1 to 24), the device will be able to insert and extract the A, B signalling bits. The $\overline{\text{TxSF}}$ pin should be held high in this mode. Superframe boundaries cannot be defined by a pulse on this input. The $\overline{\text{RxSF}}$ output functions normally and indicates the superframe boundaries based on the synchronization pattern in the F_S received bit position.

Zero Code Suppression

The combination of bits 5 and 6 in Master Control Word 1 allow one of three zero code suppression schemes to be selected. The three choices are: none, binary 8 zero suppression (B8ZS), or jammed bit (bit 7 forced high). No zero code suppression allows the device to interface with systems that have already applied some form of zero code suppression to the data input on DSTi. B8ZS zero code suppression replaces all strings of 8 zeros with a known bit pattern and a specific pattern of bipolar violations. This bit pattern and violation pattern is shown in Figure 7. The receiver monitors the received bit pattern and the bipolar violation pattern and replaces all matching strings with 8 zeros.

Loopback Modes

Remote and digital loopback modes are enabled by bits 6 and 7 in Master Control Word 2. These modes can be used for diagnostics in locating the source of a fault condition. Remote loop around loops back data received at $\overline{\text{RxA}}$ and $\overline{\text{RxB}}$ back out on TxA and TxB, thus effectively sending the received DS1 data back to the far end unaltered so that the transmission line can be tested. The received signal is still monitored with the appropriate received channels on the DS1 side made available in the proper format at DSTo.

The digital loop around mode diverts the data received at DSTi back out the DSTo pin. Data received on DSTi is, however, still transmitted out via TxA and TxB. This loop back mode can be used to test the near end interface equipment when there is no transmission line or when there is a suspected failure of the line.

The all one's transmit alarm (also known as the blue alarm or the keep alive signal) can be activated in conjunction with the digital loop around so that the transmission line sends an all 1's signal while the normal data is looped back locally.

The MT8977 also has a per channel loopback mode. See Table 6 and the following section for more information.

Per Channel Control Features

In addition to the two master control words in CSTi0 there are also 24 Per Channel Control Words. These control words only affect individual DS0 channels. The correspondence between the channels on CSTi0 and the affected DS0 channel is shown in Fig. 6.

Frame #	FPS	FDL	CRC	Signalling†
1		X		
2			CB1	
3		X		
4	0			
5		X		
6			CB2	A
7		X		
8	0			
9		X		
10			CB3	
11		X		
12	1			B
13		X		
14			CB4	
15		X		
16	0			
17		X		
18			CB5	C
19		X		
20	1			
21		X		
22			CB6	
23		X		
24	1			D

Table 3 - ESF Frame Pattern

† These signalling bits are only valid if the robbed bit signalling is active.

Frame #	F_T	F_S	Signalling †
1	1		
2		0	
3	0		
4		0	
5	1		
6		1	A
7	0		
8		1	
9	1		
10		1	
11	0		
12		0	B

Table 4 - D3/D4 Framer

† These signalling bits are only valid if the robbed bit signalling is active.

Each control word has three bits that enable robbed bit signalling, DS0 channel loopback and inversion of the DS0 channel. A full description of each of the bits is provided in Table 6.

Transmit Signalling Bits

Control ST-BUS input number 1 (CSTi1) contains 24 additional per channel control words. These 24 ST-BUS channels contain the A, B, C and D signalling bits that the device uses at transmit time. The position of these 24 per channel control words in the ST-BUS is shown in Figure 6 and the position of the ABCD signalling bits is shown in Table 7. Even though the device only inserts the signalling information in every 6th DS1 frame this information must be input every ST-BUS frame.

Robbed bit signalling can be disabled for all channels on the DS1 link by bit 1 of Master Control Word 1. It can also be disabled on a per channel basis by bit 0 in the Per Channel Control Word 1.

Operating Status Information

Status Information regarding the operation of the device is output serially via the Control ST-BUS output (CSTo). The CSTo serial stream contains Master Status Words 1 and 2, 24 Per Channel Status Words, and a Phase Status Word. The Master Status Words contain all of the information needed to determine the state of the interface and how well it is operating. The information provided includes frame and super frame synchronization, slip, bipolar violation counter, alarms, CRC error count, F_T error count, synchronization pattern mimic and a phase status word. Tables 8 and 9 give a description of each of the bits in Master Status Words 1 and 2, and Table 10 gives a description of the Phase Status Word.

Alarm Detection

The device detects the yellow alarm for both D3/D4 frame format and ESF format. The D3/D4 yellow alarm will be activated if a ‘0‘is received in bit position 2 of every DS0 channel for 600 msec. It will be released in 200 msec after the contents of the bit change. The alarm is detectable in the presence of errors on the line. The ESF yellow alarm will become active when the device has detected a string of eight 0’s followed by eight 1’s in the facility data link. It is not detectable in the presence of errors on the line. This means that the ESF yellow alarm will drop out for relatively short periods of time, so the system will have to integrate the ESF yellow alarm. The blue alarm signal, in Master Status Word 2, will also drop out if there are errors on the line.

Mimic Detection

The mimic bit in Master Status Word 1 will be set if, during synchronization, a frame alignment pattern (F_T or FPS bit pattern) was observed in more than one position, i.e., if more than one candidate for the frame synchronization position was observed. It will be reset when the device resynchronizes. The mimic bit, the terminal framing error bit and the CRC error counter can be used separately or together to decide if the receiver should be forced to reframe.

Frame #	F_T	F_S†	Notes	Frame #	F_T	F_S†	Notes
1	1		Resynchronization Data Bits	37	1		X = Concentrator Field Bits
2		0		38		X	
3	0			39	0		
4		0		40		X	
5	1			41	1		
6		0		42		X	
7	0			43	0		
8		1		44		X	
9	1			45	1		
10		1		46		X	
11	0			47	0		S = Spoiler Bits
12		1		48		S	
13	1			49	1		
14		0		50		S	
15	0			51	0		
16		0		52		S	
17	1			53	1		
18		0		54		C	C = Maintenance Field Bits
19	0			55	0		
20		1		56		C	
21	1			57	1		
22		1		58		C	
23	0			59	0		A = Alarm Field Bits
24		1		60		A	
25	1		X = Concentrator Field Bits	61	1		
26		X		62		A	
27	0			63	0		L = Line Switch Field Bits
28		X		64		L	
29	1			65	1		
30		X		66		L	
31	0			67	0		
32		X		68		L	
33	1			69	1		
34		X		70		L	
35	0			71	0		S = Spoiler Bits
36		X		72		S	

Table 5 - SLC-96 Framing Pattern

† Note: The F_S pattern has to be supplied by the user

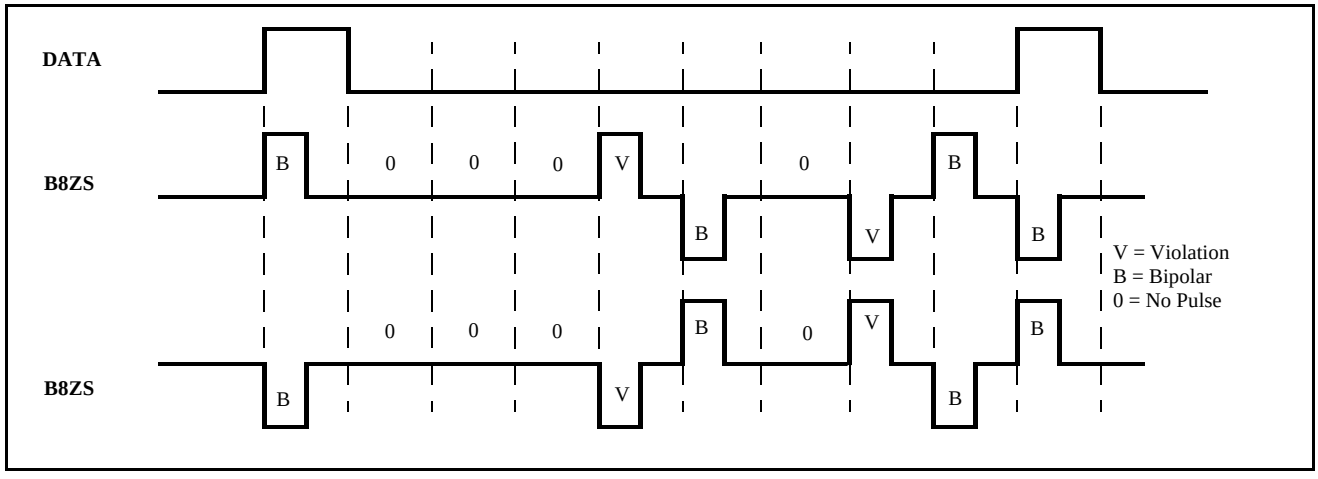


Figure 7 - B8ZS Output Coding

Bipolar Violation Counter

The Bipolar Violation bit in Master Status Word 1 will toggle after 256 violations have been detected in the received signal. It has a maximum refresh time of 96 ms. This means that the bit can not change state faster than once every 96 ms. For example, if there are 256 violations in 80 ms the BPV bit will not change state until 96 ms. Any more errors in that extra 16 ms are not counted. If there are 256 errors in 200 ms then the BPV bit will change state after 200 ms. In practical terms this puts an upper limit on the error rate that can be calculated from the BPV information, but this rate (1.7×10^{-3}) is well above any normal operating condition.

Bits 4 and 3 also provide bipolar violations information. Bit 4 will change state after 128 violations. Bit 3 changes state after 64 bipolar violations. These bits are refreshed independently and are not subject to the 96 ms refresh rate described above.

DS1/ST-BUS Phase Difference

An indication of the phase difference between the ST-BUS and the DS1 frame can be ascertained from the information provided by the eight bit Phase Status Word and the Frame Count bit. Channel three on CSTo contains the Phase Status Word. Bits 7-3 in this word indicate the number of ST-BUS channels between the ST-BUS frame pulse and the rising edge of the E8Ko signal. The remaining three bits provide one bit resolution within the channel count indicated by bits 7-3. The frame count bit in Master Status Word 2 is the ninth and most significant bit of the phase status word. It will toggle when the phase status word increments above channel 31, bit 7 or decrements below channel 0, bit 0. The E8Ko signal has a specific relationship with received DS1 frame. The rising edge of E8Ko occurs during bit 2, channel 17 of the received DS1 frame. The Phase Status Word in conjunction with the frame count bit, can be used to monitor the phase relationship between the received DS1 frame and the local ST-BUS frame.

The local 2.048 MHz ST-BUS clock must be phase-locked to the 1.544 MHz clock extracted from the received data. When the two clocks are not phase-locked, the input data rate on the DS1 side will differ from the output data rate on the ST-BUS side. If the average input data rate is higher than the average output data rate, the channel count and bit count in the phase status word will be seen to decrease over time, indicating that the E8Ko rising edge, and therefore, the DS1 frame boundary is moving with respect to the ST-BUS frame pulse. Conversely, a lower average input data rate will result in an increase in the phase reading.

In an application where it is necessary to minimize jitter transfer from the received clock to the local system clock, a phase lock loop with a relatively large time constant can be implemented using information provided by the phase status word. In such a system, the local 2.048 MHz clock is derived from a precision VCO. Frequency corrections are made on the basis of the average trend observed in the phase status word. For example, if the channel count in

the phase status word is seen to increase over time, the feedback applied to the VCO is used to decrease the system clock frequency until a reversal in the trend is observed.

The elastic buffer in the MT8977 permits the device to handle 26 ST-BUS channels or 156 UI of jitter/ wander (see description of elastic buffer in the next section). In order to prevent slips from occurring, the frequency corrections would have to be implemented such that the deviation in the phase status word is limited to 26 channels peak-to-peak. It is possible to use a more sophisticated protocol, which would center the elastic buffer and permit more jitter/wander to be handled. However, for most applications, including ACCUNET® T1.5 (138 UI), the 156 UI of jitter/wander tolerance is acceptable.

Bit	Name	Description
7-3	IC	**Internal Connections.** Must be kept at 0 for normal operation
2	Polarity	When set, the applicable channel is not inverted on the transmit or the receive side of the device. When clear, all the bits within the applicable channel are inverted both on transmit and receive side.
1	Loop	**Per Channel Loopback.** When set, the received DS0 channel is replaced with the transmitted DS0 channel. Only one DS0 channel may be looped back in this manner at a time. The transmitted DS0 channel remains unaffected. When clear the transmit and receive DS0 sections operate normally.
0	Data	**Data Channel Enable.** When set, robbed bit signalling for the applicable channel is disabled. When clear, every 6th DS1 frame is available for robbed bit signalling. This feature is enabled only if bit 1 in Master Control Word is low.

Table 6 - Per Channel Control Word 1 Input at CSTi0

Bit	Name	Description
7-4	Unused	Keep at 0 for normal operation
3 2 1-0	A B C, D	These are the 4 signalling bits inserted in the appropriate channels of the DS1 stream being output from the chip, when in ESF mode. In D3/D4 modes where there are only two signalling bits, the values of C and D are ignored.

Table 7 - Per Channel Control Word 2 Input at CSTi1

Bit	Name	Description
7	YLALR	**Yellow Alarm Indication.** This bit is set when the chip is receiving a 0 in bit position 2 of every DS0 channel.
6	MIMIC	This bit is set if the frame search algorithm found more than one possible frame candidate when it went into frame synchronization.
5	ERR	**Terminal Framing Bit Error.** The state of this bit changes every time the chip detects 4 errors in the F_T or FPS bit pattern. The bit will not change state more than once every 96ms.
4	ESFYLW	**ESF Yellow Alarm.** This bit is set when the device has observed a sequence of eight one's and eight 0's in the FDL bit positions.
3	$\overline{\text{MFSYNC}}$	**Multiframe Synchronization.** This bit is cleared when D3/D4 multiframe synchronization has been achieved. Applicable only in D3/D4 and SLC-96 modes.
2	BPV	**Bipolar Violation Count.** The state of this bit changes every time the device counts 256 bipolar violations.
1	SLIP	**Slip Indication.** This bit changes state every time the elastic buffer in the device performs a controlled slip.
0	$\overline{\text{SYN}}$	**Synchronization.** This bit is set when the device has not achieved synchronization. The bit is clear when the device has synchronized to the received DS1 data stream.

Table 8 - Master Status Word 1 (Channel 15, CSTo)

Bit	Name	Description
7	BlAlm	**Blue Alarm.** This bit is set if the receiver has detected two frames of 1's and an out of frame condition. It is reset by any 250 microsecond interval that contains a zero.
6	FrCnt	**Frame Count.** This is the ninth and most significant bit of the "Phase Status Word" (see Table 10). If the phase status word is incrementing, this bit will toggle when the phase reading exceeds channel 31, bit 7. If the phase word is decrementing, then this bit will toggle when the reading goes below channel 0, bit 0.

Bit	Name	Description
5	XSt	**External Status.** This bit reflects the state of the external status pin (XSt). The state of the XSt pin is sampled once per frame.
4-3	BPVCnt	**Bipolar Violation Count.** These two bits change state every 128 and every 64 bipolar violations, respectively.
2-0	CRCCNT	**CRC Error Count.** These three bits count received CRC errors. The counter will reset to zero when it reaches terminal count. Valid only in ESF mode.

Table 9 - Master Status Word 2 (Channel 31, CSTo)

Bit	Name	Description
7-3	ChannelCnt	**Channel Count.** These five bits indicate the ST-BUS channel count between the ST-BUS frame pulse and the rising edge of E8Ko.
2-0	BitCnt	**Bit Count.** These three bits provide one bit resolution within the channel count described above.

Table 10 - Phase Status Word (Channel 3, CSTo)

Bit	Name	Description
7-4	Unused	Unused Bits. Will be output as 0's.
3 2 1 0	A B C D	These are the 4 signalling bits as extracted from the received DS1 bit stream. The bits are debounced for 6 to 9 ms if the debounce feature is enabled via bit 7 in Master Control Word 1.

Table 11 - Per Channel Status Word Output on CSTo

Received Signalling Bits

The A, B, C and D signalling bits are output from the device in the 24 Per Channel Status Words. Their location in the serial steam output at CSTo is shown in Figure 6 and the bit positions are shown in Table 11. The internal debouncing of the signalling bits can be turned on or off by Master Control Word 1. In ESF mode, A, B, C and D bits are valid. Even though the signalling bits are only received once every six frames the device stores the information so that it is available on the ST-BUS every frame. The ST-BUS will always contain the most recent signalling bits. The state of the signalling bits is frozen if synchronization is lost.

In D3/D4 mode, only the A and B bits are valid. The state of the signalling bits is frozen when terminal frame synchronization is lost. The freeze is disabled when the device regains terminal frame synchronization. The signalling bits may go through a random transition stage until the device attains multiframe synchronization.

Clock and Framing Signals

The MT8977 requires one 2.048 MHz clock (C2i) and an 8 kHz framing signal for the ST-BUS side. Figure 2 illustrates the relationship between the two signals. The framing signal is used to delimit individual 32 channel ST-BUS frames.

The DS1 side requires two clocks. A 1.544 MHz clock used for transmit (C1.5i), and a 1.544 MHz clock extracted from the DS1 line signal and applied at E1.5i pin to clock in the received data.

The C2i and C1.5i clock must be phase-locked together. There must be 193 clock cycles of C1.5i for every 256 clock cycles of C2i. At the slave end of the link, the C2i and C1.5i must be phase locked to the extracted E1.5i clock.

The clock applied at E1.5i is internally divided down by 193 and aligned with the DS1 frame. The resulting 8 kHz clock is output at the E8Ko pin. This signal can be used as a reference for phase locking the C2i and C1.5i clocks to the extracted 1.544 MHz clock.

DS1 Line Interface

Transmit Interface

The interface to the DS1 line is made up of two unipolar outputs, TxA and TxB, which can be used to drive a bipolar transmitter circuit. The output signal on TxA and TxB corresponds to the positive and negative bipolar pulses required for the Alternate Mark Inversion signal on the T1 line. The relationship between the signal output at TxA and TxB and the AMI signal is illustrated in Figure 5. For transmission over twisted pair wire, the AMI signal has to be equalized and transformer coupled to the line.

Receiver Interface

The receiver circuitry is made up of three pins $\overline{\text{RxA}}$, $\overline{\text{RxB}}$ and RxD. The bipolar alternate mark inversion signal from the DS-1 line should be converted into a unipolar split phase format. The resulting signals are clocked into the device at $\overline{\text{RxA}}$ and $\overline{\text{RxB}}$. The signals are also NANDED together and input at RxD.

In special applications where the detection of bipolar violations is not required, it is possible to clock NRZ data directly into RxD. In this case, the $\overline{\text{RxA}}$ and $\overline{\text{RxB}}$ pins should be tied high.

Data is clocked into $\overline{\text{RxA}}$, $\overline{\text{RxB}}$ and RxD with the falling edge of the E1.5i clock. This clock signal is extracted from the received data. The relationship between the received signals and the extracted clock is shown in Figure 4.

Elastic Buffer

The MT8977 has a two frame elastic buffer which absorbs jitter in the received DS1 signal. The buffer is also used in the rate conversion between the 1.544 Mbit/s DS1 rate and the 2.048 Mbit/s ST-BUS data rate.

The received data is written into the elastic buffer with the extracted 1.544 MHz clock. The data is read out of the buffer on the ST-BUS side with the system 2.048 MHz clock. The maximum delay through the buffer is 1.875 ST-BUS frames or 60 ST-BUS channels, see Figure 8. The minimum delay required to avoid bus contention in the buffer memory is two ST-BUS channels.

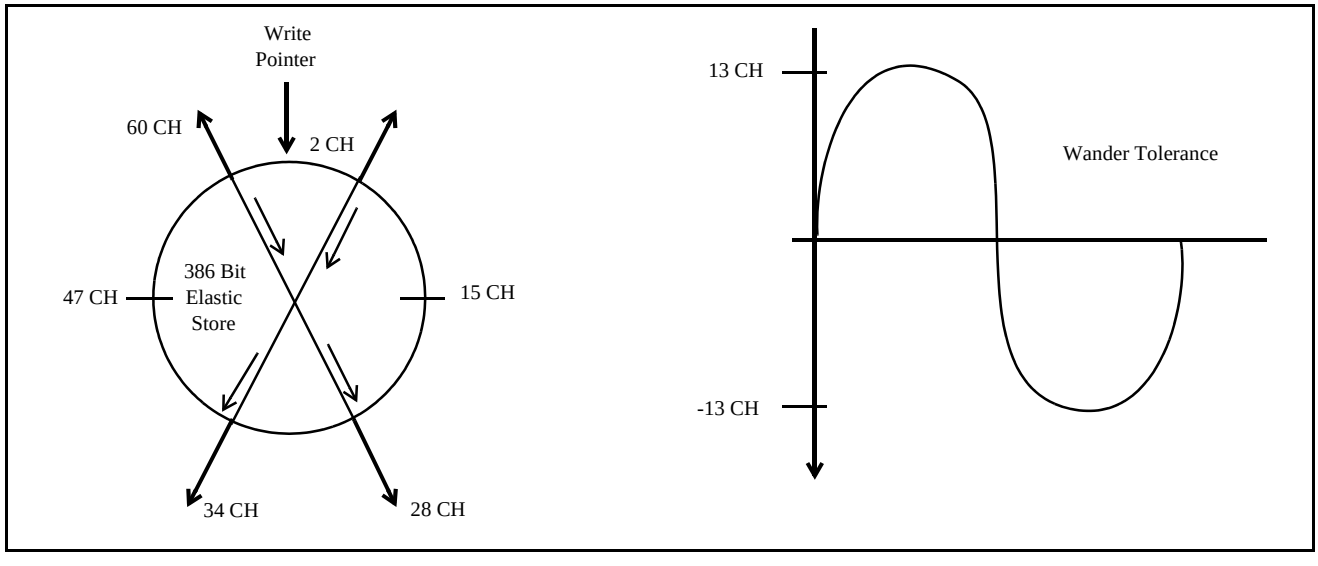


Figure 8 - Elastic Buffer Functional Diagram (156 UI Wander Tolerance)

Under normal operating conditions, the system C2i clock is phase locked to the extracted E1.5i clock using external circuitry. If the two clocks are not phase-locked, then the rate at which the data is being written into the device on the DS1 side may differ from the rate at which it is being read out on the ST-BUS side. The buffer circuit will perform a controlled slip if the throughput delay conditions described above are violated. For example, if the data on the DS1 side is being written in at a rate slower than what it is being read out on the ST-BUS side, the delay between

the received DS1 write pointer and the ST-BUS read pointer will begin to decrease over time. When this delay approaches the minimum two channel threshold, the buffer will perform a controlled slip, which will reset the internal ST-BUS read pointers so that there is exactly 34 channels delay between the two pointers. This will result in some ST-BUS channels containing information output in the previous frame. Repetition of up to one DS1 frame of information is possible.

Conversely, if the data on the DS1 side is being written into the buffer at a rate faster than it is being read out on the ST-BUS side, the delay between the DS1 frame and the ST-BUS frame will increase over time. A controlled slip will be performed when the throughput delay exceeds 60 ST-BUS channels. This slip will reset the internal ST-BUS counters so that there is a 28 channel delay between the DS1 write pointer and the ST-BUS read pointer, resulting in loss of up to one frame of received DS1 data.

Figure 8 illustrates the relationship between the read and write pointers of the receive elastic buffer. Measuring clockwise from the write pointer, if the read pointer comes within two channels of the writer pointer a frame slip will occur, which will put the read pointer 34 channels from the write pointer. Conversely, if the read pointer moves more than 60 channels from the write pointer, a slip will occur, which will put the read pointer 28 channels from the write pointer. This provides a worst case hysteresis of 13 ST-BUS channels peak (26 ST-BUS channels peak-to-peak). This can be translated into a low frequency jitter (wander) tolerance value, accounting for the DS1 to ST-BUS rate conversion, as follows:

$$(1.544/2.048)\ X\ 26\ X\ 8 = 156\ UI\ pp.$$

There is no loss of frame sync, multiframe sync or any errors in the signalling bits when the device performs a slip. The information on the FDL pins in ESF or SLC-96 mode will, however, undergo slips at the same time.

Framing Algorithm

In ESF mode, the framer searches for a correct FPS pattern. Figure 9 shows a state diagram of the framing algorithm. The dotted lines show which feature can be switched in and out depending upon the operating mode of the device.

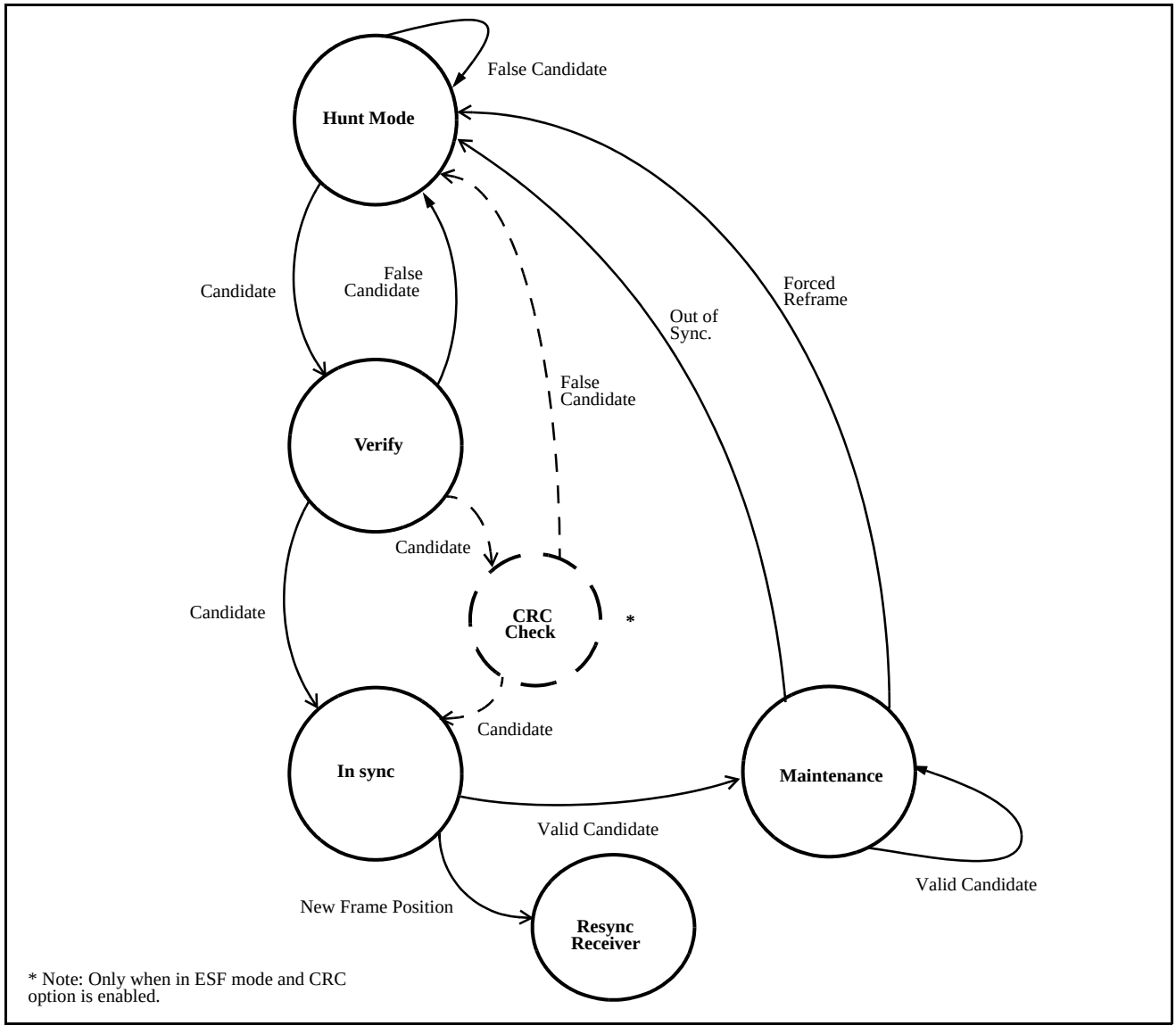


Figure 9 - Off-Line Framer State Diagram

When the device is operating in the D3/D4 format, the framer searches for the F_T pattern, i.e., a repeating 1010... pattern in a specific bit position every alternate frame. It will synchronize to this pattern and declare valid terminal frame synchronization by clearing bit 0 in Master Status Word 1. The device will subsequently initiate a search for the F_S pattern to locate the signalling frames (see Table 4). When a correct F_S pattern has been located, bit 3 in Master Status Word 1 is cleared indicating that the device has achieved multiframe synchronization.

Note: the device will remain in terminal frame synchronization even if no F_S pattern can be located.

In D3/D4 format, when the CRC/MIMIC bit in Master Control Word 1 is cleared, the device will not go into synchronization if more than one bit position in the frame has a repeating 1010.... pattern, i.e., if more than one candidate for the terminal framing position is located. The framer will continue to search until only one terminal framing pattern candidate is discovered. It is, therefore, possible that the device may not synchronize at all in the presence of PCM code sequences (e.g., sequences generated by some types of test signals), which contain mimics of the terminal framing pattern.

Setting CRC/MIMIC bit high will force the framer to synchronize to the first terminal framing pattern detected. In standard D3/D4 applications, the user's system software should monitor the multiframe synchronization state

indicated by bit 3 in Master Status Word 1. Failure of the device to achieve multiframe synchronization within 4.5ms of terminal frame synchronization, is an indication that the device has framed up to a terminal framing pattern mimic and should be forced to reframe.

One of the main features of the framer is that it performs its function "off line". That is, the framer repositions the receive circuit only when it has detected a valid frame position. When the framer exits maintenance mode the receive counters remain where they are until the framer has found a new frame position. This means that if the user forces a reframe when the device was really in the right place, there will not be any disturbance in the circuit because the framer has no effect on the receiver until it has found synchronization. The out of synchronization criterion can be controlled by bit 0 in Master Control Word 2. This bit changes the out of frame conditions for the maintenance state.

The out of sync threshold can be changed from 2 out of 4 errors in F_T (or FPS) to 4 out of 12 errors in F_T (or FPS). The average reframe time is 24 ms for ESF mode, and 12ms for D3/D4 modes.

Figure 10 is a bar graph which shows the probability of achieving frame synchronization at a specific time. The chart shows the results for ESF mode with CRC check, and D3/D4 modes of operation. The average reframe time with random data is 24 ms for ESF, and 13 msec. D3/D4 modes. The probability of a reframe time of 35 ms or less is 88% for ESF mode, and 97% for D3/D4 modes. In ESF mode it is recommended that the CRC check be enabled unless the line has a high error rate. With the CRC check disabled the average reframe time is greater because the framer must also check for mimics.

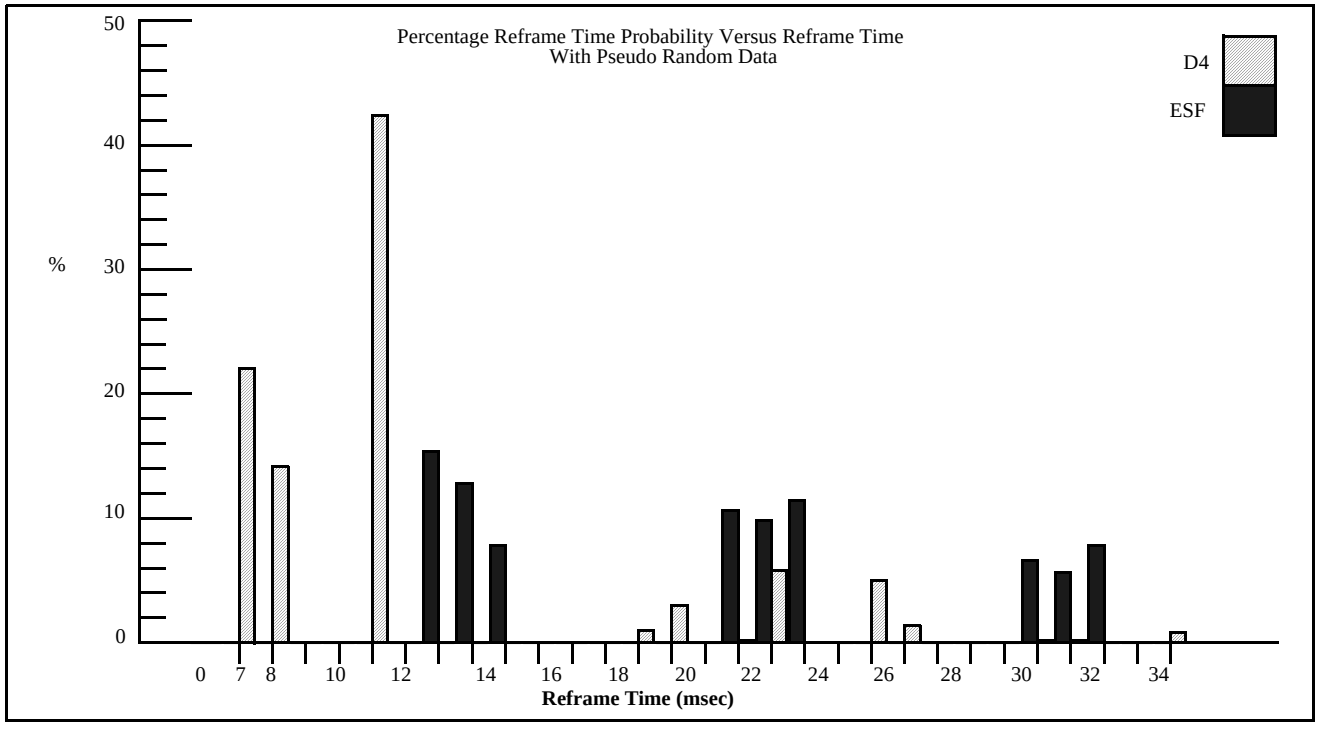


Figure 10 - Reframe Time

Applications

Figure 11 shows the external components that are required in a typical ESF application. The MT8980 is used to control and monitor the device as well as switch data to DSTi and DSTo. The MT8952, the HDLC protocol controller, is shown in this application to illustrate how the data on the FDL could be used. The digital phase-locked loop, the MT8940/41, provides all the clocks necessary to make a functional interface. The clock input to the MT8977 at E1.5i is extracted from the received data signal with an external circuit. The E1.5i clock is internally divided by 193 to obtain an 8 kHz clock which is output at E8Ko. The MT8940 uses this 8 kHz signal to provide a phase locked 2.048 MHz clock for the ST-BUS interface and a 1.544 MHz clock for the DS1 transmit side. Using the 8 kHz signal as a reference for the MT8940/41 DPLL effectively filters out the high frequency jitter in the extracted clock. Thus, the C2 and C1.5 clocks generated by the MT8940/41 will have significantly lower jitter than would be the case if the extracted 1.5 MHz clock was used as a reference directly.

An external line driver circuit is required in order to interface the device to twisted pair cabling. The split phase unipolar signals output by the MT8977 at TxA and TxB are used by the line driver circuit to generate a bipolar AMI signal. The line driver is transformer coupled to an equalization circuit and the DS1 line. Equalization of the transmitted signal is required to meet the specifications for crossconnect compatible equipment (see ANSI T1.102 and AT & T Technical Advisory #34). On the receive side the bipolar line signal is converted into a unipolar format by the line receiver circuit. The resulting split phase signals are input at the $\overline{\text{RxA}}$ and $\overline{\text{RxB}}$ pins on the MT8977. The signals are combined together to produce a composite return to zero signal which is clocked into the device at RxD. An uncommitted nand gate in the MT8940/41 can be used for this purpose.

The MT8977 can be interfaced to a high speed parallel bus or to a microprocessor using the MT8920B Parallel Access Circuit (STPA). Figure 11 shows the MT8977 interfaced to a parallel bus structure using two STPA‘s operating in modes 1 and 2.

The first STPA operating in mode 2 (MMS=0, MS1=1, $\overline{24}$/32=0), routes data and/or voice information between the parallel telecom bus and the T1 or CEPT link via DSTi and DSTo. The second STPA, operating in mode 1 (MMS = 1) provides access from the signalling and link control bus to the MT8977 status and control channels. All signalling and link functions may be controlled easily through the STPA transmit RAM’s Tx0, Tx1, while status information is read at receive RAM Rx0. In addition, interrupts can be set up to notify the system in case of slips, loss of sync, alarms, violations, etc.

Note: the configurations shown in Figures 11 and 12 using the MT8940/41 may not meet specific jitter performance requirements. A more sophisticated PLL or line interface unit with transmit jitter attenuator may be required for applications designed to meet specific standards.

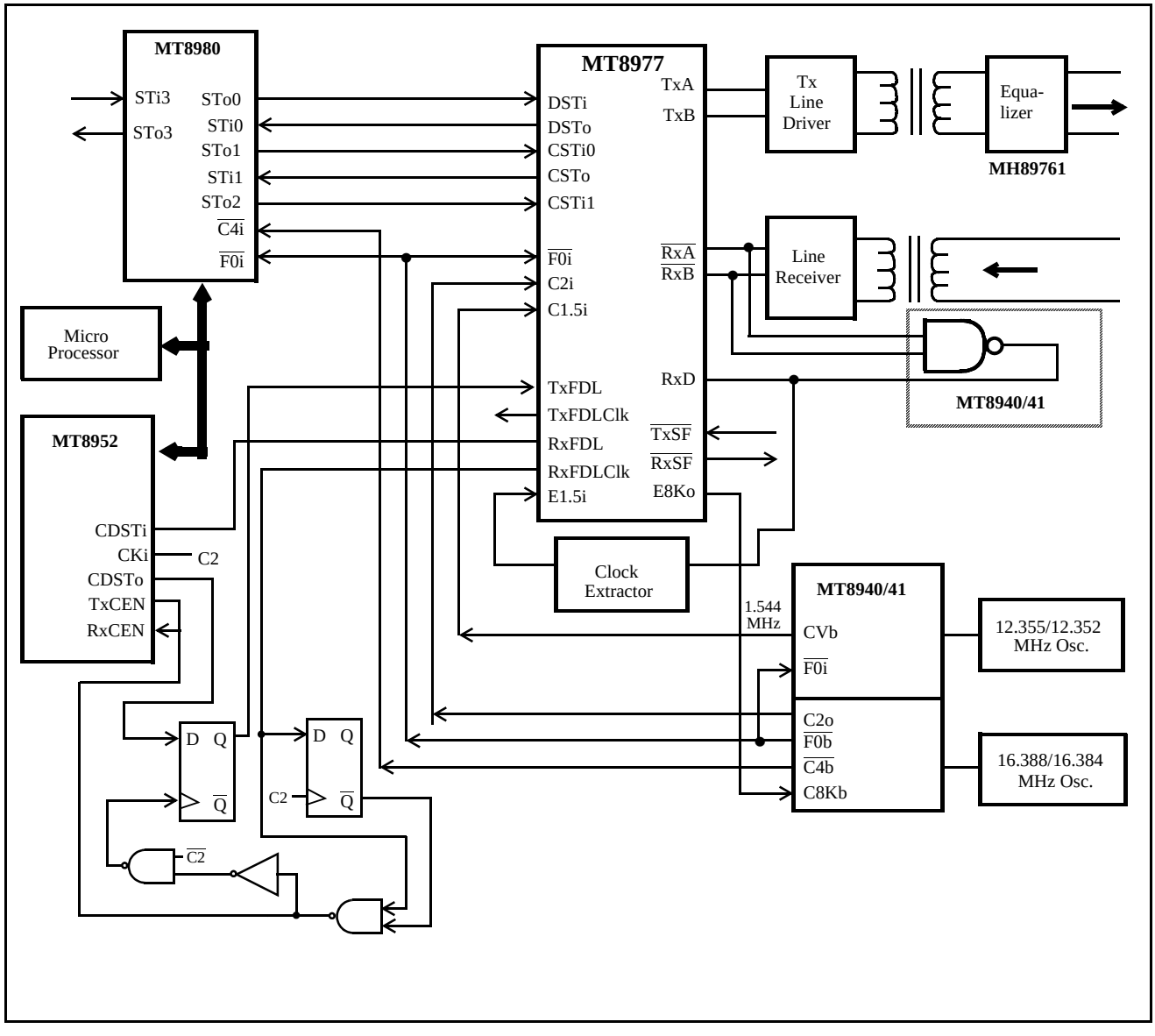


Figure 11 - Typical ESF Configuration

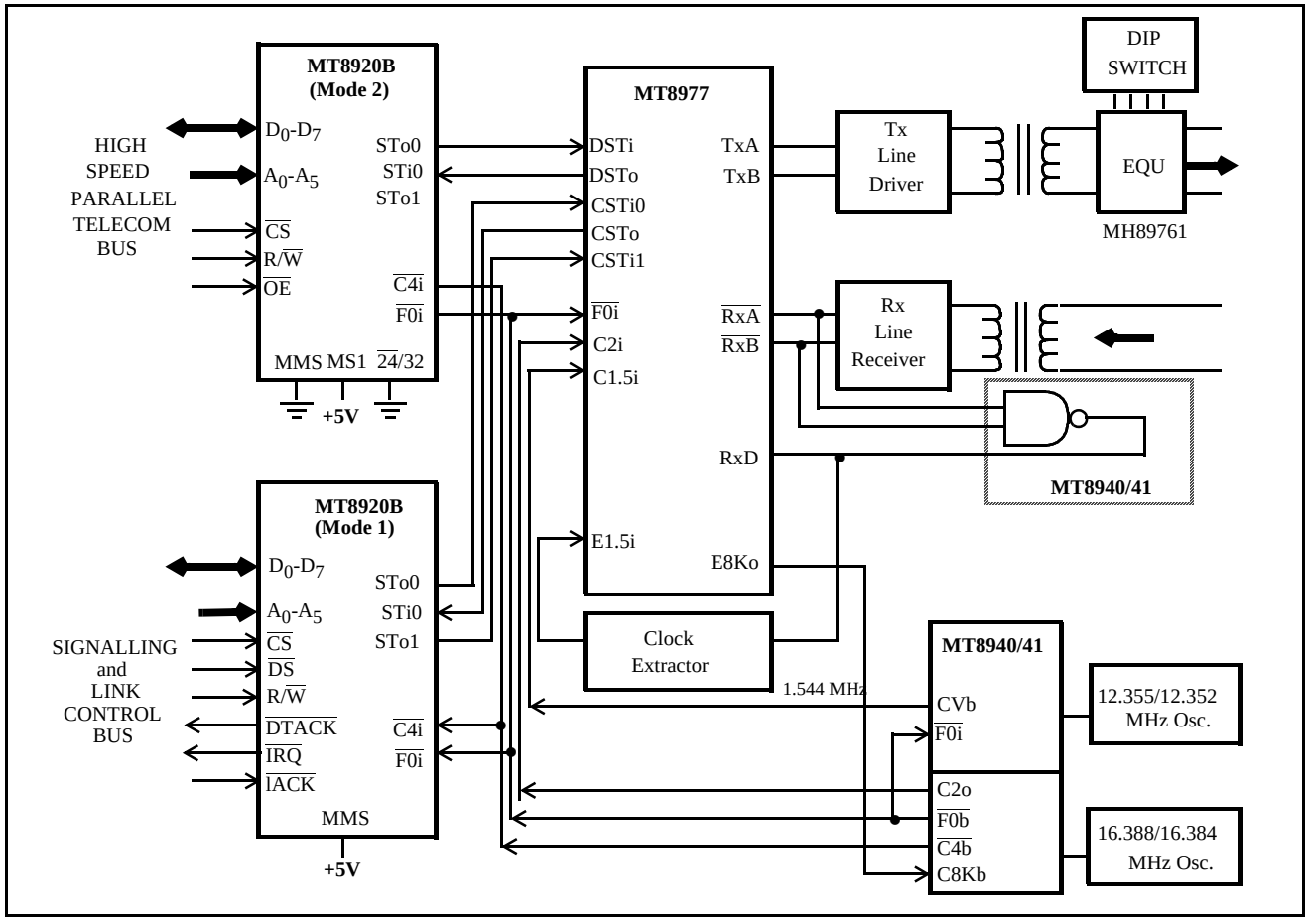


Figure 12 - Using the MT8977 in a Parallel Bus Environment

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Power Supplies with respect to V_{SS}	V_{DD}	-0.3	7	V
2	Voltage on any pin other than supplies		V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin other than supplies			40	mA
4	Storage Temperature	T_{ST}	-55	125	°C
5	Package Power Dissipation	P		800	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Inputs	Operating Temperature	T_{OP}	-40		85	°C	
2		Power Supplies	V_{DD}	4.5	5.0	5.5	V	
3		Input High Voltage	V_{IH}	2.4		V_{DD}	V	For 400 mV noise margin
4		Input Low Voltage	V_{IL}	V_{SS}		0.4	V	For 400 mV noise margin

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Clocked operation over recommended temperature ranges and power supply voltages.

		Parameters	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Inputs	Supply Current	I_{DD}		6	10	mA	Outputs Unloaded
2		Input High Voltage	V_{IH}	2.0			V	Digital Inputs
3		Input Low Voltage	V_{IL}			0.8	V	Digital Inputs
4		Input Leakage Current	I_{IL}		±1	±10	µA	Digital Inputs V_{IN}=0 to V_{DD}
5		Schmitt Trigger Input (XSt)	V_{T+}			4.0	V	
			V_{T-}	1.5			V	
6	Outputs	Output High Current	I_{OH}	7	20		mA	Source Current, V_{OH}=2.4V
7		Output Low Current	I_{OL}	2	10		mA	Sink Current, V_{OL}=0.4V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Capacitance

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input Pin Capacitance	C_I		10		pF	
2	Output Pin Capacitance	C_O		10		pF	

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Clock Timing (Figures 13 & 14)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	C2i Clock Period	t_{P20}	400	488	600	ns	
2	C2i Clock Width High or Low	t_{W20}	200	244	300	ns	t_{P20} = 488 ns
3	Frame Pulse Setup Time	t_{FPS}	50			ns	
4	Frame Pulse Hold Time	t_{FPH}	50			ns	
5	Frame Pulse Width	t_{FPW}	50			ns	
6	$\overline{\text{RxSF}}$ Output Delay	t_{FPOD}			125	ns	50 pF Load
7	$\overline{\text{TxSF}}$ Hold Time	t_{TxSFH}	0.5		124.5	µs	
8	$\overline{\text{TxSF}}$ Setup Time	t_{TxSFS}	0.5		124.5	µs	

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

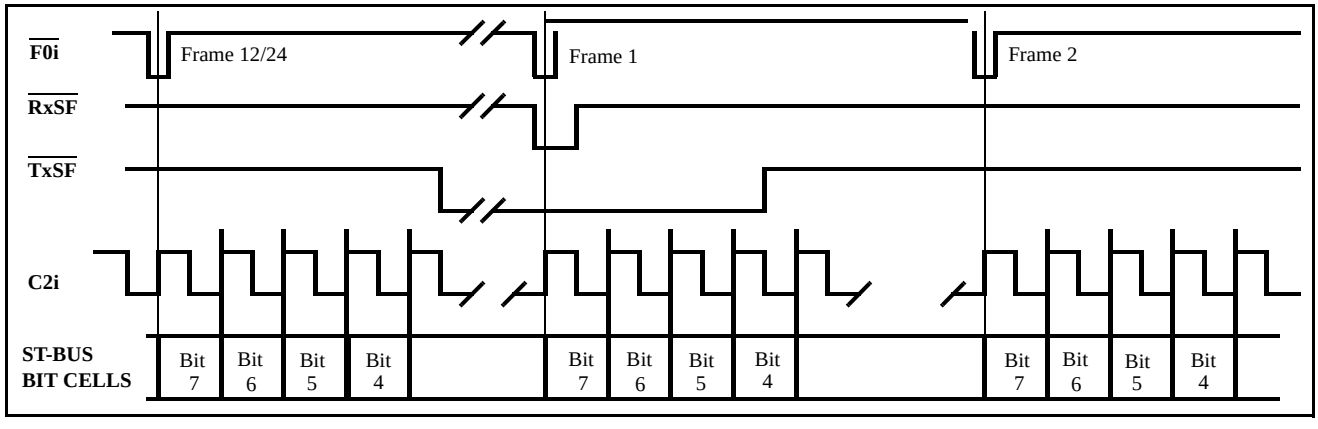


Figure 13 - Clock & Frame Alignment for ST-BUS Streams

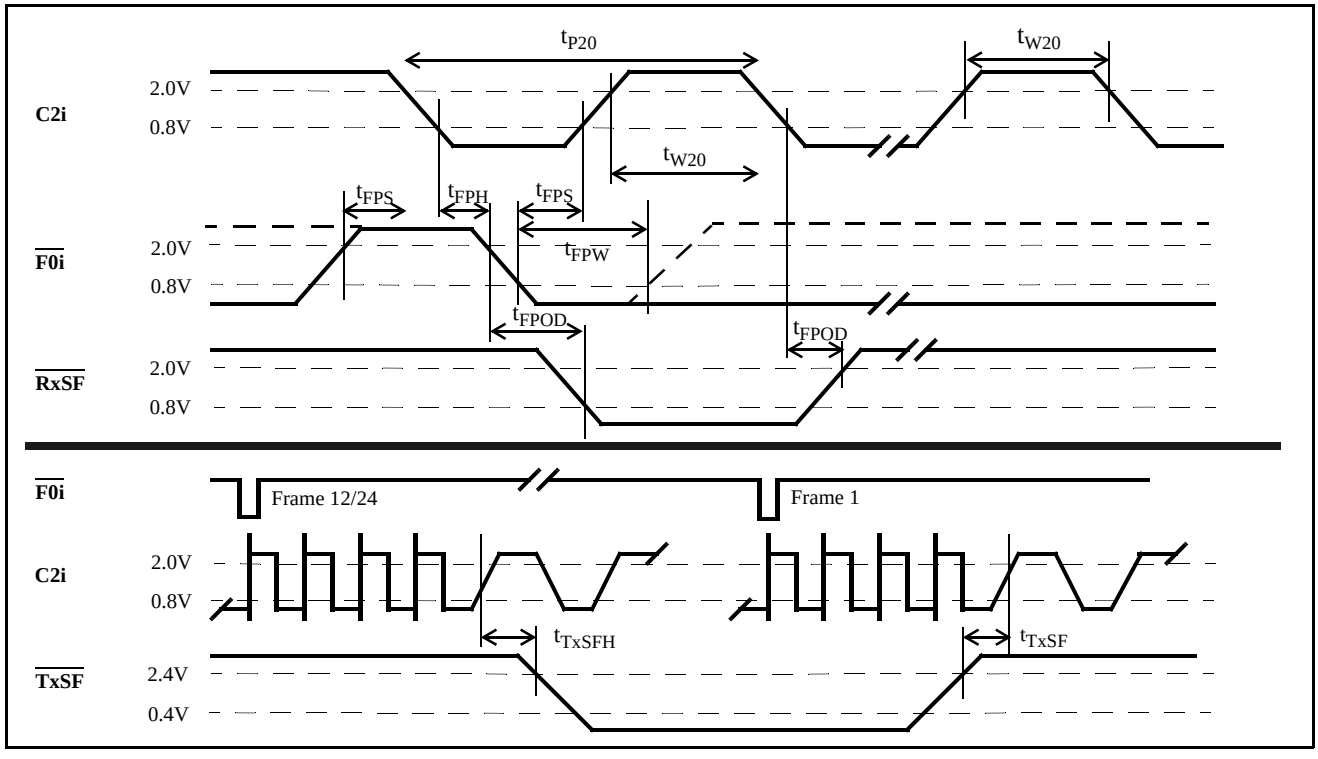


Figure 14 - Clock & Pulse Timing for ST-BUS Streams

AC Electrical Characteristics† - Timing For DS1 Link Bit Cells (Figure 15)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	E1.5i Clock Period	t_{PEC}	500	648		ns	
2	E1.5i Clock Width High or Low	t_{WEC}	250	324		ns	t_{PEC} = 648 ns

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

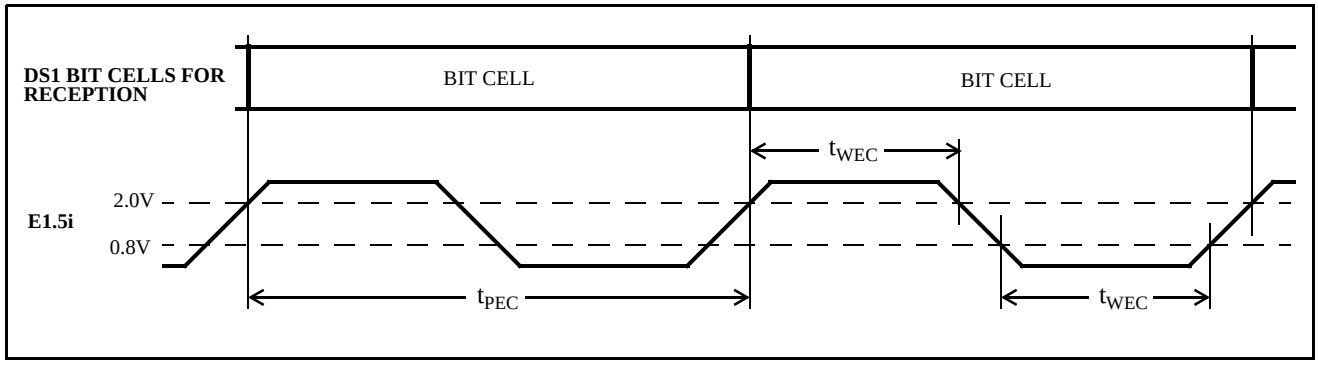


Figure 15 - DS1 Receive Clock Timing

AC Electrical Characteristics† - 2048 kbit/s ST-BUS Streams (Figure 16)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Serial Output Delay	t_{SOD}			125	ns	150 pF load
2	Serial Input Setup Time	t_{SIS}	15			ns	
3	Serial Input Hold Time	t_{SIH}	50			ns	

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

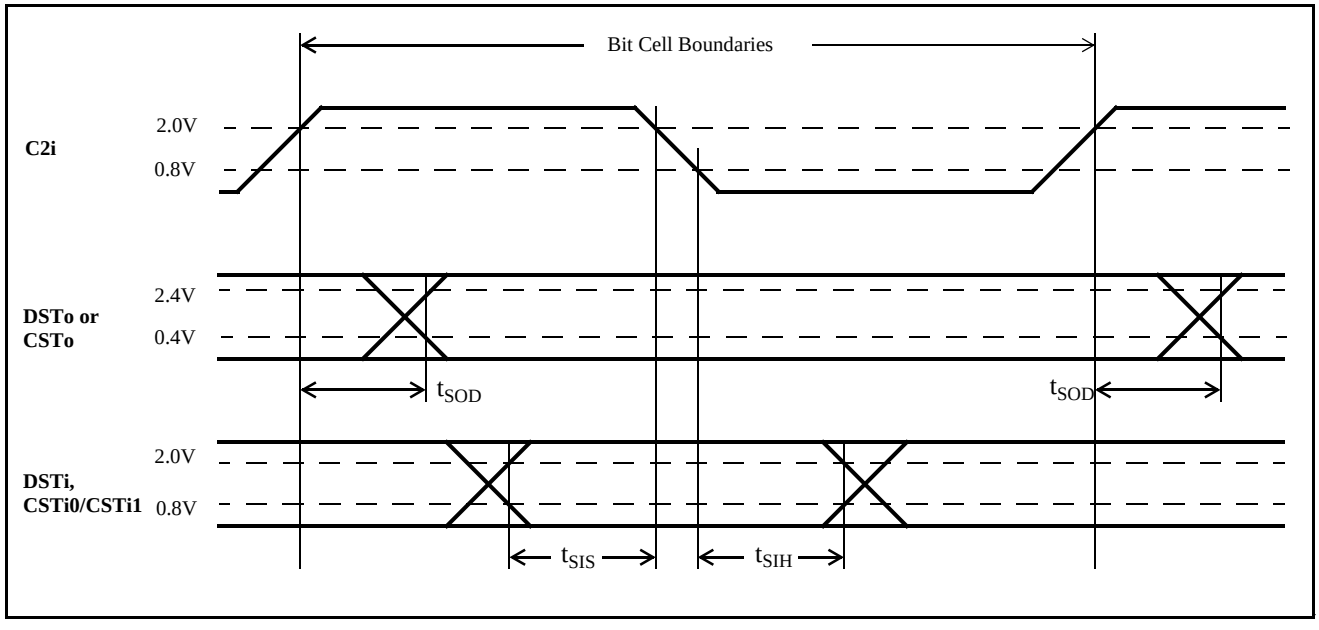


Figure 16 - ST-BUS Stream Timing

AC Electrical Characteristics† - XCtl, XSt, & E8Ko (Figures 17, 18 and 19)

	Parameters	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	External Control Delay	t_{XCD}			140	ns	50 pF Load
2	External Status Setup Time	t_{XSS}			100	ns	
3	External Status Hold Time	t_{XSH}			400	ns	
4	8 kHz Output Delay	t_{8OD}			150	ns	50 pF Load
5	8 kHz Output Low Width	t_{8OL}		78		µs	50 pF Load
6	8 kHz Output High Width	t_{8OH}		47		µs	50 pF Load
7	8 kHz Rise Time	t_{8R}			10	ns	50 pF Load
8	8 kHz Fall Time	t_{8F}			10	ns	50 pF Load

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

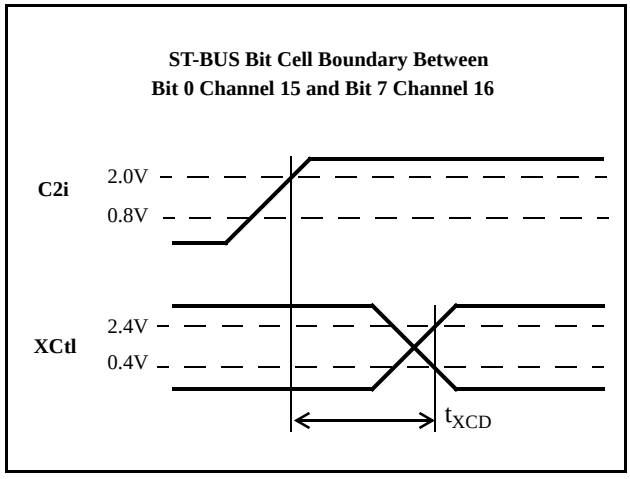


Figure 17 - XCtl Timing

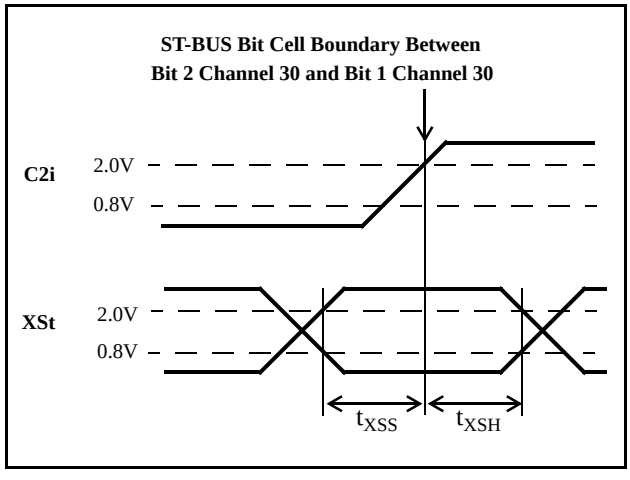


Figure 18 - XSt Timing

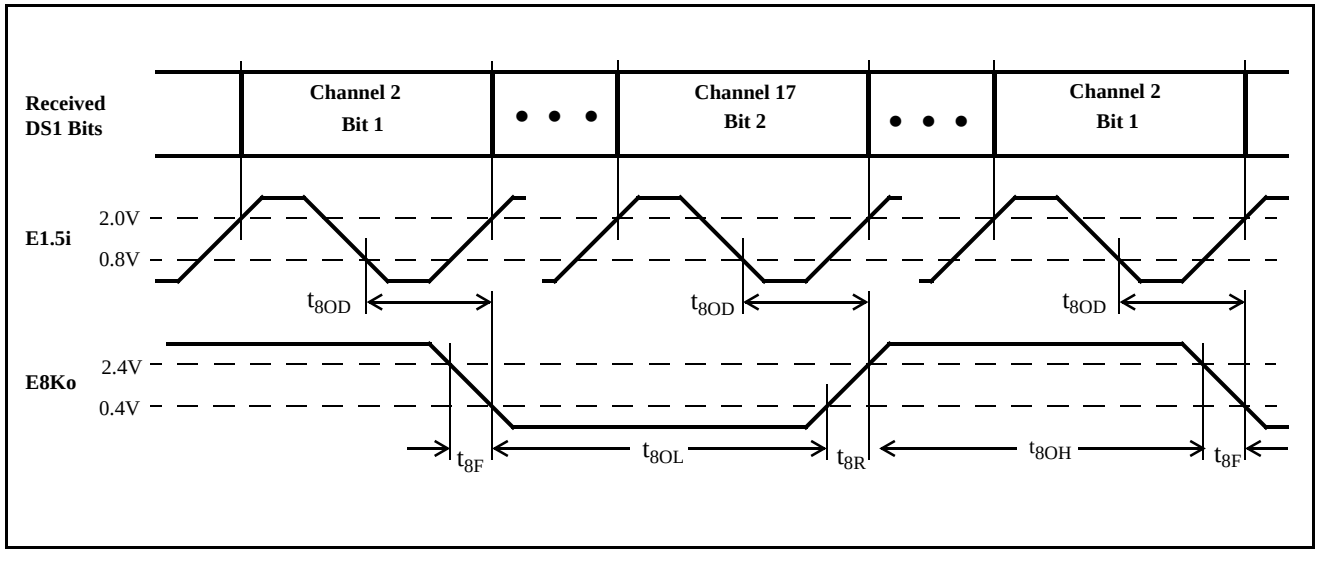


Figure 19 - E8Ko Timing

AC Electrical Characteristics† - DS1 Link Timing (Figures 20 and 21)

	Parameters	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Transmit Steering Delay	t_{TSD}	50		150	ns	150 pF Load
2	Transmit Steering Transition Time	t_{TST}			30	ns	150 pF Load
3	Received Steering Setup Time	t_{RSS}	0			ns	
4	Received Steering Hold Time	t_{RSH}	30			ns	
5	Received Data Setup Time	t_{RDS}	-15			ns	See Note 1
6	Received Data Hold Time	t_{RDH}	60			ns	See Note 1
7	C1.5i Period	$t_{PC1.5}$	500	648	800	ns	
8	C1.5i Pulse Width High or Low	$t_{WC1.5}$	250	324		ns	$t_{PC1.5}$ = 648 ns

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

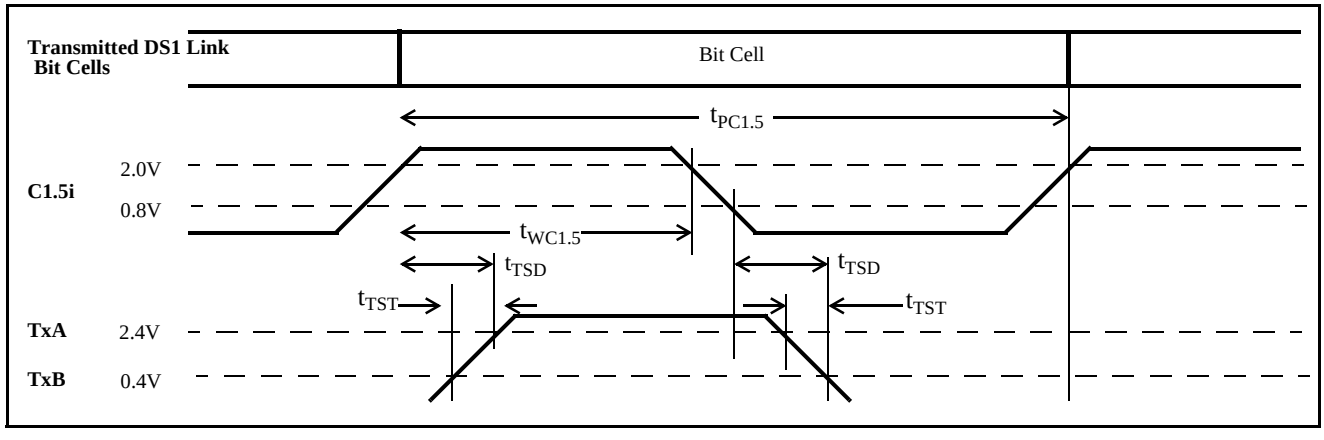


Figure 20 - Transmit Timing for DS1 Link

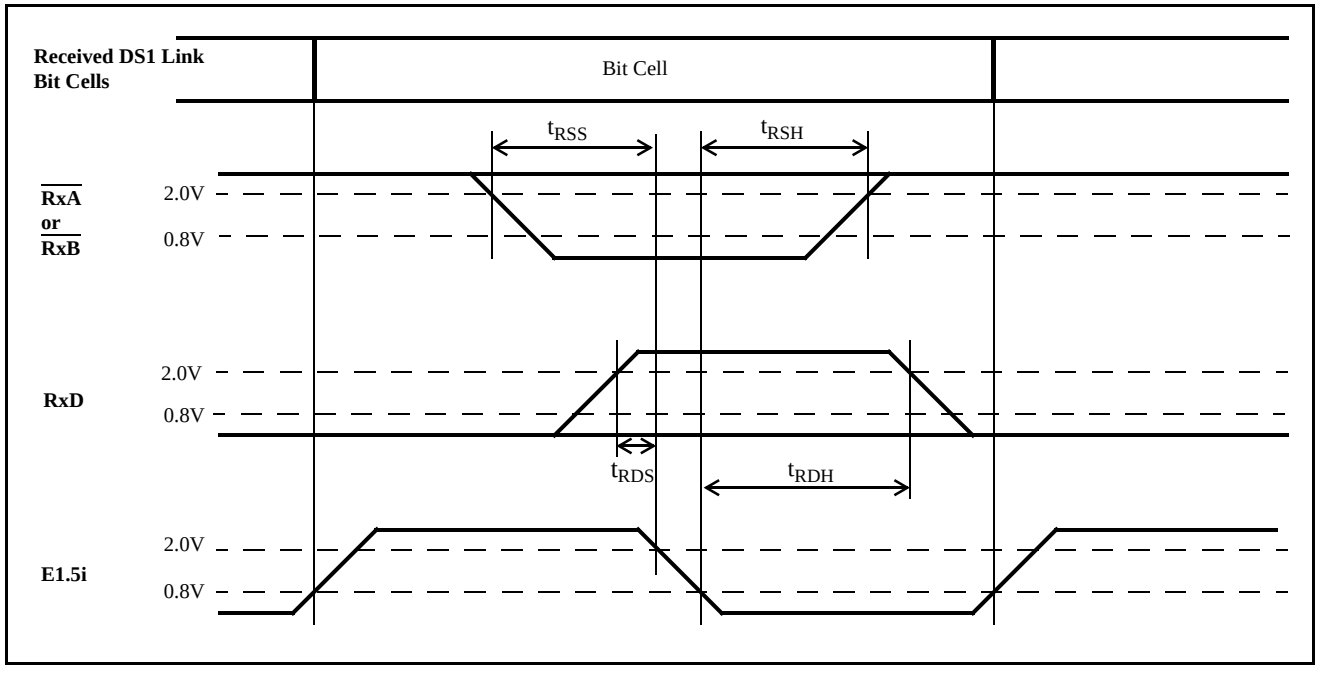


Figure 21 - Receive Timing for DS1 Link (see Note 1)

Note 1: The parameters t_{RDS} and t_{RDH} are related to device functionality. Network constraints may require tighter tolerances than the device specifications.

AC Electrical Characteristics† - DS1 Link Timing (Figures 22 and 23)

	Parameters	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Transmit FDL Setup Time	t_{DLS}	110			ns	
2	Transmit FDL Hold Time	t_{DLH}	70			ns	
3	Receive FDL Output Delay	t_{DLOD}			0	ns	50 pF Load
4	Receive FDL Clock Delay	t_{FRCD}			185		50 pF Load
5	Transmit FDL Clock Delay	t_{TFCD}			135	ns	50 pF Load

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

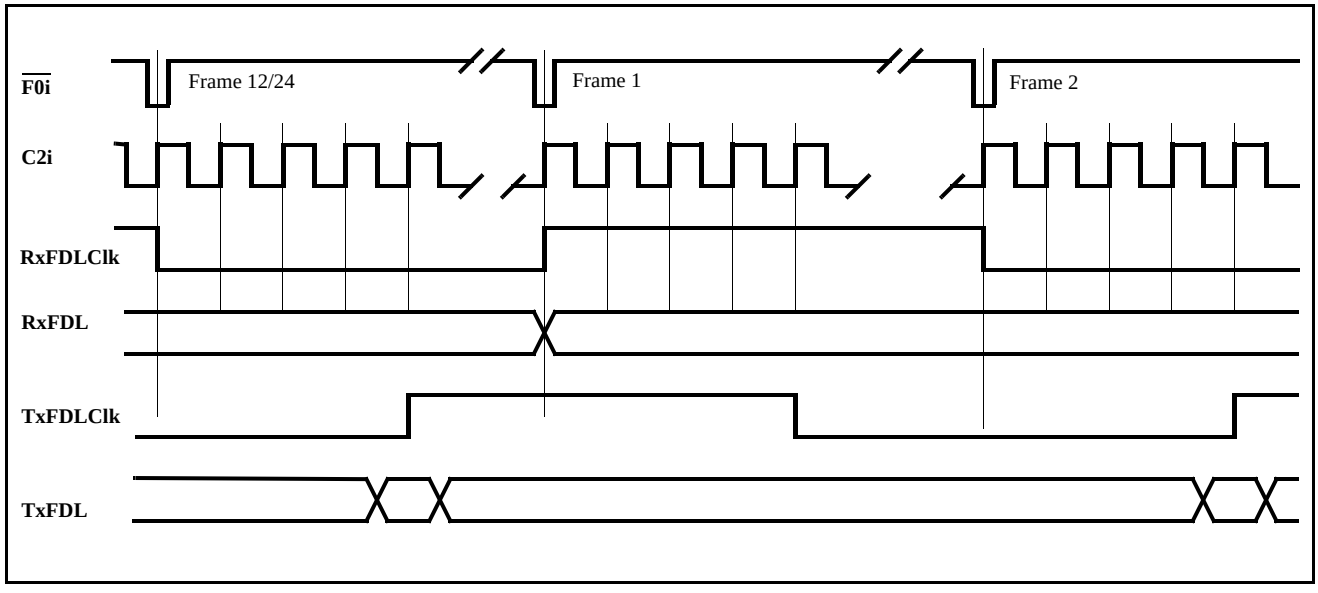


Figure 22 - Clock & Frame Alignment for RxFDL and TxFDL

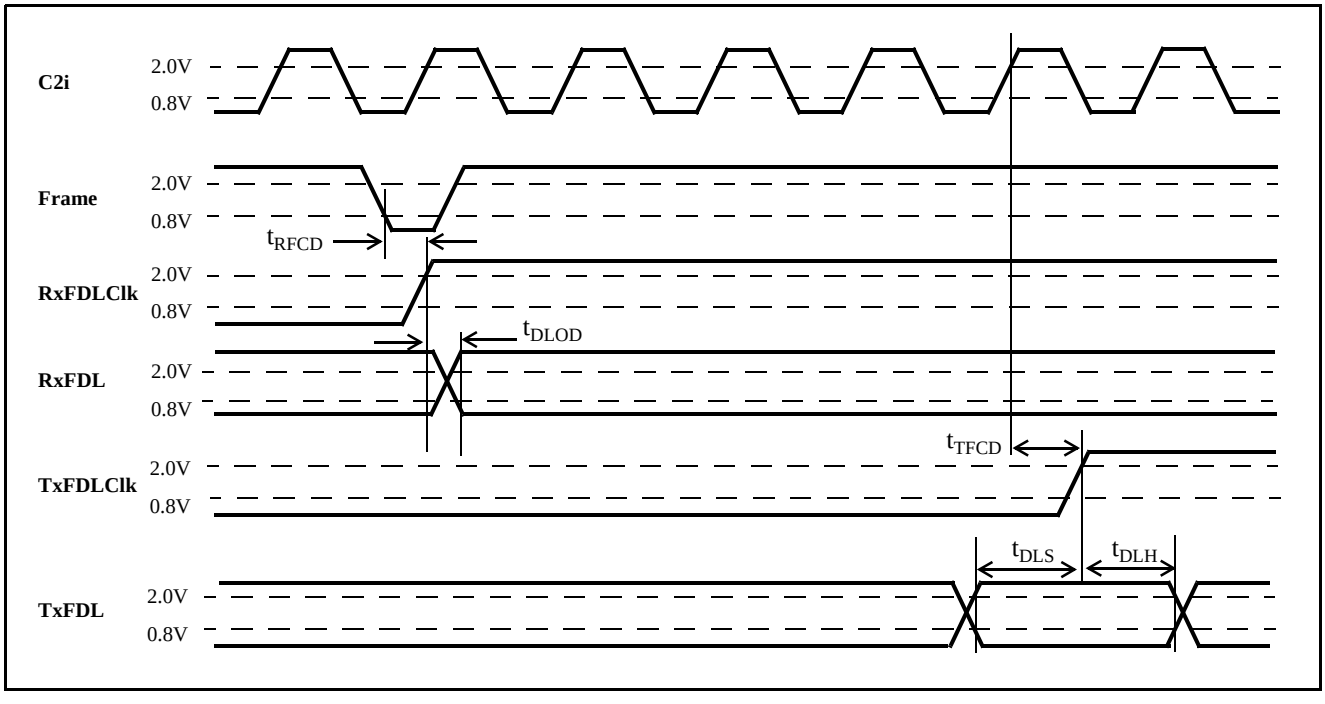


Figure 23 - Facility Data Link Timing

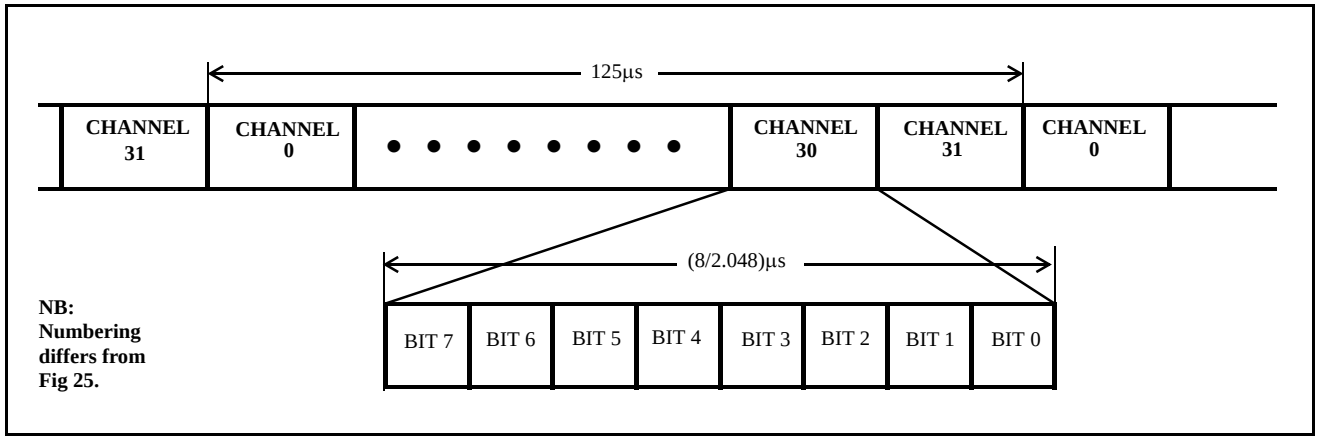


Figure 24 - Format of 2048 kbit/s ST-BUS Streams

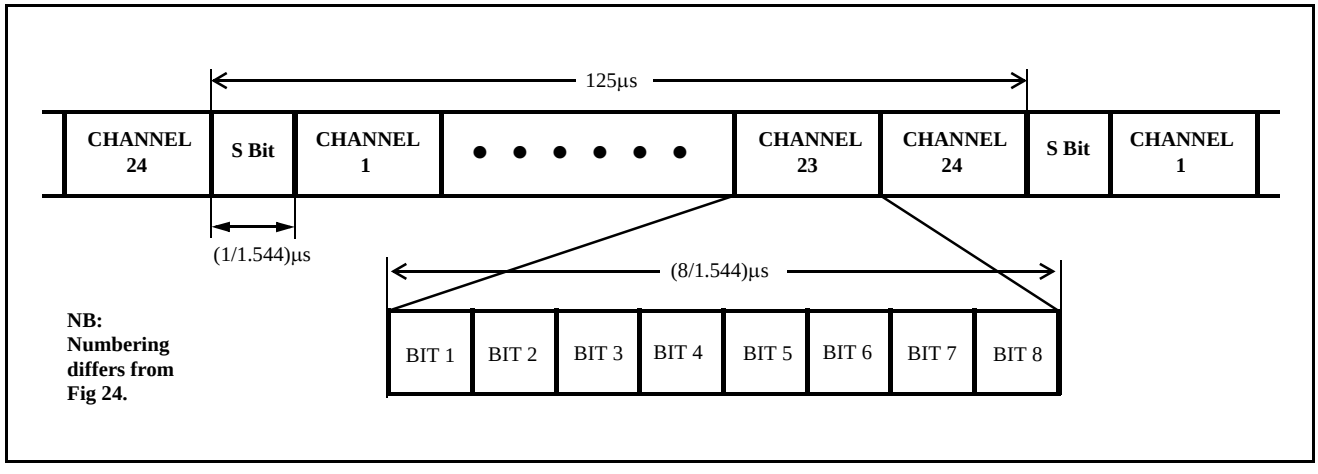


Figure 25 - DS1 Link Frame Format

Appendix

Control and Status Register Summary

7	6	5	4	3	2	1	0
Debounce 1 Disabled 0 Enabled	**TSPZCS** 1 Disabled 0 Enabled	**B8ZS** 1 B8ZS 0 Jammed Bit	**8KHSel** 1 Disabled 0 Enabled	**XCtI** 1 Set High 0 Cleared	**ESFYLW** 1 Enabled 0 Disabled	**Robbed Bit** 1 Disabled 0 Enabled	**YLALR** 1 Enabled 0 Disabled

Master Control Word 1 (Channel 15, CSTi0)

RMLOOP 1 Enabled 0 Disabled	**DGLOOP** 1 Enabled 0 Disabled	**ALL 1's** 1 Enabled 0 Disabled	**ESF/D4** 1 ESF 0 D3/D4	**Reframe** Device Reframes on High to Low Transition	**SLC-96** 1 Enabled 0 Disabled	**CRC/MIMIC** See Note 1	**Maint.** 1 4/12 0 2/4

Master Control Word 2 (Channel 31, CSTi0)

UNUSED - KEEP AT 0	**Polarity** 1 No Inversion 0 Inversion	**Loop** 1 Ch. looped back 0 Normal	**Data** 1 Enabled 0 Disabled

Per Channel Control Words (All Channels on CSTi0 Except Channels 3, 7, 11, 15, 19, 23, 27 and 31)

UNUSED - KEEP AT 0	**A** Txt. Sig. Bit	**B** Txt. Sig. Bit	**C** Txt. Sig. Bit	**D** Txt. Sig. Bit

Per Channel Control Words (All Channels on CSTi1 Except Channels 3, 7, 11, 15, 19, 23, 27 and 31)

YLAIR 1 Detected 0 Normal	**MIMIC** 1 Detected 0 Not Detected	**ERR** F_T Error Count	**ESFYLW** 1 Detected 0 Not Detected	**MFSYNC** 1 Not Detected 0 Detected	**BPV** Bipolar Violation count	**SLIP** Changes State when Slip Performed	**SYN** 1 Out-of-Sync. 0 In-Sync

Master Status Word 1 (Channel 15, CSTo)

BlAlm 1 Detected 0 Not Detected	**FrCnt** Frame Count	**XSt** 1 Xst High 0 Xst Low	**BIPOLAR VIOLATION COUNT**	**CRC-ERROR COUNT**

Master Status Word 2 (Channel 31, CSTo)

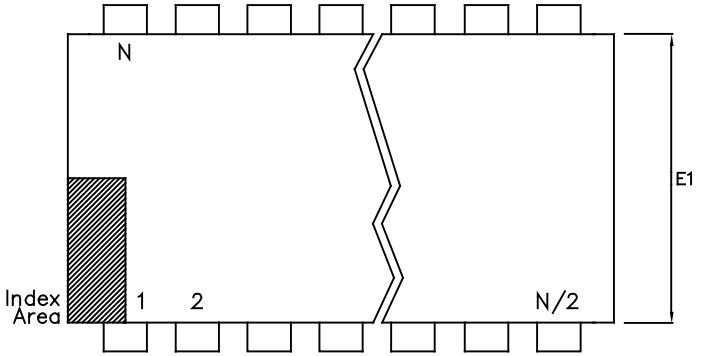
CHANNEL COUNT	**BIT COUNT**

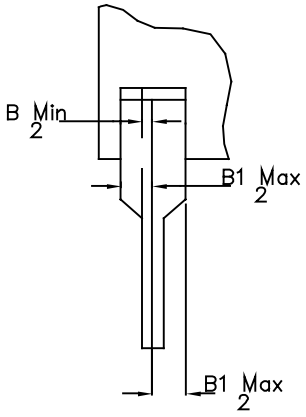
Phase Status Word (Channel 3, CSTo)

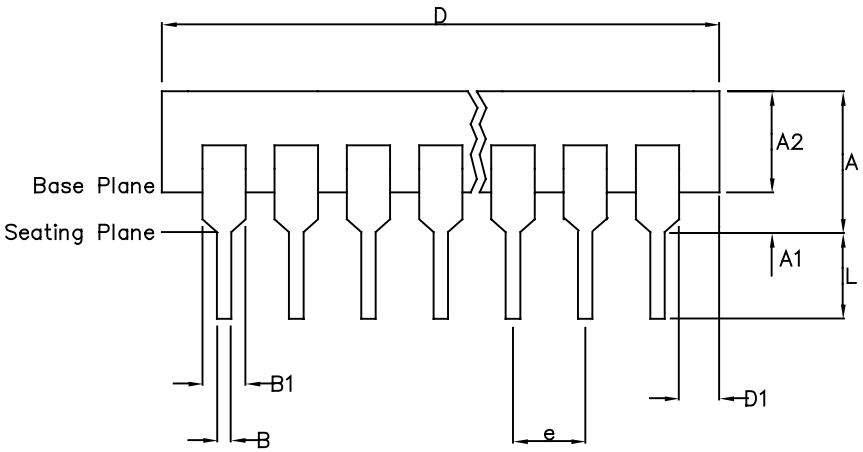
UNUSED	**A** Rec'd. Sig. Bit	**B** Rec'd. Sig. Bit	**C** Rec'd. Sig. Bit	**D** Rec'd. Sig. Bit

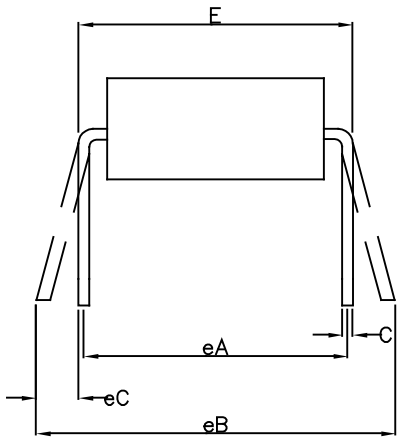
Per Channel Status Word (All Channels on CSTo Except Channels 3, 7, 11, 15, 19, 23, 27, 31)

Note 1: In ESF mode:
1: CRC calc. ignored during Sync.
0: CRC checked for Sync.
In D3/D4 mode:
1: Sync. to first correct S-bit pattern.
0: Will not Sync. if Mimic detected.









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	35.05	39.75	1.380	1.565
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	28		28	
Conforms to Jedec MS-011AB ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	4
ACN	7010	203532	213102	CDCA
DATE	20Apr95	25Nov97	15Jul02	02Dec05
APPRD.				

ZARLINK SEMICONDUCTOR

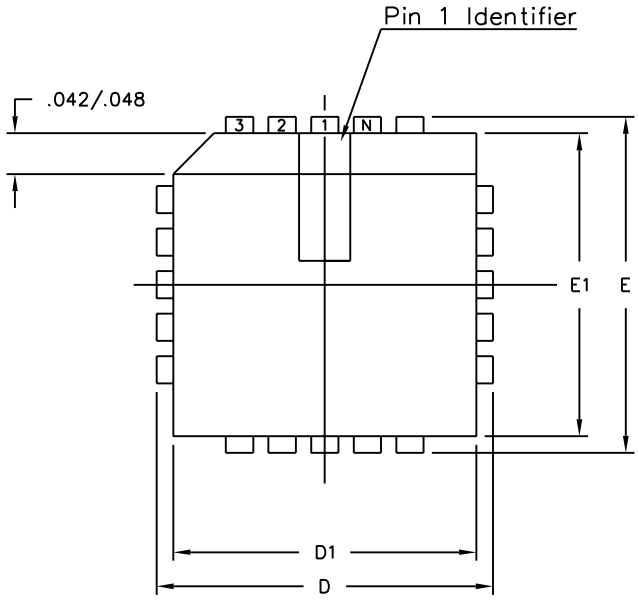
Previous package codes

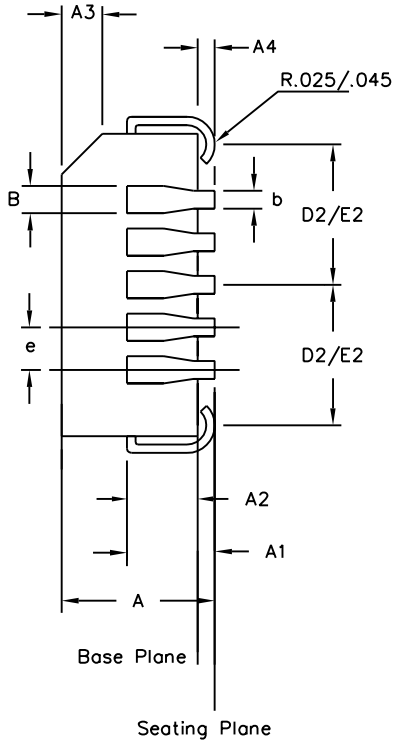
DP / E

Package Code DA

Package Outline for
28 lead 600mils PDIP

GPD00072





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207470	213094	
DATE	15Aug94	10Sep99	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

HP / P

Package Code QA

Package Outline for 44 lead PLCC

GPD00003

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visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE