

Section 15. Electrical Specifications

15.1 Absolute Maximum Ratings

Table 15-1 lists the absolute maximum ratings.

Table 15-1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	−0.3 to +7.0	V
Programming voltage	V _{PP}	−0.3 to +13.5	V
Input voltage	V _{in}	−0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	Regular specifications: −20 to +75	°C
		Wide-range specifications: −40 to +85	°C
Storage temperature	T _{stg}	−55 to +125	°C

Note: The input pins have protection circuits that guard against high static voltages and electric fields, but these high input-impedance circuits should never receive overvoltages exceeding the absolute maximum ratings shown in table 15-1.

15.2 Electrical Characteristics

15.2.1 DC Characteristics

Tables 15-2 and 15-3 list the DC characteristics of the H8/325 series.

Table 15-2. DC Characteristics (5V Version)Conditions: $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications) $T_a = -40$ to $85^\circ C$ (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement conditions
Schmitt trigger	P66 to P63, P60,	V_{T^-}	1.0	–	–	V	
input voltage	P70	V_{T^+}	–	–	$V_{CC} \times 0.7$	V	
(1)		$V_{T^+} - V_{T^-}$	0.4	–	–	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$	V_{IH}	$V_{CC} - 0.7$	–	$V_{CC} + 0.3$	V	
(2)	MD1, MD0 EXTAL, $\overline{NMI}$						
Input high voltage	Input pins other than (1) and (2)	V_{IH}	2.0	–	$V_{CC} + 0.3$	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$	V_{IL}	–0.3	–	0.5	V	
(3)	MD1, MD0, EXTAL						
Input low voltage	Input pins other than (1) and (3)	V_{IL}	–0.3	–	0.8	V	
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$ 3.5	– –	– –	V V	$I_{OH} = -200 \mu A$ $I_{OH} = -1.0 mA$
Output low voltage	All output pins P17 to P10, P27 to P20	V_{OL}	– –	– –	0.4 1.0	V V	$I_{OL} = 1.6 mA$ $I_{OL} = 10.0 mA$
Input leakage current	$\overline{RES}$	I_{iinl}	–	–	10.0	μA	$V_{in} = 0.5 V$ to $V_{CC} - 0.5 V$
	$\overline{STBY}$, $\overline{NMI}$, MD1, MD0		–	–	1.0	μA	
Leakage current in 3-state (off state)	Ports 1 to 7	I_{ITSil}	–	–	1.0	μA	$V_{in} = 0.5 V$ to $V_{CC} - 0.5 V$
Input pull-up MOS current	Ports 1 to 7	$-I_p$	30	–	250	μA	$V_{in} = 0 V$

Table 15-2. DC Characteristics (5V Version) (cont.)Conditions: $V_{CC} = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications) $T_a = -40$ to $85^\circ C$ (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement
							conditions
Input capacitance	$\overline{RES}$	C_{in}	–	–	60	pF	$V_{in} = 0V$
	$\overline{NMI}$		–	–	30	pF	$f = 1MHz$
	All input pins except $\overline{RES}$ and $\overline{NMI}$		–	–	15	pF	$T_a = 25^\circ C$
Current dissipation*1	Normal operation	I_{CC}	–	12	25	mA	$f = 6MHz$
			–	16	30	mA	$f = 8MHz$
			–	20	40	mA	$f = 10MHz$
	Sleep mode		–	8	15	mA	$f = 6MHz$
			–	10	20	mA	$f = 8MHz$
			–	12	25	mA	$f = 10MHz$
	Standby modes*2		–	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	–	–	V	

Notes: 1. Current dissipation values assume that $V_{IH \min.} = V_{CC} - 0.5V$, $V_{IL \max.} = 0.5V$, all output pins are in the no-load state, and all MOS input pull-ups are off.

2. For these values it is assumed that $V_{RAM} \leq V_{CC} < 4.5V$ and $V_{IH \min.} = V_{CC} \times 0.9$, $V_{IL \max.} = 0.3V$.

Table 15-3. DC Characteristics (3V Version for only H8/3257 and H8/3256)Conditions: $V_{CC} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $75^{\circ}C$

Item		Symbol	min	typ	max	Unit	Measurement
							conditions
Schmitt trigger	P66 to P63, P60,	$V_{T^{-}}$	$V_{CC} \times 0.15$	–	–	V	
input voltage	P70	$V_{T^{+}}$	–	–	$V_{CC} \times 0.7$	V	
(1)		$V_{T^{+}} - V_{T^{-}}$	0.2	–	–	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$	V_{IH}	$V_{CC} \times 0.9$	–	$V_{CC} + 0.3$	V	
(2)	MD1, MD0 EXTAL, $\overline{NMI}$						
Input high voltage	Input pins	V_{IH}	$V_{CC} \times 0.7$	–	$V_{CC} + 0.3$	V	
	other than (1)						
	and (2)						
Input low voltage	$\overline{RES}$, $\overline{STBY}$	V_{IL}	–0.3	–	$V_{CC} \times 0.1$	V	
(3)	MD1, MD0, EXTAL						
Input low voltage	Input pins	V_{IL}	–0.3	–	$V_{CC} \times 0.15$	V	
	other than (1)						
	and (3)						
Output high	All output pins	V_{OH}	$V_{CC} - 0.4$	–	–	V	$I_{OH} = -200 \mu A$
voltage			$V_{CC} - 0.9$	–	–	V	$I_{OH} = -1.0 \text{ mA}$
Output low	P17 to P10,	V_{OL}	–	–	0.4	V	$I_{OL} = 1.6 \text{ mA}$
voltage	P27 to P20						
	All output pins		–	–	0.4	V	$I_{OL} = 0.8 \text{ mA}$
Input leakage	$\overline{RES}$	I_{inl}	–	–	10.0	μA	$V_{in} = 0.5 \text{ V to}$
current	$\overline{STBY}$, $\overline{NMI}$,		–	–	1.0	μA	$V_{CC} - 0.5 \text{ V}$
	MD1, MD0						
Leakage current	Ports 1 to 7	I_{ITSII}	–	–	1.0	μA	$V_{in} = 0.5 \text{ V to}$
in 3-state (off state)							$V_{CC} - 0.5 \text{ V}$
Input pull-up	Ports 1 to 7	$-I_p$	3	–	120	μA	$V_{CC} = 3.3 \text{ V}$
MOS current							$V_{in} = 0 \text{ V}$

Table 15-3. DC Characteristics (3V Version for only H8/3257 and H8/3256) (cont.)Conditions: $V_{CC} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $75^{\circ}C$

Item		Symbol	min	typ	max	Unit	Measurement conditions
Input capacitance	$\overline{RES}$	C_{in}	–	–	60	pF	$V_{in} = 0V$
	$\overline{NMI}$		–	–	30	pF	$f = 1MHz$
	All input pins except $\overline{RES}$ and $\overline{NMI}$		–	–	15	pF	$T_a = 25^{\circ}C$
Current dissipation*	Normal operation	I_{CC}	–	4	–	mA	$f = 3MHz$
	Sleep mode		–	3	–	mA	
	Normal operation		–	6	12	mA	$f = 5MHz$
	Sleep mode		–	4	8	mA	
	Standby modes		–	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	–	–	V	

Note: Current dissipation values assume that $V_{IH\ min.} = V_{CC} - 0.5V$, $V_{IL\ max.} = 0.5V$, all output pins are in the no-load state, and all MOS input pull-ups are off.

Table 15-4. Allowable Output Current Sink Values

Conditions: $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20$ to $75^{\circ}C$ (regular specifications)
 $T_a = -40$ to $85^{\circ}C$ (wide-range specifications)

Item		Symbol	min	typ	max	Unit
Allowable output low current sink (per pin)	Ports 1 and 2	I_{OL}	–	–	10	mA
	Other output pins		–	–	2.0	mA
Allowable output low current sink (total)	Ports 1 and 2, total	ΣI_{OL}	–	–	80	mA
	All output pins		–	–	120	mA
Allowable output high current sink (per pin)	All output pins	$-I_{OH}$	–	–	2.0	mA
Allowable output high current sink (total)	Total of all output	$\Sigma -I_{OH}$	–	–	40	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 15-4. In particular, when driving a Darlington pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 17-1 and 17-2.

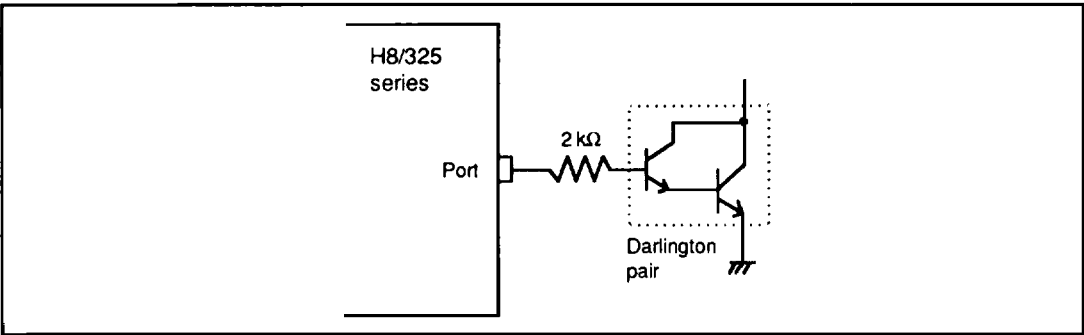


Figure 15-1. Example of Circuit for Driving a Darlington Pair

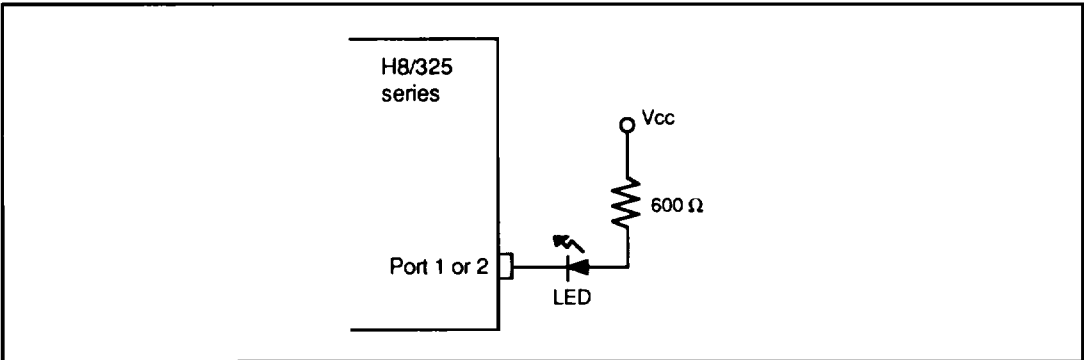


Figure 15-2. Example of Circuit for Driving a LED

Table 15-5. Allowable Output Current Sink Values (3V Version for only H8/3257 and H8/3256)Conditions: $V_{CC} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $75^{\circ}C$

Item		Symbol	min	typ	max	Unit
Allowable output low current sink (per pin)	Ports 1 and 2	IOL	–	–	2	mA
	Other output pins		–	–	1.0	mA
Allowable output low current sink (total)	Ports 1 and 2, total of 16 pins	ΣIOL	–	–	40	mA
	Total of all other output pins		–	–	60	mA
Allowable output high current sink (per pin)	All output pins	–IOH	–	–	2.0	mA
Allowable output high current sink (total)	Total of all output pins	$\Sigma -IOH$	–	–	30	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 15-5.

15.2.2 AC Characteristics

The AC characteristics of the H8/325 series are listed in three tables. Bus timing parameters are given in table 15-6, control signal timing parameters in table 15-7, and timing parameters of the on-chip supporting modules in table 15-8.

Table 15-6. Bus Timing

Condition A: $V_{CC} = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, $V_{SS} = 0V$,

$T_a = -20$ to $75^\circ C$ (regular specifications), $T_a = -40$ to $85^\circ C$ (wide-range specifications)

Condition B: $V_{CC} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$, for only H8/3257 and H8/3256

Item	Symbol	Condition B				Condition A				Unit	Measurement conditions
		5MHz		6MHz		8MHz		10MHz			
		min	max	min	max	min	max	min	max		
Clock cycle time	t _{cyc}	200	2000	166.7	2000	125	2000	100	2000	ns	Fig. 15-4
Clock pulse width Low	t _{CL}	65	–	65	–	45	–	35	–	ns	Fig. 15-4
Clock pulse width High	t _{CH}	65	–	65	–	45	–	35	–	1ns	Fig. 15-4
Clock rise time	t _{Cr}	–	25	–	15	–	15	–	15	ns	Fig. 15-4
Clock fall time	t _{Cf}	–	25	–	15	–	15	–	15	ns	Fig. 15-4
Address delay time	t _{AD}	–	90	–	70	–	60	–	55	ns	Fig. 15-4
Address hold time	t _{AH}	30	–	30	–	25	–	20	–	ns	Fig. 15-4
Address strobe delay time	t _{ASD}	–	80	–	70	–	60	–	40	ns	Fig. 15-4
Write strobe delay time	t _{WSD}	–	80	–	70	–	60	–	50	ns	Fig. 15-4
Strobe delay time	t _{SD}	–	90	–	70	–	60	–	50	ns	Fig. 15-4
Write strobe pulse width	t _{WSW}	200	–	200	–	150	–	120	–	ns	Fig. 15-4
Address setup time 1	t _{AS1}	25	–	25	–	20	–	15	–	ns	Fig. 15-4
Address setup time 2	t _{AS2}	105	–	105	–	80	–	65	–	ns	Fig. 15-4
Read data setup time	t _{RDS}	90	–	60	–	50	–	35	–	ns	Fig. 15-4
Read data hold time	t _{RDH}	0	–	0	–	0	–	0	–	ns	Fig. 15-4
Write data delay time	t _{WDD}	–	125	–	85	–	75	–	75	ns	Fig. 15-4
Read data access time	t _{ACC}	–	300	–	280	–	210	–	170	ns	Fig. 15-4
Write data setup time	t _{WDS}	10	–	30	–	15	–	10	–	ns	Fig. 15-4
Write data hold time	t _{WDH}	30	–	30	–	25	–	20	–	ns	Fig. 15-4
Wait setup time	t _{WTS}	60	–	45	–	45	–	45	–	ns	Fig. 15-5
Wait hold time	t _{WTH}	20	–	10	–	10	–	10	–	ns	Fig. 15-5
E clock delay time	t _{ED}	–	30	–	25	–	25	–	25	ns	Fig. 15-6
E clock rise time	t _{Er}	–	25	–	15	–	15	–	15	ns	Fig. 15-6
E clock fall time	t _{Ef}	–	25	–	15	–	15	–	15	ns	Fig. 15-6
Read data hold time (for E clock)	t _{RDHE}	0	–	0	–	0	–	0	–	ns	Fig. 15-6
Write data hold time (for E clock)	t _{WDHE}	60	–	50	–	40	–	30	–	ns	Fig. 15-6

Table 15-7. Control Signal TimingCondition A: $V_{CC} = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications), $T_a = -40$ to $85^\circ C$ (wide-range specifications)Condition B: $V_{CC} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$, for only H8/3257 and H8/3256

Item	Symbol	Condition B		Condition A						Unit	Measurement conditions
		5MHz		6MHz		8MHz		10MHz			
		min	max	min	max	min	max	min	max		
RES setup time	tRESS	300	–	200	–	200	–	200	–	ns	Fig. 15-7
RES pulse width	tRESW	10	–	10	–	10	–	10	–	t _{cyc}	Fig. 15-7
Mode programming setup time	tMDS	4	–	4	–	4	–	4	–	t _{cyc}	Fig. 15-7
NMI setup time (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	tNMIS	300	–	150	–	150	–	150	–	ns	Fig. 15-8
NMI hold time (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	tNMIH	10	–	10	–	10	–	10	–	ns	Fig. 15-8
Interrupt pulse width for recovery from soft- ware standby mode (NMI, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	tNMW	300	–	200	–	200	–	200	–	ns	Fig. 15-8
Crystal oscillator settling time (reset)	tOSC1	20	–	20	–	20	–	20	–	ms	Fig. 15-9
Crystal oscillator settling time (software standby)	tOSC2	10	–	10	–	10	–	10	–	ms	Fig. 15-10

Table 15-8. Timing Conditions of On-Chip Supporting ModulesCondition A: $V_{CC} = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications), $T_a = -40$ to $85^\circ C$ (wide-range specifications)Condition B: $V_{CC} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$, for only H8/3257 and H8/3256

Item		Symbol	Condition B		Condition A						Unit	Measurement conditions
			5MHz		6MHz		8MHz		10MHz			
			min	max	min	max	min	max	min	max		
FRT	Timer output delay time	tFTOD	–	150	–	100	–	100	–	100	ns	Fig. 15-11
	Timer input setup time	tFTIS	80	–	50	–	50	–	50	–	ns	Fig. 15-11
	Timer clock input setup time	tFTCS	80	–	50	–	50	–	50	–	ns	Fig. 15-12
	Timer clock pulse width	tFTCWL	1.5	–	1.5	–	1.5	–	1.5	–	t _{cyt}	Fig. 15-12

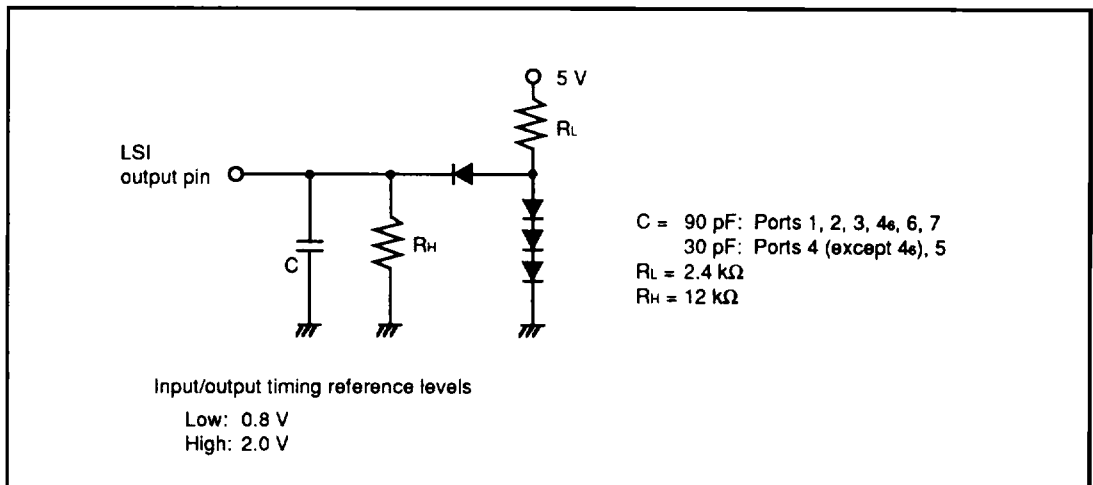
Table 15-8. Timing Conditions of On-Chip Supporting Modules (cont.)Condition A: $V_{CC} = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications), $T_a = -40$ to $85^\circ C$ (wide-range specifications)Condition B: $V_{CC} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$, for only H8/3257 and H8/3256

			Condition B				Condition A					
			5MHz		6MHz		8MHz		10MHz			Measurement
Item		Symbol	min	max	min	max	min	max	min	max	Unit	conditions
TMR	Timer output delay time	ttMOD	–	150	–	100	–	100	–	100	ns	Fig. 15-13
	Timer reset input setup time	ttMRS	80	–	50	–	50	–	50	–	ns	Fig. 15-15
	Timer clock input setup time	ttMCS	80	–	50	–	50	–	50	–	ns	Fig. 15-14
	Timer clock pulse width (single edge)	ttMCWH	1.5	–	1.5	–	1.5	–	1.5	–	t _{cyc}	Fig. 15-14
	Timer clock pulse width (both edges)	ttMCWL	2.5	–	2.5	–	2.5	–	2.5	–	t _{cyc}	Fig. 15-14
SCI	Input (Async)	t _{Scyc}	2	–	2	–	2	–	2	–	t _{cyc}	Fig. 15-16
	clock (Sync)	t _{Scyc}	4	–	4	–	4	–	4	–	t _{cyc}	Fig. 15-16
	Transmit data delay time (Sync)	ttXD	–	200	–	100	–	100	–	100	ns	Fig. 15-16
	Receive data setup time (Sync)	trXS	150	–	100	–	100	–	100	–	ns	Fig. 15-16
	Receive data hold time (Sync)	trXH	150	–	100	–	100	–	100	–	ns	Fig. 15-16
	Input clock pulse width	t _{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t _{Scyc}	Fig. 15-17
Ports	Output data delay time	tpWD	–	150	–	100	–	100	–	100	ns	Fig. 15-18
	Input data setup time	lPRS	80	–	50	–	50	–	50	–	ns	Fig. 15-18
	Input data hold time	lPRH	80	–	50	–	50	–	50	–	ns	Fig. 15-18

Table 15-8. Timing Conditions of On-Chip Supporting Modules (cont.)Condition A: $V_{CC} = 5.0V \pm 10\%$, $\phi = 0.5$ to 10MHz, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications), $T_a = -40$ to $85^\circ C$ (wide-range specifications)Condition B: $V_{CC} = 2.7$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$, for only H8/3257 and H8/3256

			Condition B		Condition A							Measurement conditions
			5MHz		6MHz		8MHz		10MHz			
Item		Symbol	min	max	min	max	min	max	min	max	Unit	
Parallel handshake interface	Handshake input strobe pulse width	t _{HSW}	1.5	–	1.5	–	1.5	–	1.5	–	t _{cyc}	Fig. 15-19
	Handshake input data setup time	t _{HSD}	10	–	10	–	10	–	10	–	ns	Fig. 15-19
	Handshake input data hold time	t _{HH}	120	–	120	–	120	–	120	–	ns	Fig. 15-19
	Handshake output strobe delay time	t _{HOSD1}	–	100	–	80	–	80	–	80	ns	Fig. 15-20
		t _{HOSD2}	–	100	–	80	–	80	–	80	ns	Fig. 15-20
	Busy output delay time	t _{HBSOD1}	–	150	–	150	–	150	–	150	ns	Fig. 15-21
		t _{HBSOD2}	–	150	–	150	–	150	–	150	ns	Fig. 15-21

• Measurement Conditions for AC Characteristics

**Figure 15-3. Output Load Circuit**

(2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes

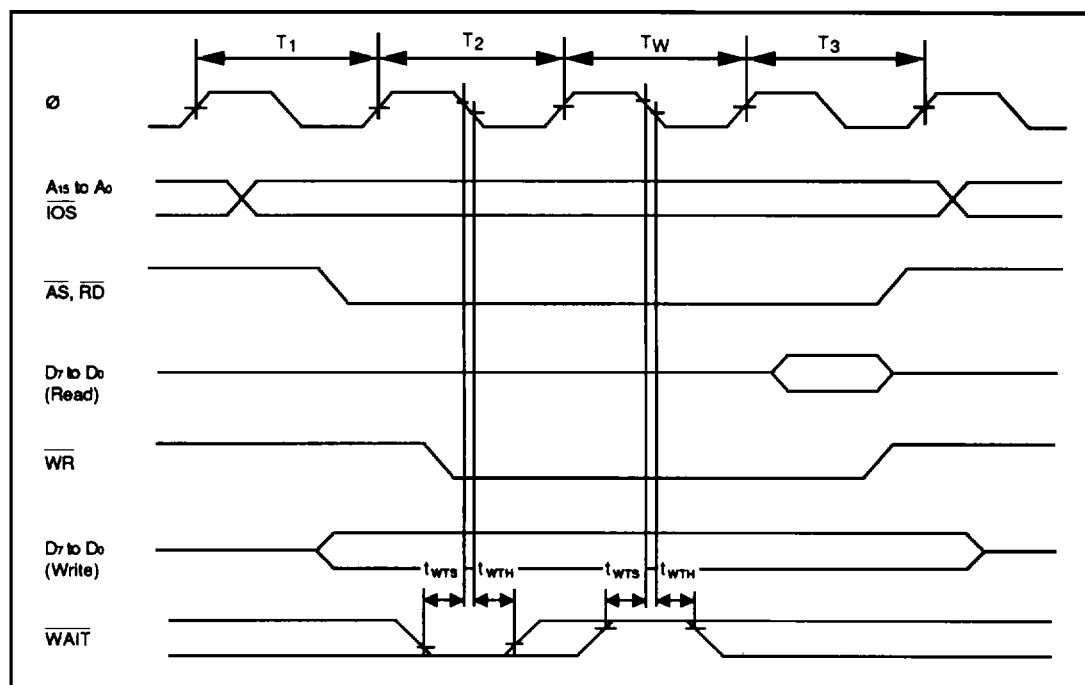


Figure 15-5. Basic Bus Cycle (with 1 Wait State) in Expanded Modes

(3) E Clock Bus Cycle

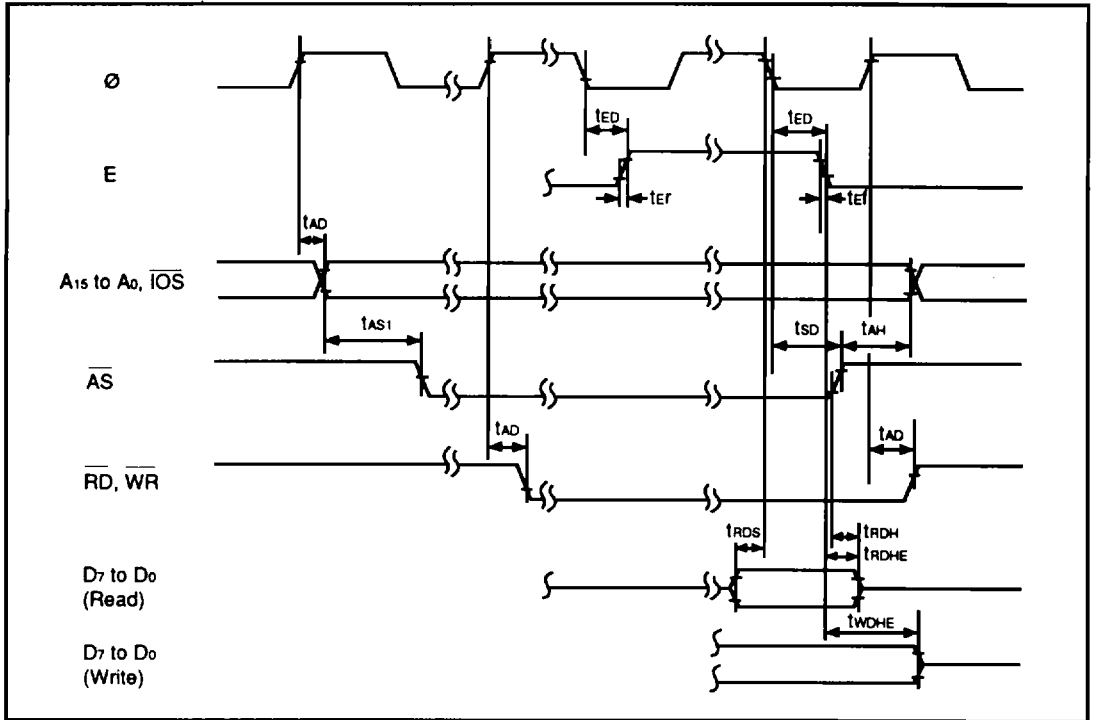


Figure 15-6. E Clock Bus Cycle

15.3.2 Control Signal Timing

(1) Reset Input Timing

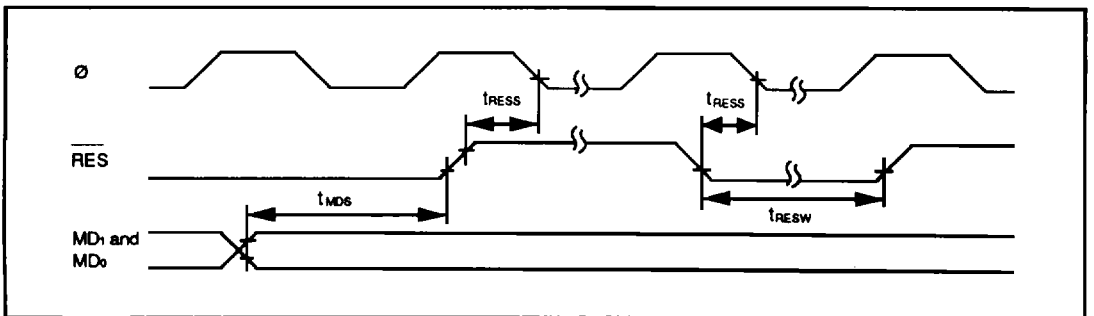


Figure 15-7. Reset Input Timing

(2) Interrupt Input Timing

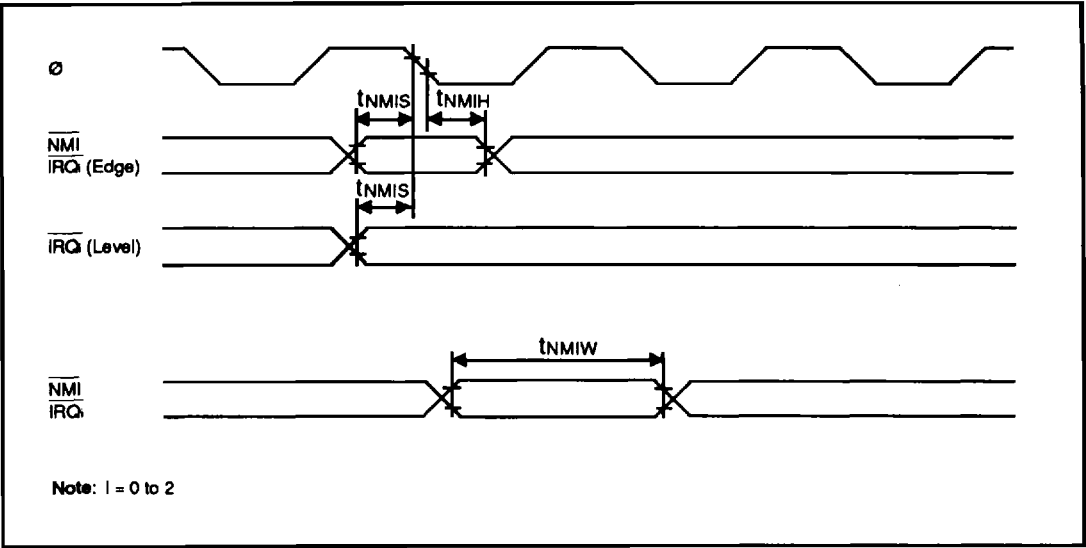


Figure 15-8. Interrupt Input Timing

(3) Clock Settling Timing

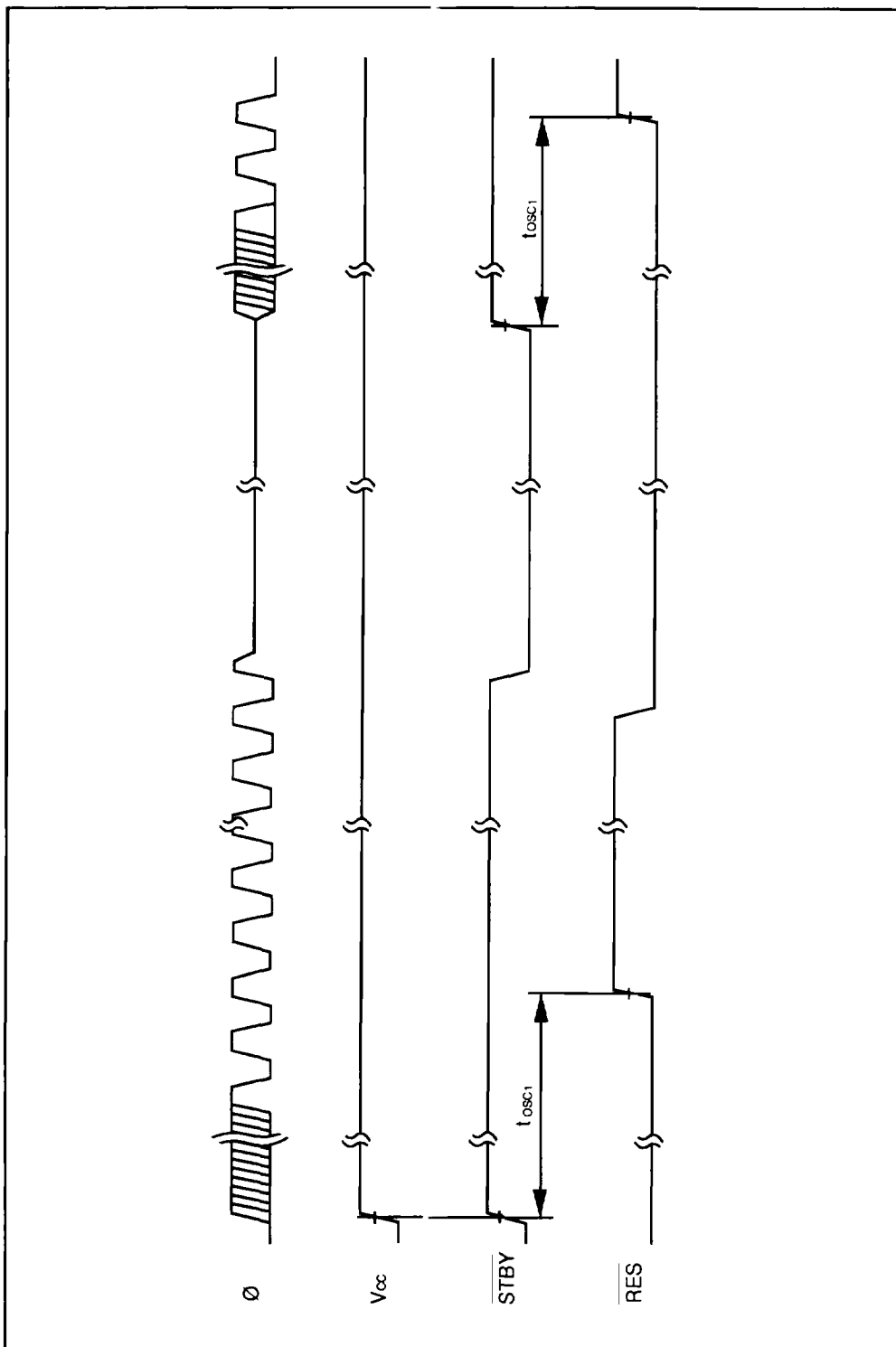


Figure 15-9. Clock Settling Timing

(4) Clock Settling Timing for Recovery from Software Standby Mode

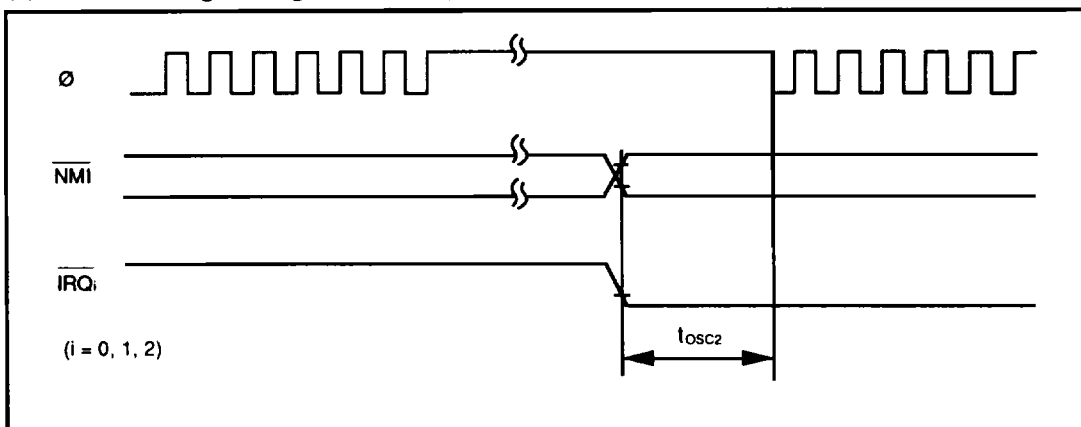


Figure 15-10. Clock Settling Timing for Recovery from Software Standby Mode

15.3.3 16-Bit Free-Running Timer Timing

(1) Free-Running Timer Input/Output Timing

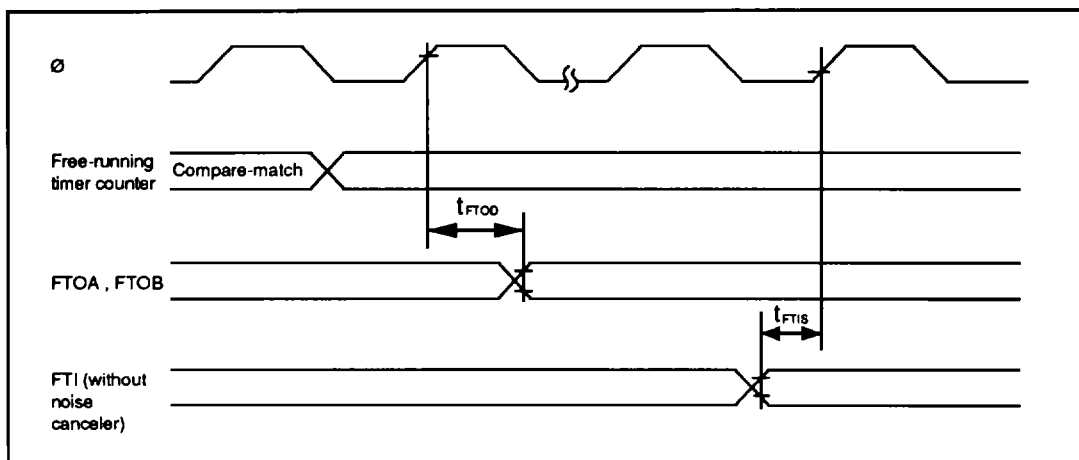


Figure 15-11. Free-Running Timer Input/Output Timing

(2) External Clock Input Timing for Free-Running Timer

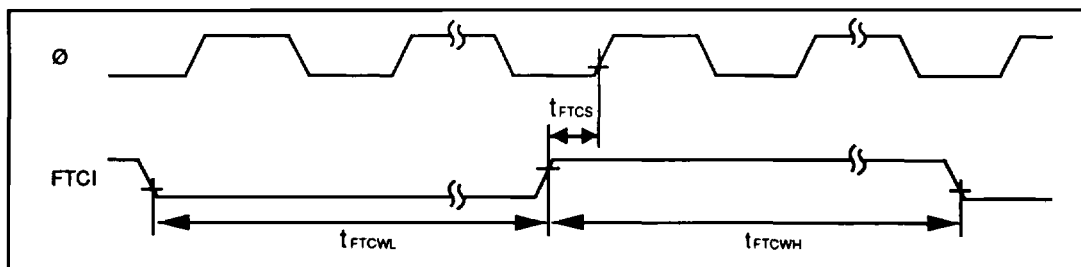


Figure 15-12. External Clock Input Timing for Free-Running Timer

15.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

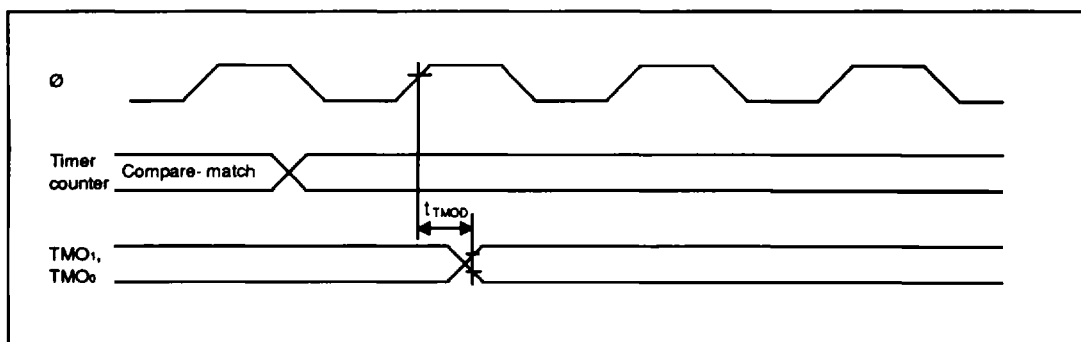


Figure 15-13. 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

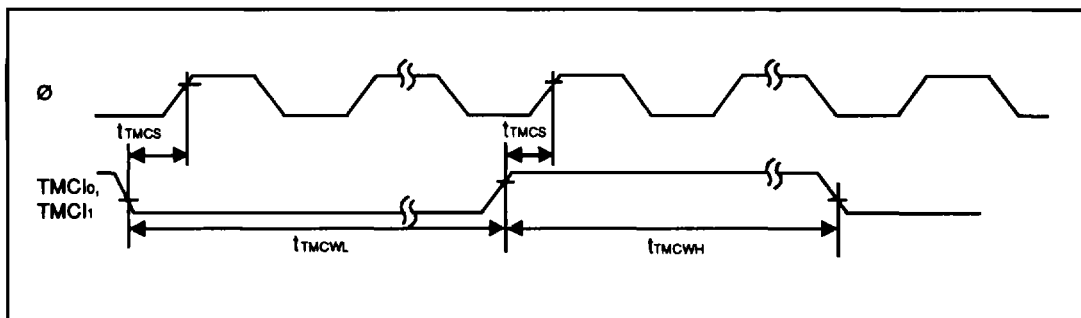


Figure 15-14. 8-Bit Timer Clock Input Timing

(3) 8-Bit Timer Reset Input Timing

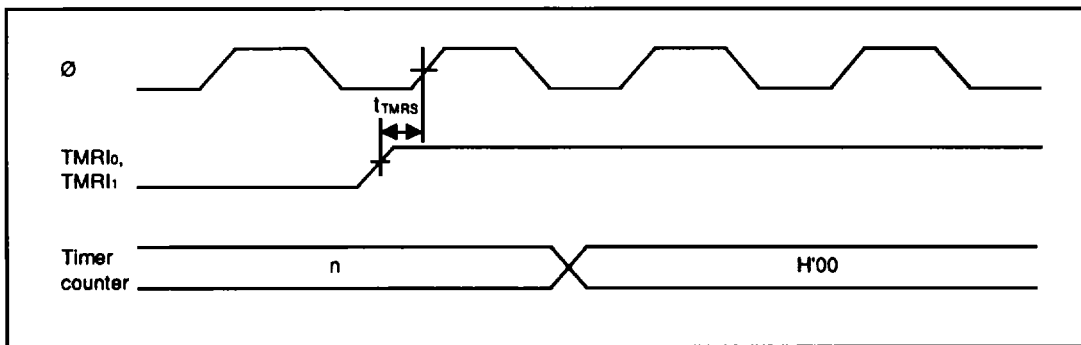


Figure 15-15. 8-Bit Timer Reset Input Timing

15.3.5 Serial Communication Interface Timing

(1) SCI Input/Output Timing

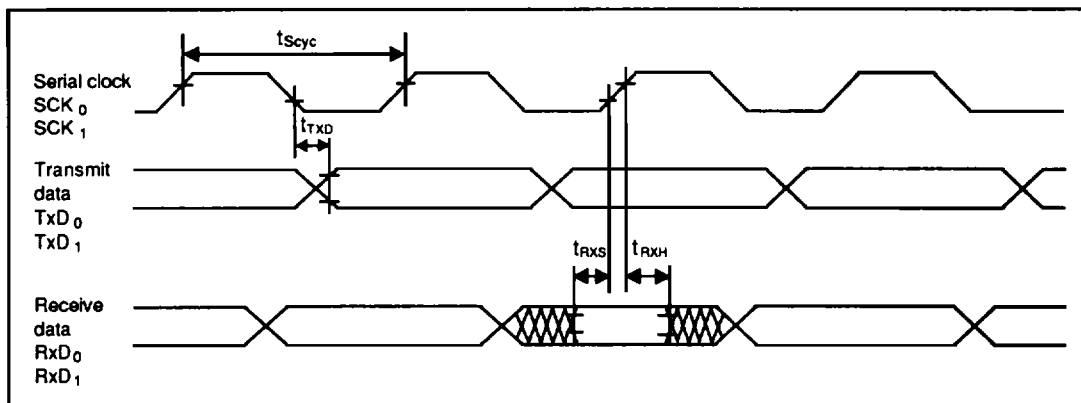


Figure 15-16. SCI Input/Output Timing (Synchronous Mode)

(2) SCI Input Clock Timing

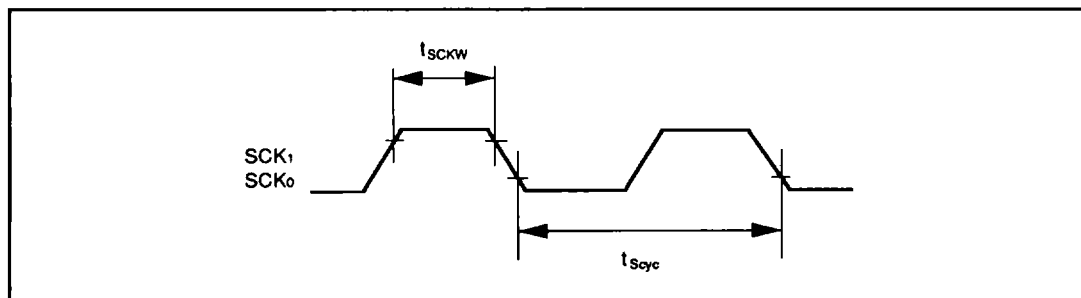


Figure 15-17. SCI Input Clock Timing

15.3.6 I/O Port Timing

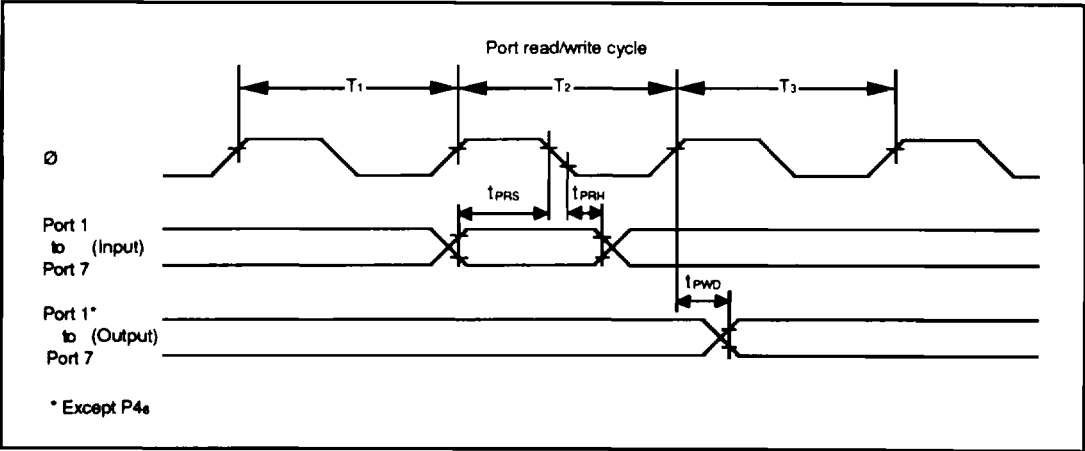


Figure 15-18. I/O Port Input/Output Timing

15.3.7 Parallel Handshake Interface Timing

(1) Input Strobe Input Timing

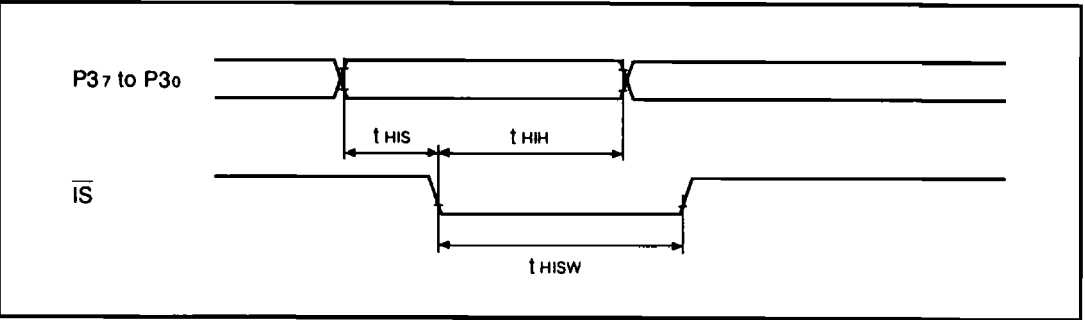


Figure 15-19. Input Strobe Input Timing

(2) Output Strobe Output Timing

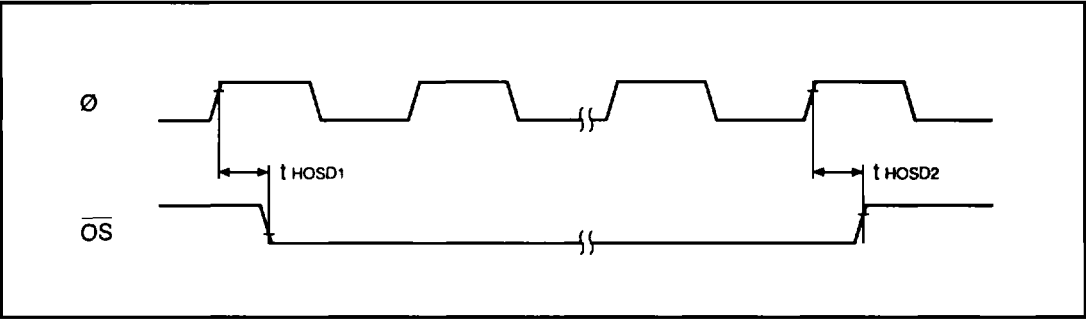


Figure 15-20. Output Strobe Output Timing

(3) Busy Output Timing

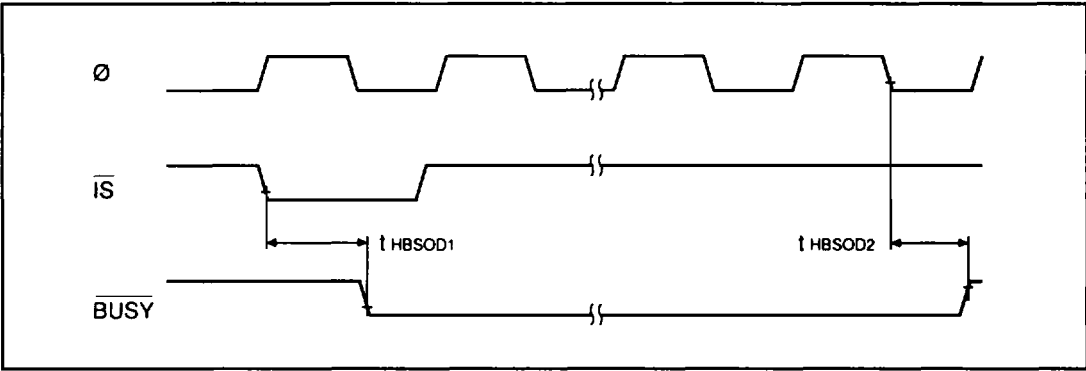


Figure 15-21. Busy Output Timing