

CD4543B Types

CMOS BCD-to-Seven-Segment Latch/Decoder/Driver For Liquid-Crystal Displays

High-Voltage Types (20-Volt Rating)

Features:

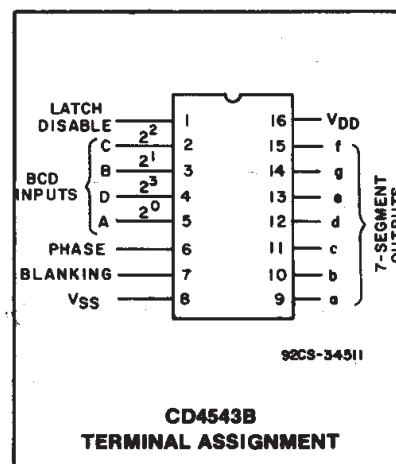
- Display blanking of all illegal input combinations
- Latch storage of code
- Capability of driving two low power TTL loads, two HTL loads, or one low power Schottky load over the full rated-temperature range
- Pin-for-pin replacement for the CD4056B (with pin 7 tied to V_{SS})
- Direct LED driving capability

■ CD4543B is a BCD-to-seven segment latch/decoder/driver designed primarily for liquid-crystal display (LCD) applications. It is also capable of driving light emitting diode (LED), incandescent, gas-discharge, and fluorescent displays. This device is functionally similar to and serves as direct replacement for the CD4056B when pin 7 is connected to V_{SS} . It differs from the CD4056B in that it has a display blanking capability instead of a level-shifting function and requires only one power supply. When the CD4056B is used in the level shifting mode, two power supplies are required. When the CD4543B is used for LCD applications, a square wave must be applied to the PHASE input and the backplane of the LCD device. For LED applications a logic 0 is required at the PHASE input for common-cathode devices; a logic 1 is required for common-anode devices (see truth table).

The CD4543B is supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
Voltages referenced to V_{SS} Terminal)	–0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	500mW
For $T_A = +100^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Derate Linearly at 12mW/ $^{\circ}\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE (T_A)	–55 $^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	–65 $^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265 $^{\circ}\text{C}$



- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25 $^{\circ}\text{C}$
- Noise margin (full package-temperature range) = 1 V at $V_{DD}=5\text{ V}$
2 V at $V_{DD}=10\text{ V}$
2.5 V at $V_{DD}=15\text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Instrument display driver
- Dashboard display driver
- Computer/calculator display driver
- Timing device driver (clocks, watches, timers)

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4543B Types

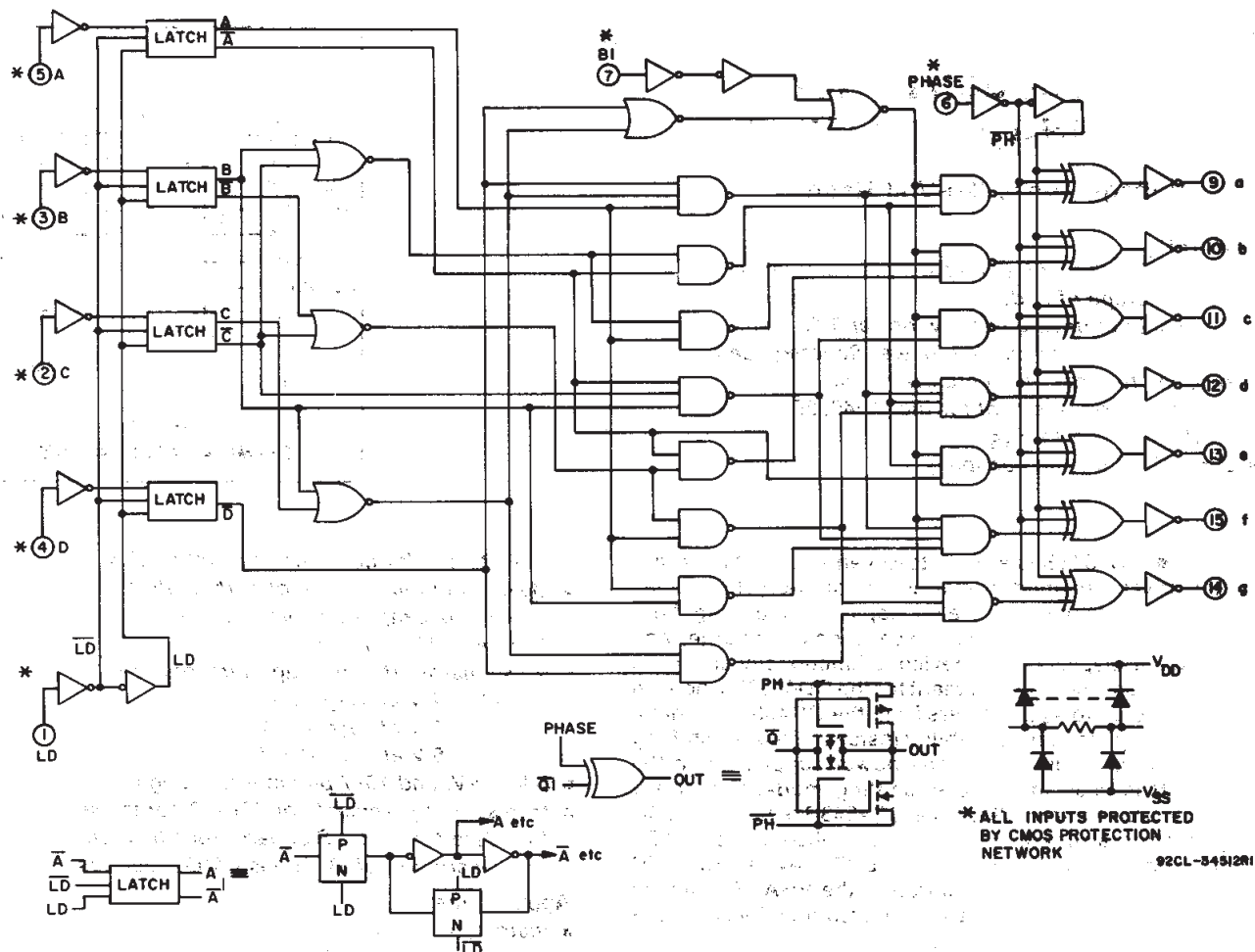


Fig. 1 - BCD-to-seven-segment latch/decoder/driver CD4543B logic circuit diagram.

RECOMMENDED OPERATING CONDITIONS at $T_A=25^\circ\text{C}$, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	TYP.	
Supply-Voltage Range (For T_A =Full Package-Temperature Range)	—	3	18	V
Latch Disable Pulse Width t_{WH}	5	250	125	ns
	10	100	50	
	15	80	40	
Minimum Data Setup Time t_{SU}	5	60	15	
	10	20	-5	
	15	10	-5	
Minimum Data Hold Time t_H	5	25	-5	
	10	20	10	
	15	20	10	

CD4543B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC		CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
		V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
									Min.	Typ.	Max.	
Quiescent Device Current Max.	I _{DD}	—	0, 5	5	5	5	150	150	—	0.04	5	μA
		—	0,10	10	10	10	300	300	—	0.04	10	
		—	0,15	15	20	20	600	600	—	0.04	20	
		—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current Min.	I _{OL}	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
		0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
		1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min.	I _{OH}	4.6	0, 5	5	-0.46	-0.44	-0.30	-0.26	-0.37	-0.75	—	mA
		2.5	0, 5	5	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
		9.5	0,10	10	-0.98	-0.92	-0.68	-0.55	-0.8	-1.6	—	
		13.5	0,15	15	-3.33	-3.18	-2.2	-1.9	-2.7	-5.4	—	
Output Voltage: Low-Level Max.	V _{OL}	—	0, 5	5	0.05				—	0	0.05	V
		—	0,10	10	0.05				—	0	0.05	
		—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min.	V _{OH}	—	0, 5	5	4.95				4.95	5	—	V
		—	0,10	10	9.95				9.95	10	—	
		—	0,15	15	14.95				14.95	15	—	
Input Low Voltage Max.	V _{IL}	0.5,4.5	—	5	1.5				—	—	1.5	V
		1, 9	—	10	3				—	—	3	
		1.5,13.5	—	15	4				—	—	4	
Input High Voltage Min.	V _{IH}	0.5,4.5	—	5	3.5				3.5	—	—	V
		1, 9	—	10	7				7	—	—	
		1.5,13.5	—	15	11				11	—	—	
Input Current Max.	I _{IN}	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

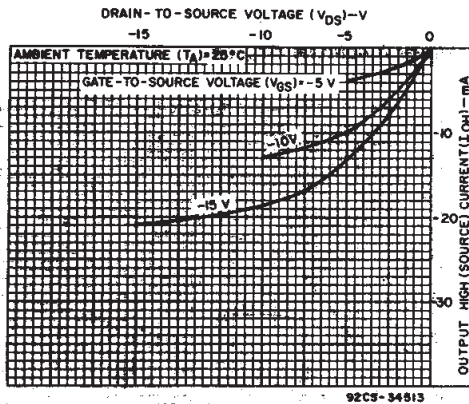


Fig. 2 - Typical output high (source) current characteristics.

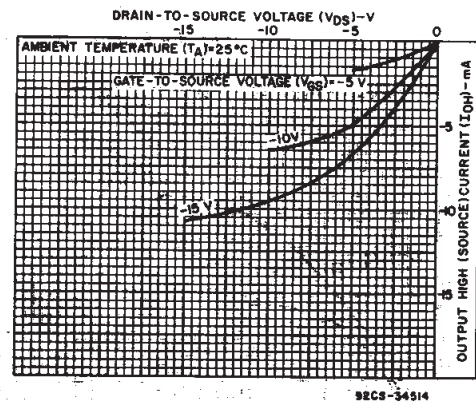


Fig. 3 - Minimum output high (source) current characteristics.

CD4543B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A=25^\circ\text{C}$; $C_L=50\text{ pF}$, Input $t_r, t_f=20\text{ ns}$, $R_L=200\text{ k}\Omega$

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS All Packages			UNITS
			MIN.	TYP.	MAX.	
Propagation Delay Time	t_{PHL}	5	—	600	1200	ns
		10	—	200	400	
		15	—	150	300	
	t_{PLH}	5	—	500	1000	
		10	—	200	400	
		15	—	150	300	
Transition Time	t_{THL}	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
	t_{TLH}	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
Latch Disable Pulse Width	t_{WH}	5	250	125	—	pF
		10	100	50	—	
		15	80	40	—	
Address Setup Time	t_{SU}	5	60	15	—	
		10	20	-5	—	
		15	10	-5	—	
Address Hold Time	t_H	5	25	-5	—	
		10	20	10	—	
		15	20	10	—	
Input Capacitance	C_{IN}	Any Input	—	5	7.5	

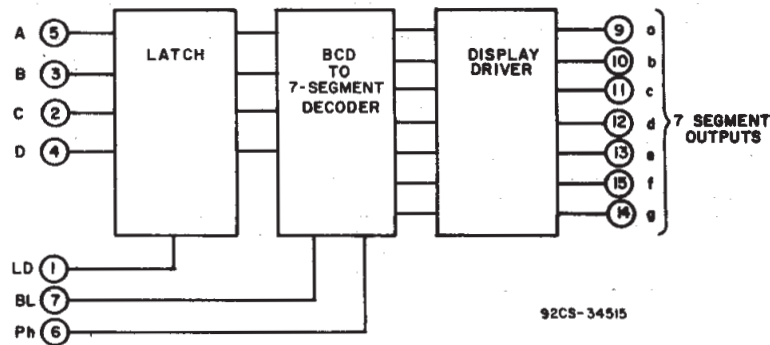


Fig. 4 - BCD-to-seven-segment latch/decoder/driver functional diagram.

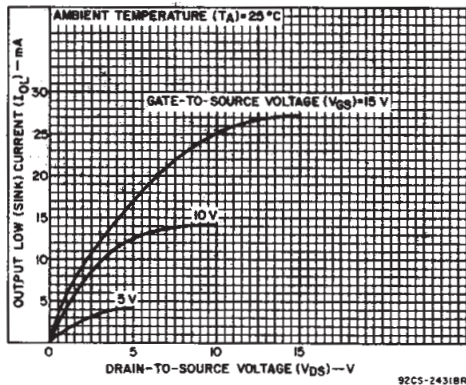


Fig. 5 - Typical output low (sink) current characteristics.

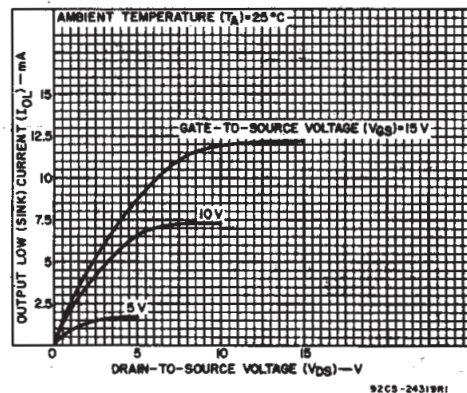


Fig. 6 - Minimum output low (sink) current characteristics.

CD4543B Types

TRUTH TABLE FOR CD4543B

INPUT CODE							OUTPUT STATE							DISPLAY CHARACTER
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	
X	1	0	X	X	X	X	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	0	1	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as above

X=Don't care.

†=Above combinations.

*=For liquid-crystal readouts, apply a square wave to Ph.

For common cathode LED readouts, select Ph=0.

For common anode LED readouts, select Ph=1.

**=Depends upon the BCD code previously applied when LD=1.

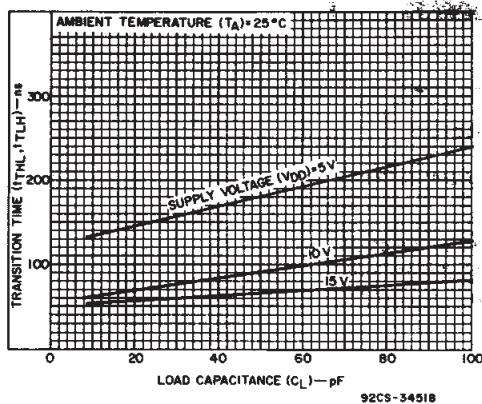


Fig. 7 - Typical transition time as a function of load capacitance.

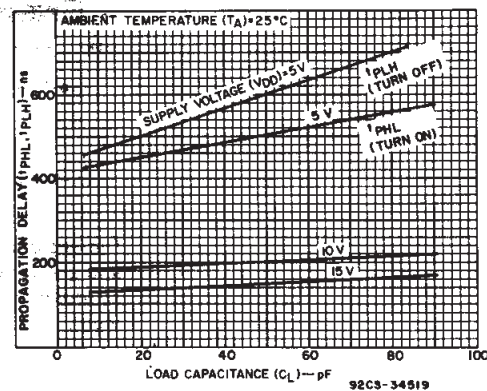


Fig. 8 - Typical propagation delay time as a function of load capacitance.

CD4543B Types

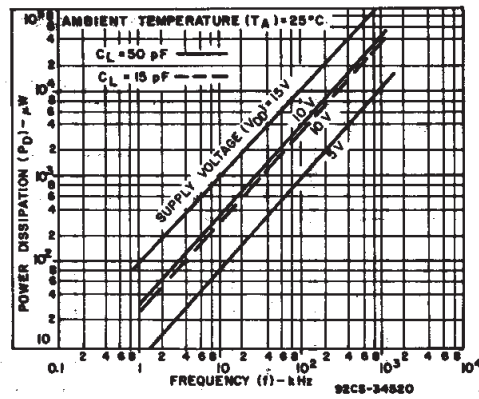


Fig. 9 - Typical dynamic power dissipation as a function of frequency.

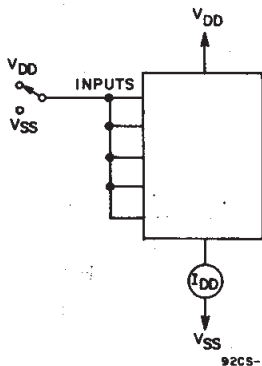


Fig. 10 - Quiescent device current test circuit.

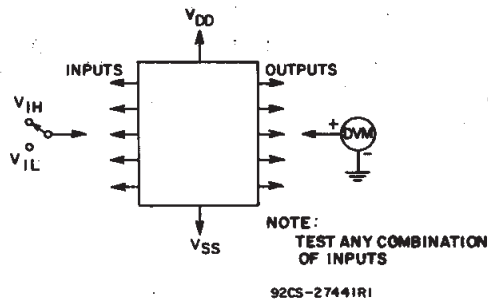


Fig. 11 - Input voltage test circuit.

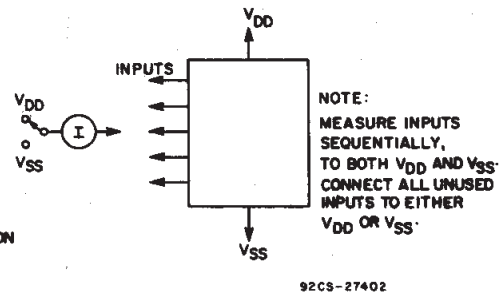
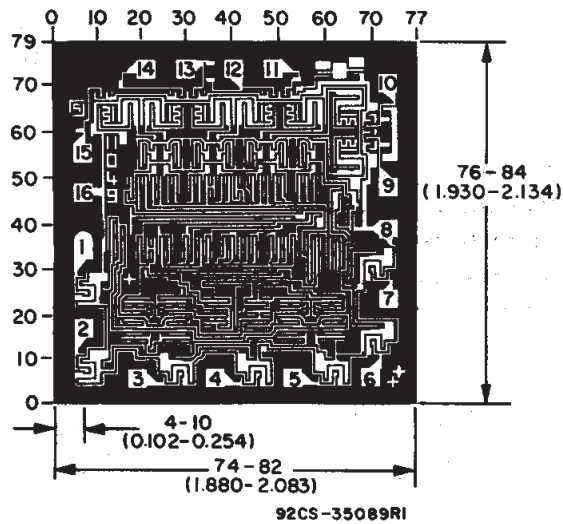


Fig. 12 - Input current test circuit.



Dimensions and pad layout for CD4543BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4543BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4543BE	Samples
CD4543BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4543BE	Samples
CD4543BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4543BM	Samples
CD4543BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4543B	Samples
CD4543BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM543B	Samples
CD4543BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM543B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4543BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4543BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4543BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4543BM96	SOIC	D	16	2500	340.5	336.1	32.0
CD4543BNSR	SO	NS	16	2000	356.0	356.0	35.0
CD4543BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



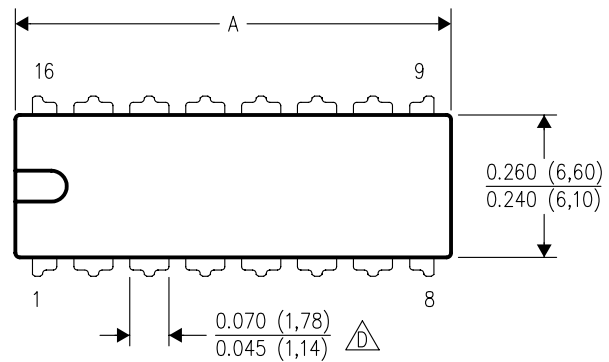
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4543BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4543BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4543BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4543BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4543BPW	PW	TSSOP	16	90	530	10.2	3600	3.5

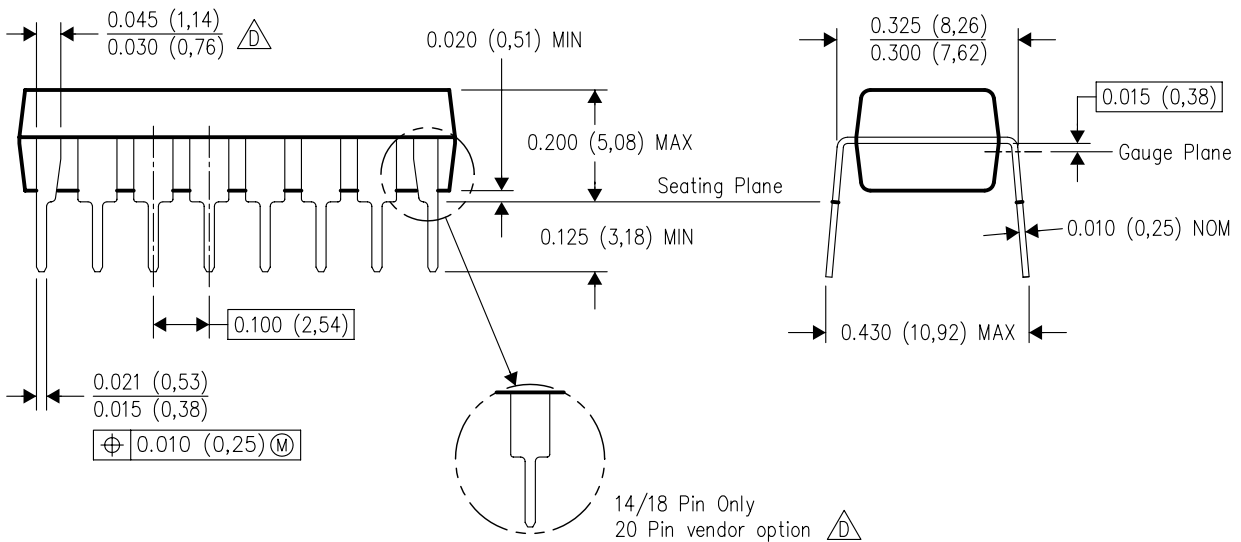
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



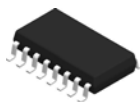
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

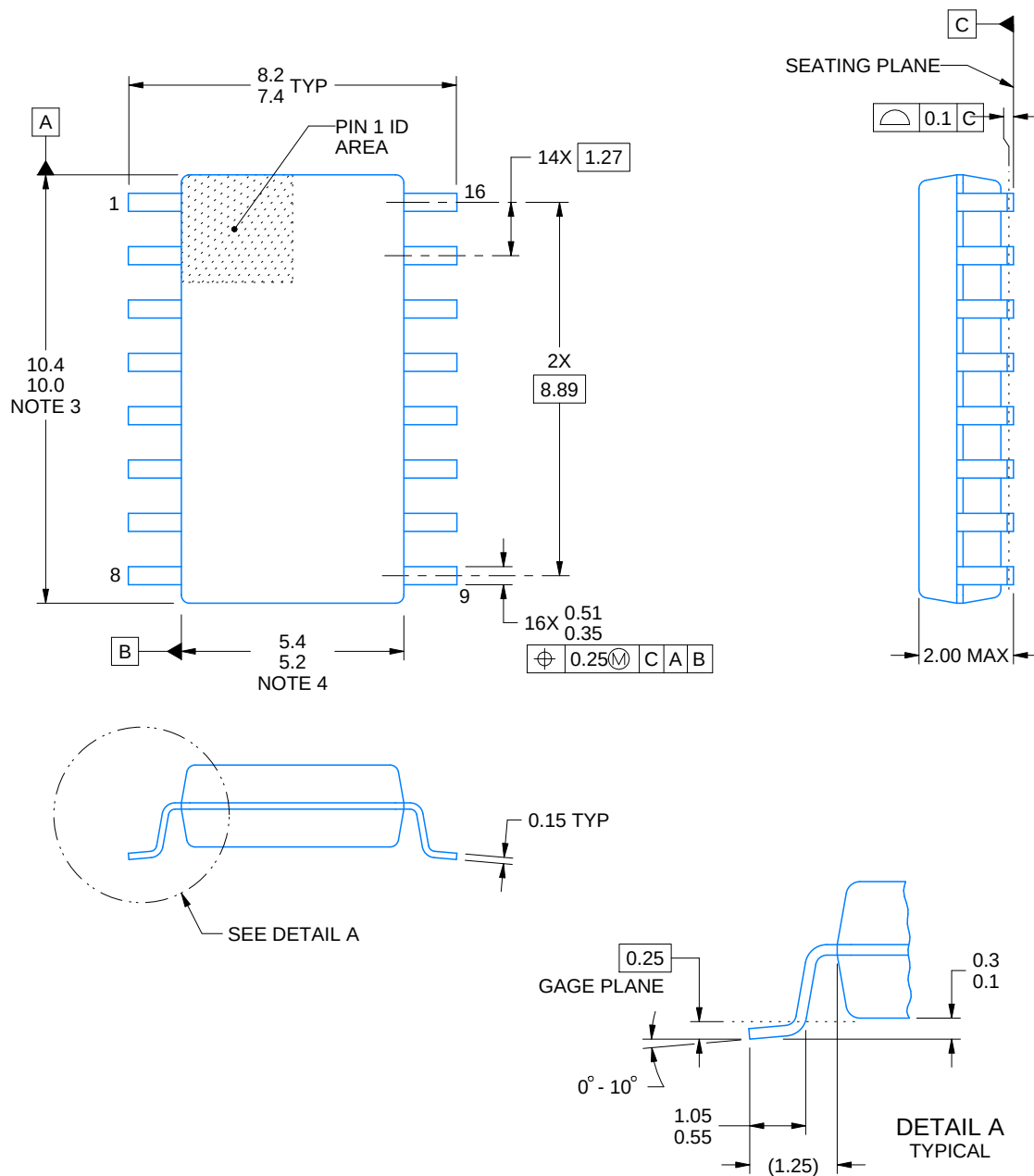


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

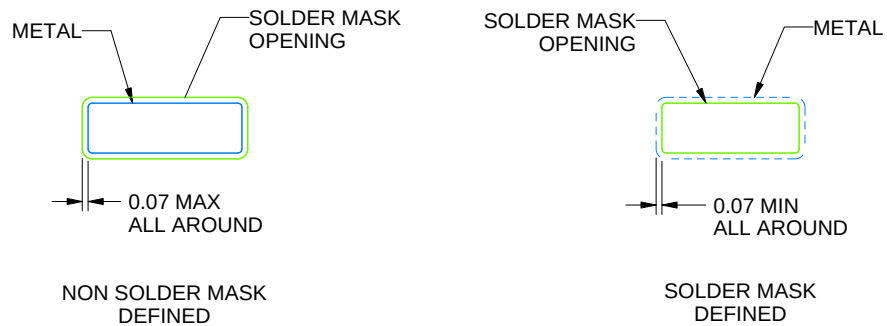
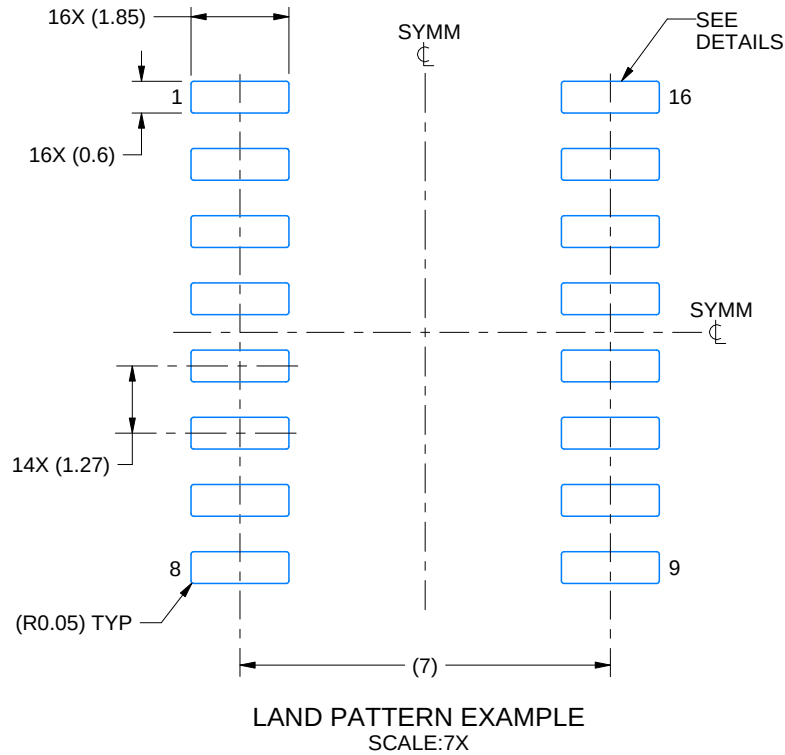
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



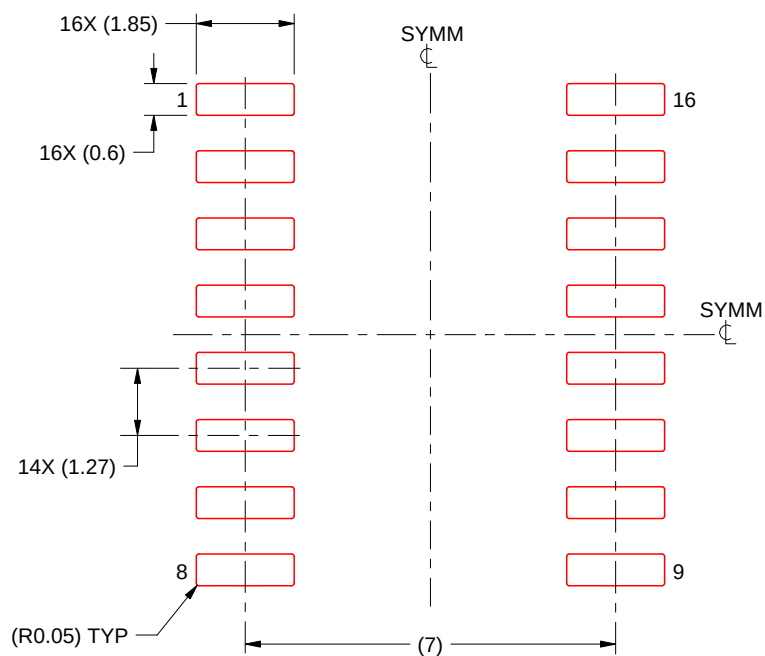
SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

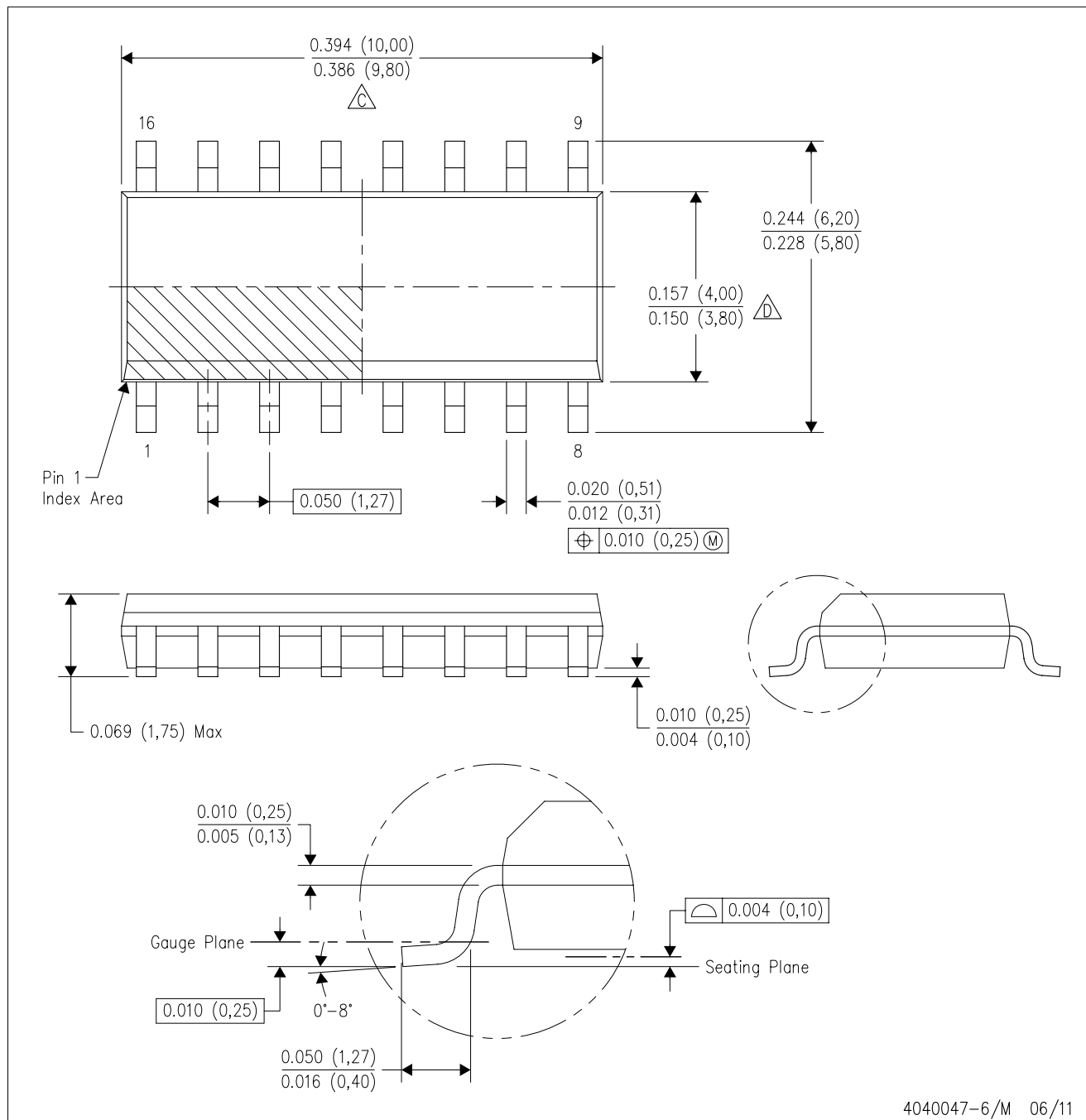
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NOTES: (continued)

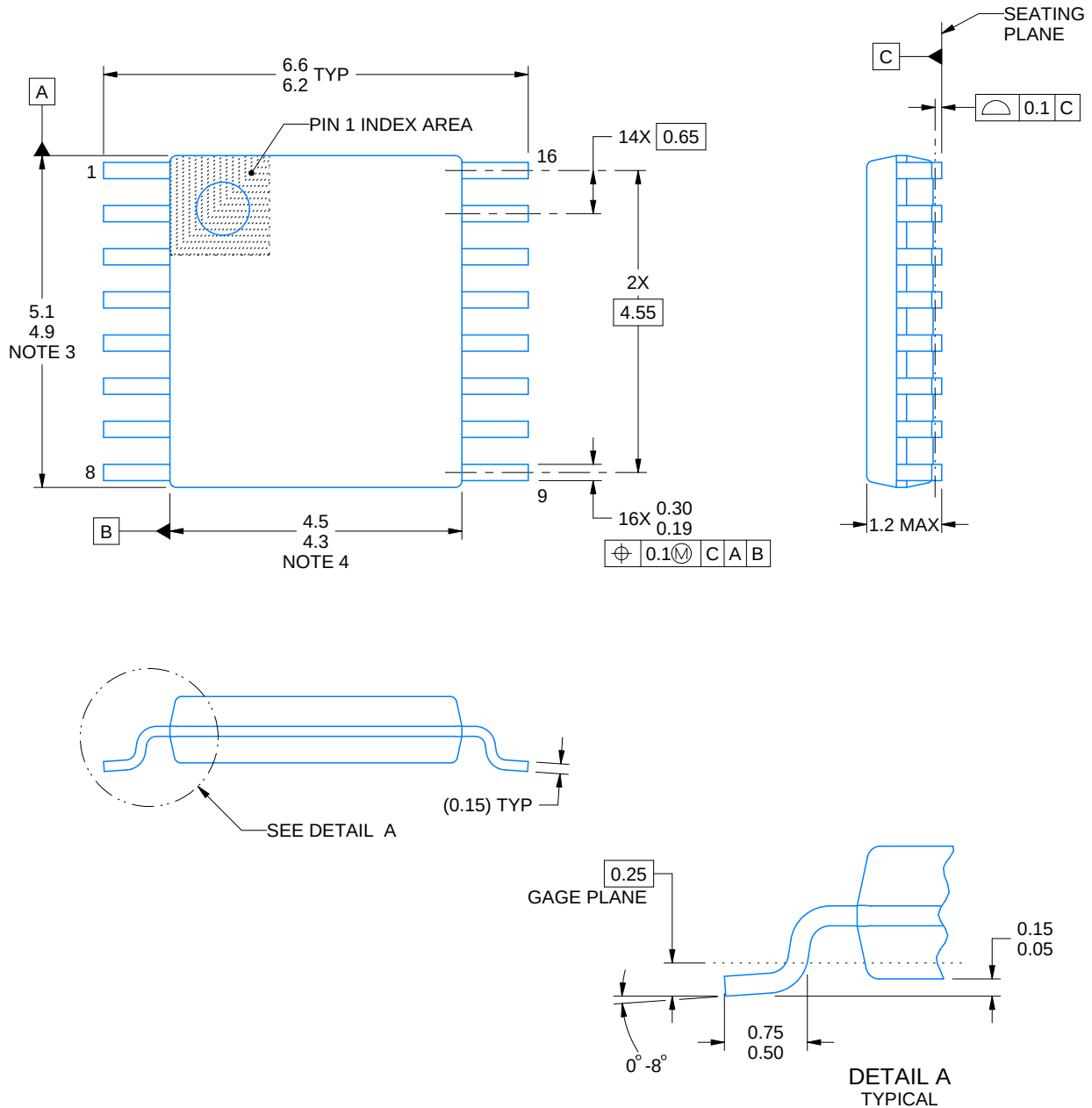
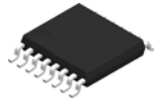
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

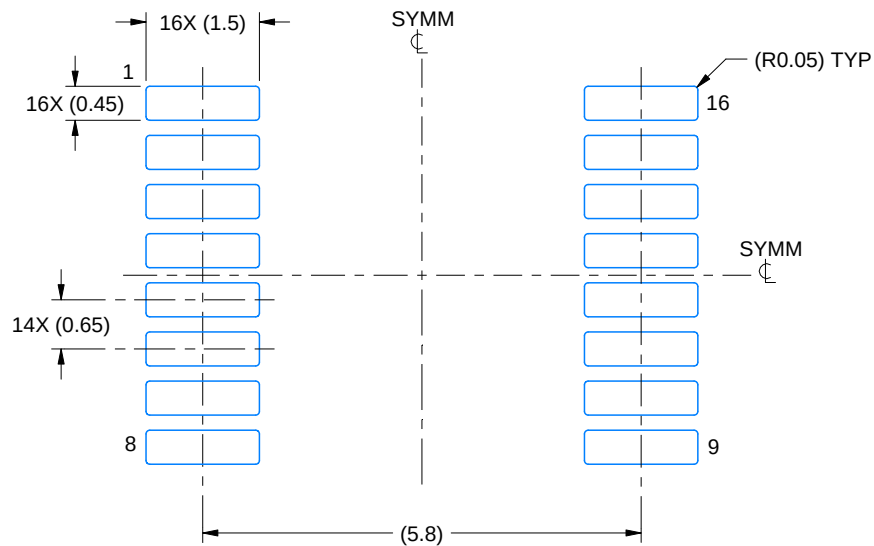
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

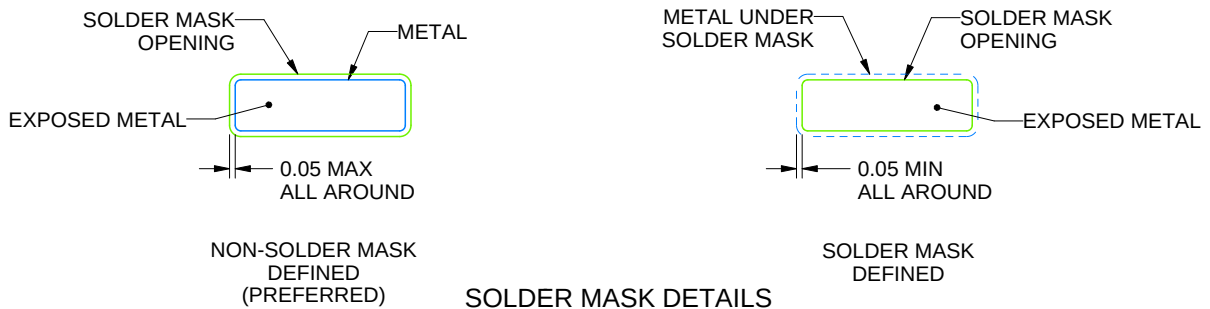
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

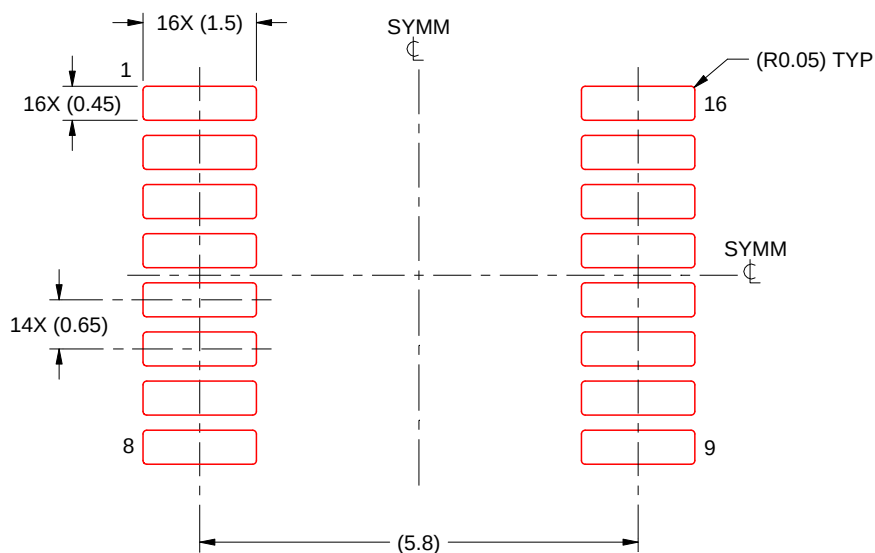
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES: (continued)

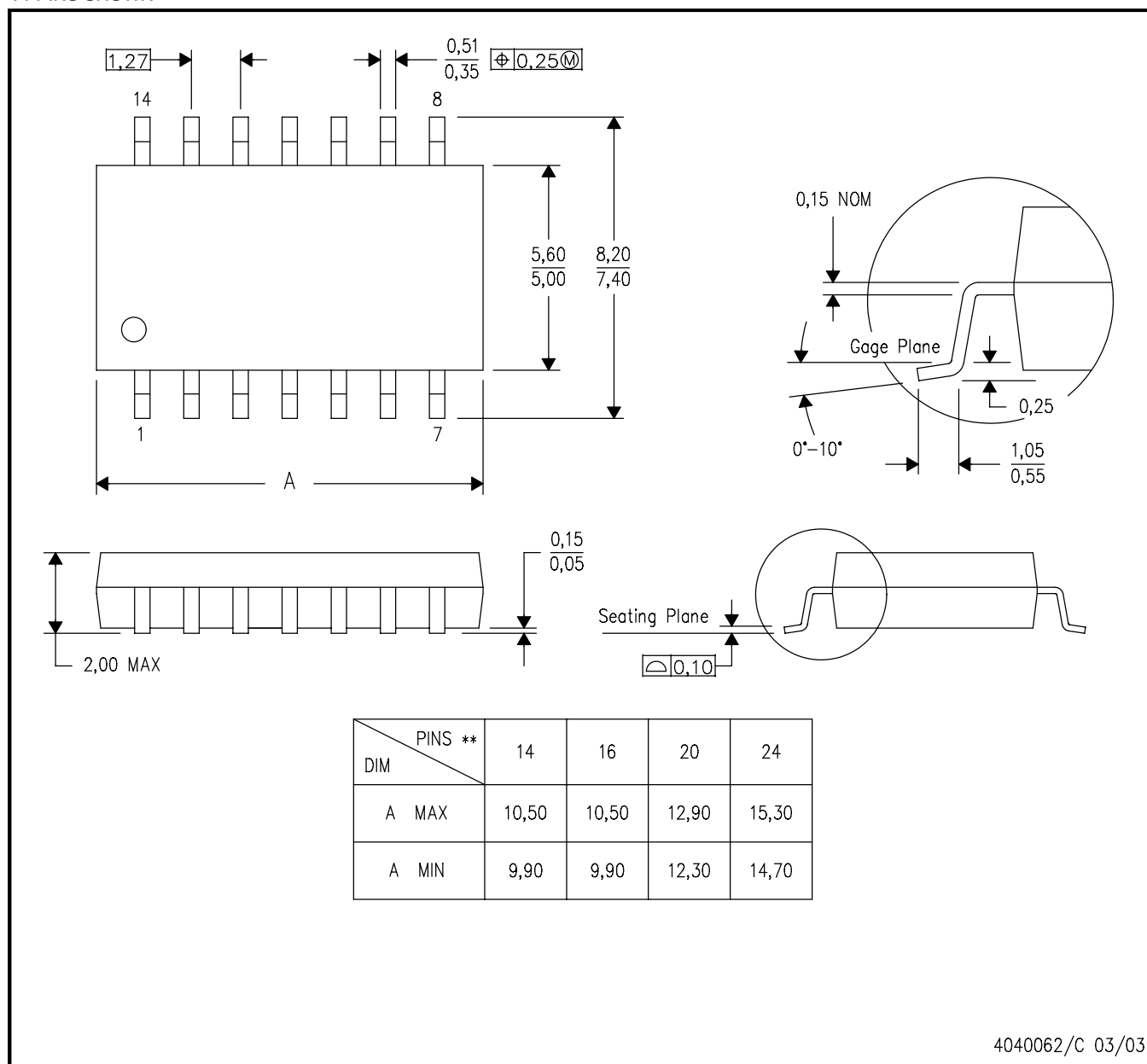
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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