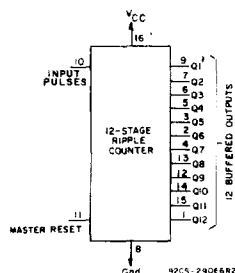


CD54/74HC4040

CD54/74HCT4040

File Number 1483

High-Speed CMOS Logic



12-Stage Binary Counter

Type Features:

- Fully static operation
- Buffered inputs
- Common reset
- Negative edge pulsing
- Typical $f_{MAX} = 50 \text{ MHz}$ @ $V_{CC} = 5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_A = 25^\circ \text{ C}$

FUNCTIONAL DIAGRAM

The RCA-CD54/74HC4040 and CD54/74HCT4040 are 12-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all stages to their zero state. All inputs and outputs are buffered.

The CD54HC4040 and CD54HCT4040 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4040 and CD74HCT4040 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic package (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

ϕ	MR	Output State
	L	No Change
	L	Advance to next state
X	H	All Outputs are low

H = high level (steady state)

L = low level (steady state)

X = don't care

Family Features:

- Fanout (Over Temperature Range):
 - Standard Outputs - 10 LSTTL Loads
 - Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
 - CD74HC/HCT: -40 to $+85^\circ \text{ C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
 - 2 to 6 V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} @ $V_{CC} = 5 \text{ V}$
- CD54HCT/CD74HCT Types:
 - 4.5 to 5.5 V Operation
 - Direct LSTTL Input Logic Compatibility
 - $V_{IL} = 0.8 \text{ V Max.}$, $V_{IH} = 2 \text{ V Min.}$
 - CMOS Input Compatibility
 - $I_L \leq 1 \mu\text{A}$ @ V_{OL} , V_{OH}

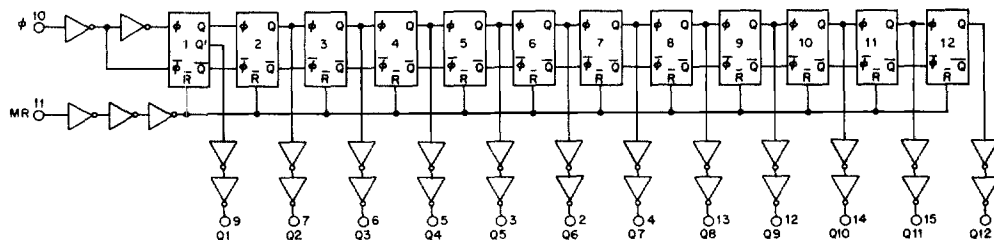


Fig. 1 - Logic block diagram.

92CL-37015R3

CD54/74HC4040

CD54/74HCT4040

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm)	
with solder contacting lead tips only	$+300^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in} , V_{out}	0	V_{CC}	V
Operating Temperature T_A :			
CD74 Types	-40	$+85$	$^\circ\text{C}$
CD54 Types	-55	$+125$	$^\circ\text{C}$
Input Rise and Fall Times t_r , t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

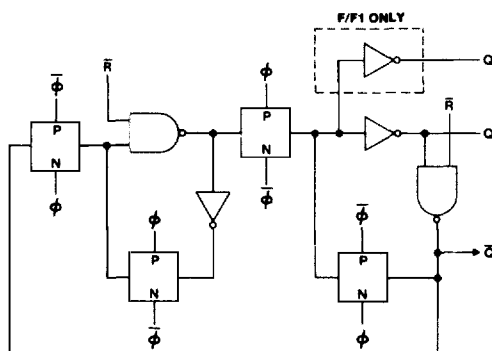


Fig. 2 - Detail for flip-flops 1, 2, 4, 5, 7, 8, 10 & 11.

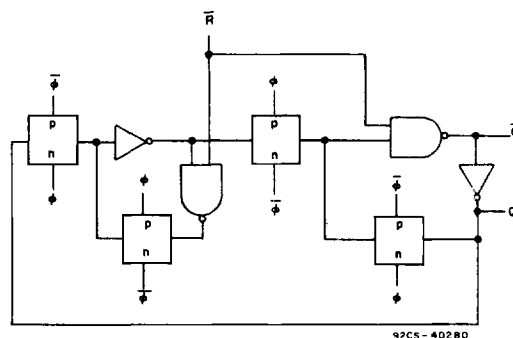


Fig. 3 - Detail for flip-flops 3, 6, 9 & 12.

CD54/74HC4040
CD54/74HCT4040

STATIC ELECTRICAL CHARACTERISTICS

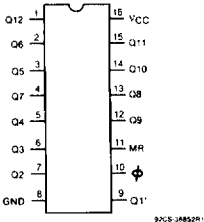
CHARACTERISTIC	CD74HC4040/CD54HC4040										CD74HCT4040/CD54HCT4040										UNITS	
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES				
	V _I V	I _O mA	V _{CC} V	+25° C			-40/ +85° C		-55/ +125° C		V _I V	V _{CC} V	+25° C			-40/ +85° C		-55/ +125° C				
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max			
High-Level Input Voltage V _{IH}				2	1.5	—	—	1.5	—	1.5	—	—	4.5	2	—	—	2	—	2	—	V	
				4.5	3.15	—	—	3.15	—	3.15	—		to	—	—	—	—	—	—			
				6	4.2	—	—	4.2	—	4.2	—		5.5	—	—	—	—	—	—			
Low-Level Input Voltage V _{IL}				2	—	—	0.5	—	0.5	—	0.5	—	4.5	—	—	0.8	—	0.8	—	0.8	V	
				4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	—	—	—	—			
				6	—	—	1.8	—	1.8	—	1.8	—	5.5	—	—	—	—	—	—			
High-Level Output Voltage V _{OH}	V _{IL}	-0.02		2	1.9	—	—	1.9	—	1.9	—	V _{IL}	4.5	4.4	—	—	4.4	—	4.4	—	V	
CMOS Loads	V _{IH}			4.5	4.4	—	—	4.4	—	4.4	—	or	to	—	—	—	—	—	—			
	V _{IH}			6	5.9	—	—	5.9	—	5.9	—	V _{IH}	5.5	—	—	—	—	—	—			
TTL Loads	V _{IL}											V _{IL}	4.5	3.98	—	—	3.84	—	3.7	—	V	
	or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or	to	—	—	—	—	—	—				
	V _{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V _{IH}	5.5	—	—	—	—	—	—				
Low-Level Output Voltage V _{OL}	V _{IL}	0.02		2	—	—	0.1	—	0.1	—	0.1	V _{IL}	4.5	—	—	0.1	—	0.1	—	0.1	V	
CMOS Loads	V _{IL}			4.5	—	—	0.1	—	0.1	—	0.1	—	or	to	—	—	—	—	—			
	V _{IH}			6	—	—	0.1	—	0.1	—	0.1	—	V _{IH}	5.5	—	—	—	—	—			
TTL Loads	V _{IL}											V _{IL}	4.5	—	—	0.26	—	0.33	—	0.4	V	
	or	4	4.5	—	—	0.26	—	0.33	—	0.4	—	or	to	—	—	—	—	—				
	V _{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	—	V _{IH}	5.5	—	—	—	—	—				
Input Leakage Current I _I	V _{CC}			6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current I _{CC}	V _{CC}	0	6	—	—	8	—	80	—	160	—	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA	
Additional Quiescent Device Current per input pin: 1 unit load Δ I _{CC} *												V _{CC} -2.1	4.5	to	—	100	360	—	450	—	490	μA
												5.5	5.5	—	—	—	—	—	—	—	—	μA

*For dual-supply systems theoretical worst case (V_i = 2.4 V, V_{cc} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
MR	0.65
φ	0.5

*Unit Load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.



TERMINAL ASSIGNMENT

CD54/74HC4040

CD54/74HCT4040

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input t_i , $t_r = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	C_L pF	Typical		
			HC	HCT	Units
Propagation Delay ϕ to Q1' Output	t_{PLH} t_{PHL}	15	11	17	ns
Propagation Delay Q_n to Q_{n+1}	t_{PLH} t_{PHL}	15	4	4	ns
Propagation Delay to MR to Q_n	t_{PHL}	15	14	17	ns
Power Dissipation Capacitance*	C_{PD}	—	40	45	pF

* C_{PD} is used to determine the power consumption, per package.

$PD = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_i / M)$ where:

$M = 2^1, 2^2, 2^3, \dots, 2^{i-2}$

C_L = output load capacitance

f_i = input frequency

Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V _{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Input Pulse Frequency	f _{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	24	—	—	—	
Input Pulse Width (Figure 4)	t _w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time (Figure 5)	t _{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Reset Pulse Width (Figure 5)	t _w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_i, t_r = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	V _{CC}	25° C						-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT				
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.			
Propagation Delay ϕ to Q1' Output (Figure 4)	t _{PLH}	2	—	140	—	—	—	175	—	—	—	210	—	—	ns		
	t _{PHL}	4.5	—	28	—	40	—	35	—	50	—	42	—	60			
		6	—	24	—	—	—	30	—	—	—	36	—	—			
Propagation Delay Q _n to Q _{n+1} (Figure 4)	t _{PLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns		
	t _{PHL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22			
		6	—	13	—	—	—	16	—	—	—	19	—	—			
Propagation Delay MR to Q _n (Figure 5)	t _{PHL}	2	—	170	—	—	—	215	—	—	—	255	—	—	ns		
		4.5	—	34	—	40	—	43	—	50	—	51	—	60			
		6	—	29	—	—	—	37	—	—	—	43	—	—			
Output Transition Time (Figure 4)	t _{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns		
	t _{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22			
		6	—	13	—	—	—	16	—	—	—	19	—	—			
Input Capacitance	C _i		—	10	—	10	—	10	—	10	—	10	—	10	pF		

CD54/74HC4040
CD54/74HCT4040

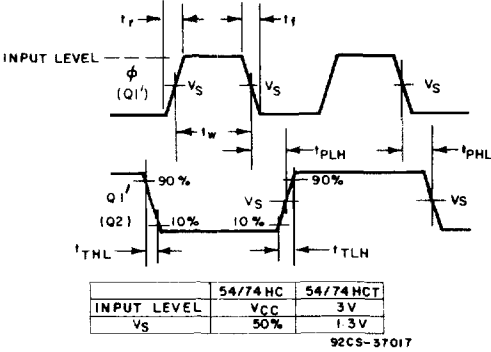


Fig. 4 - Input pulse pre-requisite times, propagation delays and output transition times.

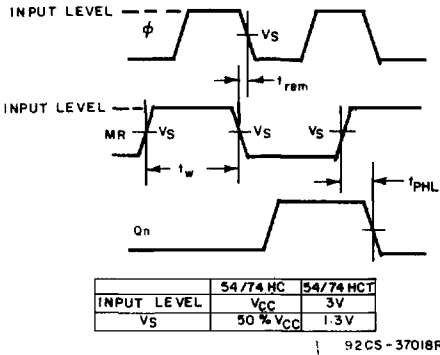


Fig. 5 - Master Reset pre-requisite and propagation delays.