

SN54HCT02, SN74HCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS065C – NOVEMBER 1988 – REVISED JUNE 2000

- Inputs Are TTL-Voltage Compatible
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

description

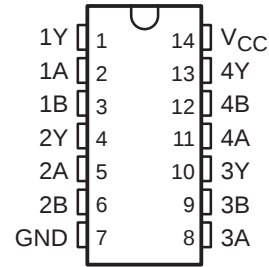
These devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A + B}$ in positive logic.

The SN54HCT02 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT02 is characterized for operation from -40°C to 85°C .

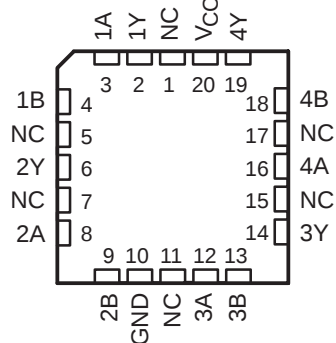
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

SN54HCT02 . . . J OR W PACKAGE
SN74HCT02 . . . D, DB, OR N PACKAGE
(TOP VIEW)

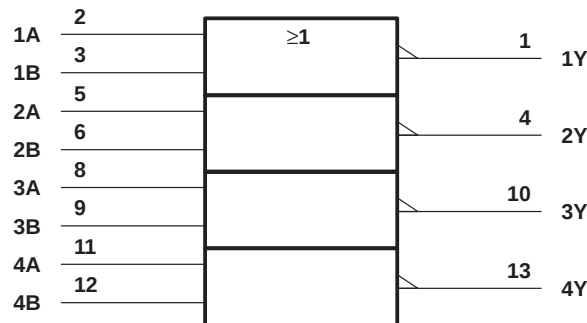


SN54HCT02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, and W packages.

logic diagram, each gate (positive logic)



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**TEXAS
INSTRUMENTS**

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SN54HCT02, SN74HCT02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			SN54HCT02			SN74HCT02			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time		0		500	0		500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT02		SN74HCT02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$	4.5 V	4.4	4.499		4.4		4.4		V
		$I_{OH} = -4\ \text{mA}$		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$	4.5 V		0.001	0.1		0.1		0.1	V
		$I_{OL} = 4\ \text{mA}$			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$		5.5 V			2		40		20	μA
$\Delta I_{CC}^\ddagger$	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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SN54HCT02, SN74HCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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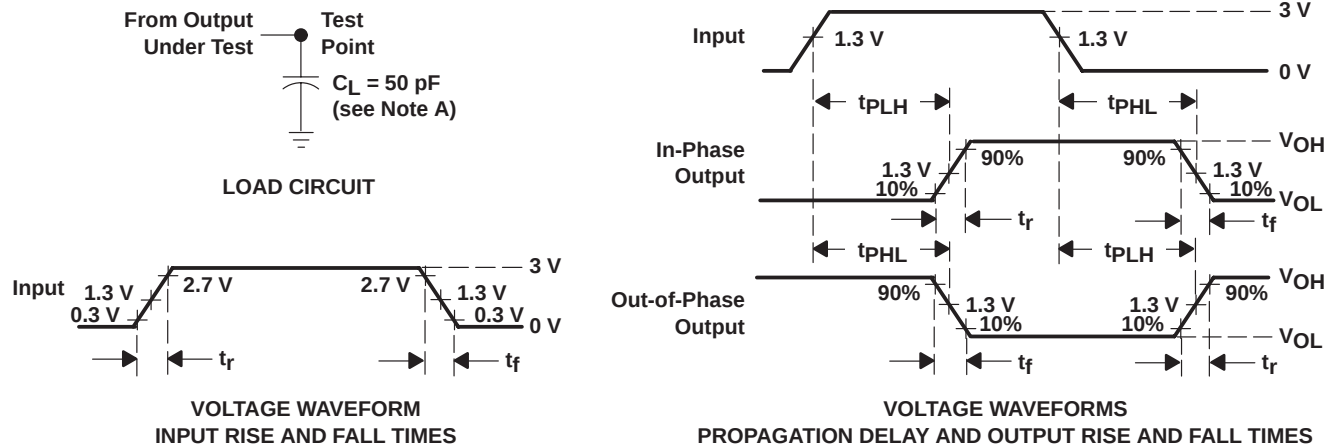
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT02		SN74HCT02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		11	20		30		25	ns
			5.5 V		10	18		27		22	
t_t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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SN74HCT02, Quadruple 2-Input Positive-NOR Gates

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74HCT02
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	CMOS
Output Drive (mA)	-4/4
No. of Gates	4
Static Current	0.02
tpd max (ns)	22

FEATURES

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DESCRIPTION

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TECHNICAL DOCUMENTS

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DATASHEET

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Full datasheet in Acrobat PDF: [sn74hct02.pdf](#) (71 KB,Rev.C) (Updated: 06/21/2000)

APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [CMOS Power Consumption and CPD Calculation \(Rev. B\)](#) (SCAA035B - Updated: 06/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [SN54/74HCT CMOS Logic Family Applications and Restrictions](#) (SCLA011 - Updated: 05/01/1996)
- [Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

View Related Documentation for [Digital Logic](#)

- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES		▲Back to Top				
ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74HCT02D	SOP (D)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HCT02N	PDIP (N)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG							▲Back to Top			REPORTED DISTRIBUTOR INVENTORY		
DEVICE INFORMATION							TI INVENTORY STATUS			AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74HCT02D	ACTIVE	SOP (D) 14	-40 TO 85	View Contents	1KU 0.22	50	N/A*	10k 07 Oct	3 WKS	Avnet AMERICA	> 1k	BUY NOW
										DigiKey AMERICA	580	BUY NOW
SN74HCT02DR	ACTIVE	SOP (D) 14	-40 TO 85	View Contents	1KU 0.22	2500	N/A*	10k 03 Oct	2 WKS	Avnet AMERICA	> 1k	BUY NOW
								10k 07 Oct				
								> 10k 14 Oct				
								> 10k 28 Oct				
SN74HCT02N	ACTIVE	PDIP (N) 14	-40 TO 85	View Contents	1KU 0.22	25	N/A*		2 WKS	Avnet AMERICA	> 1k	BUY NOW
SN74HCT02NSR	ACTIVE	SOP (NS) 14		View Contents	1KU 0.42	2000	N/A*		6 WKS			
SN74HCT02PWR	ACTIVE	TSSOP (PW) 14		View Contents	1KU 0.22	2000	N/A*		6 WKS			

Table Data Updated on: 9/26/2002