AOZ13987DI-02

ECPower™ 23V 20mΩ Smart Protection Switch With Ideal Diode True Reverse Current Blocking

General Description

AOZ13987DI-02 is protection switch intended for applications that require reverse current protection. The input operating voltage range is from 3.4V to 23V, and both VIN and VOUT terminals are rated at 28V absolute maximum. The power switch is capable for 20A surge current for 10ms. AOZ13987DI-02 provides under-voltage lockout, over-voltage, and over-temperature protection. The FLTB pin flags thermal shutdown and over-voltage faults.

AOZ13987DI-02 is the ideal solution for multi-port Type-C PD current sinking application. The Ideal Diode True Reverse Current Blocking (IDTRCB) feature prevents VIN to rise due to reverse current flow from VOUT under all conditions.

An internal soft-start circuit controls inrush current due to highly capacitive loads and the slew rate can be adjusted using an external capacitor. The integrated back-to-back MOSFET offer industry's lowest ON resistance and highest SOA to safely handle high current and wide range of output capacitances on VOUT.

The AOZ13987DI-02 is available in a thermally enhanced 3mm x 3mm DFN-12 package which can operate over -40°C to +125°C junction temperature range.

Features

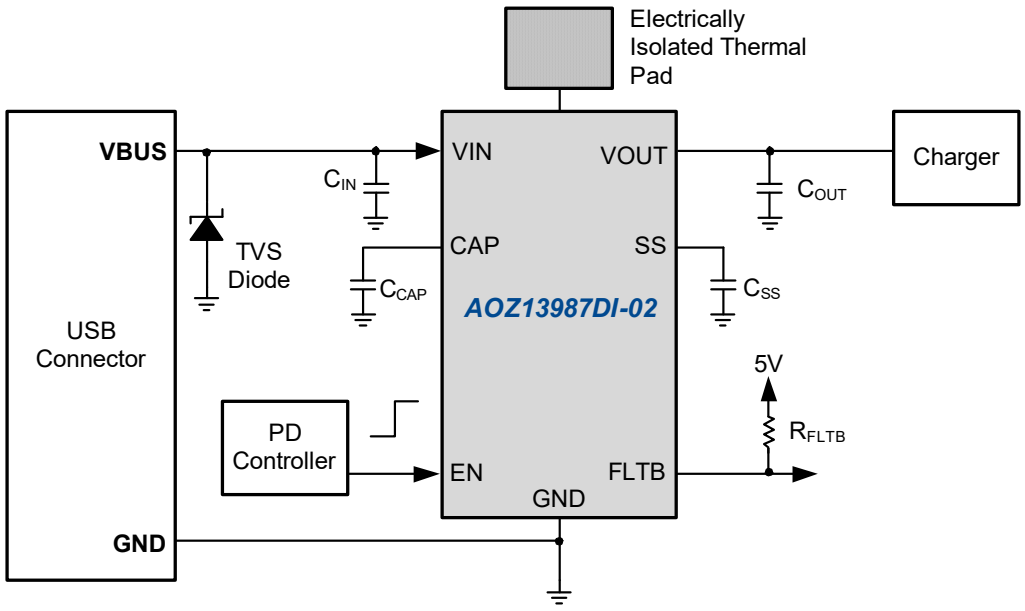
- 8A continuous sink current
- 20A peak current for 10ms @ 2% duty cycle
- 20mΩ typical ON resistance
- 3.4V to 23V operating input voltage
- VIN and VOUT are rated 28V Abs max
- Ideal Diode True Reverse Current Blocking (IDTRCB)
- Programmable soft-start
- VIN Under-Voltage Lockout (UVLO)
- VIN Over-Voltage Lockout (OVLO)
- Thermal shutdown protection
- Startup Short Circuit Protection
- IEC 61000-4-2: ±8kV on VIN and VOUT
- IEC 61000-4-5: 35V on VIN, no cap
- Thermally enhanced DFN3x3-12L package

Applications

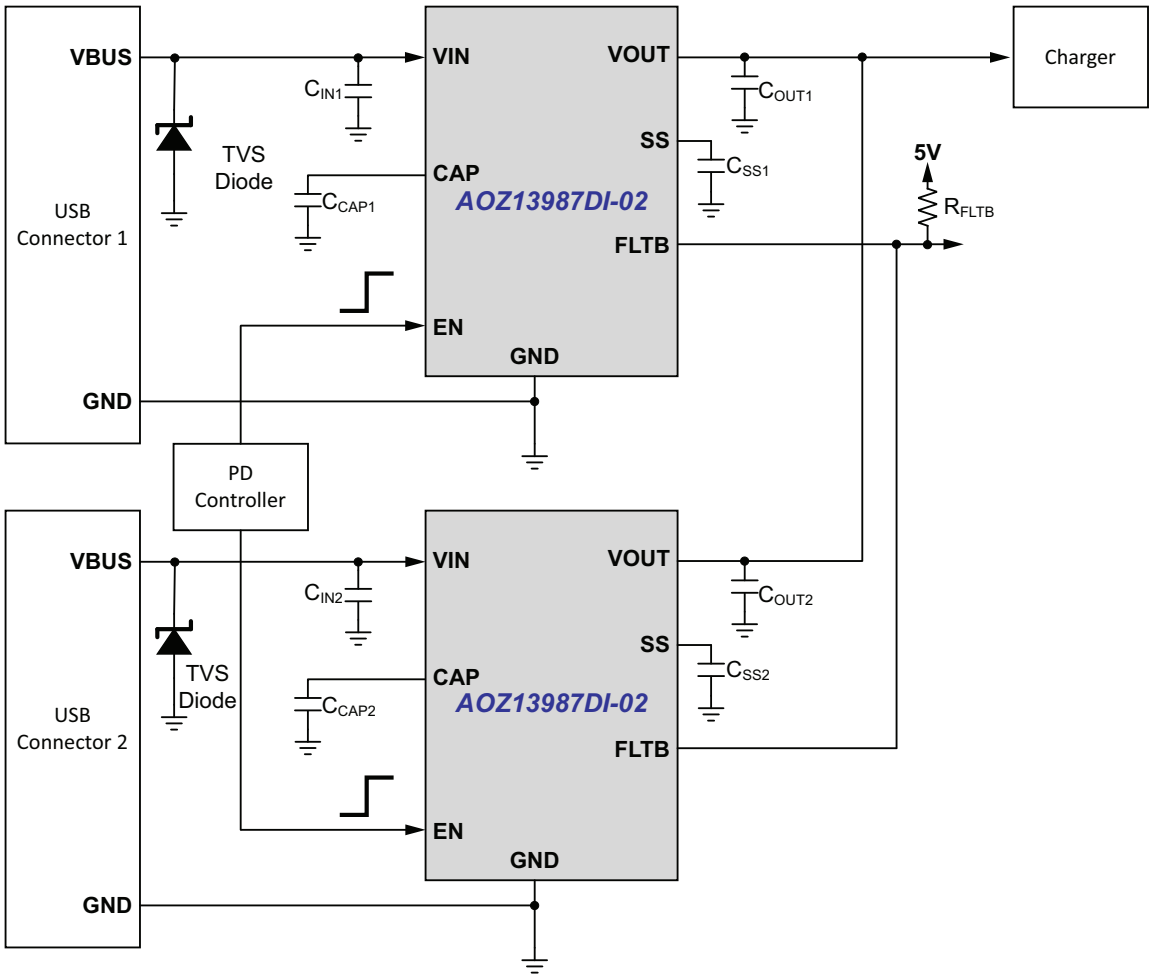
- Thunderbolt/USB Type-C PD power switch
- Notebook computers
- Docking station/dongles
- Power ORing applications

Green Product

Typical Application



Dual Port Typical Application

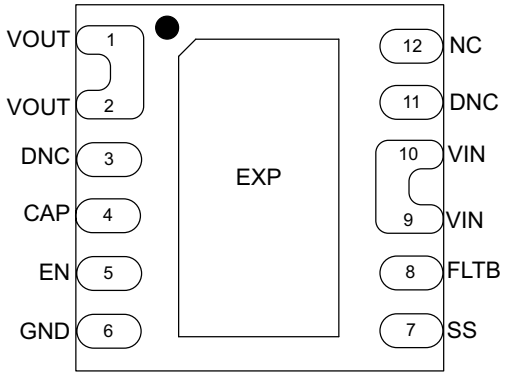


Ordering Information

Part Number	SCP Response	Junction Temperature Range	Package	Environmental
AOZ13987DI-02	Latch-off	-40°C to +125°C	DFN3x3-12L	RoHS

All AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



DFN3x3-12L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1, 2	VOUT	Output pins. Connect to internal load.
3	DNC	Do Not Connect. Internally connected to Exposed Pad (EXP).
4	CAP	Connect a 1nF capacitor to GND.
5	EN	Enable active high.
6	GND	Ground.
7	SS	Soft-start pin. Connect a capacitor C_{SS} from SS to GND to set the soft-start time.
8	FLTB	Fault Indicator, open-drain output. Pull low after a fault condition is detected.
9, 10	VIN	Connect to adapter or power input. Place a 10µF capacitor from VIN to GND.
11	DNC	Do Not Connect. Internally connected to VIN.
12	NC	No connect.
EXP	EXP	Exposed Thermal Pad. It is the common drain node for the power switches and it must be electrically isolated. Solder to a metal surface directly underneath the EXP and connect to floating copper thermal pads on multiple PCB layers through many VIAs. For best thermal performance, make the floating copper pads as large as possible.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VIN, VOUT to GND	-0.3V to +28V
EN, SS, FLTB to GND	-0.3V to +6V
CAP to VIN	-0.3V to +6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating HBM All Pins(1)	±2kV
IEC 61000-4-2: VIN and VOUT Pins	±8kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model is a 100pF capacitor discharging through a 1.5kΩ resistor.

Recommend Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
Supply Voltage (VIN)	3.4V to 23V
EN, FLTB	0V to 5.5V
SS	0V to 5.5V
CAP to VIN	0V to 5.5V
DC Switch Current (I_{SW})	0A to 8A
Peak Switch Current (I_{SW}) for 10ms @ 2% Duty Cycle	20A
Junction Temperature (T_J)	-40°C to +125°C
Package Thermal Resistance 3x3 DFN-12 (Θ_{JC}) 3x3 DFN-12 (Θ_{JA})	 2°C/W 35°C/W

Electrical Characteristics

T_A = 25°C, VIN = 20V, EN = 5V, C_{CAP} = 1nF, C_{IN} = 10µF, C_{OUT} = 10µF, C_{SS} = 5.6nF, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{VIN}	Input Supply Voltage		3.4		23	V
V_{UVLO}	Under-voltage Lockout Threshold	VIN rising	3.0		3.35	V
V_{UVLO_HYS}	Under-voltage Lockout Hysteresis			250		mV
I_{VIN_ON}	Input Quiescent Current	I_{OUT} = 0 A		550	750	µA
I_{VIN_OFF}	Input Shutdown Current	I_{OUT} = 0 A, EN = 0V		32	48	µA
I_{VOUT_OFF}	Output Leakage Current	VOUT = 20V, VIN = 0V, EN = 0 V		32	48	µA
R_{ON_20V}	Switch On Resistance(2)	I_{OUT} = 1A		20		mΩ
R_{ON_5V}		VIN = 5V, I_{OUT} = 1A		21		mΩ
V_{EN_H}	Enable Input High Threshold	EN rising			1.4	V
V_{EN_L}	Enable Input Low Threshold	EN falling	0.6			V
R_{EN_LO}	EN Input Pull-down Resistance		475	730	985	kΩ
V_{FLTB_LO}	FLTB Pull-down Voltage	FLTB sinking 3mA			0.3	V
Input Over-voltage Protection						
V_{OVP}	Over-voltage Protection Threshold	VIN rising	23.1	24	25	V
t_{OVP_DEB}	Over-voltage Protection Debounce Time	Latch off. No restart		512		µs
True Reverse Current Blocking						
V_{IDTRCB}	Ideal Diode TRCB Regulation Voltage	VIN - VOUT		35		mV

Note:

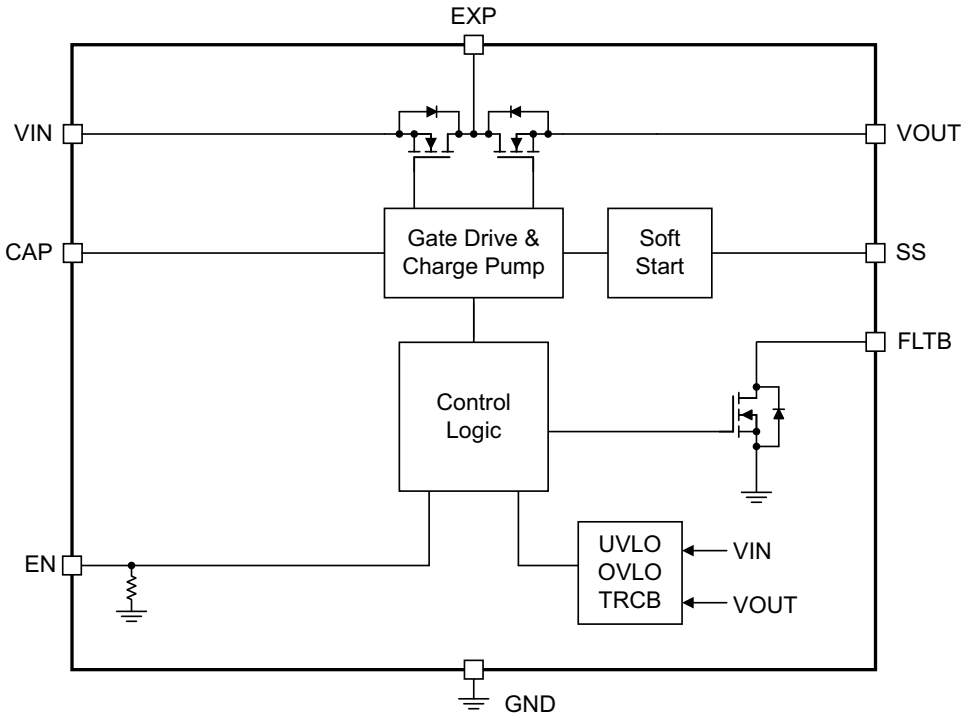
2. On resistance is tested under test mode to bypass ideal diode function.

Electrical Characteristics

T_A = 25°C, VIN = 20V, EN = 5V, C_{CAP} = 1nF, C_{IN} = 10µF, C_{OUT} = 10µF, C_{SS} = 5.6nF, unless otherwise specified.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
Dynamic Timing Characteristics						
t_{D_ON}	Turn-On Delay Time	From EN rising edge to VOUT reaching 10% of VIN		8		ms
t_{ON}	Turn-On Rise Time	VOUT from 10% to 90% of VIN		1.9		ms
t_{OFF}	Turn-Off Fall Time	From EN falling edge to I_{OUT} = 0 A		32		µs
Thermal Shutdown Protection						
T_{SD}	Thermal Shutdown Threshold	Temperature rising. System latch off.		140		°C

Functional Block Diagram



Timing Diagrams

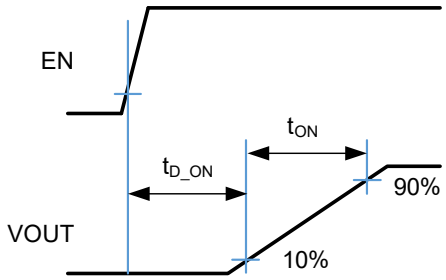


Figure 1. Turn-on Delay and Turn-on Time

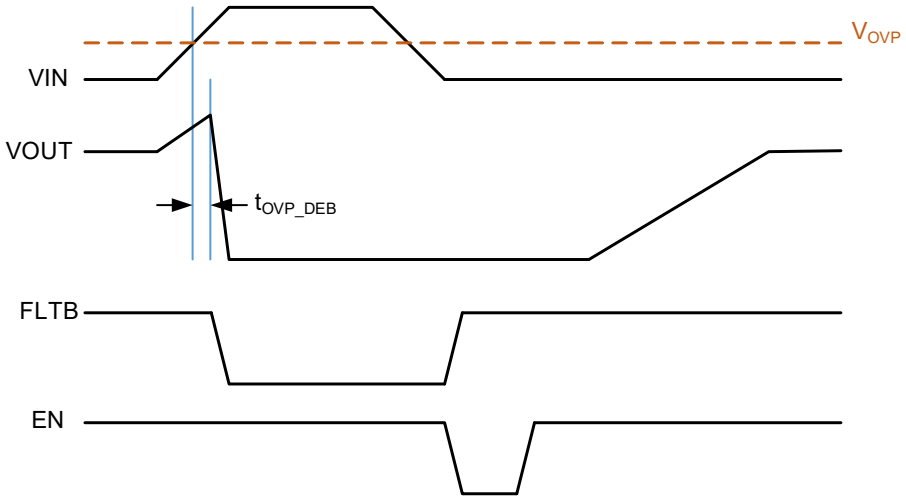
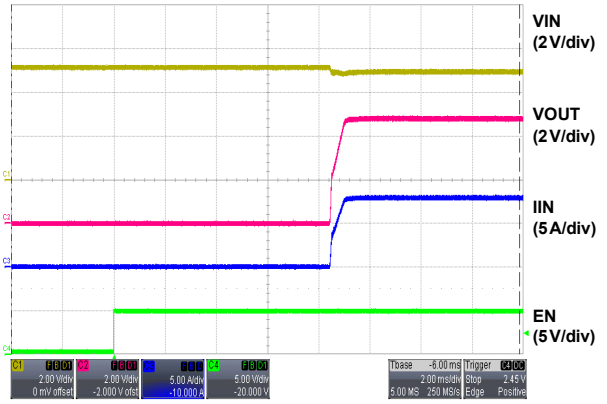


Figure 2. Over-Voltage Protection

Typical Characteristics

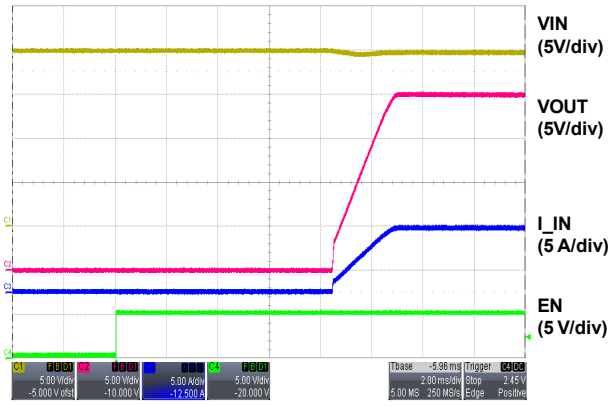
T_A = 25°C, VIN = 20V, EN = 5V, C_{IN} = 10 µF, C_{OUT} = 10µF, C_{SS} = 5.6nF, C_{CAP} = 1nF, unless otherwise specified.

Soft-Start Delay (VIN = 5V, R_{OUT} = 0.6Ω)



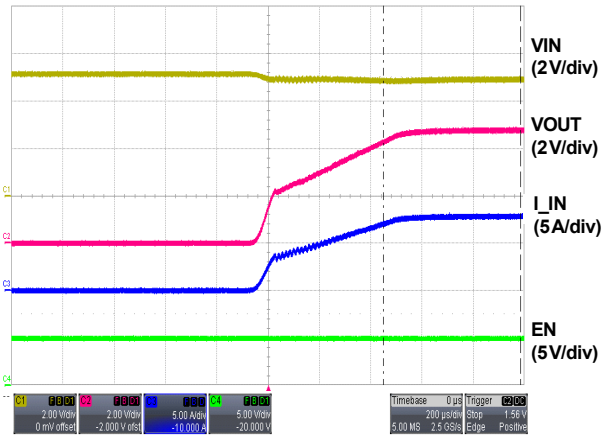
2 ms/div

Soft-Start Delay (VIN = 20V, R_{OUT} = 2.8Ω)



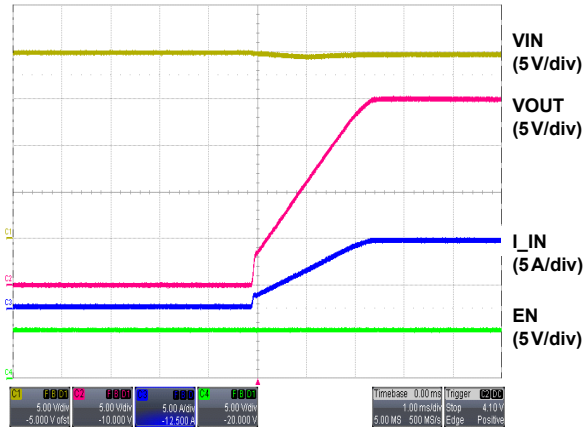
2 ms/div

Soft-Start Ramp (VIN = 5V, R_{OUT} = 0.6Ω)



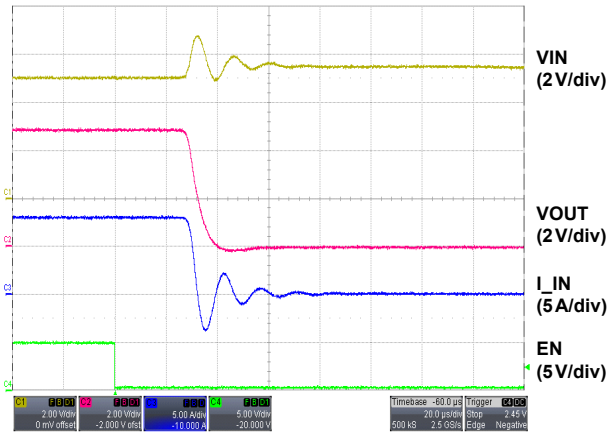
200µs/div

Soft-Start Ramp (VIN = 20V, R_{OUT} = 2.8Ω)



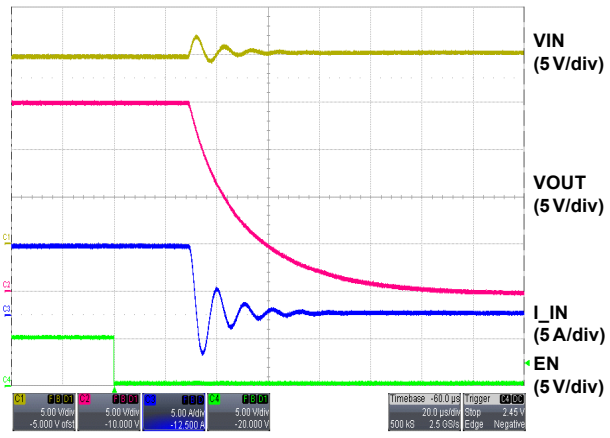
1 ms/div

Shutdown (VIN = 5V, R_{OUT} = 0.6Ω)



20 µs/div

Shutdown (VIN = 20V, R_{OUT} = 2.8Ω)

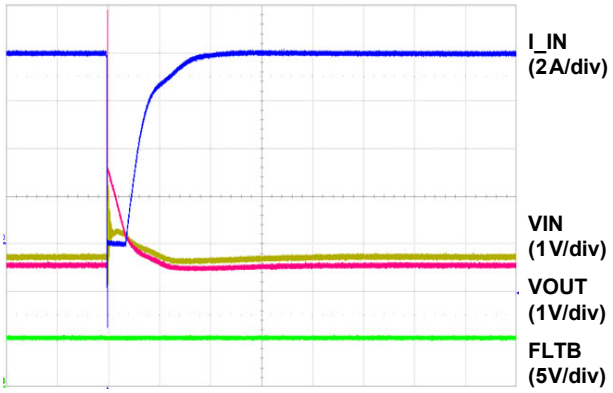


20 µs/div

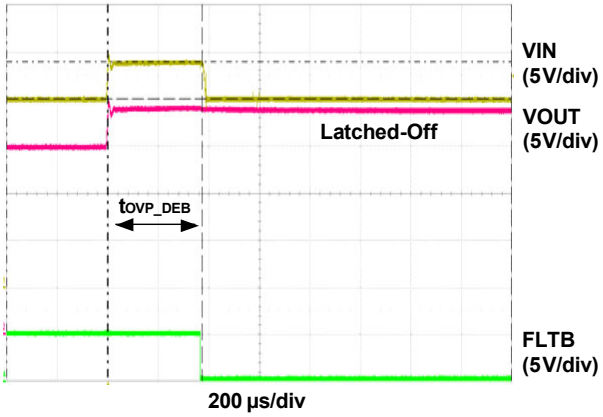
Typical Characteristics *(Continued)*

T_A = 25°C, VIN = 20V, EN = 5V, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{SS} = 5.6 nF, C_{CAP} = 1 nF, unless otherwise specified.

True Reverse Current Blocking and Recovery (R_{OUT} = 20Ω)



Over-Voltage Protection (R_{OUT} = Open)



Typical Characteristics *(Continued)*

T_A = 25°C, unless otherwise specified.

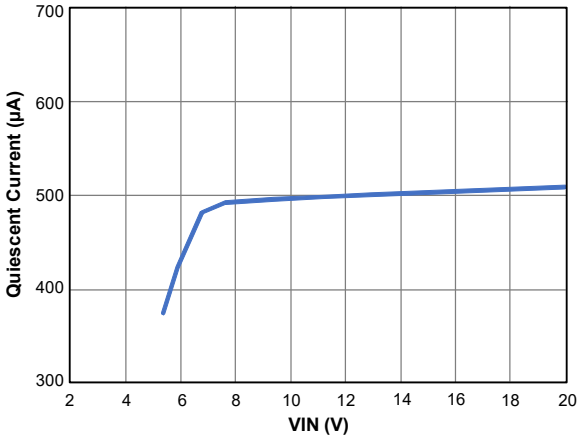


Figure 3. Quiescent Current vs. VIN

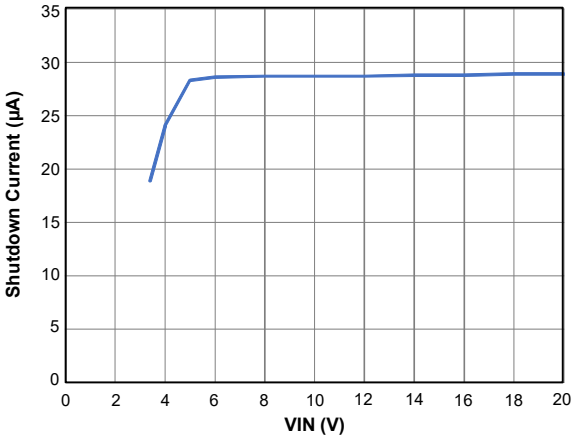


Figure 4. Shutdown Current vs. VIN

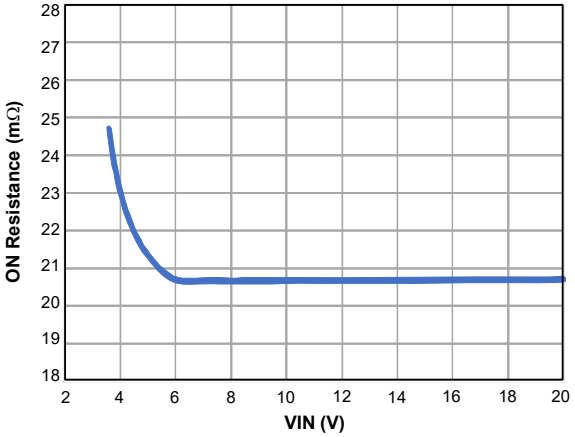


Figure 5. ON Resistance vs. VIN

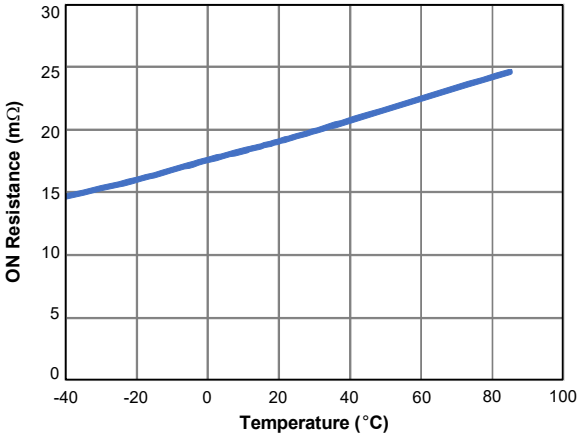


Figure 6. ON Resistance vs. Temperature (VIN=20V)

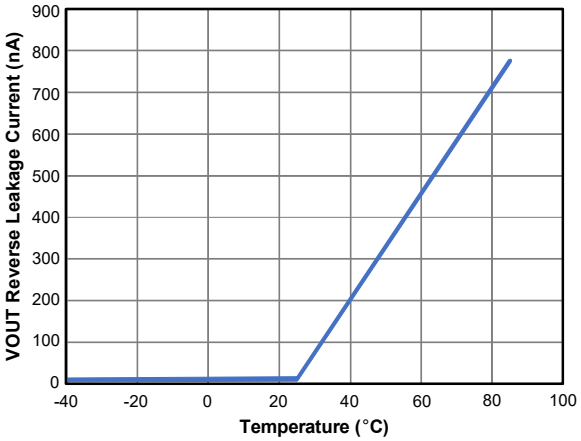


Figure 7. VOUT Reverse Leakage Current vs. Temperature

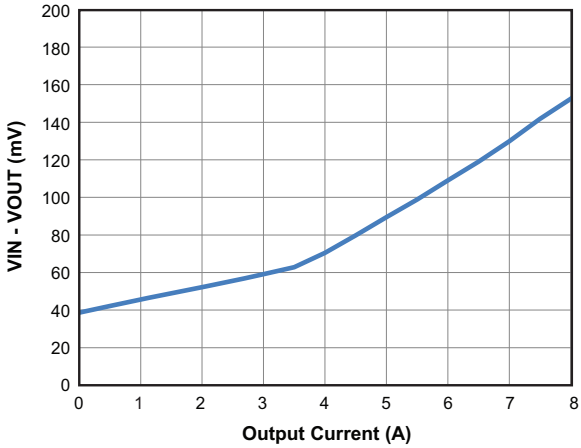


Figure 8. VIN-VOUT vs. Output Current

Detailed Description

The AOZ13987DI-02 is a high-side protection switch with programmable soft-start, over-voltage, and over-temperature protections. It is capable of operating from 3.4 V to 23 V

The internal power switch consists of back-to-back connected MOSFET. When the switch is enabled, the overall resistance between VIN and VOUT is only 20 mΩ when I_{OUT} > 3.5A, minimizing power loss and heat generation. The back-to-back configuration of MOSFET completely isolates VIN and VOUT when the switch is turned off, preventing leakage between the two pins.

Power Delivery Capability

During start-up, the voltage at VOUT linearly ramps up to the VIN voltage over a period of time set by the soft-start time. This ramp time is referred to as the soft-start time and is typically in milliseconds. Figure 9 illustrates the soft-start condition and power dissipation.

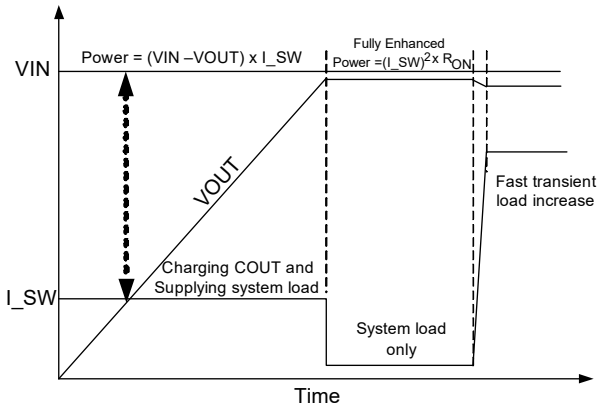


Figure 9. Soft-Start Power Dissipation

During this soft-start time, there will be a large voltage across the power switch. Also, there will be current I_SW through the switch to charge the output capacitance. In addition, there may be load current to the downstream system as well. This total current is calculated as:

$$I_{SW} = C_{OUT}\left(\frac{dVOUT}{dt}\right) + I_{SYS}$$

In the soft-start condition, the switch is operating in the linear mode, and power dissipation is high. The ability to handle this power is largely a function of the power MOSFET linear mode SOA and good package thermal performance $R\Theta_{JC}$ (Junction-to-Case) as the soft-start ramp time is in milliseconds. $R\Theta_{JA}$ (Junction-to-Ambient), which is more a function of PCB thermal performance, doesn't play a role.

With a high-reliability MOSFET as the power switch and superior packaging technology, the AOZ13987DI-02 is capable of dissipating this power. The power dissipated is:

$$Power\ Dissipated = I\_SW \times (VIN - VOUT)$$

To calculate the average power dissipation during the soft-start period: ½ of the input voltage should be used as the output voltage will ramp towards the input voltage, as shown in Figure 9.

For example, if the output capacitance C_{OUT} is 10 µF, the input voltage VIN is 20 V, the soft-start time is 2 ms, and there is an additional 1 A of system current (I_SYS), then the average power being dissipated by the part is:

$$I_{SW} = 10\,uF\left(\frac{20\,V}{2\,ms}\right) + 1\,A = 1.1\,A$$

Average Power Dissipation

$$= 1.1\,\boldsymbol{A} \times \frac{20\,\boldsymbol{V}}{2} = 11\,\boldsymbol{W}$$

Referring to the SOA curve in Figure 10, the maximum power allowed for 2 ms is 100 W (5 A x 20V or 10A x 10V). The AOZ13987DI-02 power switch is robust enough to drive a large output capacitance with load in reasonable soft-start time.

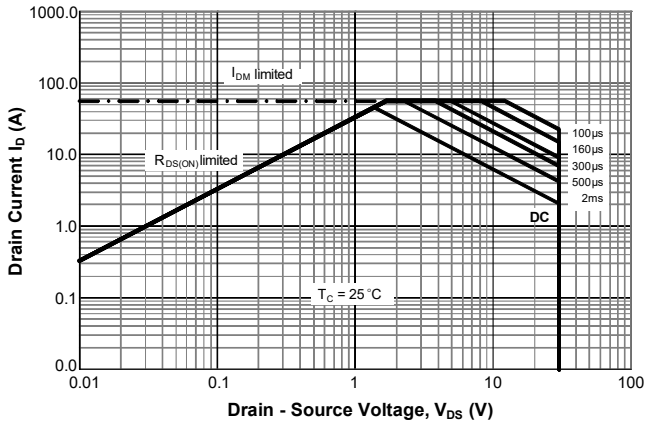


Figure 10. Safe Operating Area (SOA) Curves for Power Switch

After soft-start is completed, the power switch is fully on, and it is at its lowest resistance. The power switch acts as a resistor. Under this condition, the power dissipation is much lower than the soft-start period. However, as this is a continuous current, a low on-resistance is required to minimize power dissipation. Attention must be paid to board layout so that losses dissipated in the sinking switch are dissipated to the PCB and hence the ambient.

With a low on-resistance of 20 mΩ, the AOZ13987DI-02 provides the most efficient power delivery without much resistive power dissipation.

While Type C power delivery is limited to 20V @ 5A or a 100W, many high-end laptops require peak currents far in excess of the 5 A. While the thermal design current (TDC) for a CPU may be low, peak current (ICCmax in the case of Intel and EDP in the case of AMD) of many systems is often 2 x thermal design current. These events are typical of short duration (< 2ms) and low duty cycle, but they are important for system performance as a CPU/GPU capable of operating at several GHz can boost its compute power in those 2ms peak current events. The AOZ13987DI-02 can handle such short, high current, transient pulses without any reliability degradation, thus enhancing the performance of high-end systems when plugged into the Type C adapter. The shorter the pulse and the lower the duty cycle, the higher the pulse current that the part can sustain. The part has enough time to dissipate the heat generated from the pulse current with longer off-time, as shown in Figure 11. For example, AOZ13987DI-02 can maintain 20A for 10ms with a duty cycle of 2%.

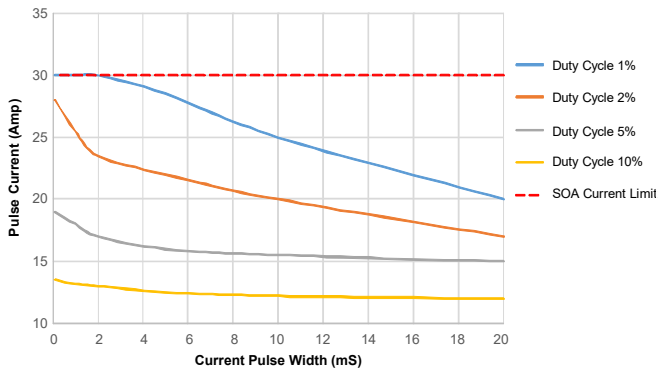


Figure 11. AOZ13987DI-02 Sinking Switch Pulsed Current vs. Duration for a Given Duty Cycle

Enable

The active high EN pin is the ON/OFF control for the power switch. The device is enabled when the EN pin is high and not in UVLO state. The EN pin must be driven to a logic high (V_{EN_H}) or logic low (V_{EN_L}) state to guarantee operation. AOZ13987DI-02 draws about 32 µA supply current when it is disabled.

Input Under-Voltage Lockout (UVLO)

The internal control circuit is powered from VIN. The under-voltage lockout (UVLO) circuit monitors the voltage at the input pin (VIN) and only allows the power switches to turn on when it is higher than 3.35V (V_{UVLO}).

Over-Voltage Protection (OVP)

The voltages at VIN pin are constantly monitored once the device is enabled. In case the voltage exceeds the OVLO threshold, over-voltage protection is activated:

1) If the power switch is on, it will be turned off after OVP debounce time (t_{OVP_DEB}) to isolate VOUT from VIN;
2) OVP will prevent power switch to be turned on if it is in off state;

In either case FLTB pin is pulled low to report the fault condition. The device can only be re-enabled by either toggling EN pin or cycling the input power supply.

True Reverse Current Blocking

When the device is ON with no load or under light load conditions, it regulates VOUT to be 35 mV below VIN. As the load current is increasing or decreasing, the device adjusts the gate drive to maintain the 35mV drop from VIN to VOUT. As the load current continues to increase the device increases the gate drive until the gate is fully turned on and VIN to VOUT drop is determined by IR drop through the MOSFET. If for any reason VOUT increases such that VIN to VOUT drop to less than 35 mV, the gate driver forces the switch to turn off.

Thermal Shutdown Protection

When the die temperature reaches 140 °C, the power switch is turned off. The device can only be re-enabled by either toggling EN pin or cycling the input power supply.

Soft-Start Slew-Rate Control

When EN pin is asserted high, the slew rate control applies voltage on the gate of the power switch in a manner such that the output voltage is ramped up linearly until VOUT reaches VIN voltage level. The output ramps up time (t_{ON}) is programmable by an external soft-start capacitor (C_{SS}). The following formula provides the estimated 10% to 90% ramp up time.

$$t_{ON} = \frac{VIN}{24} \times \left(\frac{C_{ss}}{0.0023} - 100 \right)$$

where Css is in nF and t_{ON} is in µs.

System Startup

The device is enabled when EN ≥ 1.4V and VIN is higher than UVLO threshold (V_{UVLO}). The device will check if any fault condition exists. If no fault exists, the power switch is turned on and VOUT is then ramped up after enable delay (t_{D_ON}), controlled by the soft-start time (t_{ON}) until VOUT reaches VIN voltage level. Soft-start time can be programmed externally through SS input with a capacitor C_{SS} to control in-rush current.

In-rush Current Limit and SCP at Start Up

AOZ13987DI-02 has the current limit and short circuit protection functions at start up. The current limit ramp increases linearly and reaches to a fixed current within 1.25ms. With this fixed current limit ramp, the inrush current can be effectively clamped to reduce the initial current spikes. At initial startup, the internal power switch carries large voltage close to Vin and has large power loss. To ensure the internal FET working in Safe Operation Area (SOA), a fixed timer is set to shut down the power switch if the inrush current is clamped by current limit ramp for about 512µs continuously. This timer will be reset once the inrush current drops below the current limit ramp. For short circuit event, the part will shut down after this 512µs timer is finished. In case of large output capacitors, the soft-start time needs to increase to avoid the large inrush current hit the current limit ramp for 512µs. Both current limit and SCP shutdown are disabled after soft-start time is finished.

Fault Protection

The AOZ13987DI-02 offers multiple protection against the following fault conditions: VIN over-voltage (OVLO), Reverse Current Blocking when VOUT > VIN, and over temperature.

When the device is first enabled, the power switch is off and fault conditions are checked. If any of these conditions exist:

1. VIN is higher than the OVP threshold (V_{OVLO});
2. VOUT is higher than VIN;
3. Die temperature is higher than thermal shutdown threshold (T_{SD});

The power switch will not be turned on and FLTB pin will be pulled low only for OVP and TSD conditions but not TRCB condition to indicate fault status of the device.

The power switch will be turned on once TRCB condition no longer exists. The device will continuously monitor these fault conditions. In addition, the short circuit condition is being monitored during the soft start.

Input Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on to charge output capacitors and to limit input voltage drop. It is also to prevent high-frequency noise on the power line from passing through to the output. The input capacitor should be located as close to the pin as possible. A 10µF ceramic capacitor is recommended. The USB specification limits the capacitance on VBUS to a maximum of 10µF. Use this maximum value for noise immunity due to the system and cable plug/unplug transients.

Output Capacitor Selection

The output capacitor has to supply enough current for a large peak current load that it may encounter during system transient. This bulk capacitance must be large enough to supply fast transient load in order to prevent the output from dropping.

Power Dissipation Calculation

Calculate the power dissipation for normal load condition using the following equation:

$$Power\ Dissipated = R_{ON} \times (I_{OUT})^2$$

Layout Guidelines

AOZ13987DI-02 is a protection switch designed deliver high current. Layout is critical to remove the heat generated by this current. For the most efficient heat sinking, connect as much copper as possible to the exposed pad. The exposed pad is the common drain of the power switch which must be electrically isolated.

On the top layer expand the exposed pad island as much as possible for optimal thermal performance. The exposed pad copper plane must be electrically isolated. See example in Figure 12.

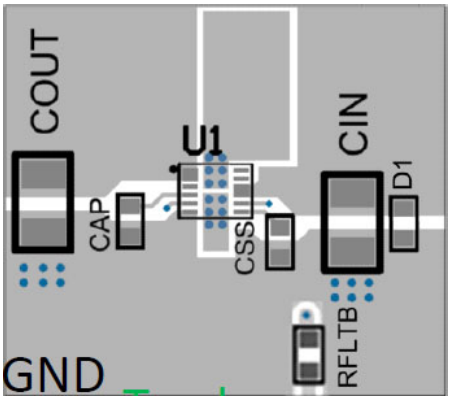


Figure 12. Top Layer Layout. Maximum number of VIAs from top layer exposed pad to inner layer.

There are two ways to create thermal islands on the inner layers as showed in Figure13. The more layers that have these electrically isolated thermal heat sink islands the better the thermal performance will be. Connect all isolated thermal island (top, inner layers and bottom) together with as many VIAs as possible.

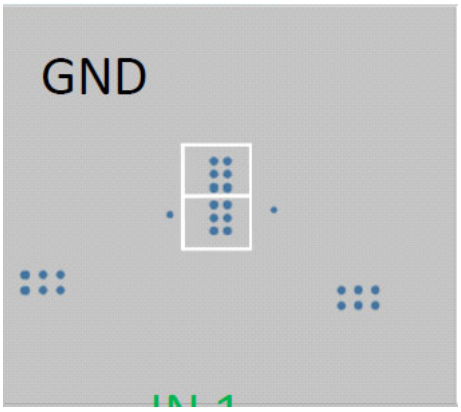


Figure 13. Inner Layer Layout. Create electrically isolated thermal island with flooded plane.

On the bottom layer, similar to the inner layers, create an isolated thermal island. Typically, there is more area available on the bottom area for a larger thermal pad. The top and bottom layers have better thermal performance than the inner layers because they are exposed to the atmosphere. See example in Figure14.

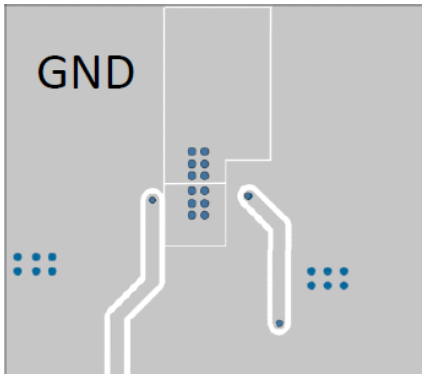
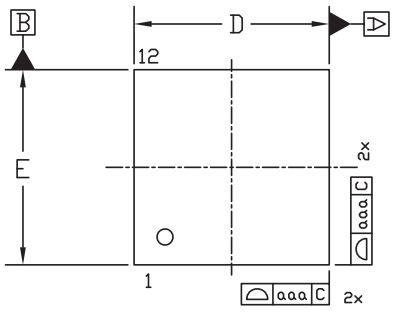
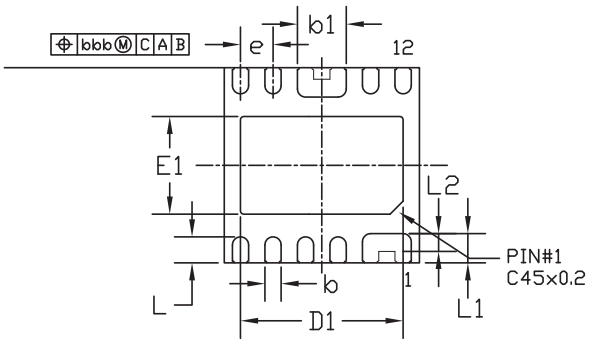


Figure 14. Bottom Layer Layout. Create a large electrically isolated thermal pad.

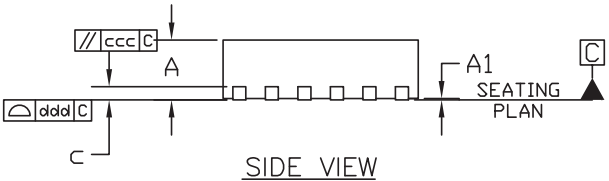
Package Dimensions, DFN3x3-12L



TOP VIEW

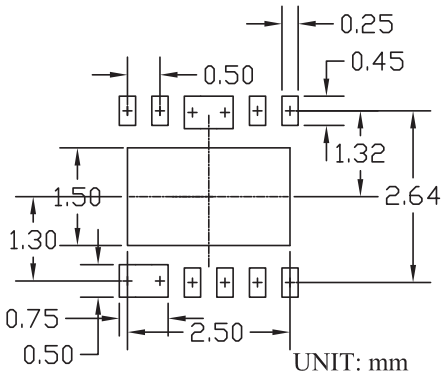


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



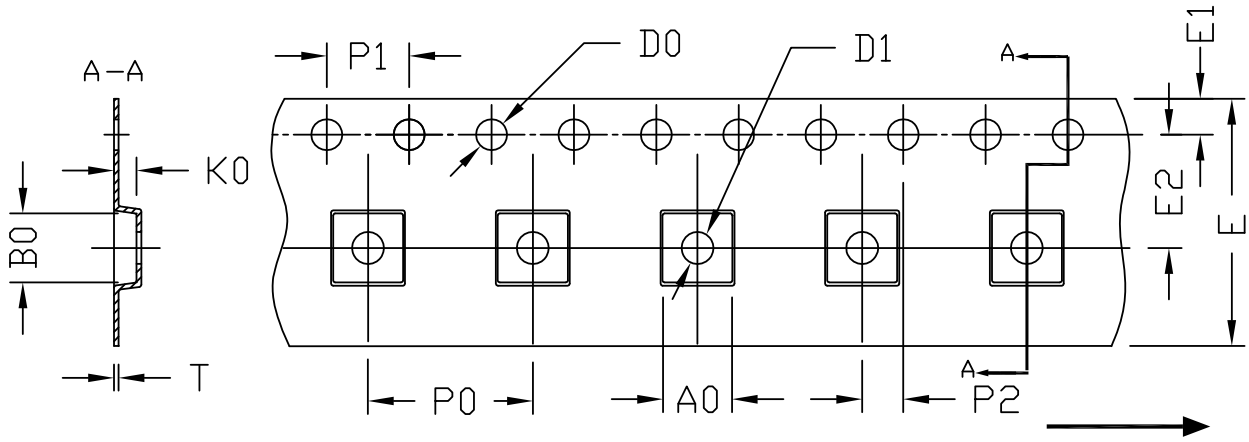
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.70	0.75	0.80	0.028	0.030	0.032
c	0.195	0.203	0.211	0.008	0.008	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.40	2.50	2.60	0.094	0.098	0.102
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	1.40	1.50	1.60	0.055	0.059	0.063
e		0.50BSC			0.020BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.35	0.45	0.55	0.014	0.018	0.022
L2	0.22	0.27	0.32	0.009	0.011	0.013
aaa		0.15			0.006	
bbb		0.10			0.004	
ccc		0.10			0.004	
ddd		0.08			0.003	

NOTE

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm. AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. COPLANARITY ddd APPLIERS TO THE TERMINALS AND ALL OTHER BOTTOM SURFACE METALLIZATION.

Tape and Reel Dimensions, DFN3x3-12L

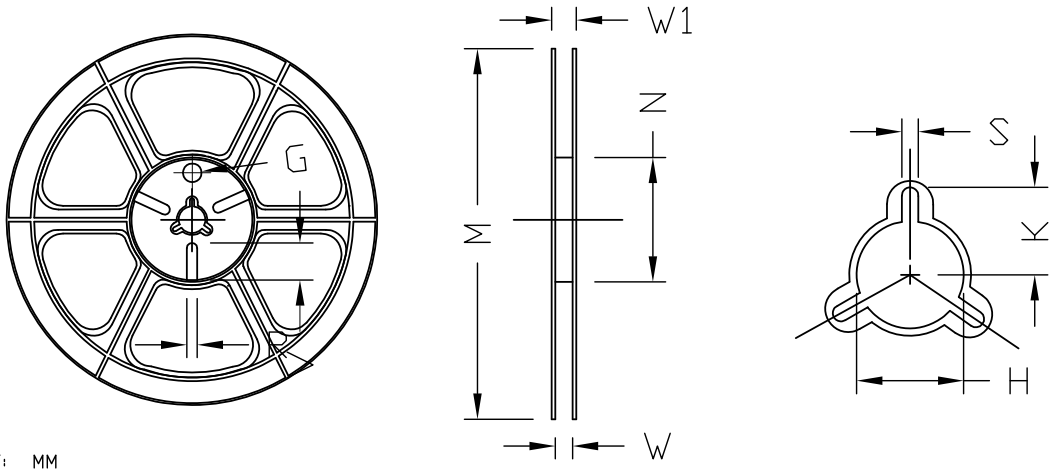
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN3x3_EP	3.40 ±0.10	3.35 ±0.10	1.10 ±0.10	1.50 +0.10 −0	1.50 +0.10 −0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel



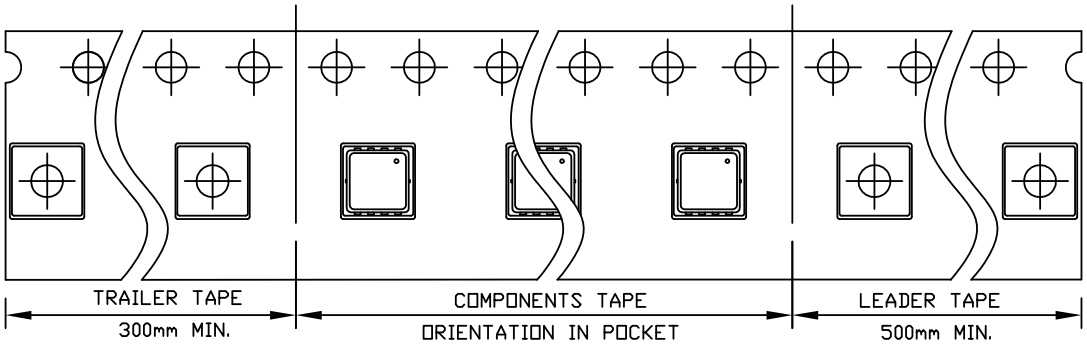
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50 −0.20	10.60	2.00 ±0.50	---	---	---

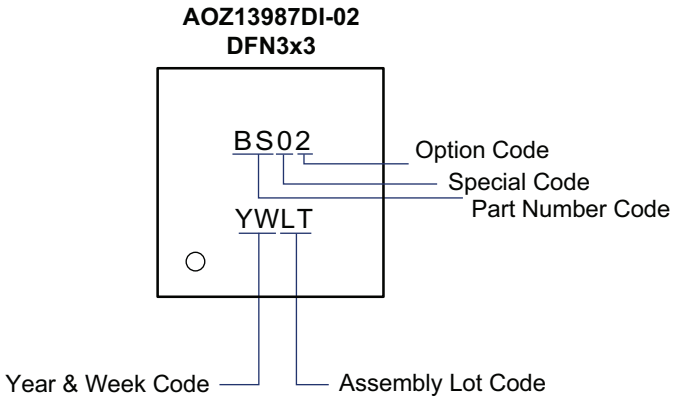
Tape and Reel Dimensions, DFN3x3-12L

DFN3x3 EP TAPE
Leader / Trailer & Orientation

Unit Per Reel:
5000pcs



Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.