ANALOG DEVICES

CMOS 10- & 12-Bit Monolithic Multiplying D/A Converters

AD7530, AD7531

FEATURES
- AD7530: 10-Bit Resolution
- AD7531: 12-Bit Resolution
- 8-, 9- and 10-Bit End Point Linearity
- DTL/TTL/CMOS Compatible
- Nonlinearity Tempco: 2ppm of FSR/°C
- Low Power Dissipation: 20mW
- Current Settling Time: 500ns
- Feedthrough Error: 10mV p-p @ 50kHz
- Low Cost

Note: AD7533 is Recommended for New 10-Bit Designs. AD7541A or AD7545 is Recommended for New 12-Bit Designs.

GENERAL DESCRIPTION

The AD7530 (AD7531) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The device uses advanced CMOS and thin film technologies providing up to 10-bit accuracy with DTL/TTL/CMOS compatibility.

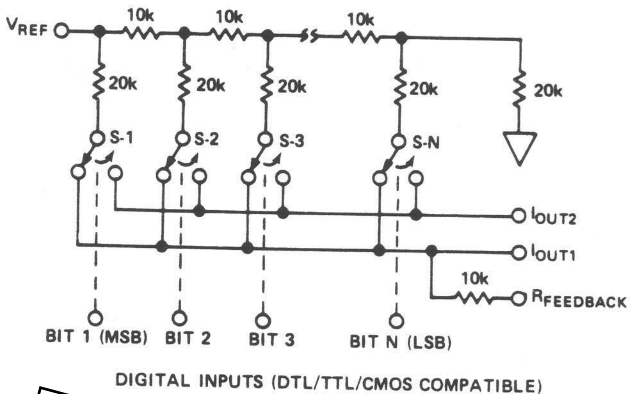
The AD7530 (AD7531) operates from a +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

ORDERING INFORMATION

Nonlinearity	Temperature Range 0 to +70°C	−25°C to +85°C
0.2% (8-Bit)	AD7530JN	AD7530JD
	AD7531JN	AD7531JD
0.1% (9-Bit)	AD7530KN	AD7530KD
	AD7531KN	AD7531KD
0.05% (10-Bit)	AD7530LN	AD7530LD
	AD7531LN	AD7531LD

AD7530, AD7531 FUNCTIONAL BLOCK DIAGRAM



AD7530: N = 10
AD7531: N = 12
(Switches shown in "High" state)

PACKAGE IDENTIFICATION[1]

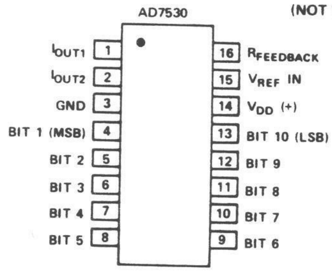
Suffix D: Ceramic DIP
- AD7530: (D16A)
- AD7531: (D18A)

Suffix N: Plastic DIP
- AD7530: (N16B)
- AD7531: (N18B)

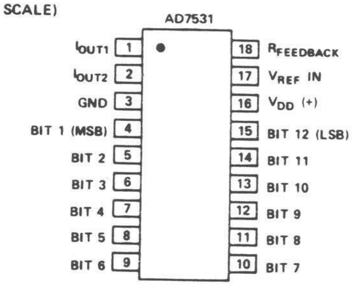
[1] See Section 19 for package outline information.

PIN CONFIGURATION

(NOT TO SCALE)



16-PIN DIP TOP VIEW



18-PIN DIP TOP VIEW

SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER		AD7530	AD7531	TEST CONDITIONS
DC ACCURACY (Note 1)				
Resolution		10 Bits	12 Bits	
Relative Accuracy	AD7530J	0.2% of FSR max (8 Bit)	*	
	AD7530K	0.1% of FSR max (9 Bit)	*	
	AD7530L	0.05% of FSR max (10 Bit)	*	$-10V < V_{REF} < +10V$
Nonlinearity Tempco		2ppm of FSR/°C max	*	
Gain Error		0.3% of FSR typ	*	
Gain Error Tempco		10ppm of FSR/°C max	*	
Output Leakage Current (Either Output)		300nA max	*	Over specified temperature range.
Power Supply Rejection		50ppm of FSR/% typ	*	
AC ACCURACY				
Output Current Settling Time		500ns typ	*	To 0.05% All digital inputs low to high and high to low
Feedthrough Error (Note 2)		10mV p-p max	*	V_{REF} = 20V p-p, 50kHz. All digital inputs low
REFERENCE INPUT				
Input Range		±10V	*	
Input Resistance		±1mA	*	
		10kΩ typ	*	
ANALOG OUTPUT				
Output Current Range (Both Outputs)		±1mA	*	
Output Capacitance	I_{OUT1}	120pF typ	*	All digital inputs high
	I_{OUT2}	37pF typ	*	
	I_{OUT1}	37pF typ	*	All digital input low
	I_{OUT2}	120pF typ	*	
Output Noise (Both Outputs)		Equivalent to 10kΩ Johnson noise typ	*	
DIGITAL INPUTS (Note 3)				
Low State Threshold		0.8V max	*	Over specified temperature range
High State Threshold		2.4V min	*	Over specified temperature range
Input Current (low to high state)		1μA typ	*	
Input Coding		Binary	*	See Tables I & II
POWER REQUIREMENTS				
Power Supply Voltage Range		+5V to +15V	*	
I_{DD}		5nA typ	*	All digital inputs at GND
		2mA max	*	All digital inputs high or low
Total Dissipation		20mW typ	*	

NOTES
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] To minimize feedthrough with the ceramic package, the user must ground the metal lid. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.
[3] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
*Same specifications as for AD7530.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to Gnd) . . . . +17V
V_{REF} (to Gnd). . . . . ±25V
Digital Input Voltage Range . . . . V_{DD} to Gnd
Voltage at Pin 1, Pin 2 . . . . −100mV to V_{DD}
Power Dissipation (package)
up to +75°C. 450mW
Operating Temperature
JN, KN, LN Versions . . . . 0 to +75°C
JD, KD, LD Versions . . . . −25°C to +85°C
Storage Temperature . . . . −65°C to +150°C

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

APPLICATIONS

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 1 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table I. Protection Schottky shown in Figure 1 is not required when using TRIFET output amplifiers such as the AD542 or AD544.

R1 provides full scale trim capability [i.e.—load the DAC register to 11 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}(1 - 2^{-10})$]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at I_{OUT1}).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leqslant 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ).

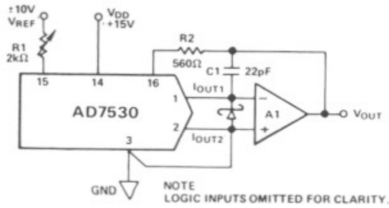


Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table I. Code Table — Unipolar Binary Operation

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 2 and Table II illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) or an ac reference the circuit provides offset binary operation. Protection Schottky shown in Figure 2 is not required when using TRIFET output amplifiers such as the AD542 or AD544.

With the DAC register loaded to 10 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full Scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

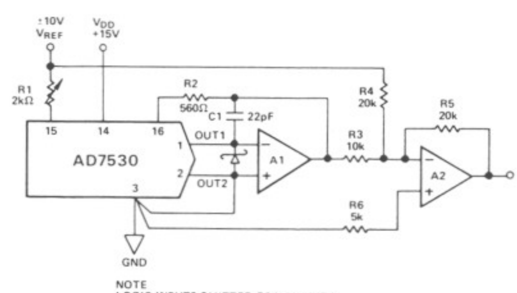


Figure 2. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

Table II Code Table — Bipolar (Offset Binary) Operation

TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})\,(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]\,[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

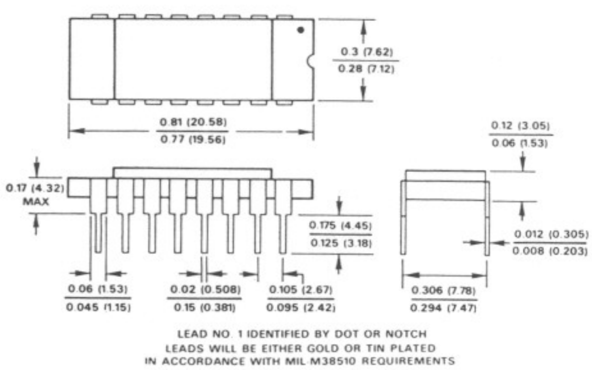
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

OUTLINE DIMENSIONS

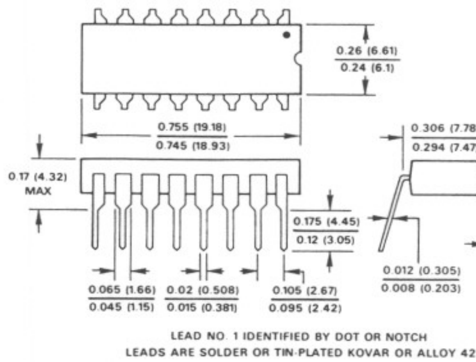
Dimensions shown in inches and (mm).

AD7530

16-PIN CERAMIC DIP

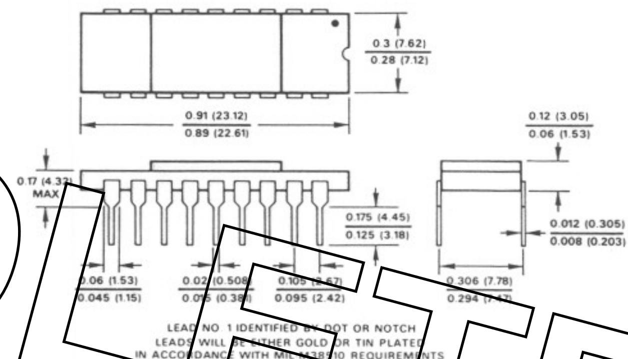


16-PIN PLASTIC DIP

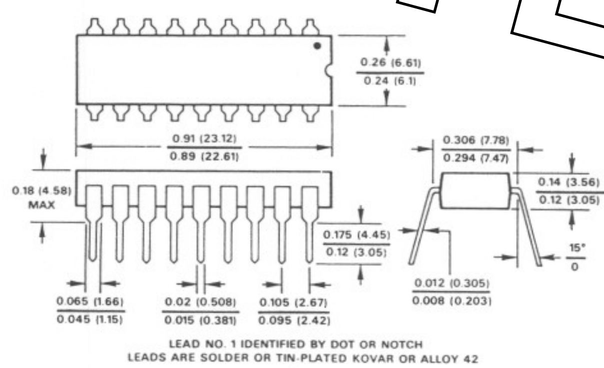


AD7531

18-PIN CERAMIC DIP



18-PIN PLASTIC DIP



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