

EVALUATION KIT  
AVAILABLE

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

MAX4940/MAX4940A

## General Description

The MAX4940/MAX4940A integrated circuits generate high-voltage, high-frequency, unipolar or bipolar pulses from low-voltage logic inputs. These quad/dual pulsers feature independent logic inputs, independent high-voltage pulser outputs with active clamps and independent high-voltage supply inputs.

The MAX4940/MAX4940A feature quad, high-voltage pulsers with  $8.5\Omega$  output impedance for the high-voltage outputs and a  $21\Omega$  impedance for the active clamp. The high-voltage outputs can provide 2.0A (typ) output current.

All devices use two logic inputs per channel to control the positive and negative pulses. The MAX4940/MAX4940A have a dedicated input to control the active clamp. All devices feature an independent enable input EN. All digital inputs are CMOS compatible (see the *Ordering Information/Selector Guide*).

The MAX4940/MAX4940A are available in a 56-pin, 8mm x 8mm, TQFN exposed pad package and are specified over the  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  commercial temperature range.

**Warning:** Exercise caution. The MAX4940/MAX4940A are designed to operate with high voltages.

## Applications

Ultrasound Medical Imaging  
Flaw Detection  
Piezoelectric Drivers  
Test Instruments  
Cleaning Equipment

## Features

- ◆ High-Density Quad-Channel Pulser in One Package
- ◆ 0 to +220V Unipolar or  $\pm 110\text{V}$  Bipolar Outputs
- ◆  $8.5\Omega$  (typ) Output Impedance and 2.0A (typ) Output Current
- ◆  $21\Omega$  (typ) Always-On Active Clamp with Integrated Blocking Diodes
- ◆ Integrated Output Diodes (MAX4940A Only)
- ◆ No Special Power-Supply Sequencing Required for Trilevel Applications
- ◆ Matched Rise/Fall Times and Matched Propagation Delays
- ◆ CMOS-Compatible Logic Inputs
- ◆ 56-Pin, 8mm x 8mm, TQFN Package

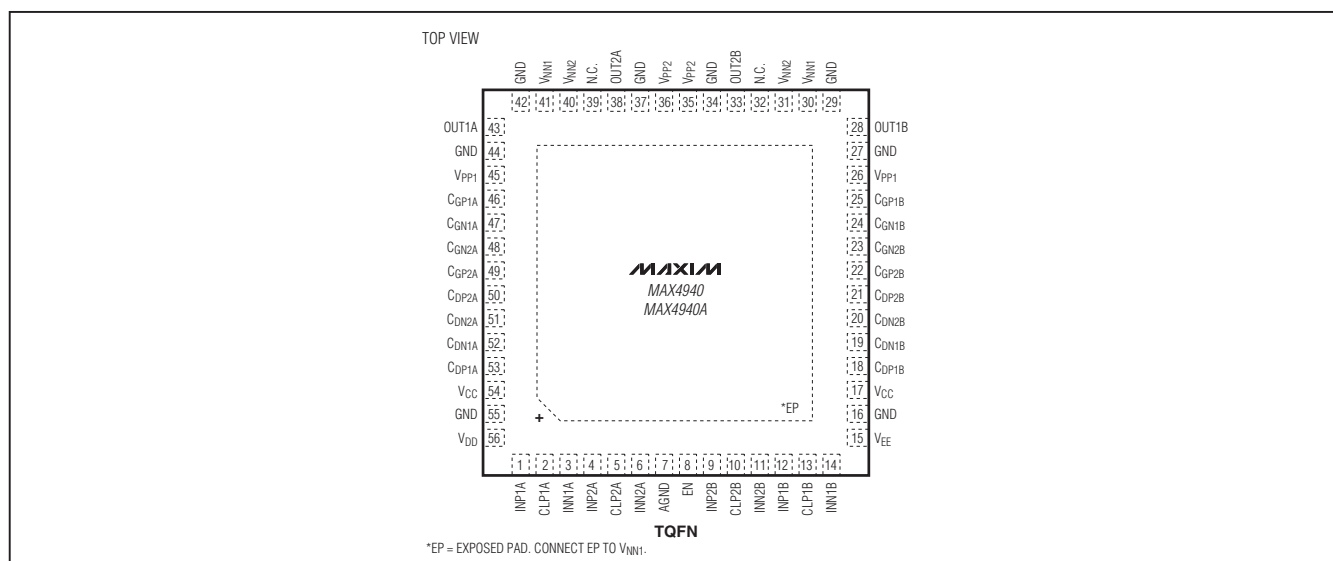
## Ordering Information/ Selector Guide

| PART         | OUTPUT<br>BLOCKING<br>DIODE | OUTPUT<br>CURRENT<br>(A) | PIN-<br>PACKAGE |
|--------------|-----------------------------|--------------------------|-----------------|
| MAX4940CTN+  | None                        | 2.0 (typ)                | 56 TQFN-EP*     |
| MAX4940ACTN+ | OUT2A,<br>OUT2B             | 2.0 (typ)                | 56 TQFN-EP*     |

**Note:** Devices operate over the  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  temperature range.  
+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

## Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

|                                                                                          |                                                         |
|------------------------------------------------------------------------------------------|---------------------------------------------------------|
| V <sub>DD</sub> Logic Supply Voltage                                                     | -0.3V to +6V                                            |
| V <sub>CC</sub> Output Driver Positive Supply Voltage                                    | -0.3V to +15V                                           |
| V <sub>EE</sub> Output Driver Negative Supply Voltage                                    | -15V to +0.3V                                           |
| V <sub>PP</sub> High-Positive Supply Voltage                                             | -0.3V to (V <sub>NN</sub> + 220V)                       |
| V <sub>NN</sub> Low-Negative Supply Voltage                                              | -220V to +0.3V                                          |
| V <sub>PP1</sub> - V <sub>NN1</sub> , V <sub>PP2</sub> - V <sub>NN2</sub> Supply Voltage | -0.6V to +250V                                          |
| INP <sub>-</sub> , INN <sub>-</sub> , CLP <sub>-</sub> , EN Logic Input                  | -0.3V to (V <sub>DD</sub> + 0.3V)                       |
| C <sub>GN</sub> Voltage                                                                  | (-0.3V + V <sub>NN</sub> ) to (+15V + V <sub>NN</sub> ) |
| C <sub>GP</sub> Voltage                                                                  | (+0.3V + V <sub>PP</sub> ) to (-15V + V <sub>PP</sub> ) |

|                                                       |                          |
|-------------------------------------------------------|--------------------------|
| C <sub>DP</sub> , C <sub>DN</sub> Voltage             | -0.3V to V <sub>CC</sub> |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C) |                          |
| 56-Pin TQFN (derate 47.6mW/°C above +70°C)            | 3809mW                   |
| Thermal Resistance (Note 1)                           |                          |
| θ <sub>JA</sub>                                       | 21°C/W                   |
| θ <sub>JC</sub>                                       | 1°C/W                    |
| Operating Temperature Range                           | 0°C to +70°C             |
| Junction Temperature                                  | +150°C                   |
| Storage Temperature Range                             | -65°C to +150°C          |
| Lead Temperature (soldering, 10s)                     | +300°C                   |

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +3V, V<sub>CC</sub> = +12V, V<sub>EE</sub> = -12V, V<sub>PP</sub> = +100V, V<sub>NN</sub> = -100V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

| PARAMETER                                                                                            | SYMBOL           | CONDITIONS                                                                                                                                                                                        | MIN                        | TYP              | MAX                        | UNITS |
|------------------------------------------------------------------------------------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|------------------|----------------------------|-------|
| <b>POWER SUPPLY (V<sub>DD</sub>, V<sub>CC</sub>, V<sub>EE</sub>, V<sub>PP</sub>, V<sub>NN</sub>)</b> |                  |                                                                                                                                                                                                   |                            |                  |                            |       |
| Logic Supply Voltage                                                                                 | V <sub>DD</sub>  |                                                                                                                                                                                                   | 2.37                       | 3                | 6                          | V     |
| Positive Drive Supply Voltage                                                                        | V <sub>CC</sub>  |                                                                                                                                                                                                   | 4.75                       | 12               | 12.6                       | V     |
| Negative Drive Supply Voltage                                                                        | V <sub>EE</sub>  |                                                                                                                                                                                                   | 1.05 x (-V <sub>CC</sub> ) | -V <sub>CC</sub> | 0.95 x (-V <sub>CC</sub> ) | V     |
| High-Side Supply Voltage                                                                             | V <sub>PP1</sub> |                                                                                                                                                                                                   | 0                          |                  | +200                       | V     |
| Low-Side Supply Voltage                                                                              | V <sub>NN1</sub> |                                                                                                                                                                                                   | -200                       |                  | 0                          | V     |
| High-Side Supply Voltage                                                                             | V <sub>PP2</sub> |                                                                                                                                                                                                   | 0                          |                  | V <sub>PP1</sub>           | V     |
| Low-Side Supply Voltage                                                                              | V <sub>NN2</sub> |                                                                                                                                                                                                   | V <sub>NN1</sub>           |                  | 0                          | V     |
| V <sub>PP</sub> - V <sub>NN</sub> Supply Voltage                                                     |                  |                                                                                                                                                                                                   | 0                          |                  | +200                       | V     |
| <b>SUPPLY CURRENT (for single channel)</b>                                                           |                  |                                                                                                                                                                                                   |                            |                  |                            |       |
| V <sub>DD</sub> Supply Current                                                                       | I <sub>DD</sub>  | V <sub>NN</sub> /V <sub>INP</sub> /V <sub>CLP</sub> = 0 or V <sub>DD</sub> , V <sub>EN</sub> = 0                                                                                                  |                            |                  | 1                          | μA    |
|                                                                                                      |                  | V <sub>EN</sub> = V <sub>DD</sub> , V <sub>CLP</sub> = 0 or V <sub>DD</sub> , V <sub>NN</sub> = V <sub>INP</sub> , f = 5MHz, one channel switching                                                |                            | 100              | 200                        | μA    |
| V <sub>CC</sub> Supply Current                                                                       | I <sub>CC</sub>  | V <sub>EN</sub> = 0 (static)                                                                                                                                                                      |                            |                  | 1                          | μA    |
|                                                                                                      |                  | V <sub>EN</sub> = V <sub>DD</sub> (static)                                                                                                                                                        |                            |                  | 10                         | μA    |
|                                                                                                      |                  | V <sub>EN</sub> = V <sub>DD</sub> , V <sub>CLP</sub> = 0 or V <sub>DD</sub> , V <sub>NN</sub> = V <sub>INP</sub> , f = 5MHz, V <sub>CC</sub> = +12V, V <sub>DD</sub> = +3V, one channel switching |                            | 36               |                            | mA    |
|                                                                                                      |                  | V <sub>EN</sub> = V <sub>DD</sub> , V <sub>CLP</sub> = 0 or V <sub>DD</sub> , V <sub>NN</sub> = V <sub>INP</sub> , f = 5MHz, V <sub>CC</sub> = +5V, V <sub>DD</sub> = +3V, one channel switching  |                            | 15               |                            |       |

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

MAX4940/MAX4940A

## ELECTRICAL CHARACTERISTICS (continued)

(VDD = +3V, VCC = +12V, VEE = -12V, VPP\_ = +100V, VNN\_ = -100V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

| PARAMETER                              | SYMBOL | CONDITIONS                                                                                                                 |                | MIN                   | TYP | MAX | UNITS |
|----------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------|----------------|-----------------------|-----|-----|-------|
| VEE_ Supply Current                    | IEE_   | VEN = 0 or VDD (static)                                                                                                    |                | 1                     |     |     | μA    |
|                                        |        | VEE = -5V, VEN = VDD, VCLP_ = VDD, PRF = 10kHz, f = 5MHz, four pulses, no load, one channel switching                      |                | 100                   |     |     |       |
|                                        |        | VEE = -12V, VEN = VDD, VCLP_ = VDD, PRF = 10kHz, f = 5MHz, four pulses, no load, one channel switching                     |                | 200                   |     |     |       |
| VPP_ Supply Current                    | IPP_   | VEN = 0 or VDD (static)                                                                                                    |                | 1                     |     |     | μA    |
|                                        |        | VEN = VDD, VCLP_ = 0 or VDD, VINN_ = VINP_ , f = 5MHz, VPP_ = +5V, VNN_ = -5V, no load, one channel switching              |                | 9                     |     |     | mA    |
|                                        |        | VEN = VDD, VCLP_ = 0 or VDD, VPP_ = +80V, VNN_ = -80V, PRF = 10kHz, f = 10MHz, four pulses, no load, one channel switching |                | 0.6                   |     |     |       |
| VNN_ Supply Current                    | INN_   | VEN = 0 or VDD (static)                                                                                                    |                | 1                     |     |     | μA    |
|                                        |        | VEN = VDD, VCLP_ = 0 or VDD, VINN_ = VINP_ , f = 5MHz, VPP_ = +5V, VNN_ = -5V, no load, one channel switching              |                | 9                     |     |     | mA    |
|                                        |        | VEN = VDD, VINC_ = 0 or VDD, VPP_ = +80V, VNN_ = -80V, PRF = 10kHz, f = 10MHz, four pulses, no load, one channel switching |                | 0.6                   |     |     |       |
| LOGIC INPUTS (EN, INN_ , INP_ , CLP_ ) |        |                                                                                                                            |                |                       |     |     |       |
| Low-Level Input Voltage                | VIL    |                                                                                                                            |                | 0.25 x VDD            |     |     | V     |
| High-Level Input Voltage               | VIH    |                                                                                                                            |                | 0.75 x VDD            |     |     | V     |
| Logic-Input Capacitance                | CIN    |                                                                                                                            |                | 5                     |     |     | pF    |
| Logic-Input Leakage                    | IIN    | VIN = 0 or VDD                                                                                                             |                | 0 ±1                  |     |     | μA    |
| OUTPUT (OUT_ )                         |        |                                                                                                                            |                |                       |     |     |       |
| OUT_ Output-Voltage Range              | VOUT_  | No load at OUT_                                                                                                            |                | VNN_ VPP_             |     | V   |       |
|                                        |        | 100mA load (MAX4940), VCC = +12V ±5%                                                                                       |                | VNN_ + 1.5 VPP_ - 1.5 |     | V   |       |
|                                        |        | 100mA load (MAX4940A), VCC = +12V ±5%                                                                                      |                | VNN_ + 2.5 VPP_ - 2.5 |     | V   |       |
| Low-Side Output Impedance (MAX4940)    | ROLS   | IOUT_ = -50mA                                                                                                              | VCC = +12V ±5% | 7.5 14                |     | Ω   |       |
|                                        |        |                                                                                                                            | VCC = +5V ±5%  | 8 18                  |     |     |       |
| High-Side Output Impedance (MAX4940)   | ROHS   | IOUT_ = -50mA                                                                                                              | VCC = +12V ±5% | 9 14                  |     | Ω   |       |
|                                        |        |                                                                                                                            | VCC = +5V ±5%  | 10.5 18               |     |     |       |

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## ELECTRICAL CHARACTERISTICS (continued)

(VDD = +3V, VCC = +12V, VEE = -12V, VPP\_ = +100V, VNN\_ = -100V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

| PARAMETER                                                                      | SYMBOL  | CONDITIONS                                                            | MIN                             | TYP          | MAX      | UNITS |
|--------------------------------------------------------------------------------|---------|-----------------------------------------------------------------------|---------------------------------|--------------|----------|-------|
| Low-Side Output Impedance (MAX4940A)                                           | ROLS    | IOUT_ = -50mA                                                         | VCC = +12V ±5%<br>VCC = +5V ±5% | 8.5<br>10.0  | 17<br>21 | Ω     |
| High-Side Output Impedance (MAX4940A)                                          | ROHS    | IOUT_ = -50mA                                                         | VCC = +12V ±5%<br>VCC = +5V ±5% | 11.5<br>13.0 | 17<br>21 | Ω     |
| Low-Side Signal CLAMP Output Impedance                                         | ROLSC   | IOUT_ = -50mA                                                         | VCC = +12V ±5%<br>VCC = +5V ±5% | 18.7<br>20   | 45<br>60 | Ω     |
| High-Side Signal CLAMP Output Impedance                                        | ROHSC   | IOUT_ = -50mA                                                         | VCC = +12V ±5%<br>VCC = +5V ±5% | 26.5<br>37.0 | 45<br>60 | Ω     |
| <b>PEAK CURRENT</b>                                                            |         |                                                                       |                                 |              |          |       |
| Low-Side Output Current                                                        | IOL     | VCC = +12V ±5%, VOUT_ - VNN_ = 100V                                   | 1.3                             | 2.0          |          | A     |
| High-Side Output Current                                                       | IOH     | VCC = +12V ±5%, VOUT_ - VPP_ = 100V                                   | 1.3                             | 2.0          |          | A     |
| Low-Side Output Current Clamp                                                  | IOLC    | VCC = +12V ±5%, VOUT_ = +40V                                          | 0.47                            | 0.9          |          | A     |
| High-Side Output Current Clamp                                                 | IOHC    | VCC = +12V ±5%, VOUT_ = +40V                                          | 0.47                            | 0.9          |          | A     |
| Off-Output Capacitance                                                         | CO(OFF) | MAX4940, MAX4940A (OUT1_)                                             |                                 | 75           |          | pF    |
|                                                                                |         | MAX4940A (OUT2_)                                                      |                                 | 45           |          | pF    |
| Off-Output Leakage Current                                                     | ILK     | VNN_ = -100V, VPP_ = +100V, VEN = 0, VOUT_ = -100V to +100V           |                                 |              | ±1       | μA    |
| <b>GATE-SOURCE RESISTANCE</b>                                                  |         |                                                                       |                                 |              |          |       |
| Gate-Source Resistance                                                         | RGS     | VEN = VDD                                                             | 5                               | 7.5          | 10       | kΩ    |
| <b>DYNAMIC CHARACTERISTICS (RL = 100Ω, CL = 100pF, unless otherwise noted)</b> |         |                                                                       |                                 |              |          |       |
| Logic Input-to-Output Rise Propagation Delay (Figure 1)                        | tPLH    | INN_/INP_ at 50% to OUT_ 10/90%, VCC = +12V, VPP_ = +5V, VNN_ = -5V   |                                 | 15           |          | ns    |
| Logic Input-to-Output Fall Propagation Delay (Figure 1)                        | tPHL    | INN_/INP_ at 50% to OUT_ 10/90%, VCC = +12V, VPP_ = +5V, VNN_ = -5V   |                                 | 15           |          | ns    |
| Logic Input-to-Output Rise Propagation Delay Clamp (Figure 1)                  | tPLO    | INN_/INP_ at 50% to OUT_ 10/90%, VCC = +12V, VPP_ = +5V, VNN_ = -5V   |                                 | 15           |          | ns    |
| Logic Input-to-Output Fall Propagation Delay Clamp (Figure 1)                  | tPHO    | INN_/INP_ at 50% to OUT_ 10/90%, VCC = +12V, VPP_ = +5V, VNN_ = -5V   |                                 | 15           |          | ns    |
| OUT_ Rise Time (GND to VPP_) (Figure 1)                                        | tROP    | VPP_ = +100V, VNN_ = -100V, 10% to 90%, VCC_ = +12V ±5%, VEE_ = -VCC_ |                                 | 9            | 20       | ns    |
| OUT_ Rise Time (VNN_ to VPP_) (Figure 1)                                       | tRNP    | VPP_ = +100V, VNN_ = -100V, 10% to 90%, VCC_ = +12V ±5%, VEE_ = -VCC_ |                                 | 10.5         | 35       | ns    |
| OUT_ Fall Time (GND to VNN_) (Figure 1)                                        | tFON    | VPP_ = +100V, VNN_ = -100V, 10% to 90%, VCC_ = +12V ±5%, VEE_ = -VCC_ |                                 | 9            | 20       | ns    |
| OUT_ Fall Time (VPP_ to VNN_) (Figure 1)                                       | tFPN    | VPP_ = +100V, VNN_ = -100V, 10% to 90%, VCC = +12V ±5%, VEE_ = -VCC_  |                                 | 10.5         | 35       | ns    |
| OUT_ Rise Time (VNN_ to GND) (Figure 1)                                        | tRNO    | VPP_ = +100V, VNN_ = -100V, 10% to 90%, VCC = +12V ±5%, VEE_ = -VCC_  |                                 | 17           | 35       | ns    |

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MAX4940/MAX4940A

## ELECTRICAL CHARACTERISTICS (continued)

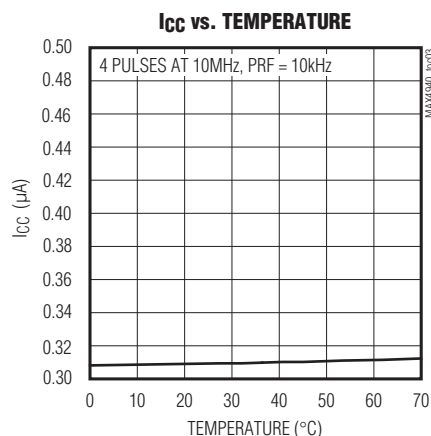
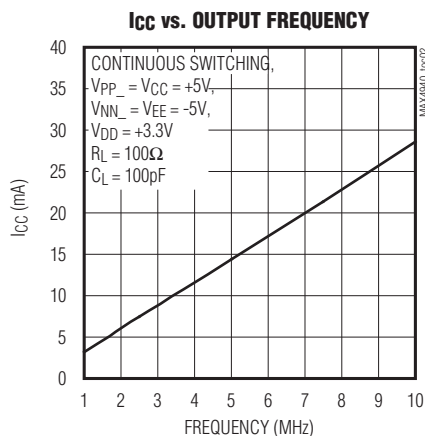
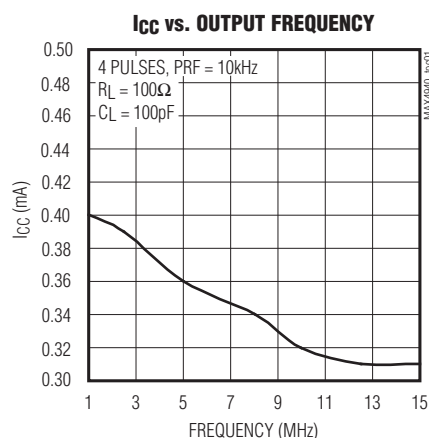
(VDD = +3V, VCC = +12V, VEE = -12V, VPP\_ = +100V, VNN\_ = -100V, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

| PARAMETER                                  | SYMBOL  | CONDITIONS                                                                                 | MIN | TYP | MAX | UNITS |
|--------------------------------------------|---------|--------------------------------------------------------------------------------------------|-----|-----|-----|-------|
| OUT_ Fall Time (VPP_ to GND)<br>(Figure 1) | tFPO    | VPP_ = +100V, VNN_ = -100V, 10% to 90%,<br>VCC = +12V ±5%, VEE_ = -VCC_                    |     | 17  | 35  | ns    |
| Output Enable Time from EN<br>(Figure 2)   | tEN     | VPP_ = +5V, VNN_ = -5V                                                                     |     |     | 100 | ns    |
| Output Disable Time from EN<br>(Figure 2)  | tDI     | VPP_ = +5V, VNN_ = -5V                                                                     |     |     | 150 | ns    |
| 2nd Harmonic Distortion LV                 | THD2_LV | fOUT_ = 5MHz, VPP_ = -VNN_ = +5V,<br>VCC = +12V                                            |     | -40 |     | dB    |
| 2nd Harmonic Distortion HV                 | THD2_HV | fOUT_ = 5MHz, VPP_ = -VNN_ = +50V, VCC<br>= +12V, 10 periods                               |     | -45 |     | dB    |
| Pulse Cancellation                         | 2HD     | fOUT_ = 5MHz, VPP_ = -VNN_ = +50V,<br>VCC = +12V, 10 periods, 1st harmonic<br>cancellation |     | -43 |     | dB    |
| RMS Output Jitter                          | tj      |                                                                                            |     | 10  |     | ps    |
| Crosstalk                                  | CT      | Adjacent channels, f = 5MHz                                                                |     | -60 |     | dB    |

**Note 2:** Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at TA = +70°C. Specifications at TA = 0°C are guaranteed by design.

## Typical Operating Characteristics

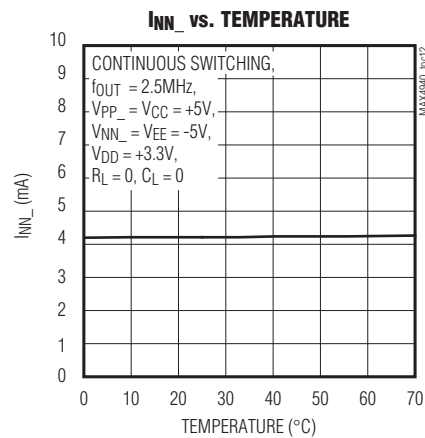
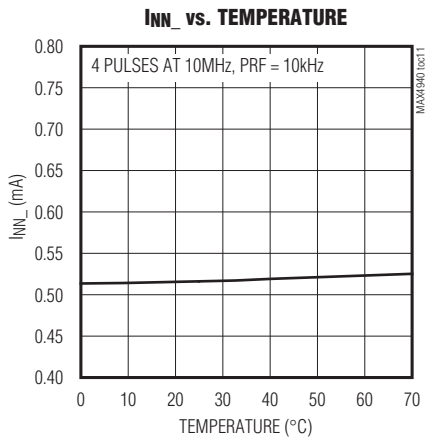
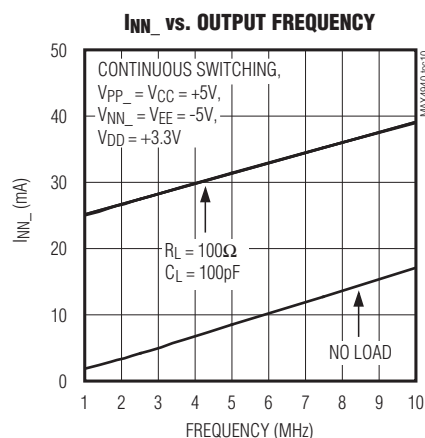
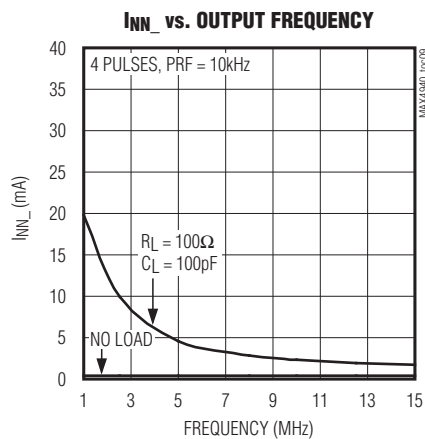
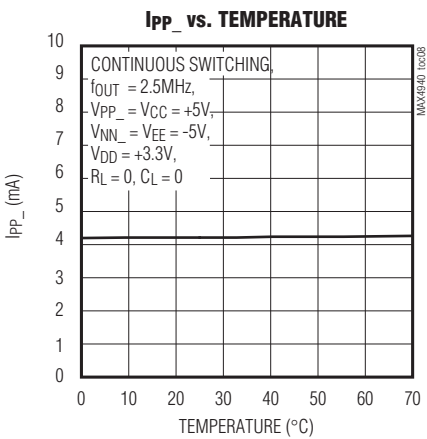
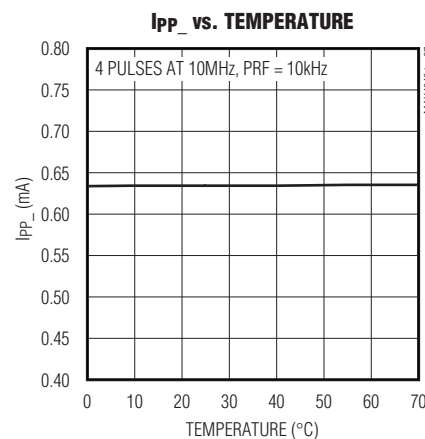
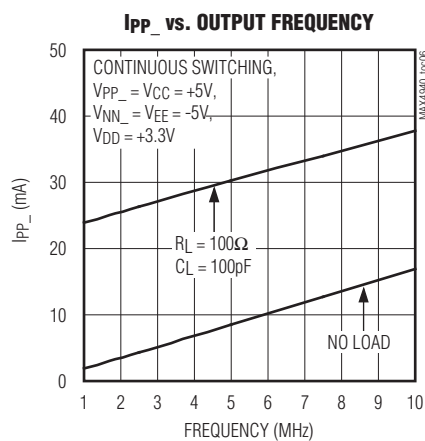
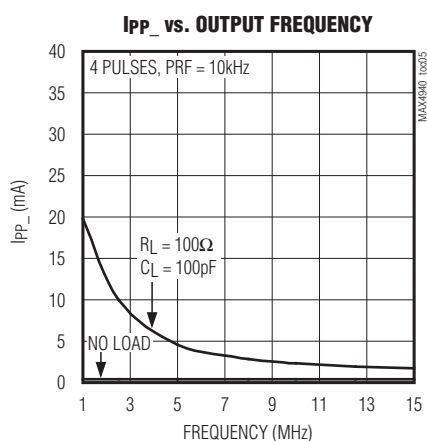
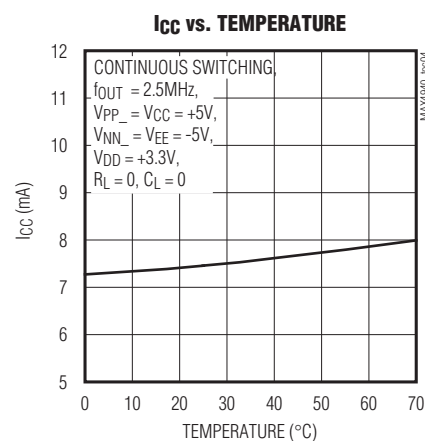
(VDD = +3.3V, VCC = +12V, VEE = -12V, VPP\_ = +100V, VNN\_ = -100V, fOUT = 5MHz, RL = 100Ω, CL = 100pF, TA = +25°C, unless otherwise noted.)



# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Typical Operating Characteristics (continued)

( $V_{DD} = +3.3V$ ,  $V_{CC} = +12V$ ,  $V_{EE} = -12V$ ,  $V_{PP\_} = +100V$ ,  $V_{NN\_} = -100V$ ,  $f_{OUT} = 5MHz$ ,  $R_L = 100\Omega$ ,  $C_L = 100pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

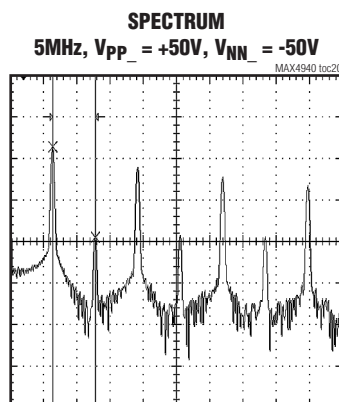
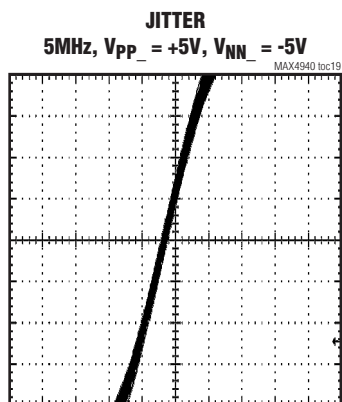
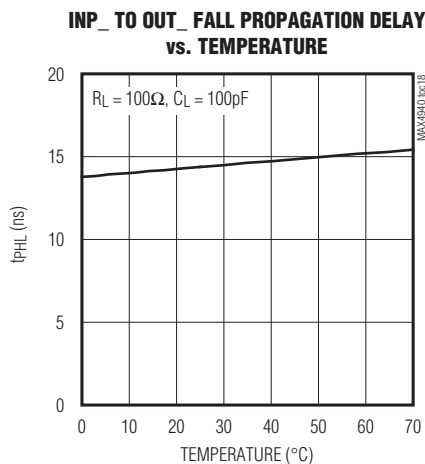
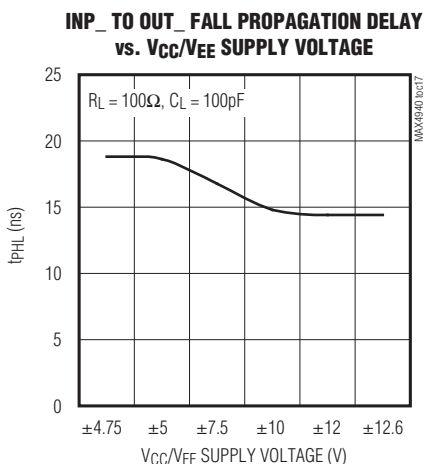
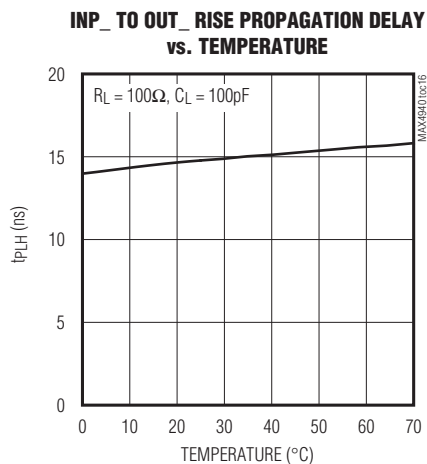
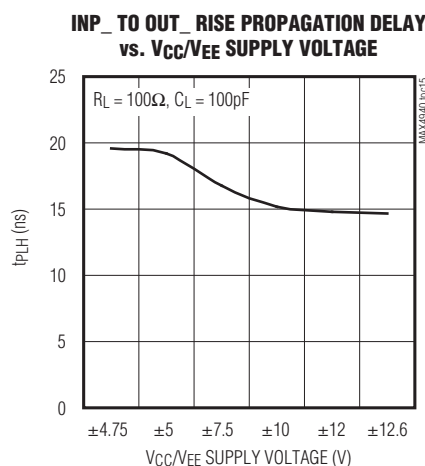
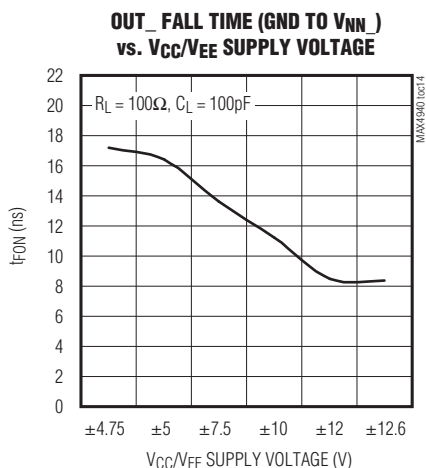
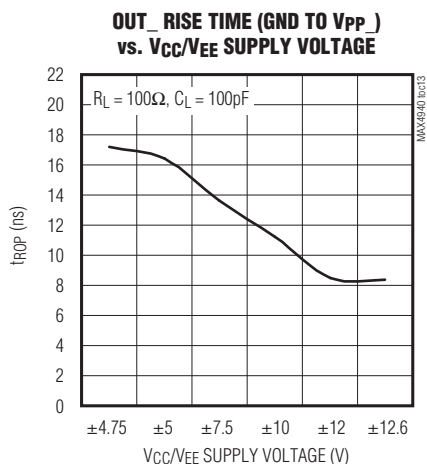


# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Typical Operating Characteristics (continued)

( $V_{DD} = +3.3V$ ,  $V_{CC} = +12V$ ,  $V_{EE} = -12V$ ,  $V_{PP\_} = +100V$ ,  $V_{NN\_} = -100V$ ,  $f_{OUT} = 5MHz$ ,  $R_L = 100\Omega$ ,  $C_L = 100pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX4940/MAX4940A



# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

MAX4940/MAX4940A

## Pin Description

| PIN                                  | NAME  | FUNCTION                                                                                                                                     |
|--------------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                    | INP1A | Channel 1A High-Side Logic Input. See the <i>Truth Tables</i> section.                                                                       |
| 2                                    | CLP1A | Channel 1A Clamp Logic Input. Clamp is turned on when CLP1A is high and when INP1A and INN1A are low. See the <i>Truth Table</i> section.    |
| 3                                    | INN1A | Channel 1A Low-Side Logic Input. See the <i>Truth Tables</i> section.                                                                        |
| 4                                    | INP2A | Channel 2A High-Side Logic Input. See the <i>Truth Tables</i> section.                                                                       |
| 5                                    | CLP2A | Channel 2A Clamp Logic Input. Clamp is turned on when CLP2A is high and when INP2A and INN2A are low. See the <i>Truth Tables</i> section.   |
| 6                                    | INN2A | Channel 2A Low-Side Logic Input. See the <i>Truth Tables</i> section.                                                                        |
| 7                                    | AGND  | Analog Ground. Must be connected to common GND.                                                                                              |
| 8                                    | EN    | Enable Logic Input. Drive EN high to enable OUT1A, OUT1B, OUT2A, and OUT2B.                                                                  |
| 9                                    | INP2B | Channel 2B High-Side Logic Input. See the <i>Truth Tables</i> section.                                                                       |
| 10                                   | CLP2B | Channel 2B Clamp Logic Input. Clamp is turned on when CLP2B is high and when INP2B and INN2B are low. See the <i>Truth Tables</i> section.   |
| 11                                   | INN2B | Channel 2B Low-Side Logic Input. See the <i>Truth Tables</i> section.                                                                        |
| 12                                   | INP1B | Channel 1B High-Side Logic Input. See the <i>Truth Tables</i> section.                                                                       |
| 13                                   | CLP1B | Channel 1B Clamp Logic Input. Clamp is turned on when CLP1B is high and when INP1B and INN1B are low. See the <i>Truth Tables</i> section.   |
| 14                                   | INN1B | Channel 1B Low-Side Logic Input. See the <i>Truth Tables</i> section.                                                                        |
| 15                                   | VEE   | Negative Supply Input. Gate-drive supply voltage for the clamp. Bypass VEE to GND with a 0.1μF capacitor as close as possible to the device. |
| 16, 27, 29,<br>34, 37, 42,<br>44, 55 | GND   | Ground                                                                                                                                       |
| 17, 54                               | VCC   | Gate-Drive Supply Voltage Input. Bypass VCC to GND with a 0.1μF capacitor as close as possible to the device.                                |
| 18                                   | CDP1B | Channel 1B High-Side Driver Output. Connect a 3.3nF capacitor between CDP1B and CGP1B as close as possible to the device.                    |
| 19                                   | CDN1B | Channel 1B Low-Side Driver Output. Connect a 3.3nF capacitor between CDN1B and CGN1B as close as possible to the device.                     |
| 20                                   | CDN2B | Channel 2B Low-Side Driver Output. Connect a 3.3nF capacitor between CDN2B and CGN2B as close as possible to the device.                     |
| 21                                   | CDP2B | Channel 2B High-Side Driver Output. Connect a 3.3nF capacitor between CDP2B and CGP2B as close as possible to the device.                    |
| 22                                   | CGP2B | Channel 2B High-Side Gate Input. Connect a 3.3nF capacitor between CDP2B and CGP2B as close as possible to the device.                       |
| 23                                   | CGN2B | Channel 2B Low-Side Gate Input. Connect a 3.3nF capacitor between CDN2B and CGN2B as close as possible to the device.                        |
| 24                                   | CGN1B | Channel 1B Low-Side Gate Input. Connect a 3.3nF capacitor between CDN1B and CGN1B as close as possible to the device.                        |
| 25                                   | CGP1B | Channel 1B High-Side Gate Input. Connect a 3.3nF capacitor between CDP1B and CGP1B as close as possible to the device.                       |

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Pin Description (continued)

| PIN    | NAME              | FUNCTION                                                                                                                                          |
|--------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 26, 45 | V <sub>PP1</sub>  | Channel 1A, 1B High-Side Positive Supply Voltage Input. Bypass V <sub>PP1</sub> to GND with a 0.1μF capacitor as close as possible to the device. |
| 28     | OUT1B             | Channel 1B Output                                                                                                                                 |
| 30, 41 | V <sub>NN1</sub>  | Channel 1A, 1B Low-Side Negative Supply Voltage Input. Bypass V <sub>NN1</sub> to GND with a 0.1μF capacitor as close as possible to the device.  |
| 31, 40 | V <sub>NN2</sub>  | Channel 2A, 2B Low-Side Negative Supply Voltage Input. Bypass V <sub>NN2</sub> to GND with a 0.1μF capacitor as close as possible to the device.  |
| 32, 39 | N.C.              | No Connection. Not connected internally.                                                                                                          |
| 33     | OUT2B             | Channel 2B Output                                                                                                                                 |
| 35, 36 | V <sub>PP2</sub>  | Channel 2A, 2B High-Side Positive Supply Voltage Input. Bypass V <sub>PP2</sub> to GND with a 0.1μF capacitor as close as possible to the device. |
| 38     | OUT2A             | Channel 2A Output                                                                                                                                 |
| 43     | OUT1A             | Channel 1A Output                                                                                                                                 |
| 46     | C <sub>GP1A</sub> | Channel 1A High-Side Gate Input. Connect a 3.3nF capacitor between C <sub>DP1A</sub> and C <sub>GP1A</sub> as close as possible to the device.    |
| 47     | C <sub>GN1A</sub> | Channel 1A Low-Side Gate Input. Connect a 3.3nF capacitor between C <sub>DN1A</sub> and C <sub>GN1A</sub> as close as possible to the device.     |
| 48     | C <sub>GN2A</sub> | Channel 2A Low-Side Gate Input. Connect a 3.3nF capacitor between C <sub>DN2A</sub> and C <sub>GN2A</sub> as close as possible to the device.     |
| 49     | C <sub>GP2A</sub> | Channel 2A High-Side Gate Input. Connect a 3.3nF capacitor between C <sub>DP2A</sub> and C <sub>GP2A</sub> as close as possible to the device.    |
| 50     | C <sub>DP2A</sub> | Channel 2A High-Side Driver Output. Connect a 3.3nF capacitor between C <sub>DP2A</sub> and C <sub>GP2A</sub> as close as possible to the device. |
| 51     | C <sub>DN2A</sub> | Channel 2A Low-Side Driver Output. Connect a 3.3nF capacitor between C <sub>DN2A</sub> and C <sub>GN2A</sub> as close as possible to the device.  |
| 52     | C <sub>DN1A</sub> | Channel 1A Low-Side Driver Output. Connect a 3.3nF capacitor between C <sub>DN1A</sub> and C <sub>GN1A</sub> as close as possible to the device.  |
| 53     | C <sub>DP1A</sub> | Channel 1A High-Side Driver Output. Connect a 3.3nF capacitor between C <sub>DP1A</sub> and C <sub>GP1A</sub> as close as possible to the device. |
| 56     | V <sub>DD</sub>   | Logic-Supply Voltage Input. Bypass V <sub>DD</sub> to GND with a 0.1μF capacitor as close as possible to the device.                              |
| —      | EP                | Exposed Pad. EP must be connected to V <sub>NN1</sub> .                                                                                           |

MAX4940/MAX4940A

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Detailed Description

The MAX4940/MAX4940A are quad high-voltage, high-speed pulsers that can be independently configured for either unipolar/bipolar/multilevel pulse outputs (see Figures 5 and 6.). These devices have independent logic inputs for full pulse control and independent active clamps. The clamp input, CLP\_, can be set high to activate the clamp automatically when the device is not pulsing to the positive or negative high-voltage supplies.

## Logic Inputs (INP\_, INN\_, CLP\_, EN)

INP\_ controls the on and off states of the high-side FET, INN\_ controls the on and off states of the low-side FET, and CLP\_ controls the active clamp. A global enable input (EN) can be used to enable/disable all channels. These signals give complete control of the output stage of each driver (see the *Truth Tables* section for all logic combinations). The MAX4940/MAX4940A logic inputs are **CMOS logic compatible and the logic levels are referenced to V<sub>DD</sub>** for maximum flexibility. The low 5pF (typ) input capacitance of the logic inputs reduce loading and increase switching speed.

## Truth Tables

### MAX4940

| INPUTS |      |      |      | OUTPUTS          | STATE                           |
|--------|------|------|------|------------------|---------------------------------|
| EN     | INP_ | INN_ | CLP_ | OUT_             |                                 |
| 0      | X    | X    | X    | High impedance   | Powered up, INP_/INN_ disabled. |
| 1      | 0    | 0    | 0    | High impedance   | Powered up, all inputs enabled. |
| 1      | 0    | 0    | 1    | GND              | Powered up, all inputs enabled. |
| 1      | 0    | 1    | X    | V <sub>NN_</sub> | Powered up, all inputs enabled. |
| 1      | 1    | 0    | X    | V <sub>PP_</sub> | Powered up, all inputs enabled. |
| 1      | 1    | 1    | X    | Not allowed      | Not allowed.                    |

### MAX4940A

| INPUTS |                |                |                | OUTPUTS          | STATE                           |
|--------|----------------|----------------|----------------|------------------|---------------------------------|
| EN     | INP1A<br>INP1B | INN1A<br>INN1B | CLP1A<br>CLP1B | OUT1A<br>OUT1B   |                                 |
| 0      | X              | X              | X              | High impedance   | Powered up, INP_/INN_ disabled. |
| 1      | 0              | 0              | 0              | High impedance   | Powered up, all inputs enabled. |
| 1      | 0              | 0              | 1              | GND              | Powered up, all inputs enabled. |
| 1      | 0              | 1              | 0              | V <sub>NN_</sub> | Powered up, all inputs enabled. |
| 1      | 1              | 0              | 0              | V <sub>PP_</sub> | Powered up, all inputs enabled. |
| 1      | 1              | 1              | 1              | Not allowed      | Not allowed.                    |

| INPUTS |                |                |                | OUTPUTS          | STATE                           |
|--------|----------------|----------------|----------------|------------------|---------------------------------|
| EN     | INP2A<br>INP2B | INN2A<br>INN2B | CLP2A<br>CLP2B | OUT2A<br>OUT2B   |                                 |
| 0      | X              | X              | X              | High impedance   | Powered up, INP_/INN_ disabled. |
| 1      | 0              | 0              | 0              | High impedance   | Powered up, all inputs enabled. |
| 1      | 0              | 0              | 1              | GND              | Powered up, all inputs enabled. |
| 1      | 0              | 1              | X              | V <sub>NN_</sub> | Powered up, all inputs enabled. |
| 1      | 1              | 0              | X              | V <sub>PP_</sub> | Powered up, all inputs enabled. |
| 1      | 1              | 1              | X              | Not allowed      | Not allowed.                    |

X = Don't care.

0 = Logic-low.

1 = Logic-high.

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Active Clamps

The MAX4940/MAX4940A feature an integrated active clamp circuit to improve pulse quality and reduce 2nd harmonic distortion. The clamp circuit consists of an n-channel (DC-coupled) and a p-channel (DC-coupled) high-voltage FETs that are switched on or off by the logic clamp input (CLP\_).

The MAX4940/MAX4940A feature protected clamp devices, allowing the clamp circuit to be used in bipolar pulsing circuits (see Figures 3 and 4). A diode in series with the OUT\_ output prevents the body diode of the low-side FET from turning on when a voltage lower than GND is present. Another diode in series with the OUT\_ output prevents the body diode of the high-side FET from turning on when a voltage higher than ground is present. The MAX4940/MAX4940A have an active clamp on all outputs.

For the MAX4940 only, the user can connect the active clamp input (CLP\_) to a logic-high voltage and drive only the INP\_ and INN\_ inputs to minimize the number of signals used to drive the device. In this case, whenever both the INP\_ and INN\_ inputs are low and the CLP\_ input is high, the active clamp circuit pulls the output to GND (see the *Truth Tables* section for more information).

## Integrated Blocking Diodes (MAX4940A Only)

The high-voltage OUT2A/OUT2B outputs of the MAX4940A feature integrated blocking diodes that allow the user to implement multilevel pulsing by connecting the outputs of multiple pulser channels in parallel. Internal diodes in series with the OUT2A and OUT2B outputs prevent the body diode of the high-side and low-side FETs from switching on when a voltage greater than VNN2 or VPP2 is present on the output (see Figure 4).

## Thermal Protection

A thermal shutdown circuit with a typical threshold of +155°C prevents damage due to excessive power dissipation. When the junction temperature exceeds  $T_J = +155^\circ\text{C}$ , all outputs are disabled. Normal operation typically resumes after the IC's junction temperature drops below +130°C.

## Applications Information

### AC-Coupling Capacitor Selection

The value of all AC-coupling capacitors (between CDP\_ and CGP\_, and between CDN\_ and CGN\_) should be between 1nF to 10nF. The voltage rating of the capacitor should be greater than VPP\_ and VNN\_. The capacitors should be placed as close as possible to the device.

## Power Dissipation

The power dissipation of the MAX4940/MAX4940A consists of three major components caused by the current consumption from VCC, VPP\_, and VNN\_. The sum of these components (PVCC, PVPP\_, and PVNN\_) must be kept below the maximum power-dissipation limit. See the *Typical Operating Characteristics* section for more information on typical supply currents versus switching frequencies.

The device consumes most of the supply current from VCC supply to charge and discharge internal nodes such as the gate capacitance of the high-side FET ( $C_P$ ) and the low-side FET ( $C_N$ ). Neglecting the small quiescent supply current and a small amount of current used to charge and discharge the capacitances at the internal gate clamp FETs, the power consumption can be estimated as follows:

$$P_{VCC} = \left[ (C_N \times V_{CC}^2 \times f_{IN}) + (C_P \times V_{CC}^2 \times f_{INP}) \right] \times (BRF \times BTD)$$

$$f_{IN} = f_{INN\_} + f_{INP\_}$$

where  $f_{INN\_}$  and  $f_{INP\_}$  are the switching frequency of the inputs INN\_, INP\_, respectively, and where BRF is the burst response frequency, and BTD is the burst time duration. The typical values of the gate capacitances are  $C_N = 1.2\mu\text{F}$ ,  $C_P = 0.4\mu\text{F}$ .

See the *Typical Operating Characteristics* for VPP\_ and VNN\_ power consumption.

## Power Supplies and Bypassing

The MAX4940/MAX4940A operate from independent supply voltage sets (only VDD, VCC, and VEE are common to all channels). VPP1/VNN1 supply two channels and VPP2/VNN2 supply the other two channels. The logic input circuit operates from a +2.37V to +6V single supply (VDD). The level-shift driver dual supplies, VCC/VEE operate from  $\pm 4.75\text{V}$  to  $\pm 12.6\text{V}$ .

The VPP\_/VNN\_ high-side and low-side supplies are driven from a single positive supply up to +220V, from a single negative supply up to -220V, or from  $\pm 110\text{V}$  dual supplies. Either VPP\_ or VNN\_ can be set at 0. Bypass each supply input to ground with a 0.1 $\mu\text{F}$  capacitor as close as possible to the device.

Depending on the applications, additional bypassing may be needed to maintain the input of both VNN\_ and VPP\_ stable during output transitions. For example, with  $C_{OUT} = 100\text{pF}$  and  $R_{OUT} = 100\Omega$  load, the use of an additional 10 $\mu\text{F}$  (typ) electrolytic capacitor is recommended.

## ***Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers***

### Exposed Pad and Layout Concerns

The MAX940/MAX940A provide an exposed pad (EP) underneath the TQFN package for improved thermal performance. EP is internally connected to V<sub>NN1</sub>. Connect EP to V<sub>NN1</sub> externally. To aid heat dissipation, connect EP to a similarly sized pad on the component side of the PCB. This pad should be connected through the solder-side copper by several plated holes to a large heat spreading copper area to conduct heat away from the device.

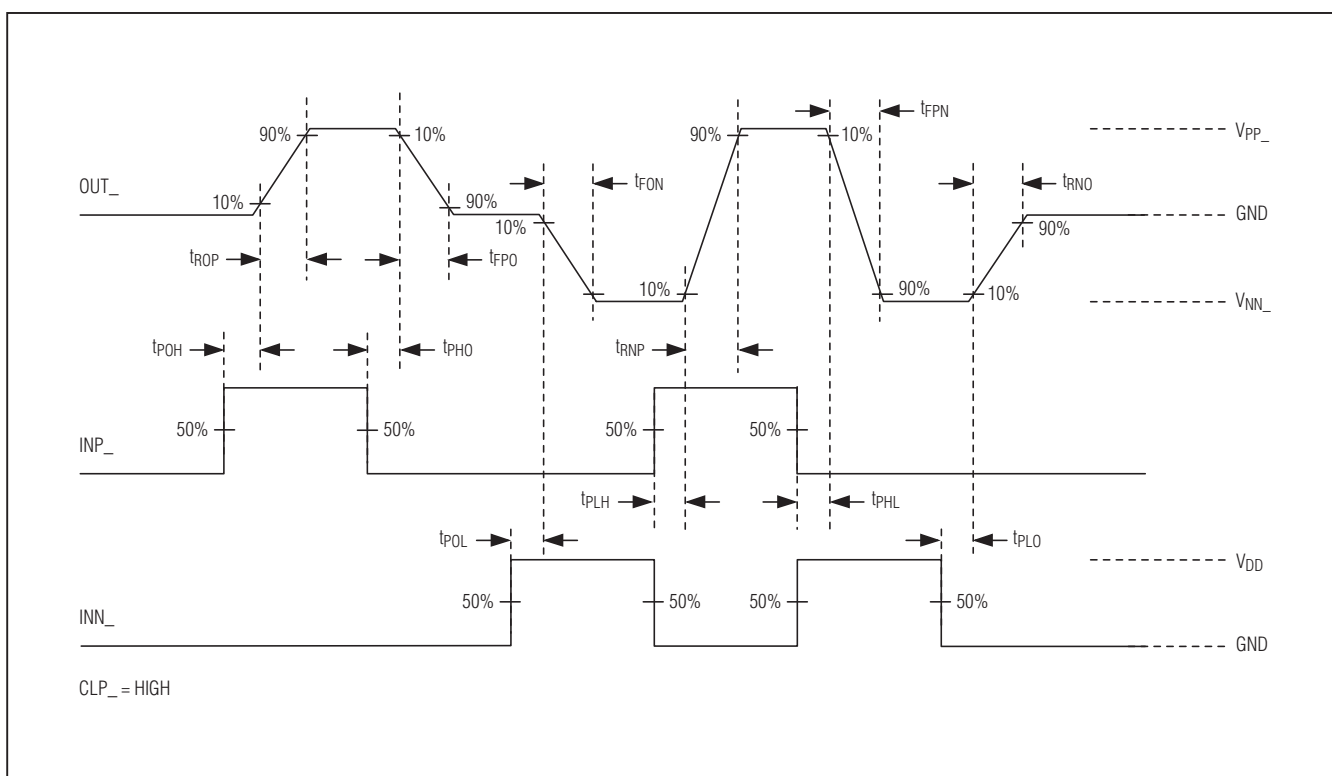
The MAX4940/MAX4940A high-speed pulsers require low-inductance bypass capacitors to their supply inputs. High-speed PCB trace design practices are recommended. Pay

particular attention to **minimize trace lengths and use sufficient trace width** to reduce inductance. Use of surface-mount components is recommended.

## Supply Sequencing

In a typical trilevel application when VNN1 and VNN2 are externally shorted ( $V_{NN1} = V_{NN2}$ ), the MAX4940/MAX4940A do not require any power sequencing. In general, and in particular for the multilevel application, VNN1 must be less than or equal to VNN2 ( $V_{NN1} \leq V_{NN2}$ ) at all times. No other power-supply sequencing is required for the MAX4940/MAX4940A.

## Timing Diagrams

Figure 1. Detail Timing ( $R_L = 100\Omega$ ,  $C_L = 100\text{pF}$ )

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Timing Diagrams (continued)

MAX4940/MAX4940A

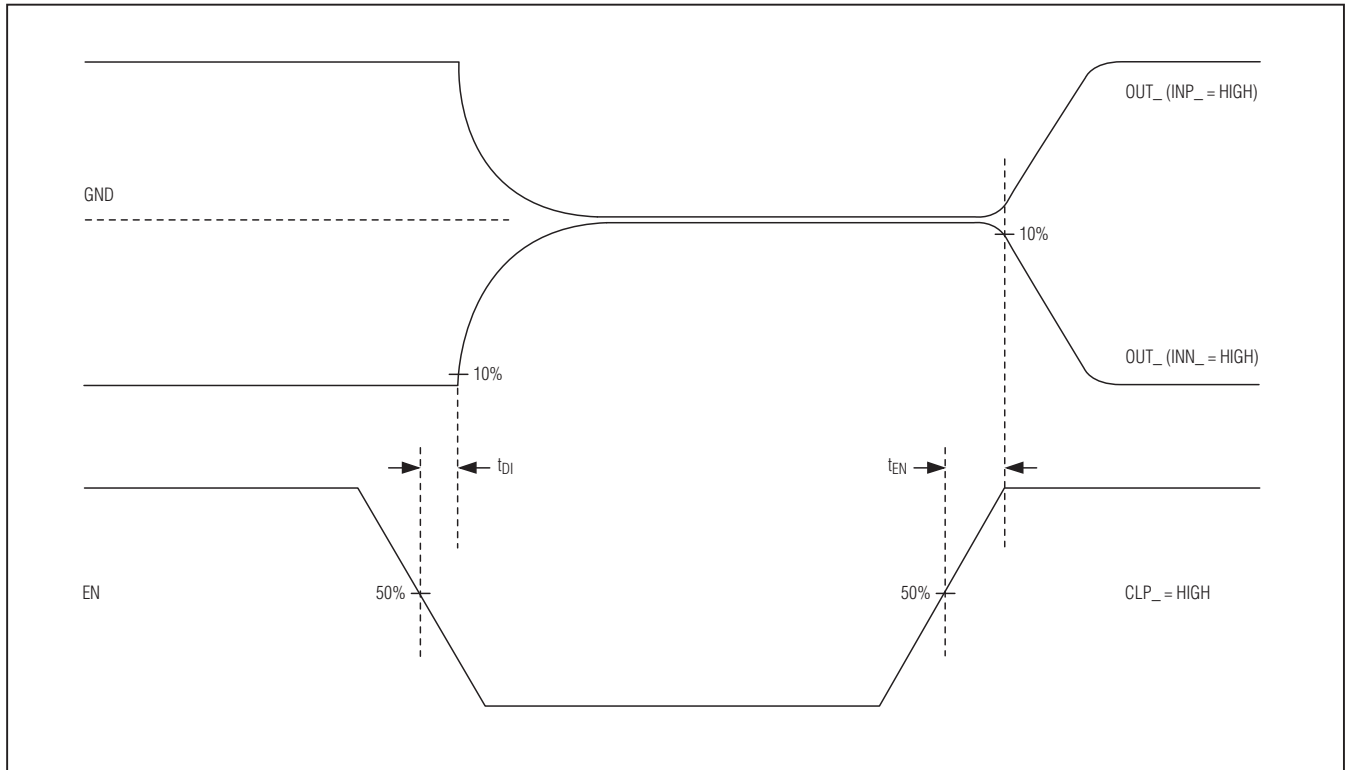


Figure 2. Enable Timing ( $R_L = 100\Omega$ ,  $C_L = 100pF$ )

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Functional Diagrams

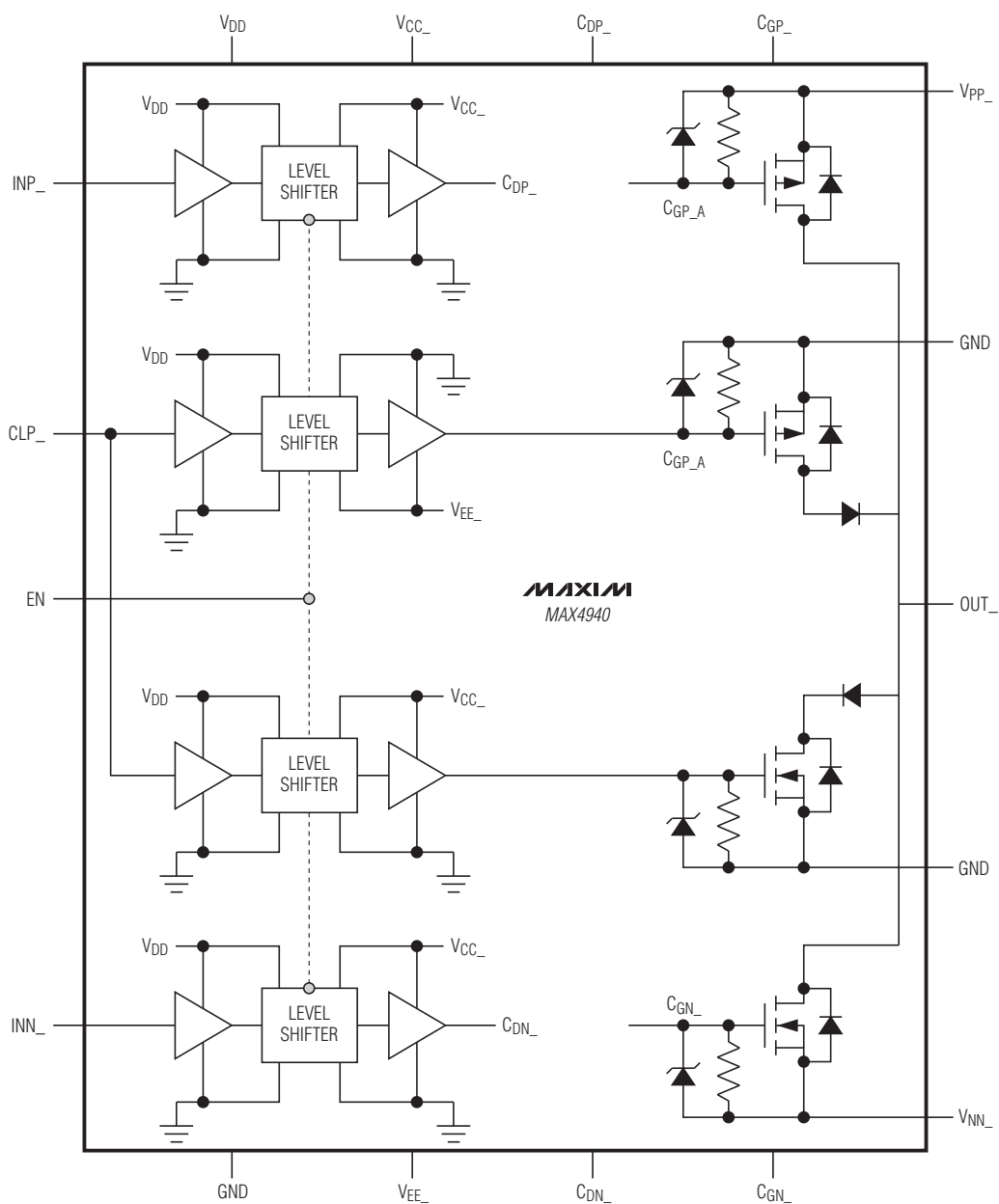


Figure 3. MAX4940 Simplified Functional Diagram for One Channel

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Functional Diagrams (continued)

MAX4940/MAX4940A

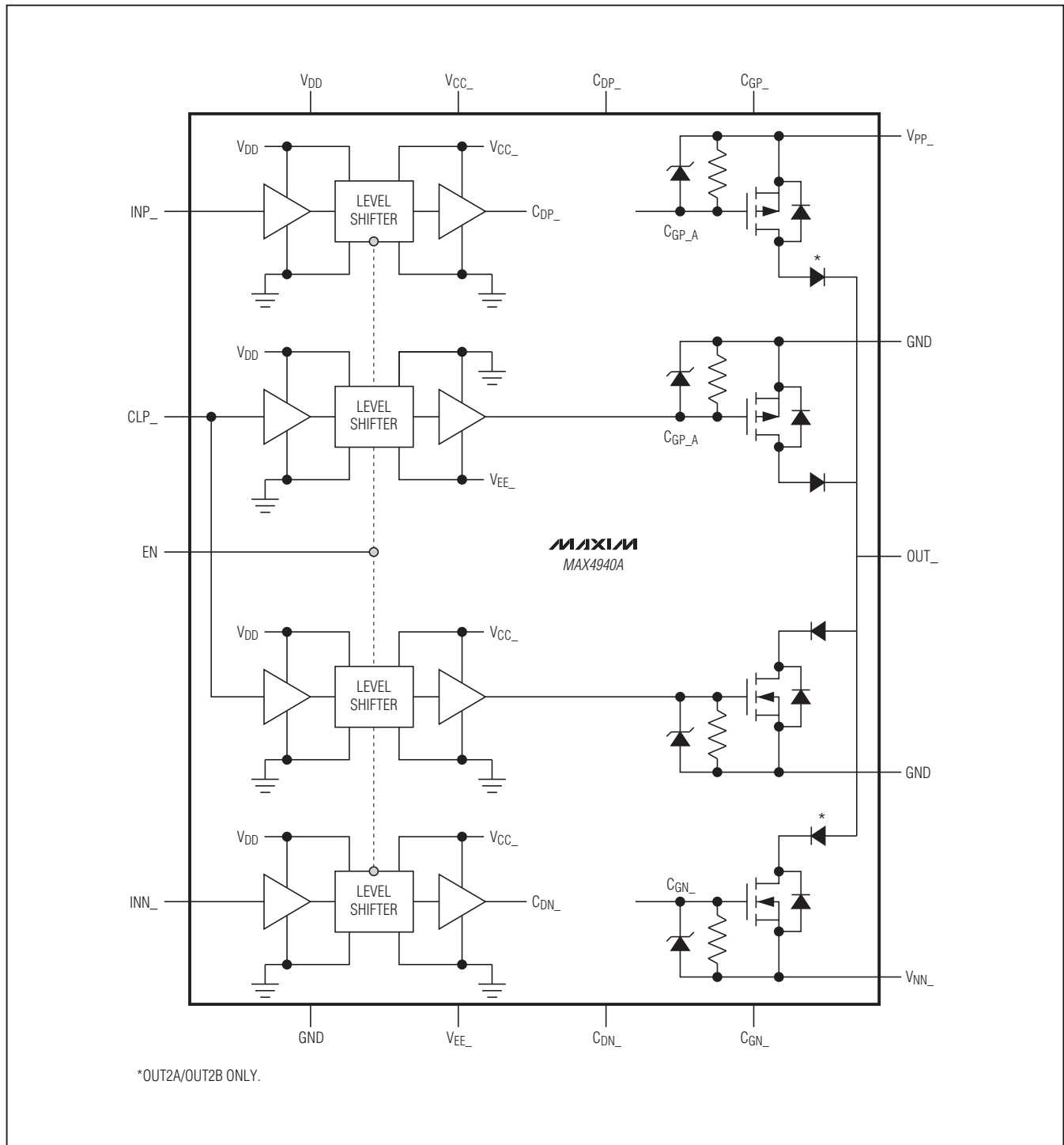


Figure 4. MAX4940A Simplified Functional Diagram for One Channel

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Typical Application Circuits

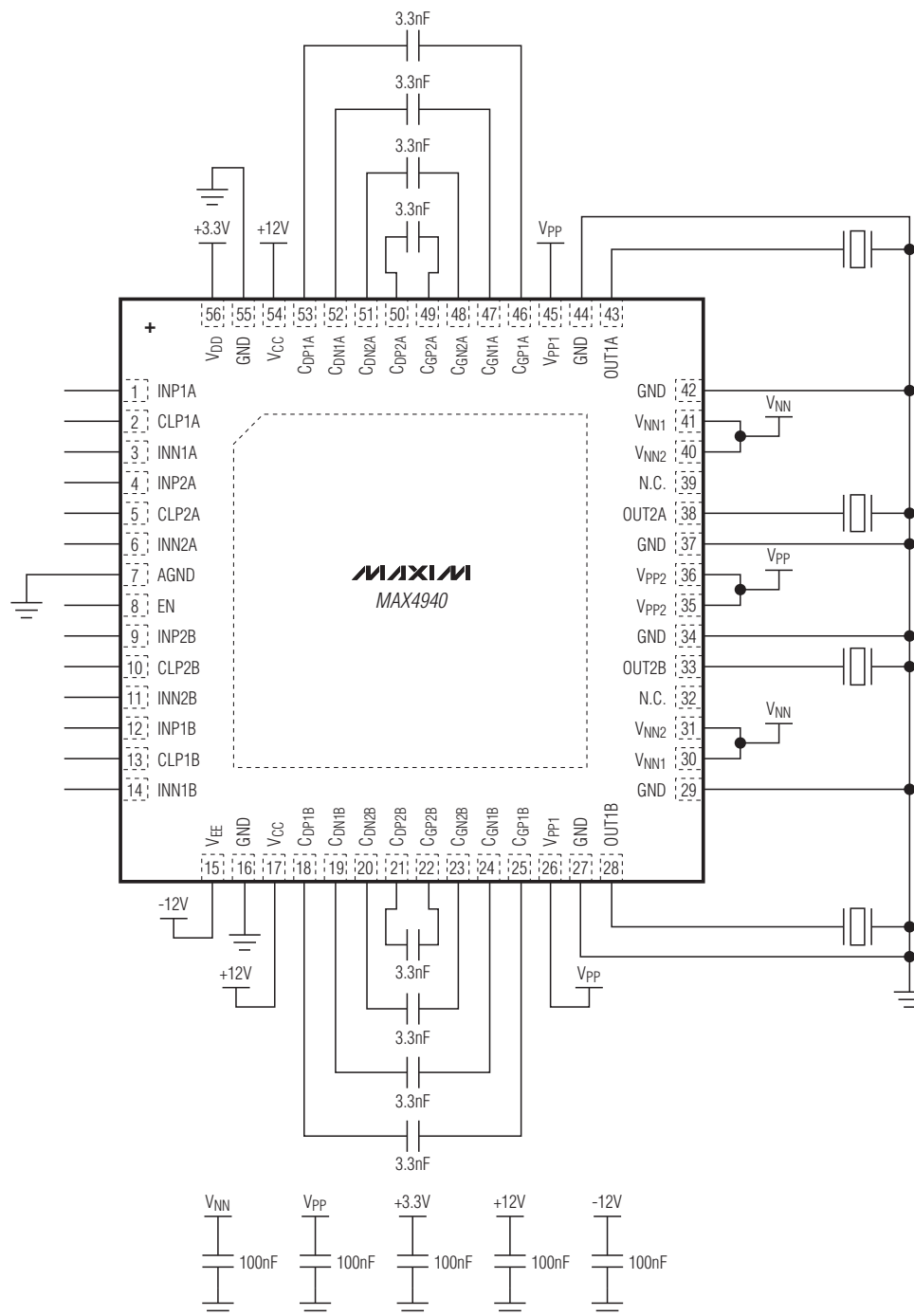


Figure 5. MAX4940 Quad Pulsing with Always-On Active Return-to-Zero

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Typical Application Circuits (continued)

MAX4940/MAX4940A

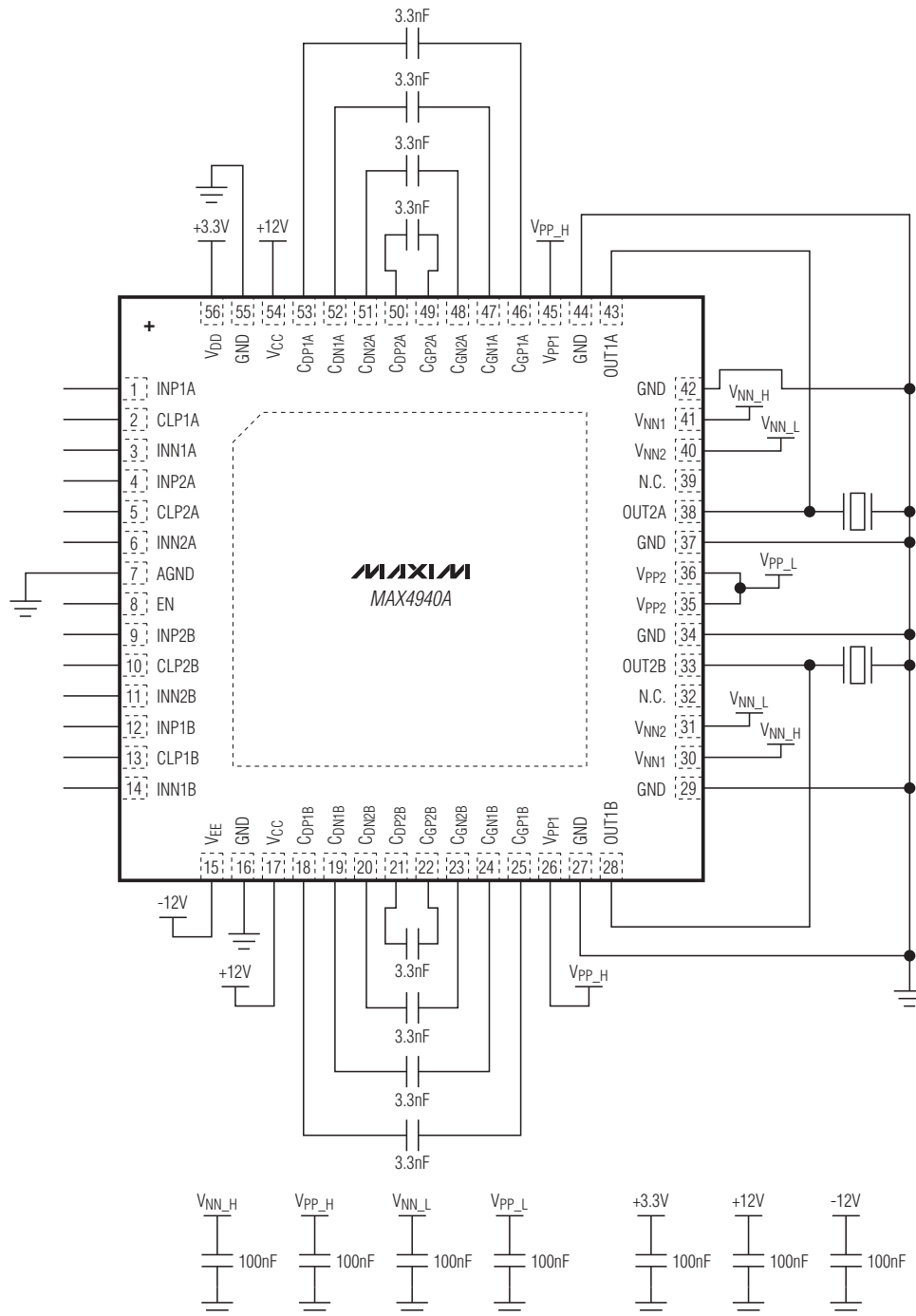


Figure 6. MAX4940A Dual Five-Level Pulsing

# Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO.            |
|--------------|--------------|-------------------------|
| 56 TQFN      | T5688-3      | <a href="#">21-0135</a> |

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