

Fast Sample and Hold

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Maximum Acquisition Time (10V Step to 0.1%).....4μs
(10V Step to 0.01%).....6μs**
- **Maximum Drift Current (Max. Over Temp.)10nA**
- **TTL Compatible Control Input**
- **Power Supply Rejection≥ 80dB**

Applications

- Data Acquisition Systems
- D to A Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Op Amp

Description

The HA-2420/883 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

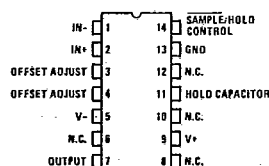
With an external hold capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

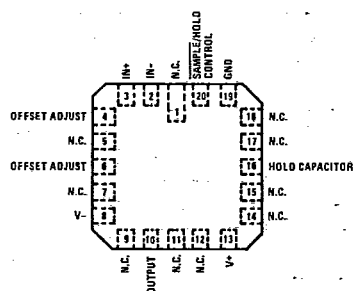
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note 517.

Pinouts

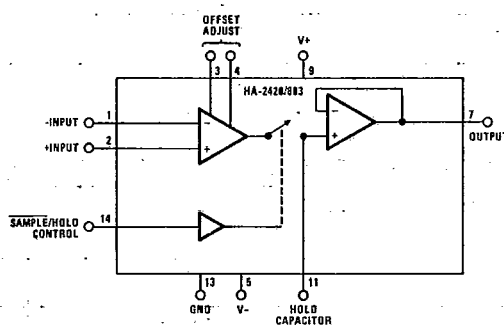
HA1-2420/883 (CERAMIC DIP)
TOP VIEW



HA4-2420/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



NOTE: Pin Numbers Correspond to DIP Package Only.

T-73-65

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals	40V	Thermal Resistance, Junction-to-Ambient (θ_{ja})	
Differential Input Voltage	$\pm 24V$	Ceramic DIP Package	96°C/W
Digital Input Voltage (S/H Pin)	+8V, -15V	Ceramic LCC Package	88°C/W
Output Current	Short Circuit Protected	Power Dissipation	
Storage Temperature Range	$-65^{\circ}C < T_A < +150^{\circ}C$	Ceramic DIP Package	1.03W @ +75°C
Lead Temperature (Soldering 10 Seconds)	275°C	Ceramic LCC Package	1.14W @ +75°C
Junction Temperature	+175°C	Power Dissipation Derating Factor (Above +75°C)	
Thermal Resistance, Junction-to-Case (θ_{jc})		Ceramic DIP Package	10mW/°C
Ceramic DIP Package	24°C/W	Ceramic LCC Package	11.4mW/°C
Ceramic LCC Package	20°C/W	ESD Classification	$\leq 2000V$

Recommended Operating Conditions

Operating Temperature Range	$-55^{\circ}C < T_A < +125^{\circ}C$	Logic Level Low (V_{IL})	0V to 0.8V
Operating Supply Voltage ($\pm V_{SUPPLY}$)	$\pm 15V$	Logic Level High (V_{IH})	2.0V to 5.0V
Analog Input Voltage (V_S)	$\pm 10V$		

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at V+ = +15V; V- = -15V; V_{IL} = 0.8V (Sample); V_{IH} = 2.0V (Hold); C_H = 1000pF, -Input Tied to Output, Unless Otherwise Specified

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Offset Voltage	V_{IO}		1	+25°C	-4	4	mV
			2, 3	-55°C, +125°C	-6	6	mV
Input Bias Current	I_{B+}		1	+25°C	-200	200	nA
			2, 3	-55°C, +125°C	-400	400	nA
	I_{B-}		1	+25°C	-200	200	nA
			2, 3	-55°C, +125°C	-400	400	nA
Input Offset Current	I_{IO}		1	+25°C	-50	50	nA
			2, 3	-55°C, +125°C	-100	100	nA
Open Loop Voltage Gain	+A _{VS}	$R_L = 2k\Omega, C_L = 50pF, V_{OUT} = +10V$	1	+25°C	25k	—	V/V
			2, 3	-55°C, +125°C	25k	—	V/V
	-A _{VS}	$R_L = 2k\Omega, C_L = 50pF, V_{OUT} = -10V$	1	+25°C	25k	—	V/V
			2, 3	-55°C, +125°C	25k	—	V/V
Common Mode Rejection Ratio	-CMRR	$V_+ = 25V, V_- = -5V, V_{OUT} = +10V, V_{S/H} = 10.8V$	1	+25°C	80	—	dB
			2, 3	-55°C, +125°C	80	—	dB
	+CMRR	$V_+ = 5V, V_- = -25V, V_{OUT} = -10V, V_{S/H} = -9.2V$	1	+25°C	80	—	dB
			2, 3	-55°C, +125°C	80	—	dB
Output Current	+I _O	$V_{OUT} = +10V$	1	+25°C	+15.0	—	mA
	-I _O	$V_{OUT} = -10V$	1	+25°C	-15.0	—	mA
Output Voltage Swing	+V _{OP}	$R_L = 2k\Omega, C_L = 50pF$	1	+25°C	+10.0	—	V
			2, 3	-55°C, +125°C	+10.0	—	V
	-V _{OP}	$R_L = 2k\Omega, C_L = 50pF$	1	+25°C	—	-10.0	V
			2, 3	-55°C, +125°C	—	-10.0	V
Power Supply Current	+I _{CC}		1	+25°C	—	5.5	mA
	-I _{CC}		1	+25°C	-3.5	—	mA
Power Supply Rejection Ratio	+PSRR	$V_+ = 10V, 20V, V_- = -15V, -15V$	1	+25°C	80	—	dB
			2, 3	-55°C, +125°C	80	—	dB
	-PSRR	$V_+ = 15V, 15V, V_- = -10V, -20V$	1	+25°C	80	—	dB
			2, 3	-55°C, +125°C	80	—	dB
Digital Input Current	I _{IN1}	$V_{IN1} = 0V$	1	+25°C	—	800	μA
			2, 3	-55°C, +125°C	—	800	μA
	I _{IN2}	$V_{IN2} = 5.0V$	1	+25°C	—	20	μA
			2, 3	-55°C, +125°C	—	20	μA
Digital Input Voltage	V_{IL}		1	+25°C	—	0.8	V
			2, 3	-55°C, +125°C	—	0.8	V
	V_{IH}		1	+25°C	2.0	—	V
			2, 3	-55°C, +125°C	2.0	—	V
Drift Current	I _D	$V_{IN} = 0V, R_L = 2k\Omega, C_L = 50pF, S/H = 4.0V$	2	+125°C	-10	10	nA

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

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TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at $V^+ = +15V$, $V^- = -15V$, $V_{IL} = 0.8V$ (Sample), $V_{IH} = 2.0V$ (Hold), $C_H = 1000pF$, -Input Tied to Output, Unless Otherwise Specified

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMP	LIMITS		UNITS
					MIN	MAX	
Hold Step Error	ERROR	$V_{IN} = 0V, 4V, t_{rise}(VS/H) = 30ns$	4	+25°C	-20	20	mV
Transient Response Rise Time & Fall Time	$TR_{(tr)}$	$C_L = 50pF, R_L = 2k\Omega, A_V = +1,$ $V_{OUT} = 200mV$ peak-to-peak	4	+25°C	—	100	ns
	$TR_{(tf)}$	$C_L = 50pF, R_L = 2k\Omega, A_V = +1,$ $V_{OUT} = 200mV$ peak-to-peak	4	+25°C	—	100	ns
Transient Response Overshoot	$TR_{(+OS)}$	$C_L = 50pF, R_L = 2k\Omega, A_V = +1,$ $V_{OUT} = 200mV$ peak-to-peak	4	+25°C	—	40	%
	$TR_{(-OS)}$	$C_L = 50pF, R_L = 2k\Omega, A_V = +1,$ $V_{OUT} = 200mV$ peak-to-peak	4	+25°C	—	40	%
Transient Response Slew Rate	$TR_{(+SR)}$	$C_L = 50pF, R_L = 2k\Omega, A_V = +1,$ $V_{OUT} = 10V$ peak-to-peak	4	+25°C	3.5	—	V/ μs
	$TR_{(-SR)}$	$C_L = 50pF, R_L = 2k\Omega, A_V = +1,$ $V_{OUT} = 10V$ peak-to-peak	4	+25°C	3.5	—	V/ μs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at $V^+ = +15V$, $V^- = -15V$, $V_{IL} = 0.8V$ (Sample), $V_{IH} = 2.0V$ (Hold), $C_H = 1000pF$, -Input Tied to Output, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS		UNITS
					MIN	MAX	
Hold Mode Feedthru Attenuation	V_{atten}	$R_L = 2k\Omega, C_L = 50pF, A_V = +1,$ $V_{IN} = 20V_{p-p}, f_{IN} = 50kHz$	1	+25°C, -55°C, +125°C	70	—	dB
Gain Bandwidth Product	GBWP	$R_L = 2k\Omega, C_L = 50pF, A_V = +1,$ $V_{IN} = 100mV_{p-p}$	1	+25°C,	2.5	—	MHz
Acquisition Time (0.1%)	$+t_{acq}$ (0.1%)	$R_L = 2k\Omega, C_L = 50pF, A_V = +1,$ $V_{OUT} = 0V, +10V$	1	+25°C,	—	4	μs
	$-t_{acq}$ (0.1%)	$R_L = 2k\Omega, C_L = 50pF, A_V = +1,$ $V_{OUT} = 0V, -10V$	1	+25°C,	—	4	μs
Acquisition Time (0.01%)	$+t_{acq}$ (0.01%)	$R_L = 2k\Omega, C_L = 50pF, A_V = +1,$ $V_{OUT} = 0V, +10V$	1	+25°C,	—	6	μs
	$-t_{acq}$ (0.01%)	$R_L = 2k\Omega, C_L = 50pF, A_V = +1,$ $V_{OUT} = 0V, -10V$	1	+25°C,	—	6	μs

NOTE: 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 4
Group A Test Requirements	1, 2, 3, 4
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

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Test Circuits

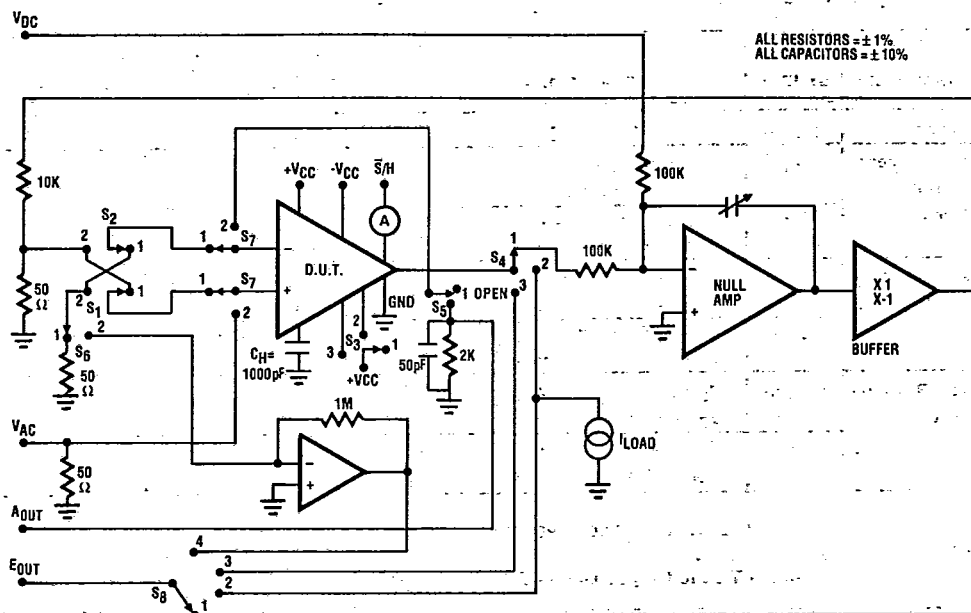
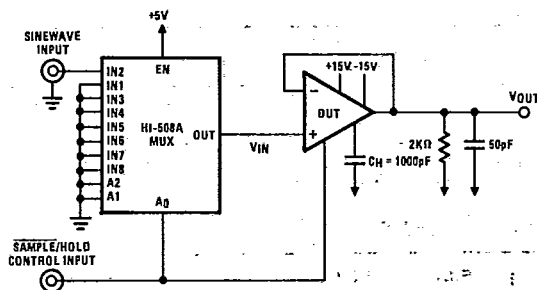


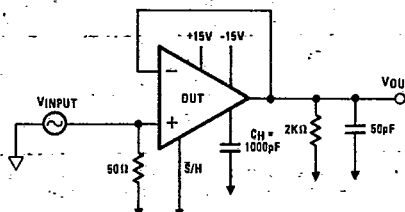
FIGURE 1.

Test Fixture Schematic (Switch Positions S₁ - S₈ Determine Configuration. See Chart A)

HOLD MODE FEEDTHROUGH ATTENUATION



GAIN BANDWIDTH PRODUCT



NOTE:

Compute Hold Mode Feedthrough Attenuation from the Formula:

$$\text{Feedthrough Attenuation} = 20 \log \left(\frac{V_{\text{OUT HOLD}}}{V_{\text{IN HOLD}}} \right)$$

Where $V_{\text{OUT HOLD}}$ = Peak-Peak Value of Output Sinewave During the Hold ModeGBWP is the Frequency of V_{INPUT} at which:

$$20 \log \left(\frac{V_{\text{OUT}}}{V_{\text{INPUT}}} \right) = -3\text{dB}$$

CHART A. TEST CIRCUIT CONDITIONS (SEE TEST CIRCUIT — FIGURE 1)

PARAMETER	NOTES	APPLY (IN VOLTS DC)				SWITCH POSITION								MEASURE		MEASURED PARAMETER EQUATION	UNITS		
		+V	-V	VDC	S/H	EOUT	S1	S2	S3	S4	S5	S6	S7	S8	VALUE			UNITS	
V _{IO}		15	-15	0	0.8	—	1	1	1	1	1	1	1	1	1	E1	V	V _{IO} = E1/200	mV
I _{IO}		15	-15	0	0.8	—	—	—	—	—	—	—	—	—	—		V	I _{IO} = (E7-E10)/10 ⁶	nA
I _{B+}		15	-15	0	0.8	—	2	2	1	1	1	2	1	4		E7	V	I _{B+} = E7/10 ⁶	nA
I _{B-}		15	-15	0	0.8	—	1	1	1	1	1	2	1	4		E10	V	I _{B-} = E10/10 ⁶	nA
+A _{VS}	1	15	-15	0	0.8	—	1	1	1	1	1	2	1	1		E25	V	+A _{VS} = 20log ₁₀ [(E25-E26)/200]	dB
	1	15	-15	-10	0.8	—	1	1	1	1	1	2	1	1		E26	V		
-A _{VS}	1	15	-15	0	0.8	—	1	1	1	1	1	2	1	1		E27	V	-A _{VS} = 20log ₁₀ [(E27-E28)/200]	dB
	1	15	-15	+10	0.8	—	1	1	1	1	1	2	1	1		E28	V		
-CMRR	4	25	-5	-10	10.8	—	1	1	1	1	1	1	1	1		E17	V	-CMRR = 20log ₁₀ [10/((E1-E17)/200)]	dB
+CMRR	5	5	-25	+10	-9.2	—	1	1	1	1	1	1	1	1		E18	V	+CMRR = 20log ₁₀ [10/((E1-E18)/200)]	dB
+I _O		15	-15	-13	0.8	10	1	1	1	3	1	1	1	3		I21	mA	+I _O = I21	mA
-I _O		15	-15	+13	0.8	-10	1	1	1	3	1	1	1	3		I22	mA	-I _O = I22	mA
+V _{OP}	1	15	-15	-14	0.8	—	1	1	1	3	2	1	1	3		E23	V	+V _{OP} = E23	V
-V _{OP}	1	15	-15	+14	0.8	—	1	1	1	3	2	1	1	3		E24	V	-V _{OP} = E24	V
+I _{CC}		15	-15	0	0.8	—	1	1	1	1	1	1	1	1			mA		mA
-I _{CC}		15	-15	0	0.8	—	1	1	1	1	1	1	1	1			mA		mA
+PSRR		10	-15	0	0.8	—	1	1	1	1	1	1	1	1		E13	V	+PSRR = 20log ₁₀ [10/(E13-E14)]	dB
		20	-15	0	0.8	—	1	1	1	1	1	1	1	1		E14	V		
-PSRR		15	-10	0	0.8	—	1	1	1	1	1	1	1	1		E15	V	-PSRR = 20log ₁₀ [10/(E15-E16)]	dB
		15	-20	0	0.8	—	1	1	1	1	1	1	1	1		E16	V		
I _{IN1}		15	-15	0	0	—	1	1	1	1	1	1	1	1		I _{S/H}	μA		μA
I _{IN2}		15	-15	0	5	—	1	1	1	1	1	1	1	1		I _{S/H}	μA		μA
I _D	1, 6	15	-15	0	4.0	—	1	1	1	3	2	1	2	1		AOUT	mV	I _D = C _H x ΔV/ΔT	nA
Hold Step Error	1, 6	15	-15	0	0	—	1	1	1	3	2	1	2	1		AOUT1	mV	V _{Error} = AOUT1-AOUT2	mV
		15	-15	0	4.0	—	1	1	1	3	2	1	2	1		AOUT2	mV		
TR _(tr)	2	15	-15	—	0.8	—	1	1	1	3	2	1	2	1		AOUT	See Notes	TR _(tr) = 10% to 90%	ns
TR _(ff)	2	15	-15	—	0.8	—	1	1	1	3	2	1	2	1		AOUT	See Notes	TR _(ff) = 90% to 10%	ns
TR _(+OS)	2	15	-15	—	0.8	—	1	1	1	3	2	1	2	1		AOUT	See Notes	TR _(+OS) = (V _{peak} -V _{final})/V _{final} x 100	%
TR _(-OS)	2	15	-15	—	0.8	—	1	1	1	3	2	1	2	1		AOUT	See Notes	TR _(-OS) = (V _{peak} -V _{final})/V _{final} x 100	%
TR _(+SR)	3	15	-15	—	0.8	—	1	1	1	3	2	1	2	1		AOUT	See Notes	TR _(+SR) = ΔV/ΔT	V/μs
TR _(-SR)	3	15	-15	—	0.8	—	1	1	1	3	2	1	2	1		AOUT	See Notes	TR _(-SR) = ΔV/ΔT	V/μs

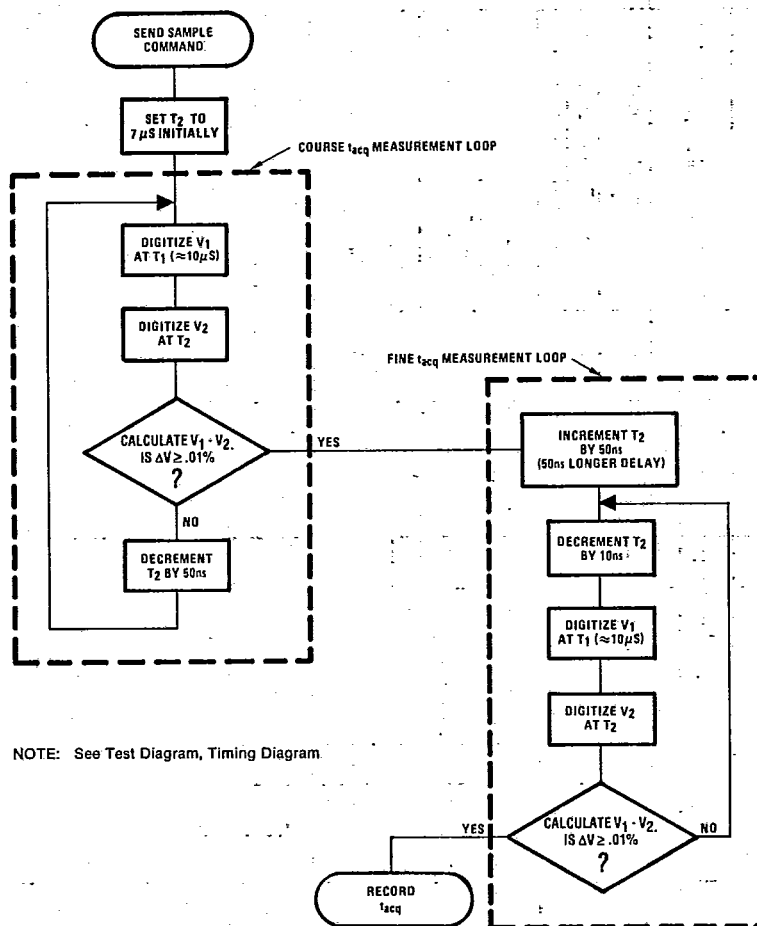
NOTES: 1. R_{LDC} = 2kΩ
 2. V_{OUT} = 200mV_{p-p}, R_L = 2kΩ, C_L = 50pF
 3. V_{OUT} = 10V Step, R_L = 2kΩ, C_L = 50pF
 4. Package GND held at +10V for this test.
 5. Package GND held at -10V for this test.
 6. V_{AC} = 0V

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 SAMPLE & HOLD
 AMPLIFIERS

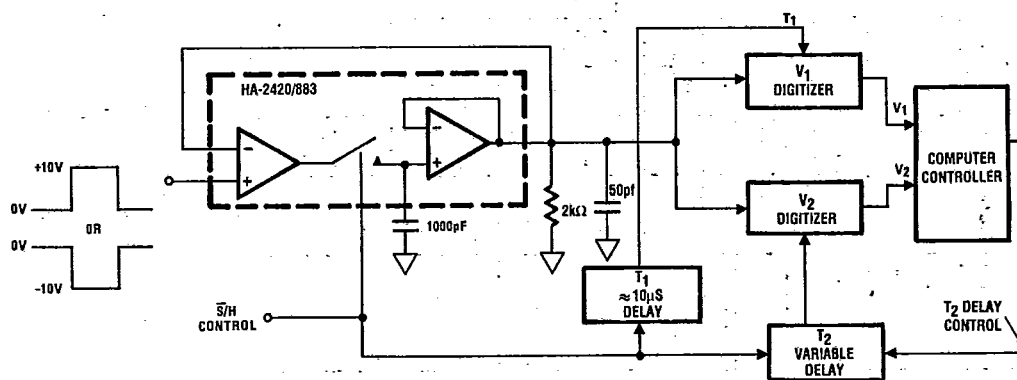
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Test Circuits (Continued)

ACQUISITION TIME

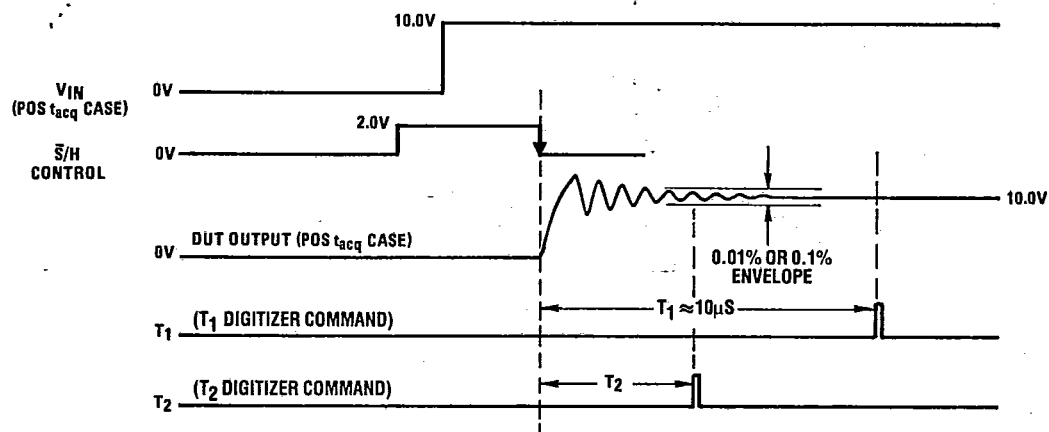
(t_{acq} to 0.01% is shown, t_{acq} to 0.1% is done in the same manner)

NOTE: See Test Diagram, Timing Diagram

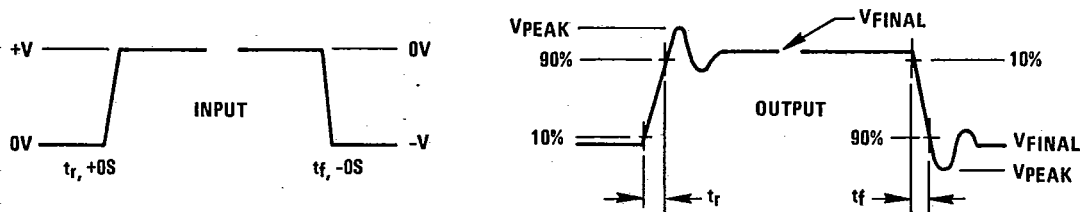


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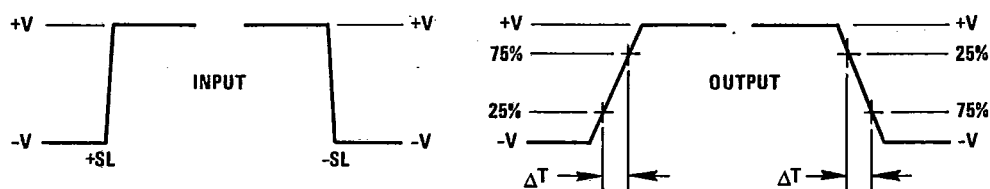
Timing Waveforms

TIMING DIAGRAM FOR ACQUISITION TIME, (POSITIVE t_{acq} CASE)

OVERSHOOT, RISE & FALL TIME WAVEFORMS



SLEW RATE WAVEFORMS



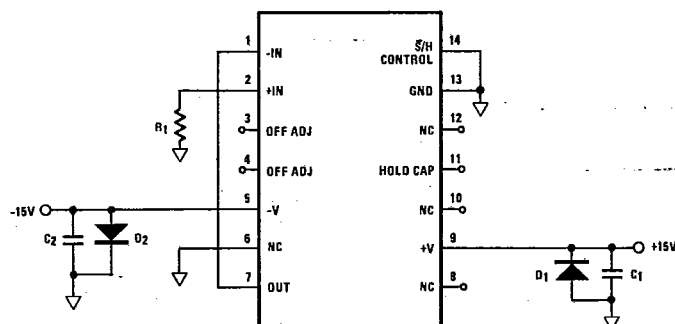
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SAMPLE & HOLD
AMPLIFIERS

Burn-In Circuits

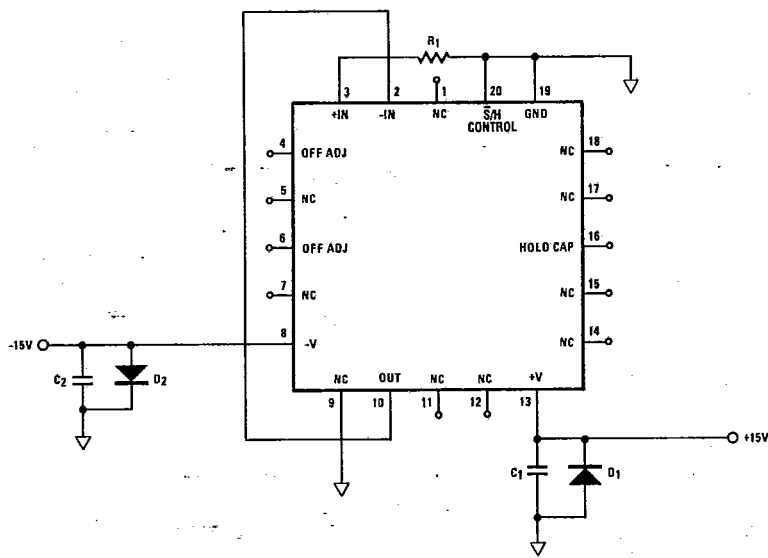
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HA-2420/883 (CERAMIC DIP)



$R_1 = 100k\Omega, \pm 5\%$ (per socket)
 $C_1 = C_2 = 0.1\mu F$ (one per row) or
 $0.01\mu F$ (one per socket)
 $D_1 = D_2 = 1N4002$ or equivalent (per board)

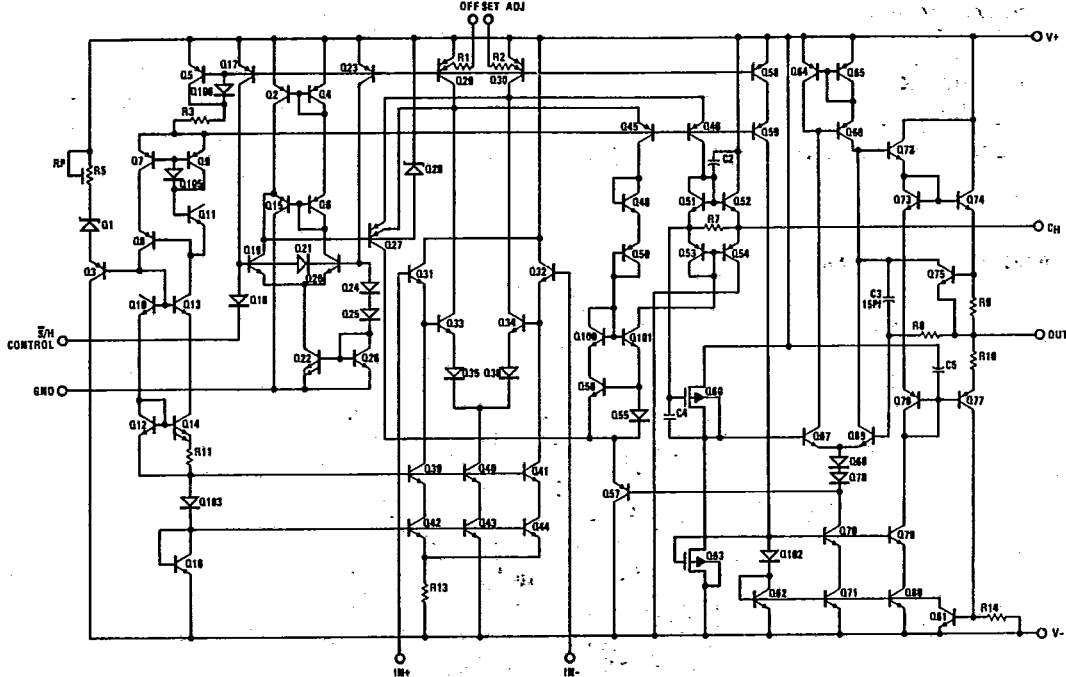
HA-2420/883 (CERAMIC LCC)



$R_1 = 100k\Omega, \pm 5\%$ (per socket)
 $C_1 = C_2 = 0.1\mu F$ (one per row) or
 $0.01\mu F$ (one per socket)
 $D_1 = D_2 = 1N4002$ or equivalent (per board)

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Schematic Diagram



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SAMPLE & HOLD
AMPLIFIERS

T-73-65

Die Characteristics**DIE DIMENSIONS:** 97 x 61 x 19 mils**METALLIZATION**

Type: Al

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$ **GLASSIVATION**

Type: Silox

Thickness: $14\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$ **WORST CASE CURRENT DENSITY:** $1.7 \times 10^5 \text{ A/cm}^2$ **TRANSISTOR COUNT:**

HA-2420/883 78

PROCESS: Bipolar-DI**DIE ATTACH**

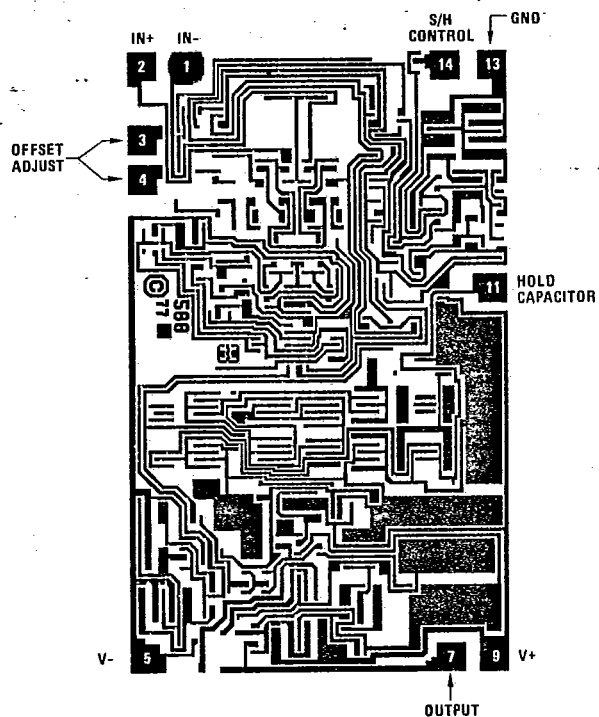
Material: Gold/Silicon Eutectic Alloy

Temperature: Ceramic DIP — 460°C (Max)

Ceramic LCC — 420°C (Max)

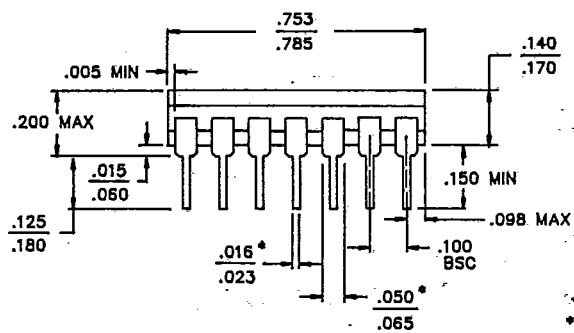
Metallization Mask Layout

HA-2420/883



NOTE: Pad Numbers Correspond to DIP Package Only.

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Packaging†**14 PIN CERAMIC DIP**

* INCREASE MAX LIMIT BY .003 INCHES
MEASURED AT CENTER OF FLAT FOR
SOLDER FINISH

LEAD MATERIAL: Type B**LEAD FINISH:** Type A**PACKAGE MATERIAL:** Ceramic, 90% Alumina**PACKAGE SEAL:**

Material: Glass Frit

Temperature: 450°C ± 10°C

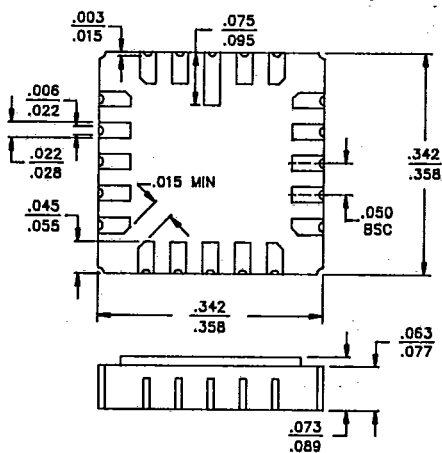
Method: Furnace Seal

INTERNAL LEAD WIRE:

Material: Aluminum

Diameter: 1.25 Mil

Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 D-1**20 PAD CERAMIC LCC****PAD MATERIAL:** Type C**PAD FINISH:** Type A**FINISH DIMENSION:** Type A**PACKAGE MATERIAL:** Multilayer Ceramic, 90% Alumina**PACKAGE SEAL:**

Material: Gold/Tin (80/20)

Temperature: 320°C ± 10°C

Method: Furnace Braze

INTERNAL LEAD WIRE:

Material: Aluminum

Diameter: 1.25 Mil

Bonding Method: Ultrasonic

COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in Inches.



HARRIS

T-73-65

HA-2420

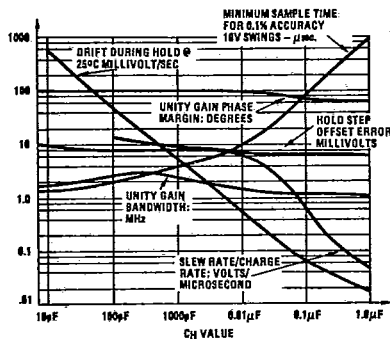
DESIGN INFORMATION

Fast Sample and Hold

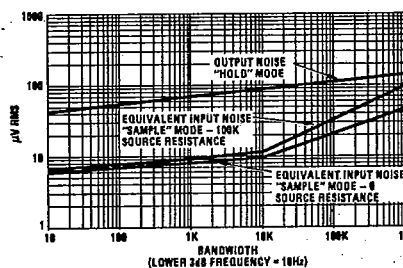
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: $V_{SUPPLY} = \pm 15VDC$, $T_A = +25^\circ C$, $C_H = 1000pF$

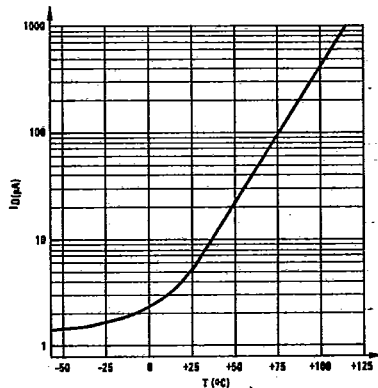
**TYPICAL SAMPLE AND HOLD PERFORMANCE
AS A FUNCTION OF HOLDING CAPACITOR**



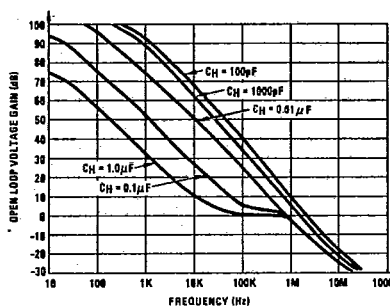
BROADBAND NOISE CHARACTERISTICS



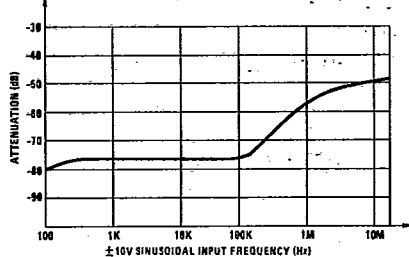
DRIFT CURRENT vs. TEMPERATURE



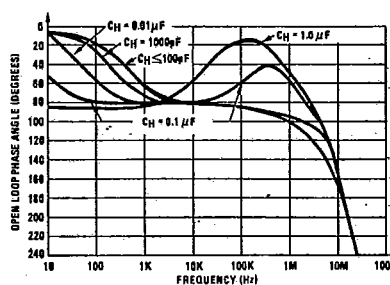
OPEN LOOP FREQUENCY RESPONSE



**HOLD MODE FEEDTHROUGH ATTENUATION
 $C_H = 1000pF$**



OPEN LOOP PHASE RESPONSE



T-73-65

DESIGN INFORMATION (Continued)

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Offset and Gain Adjustment

HOLD STEP vs. INPUT VOLTAGE

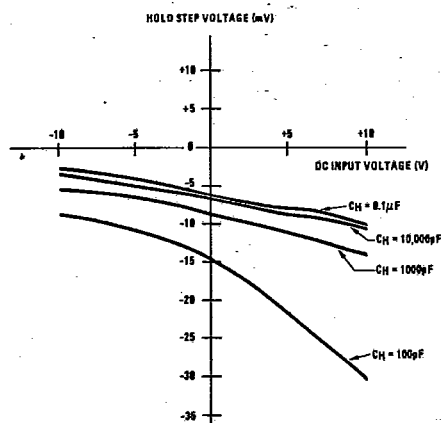


FIGURE 1.

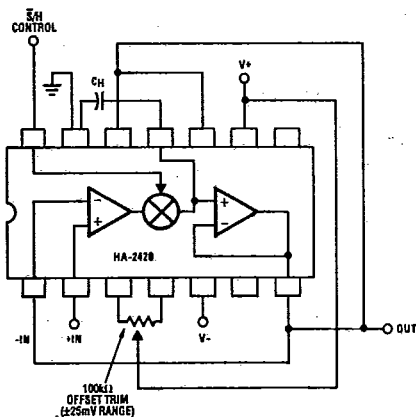
BASIC SAMPLE-AND-HOLD
(TOP VIEW)

FIGURE 2.

OFFSET ADJUSTMENT

The offset voltage of the HA-2420 may be adjusted using a 100kΩ trim pot, as shown in Figure 2. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the S/H control.
2. Adjust the trim pot for zero volts output in the hold mode.

GAIN ADJUSTMENT

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.08% gain error ($C_H = 1000pF$). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage (V_{-10} NOMINAL). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10} \text{ NOMINAL}) + (-10V)}{2}$$

2

INVERTING CONFIGURATION

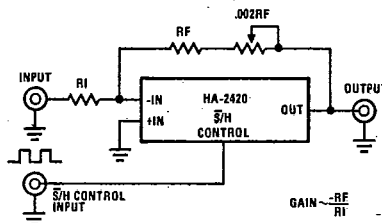


FIGURE 3.

NONINVERTING CONFIGURATION

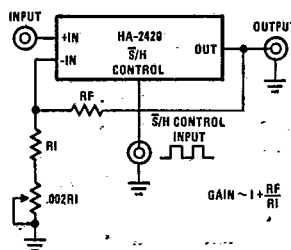


FIGURE 4.

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SAMPLE & HOLD
AMPLIFIERS