MC10165

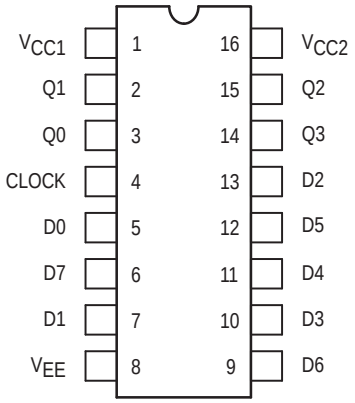
8-Input Priority Encoder

The MC10165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

The input is active when high, (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

- P_D = 545 mW typ/pkg (No Load)
- t_{pd} = 4.5 ns typ (Data to Output)
- t_r, t_f = 2.0 ns typ (20%–80%)

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	X	X	X	X	X	X	X	H	L	L	L
L	H	X	X	X	X	X	X	H	L	L	H
L	L	H	X	X	X	X	X	H	L	H	L
L	L	L	H	X	X	X	X	H	L	H	H
L	L	L	L	H	X	X	X	H	H	L	L
L	L	L	L	L	H	X	X	H	H	L	H
L	L	L	L	L	L	H	X	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

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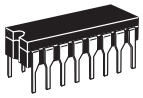
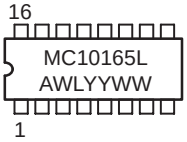
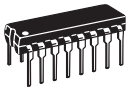
MARKING DIAGRAMS

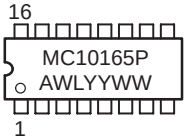


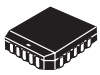
CDIP–16
L SUFFIX
CASE 620



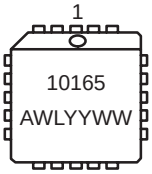


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

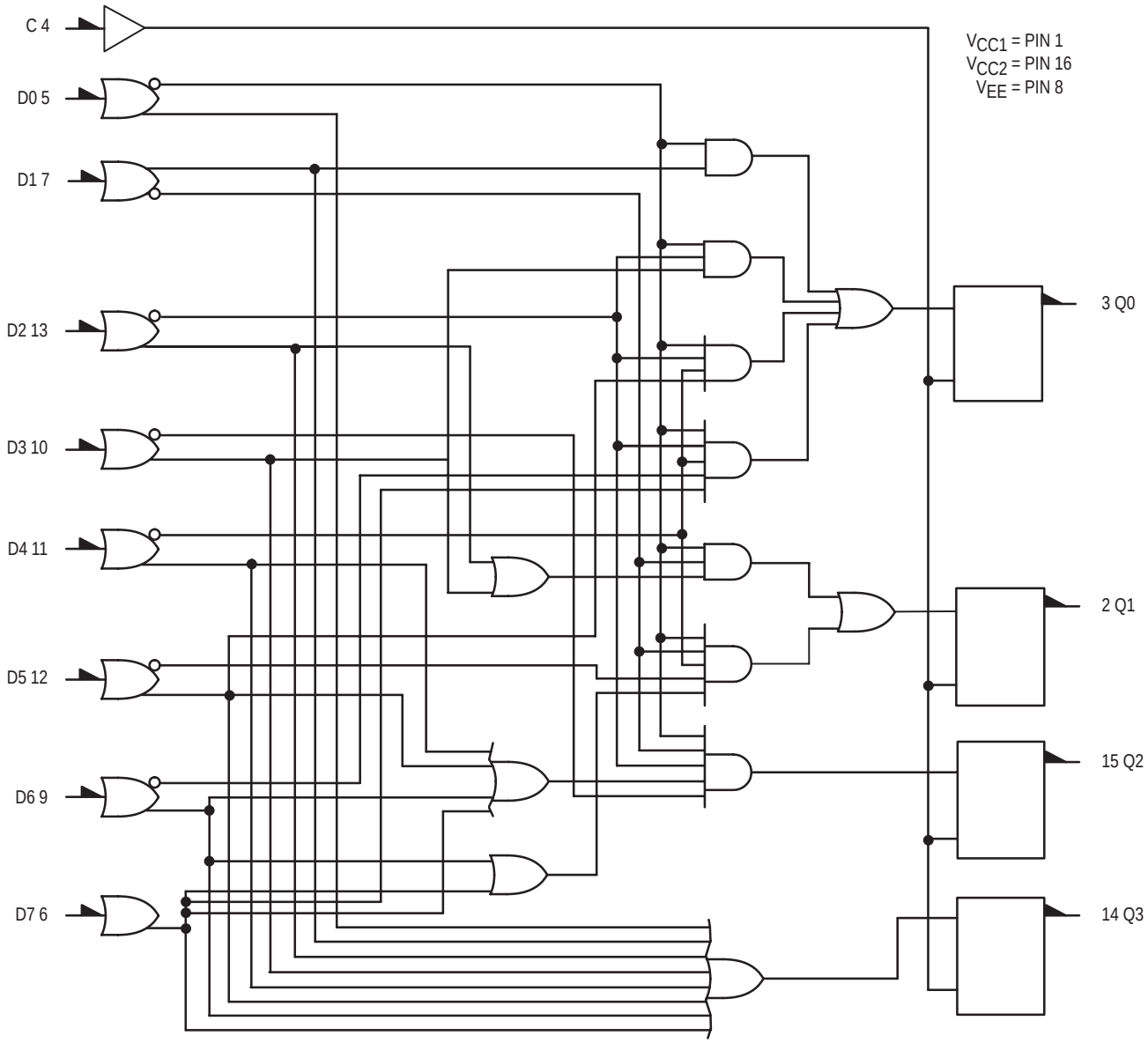


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10165L	CDIP–16	25 Units / Rail
MC10165P	PDIP–16	25 Units / Rail
MC10165FN	PLCC–20	46 Units / Rail

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		144		105	131		144	mAdc
Input Current	I_{inH}	4 5		390 350			245 220		245 220	µAdc
	I_{inL}	4 5	0.5 0.5		0.5 0.5			0.3 0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3 14 15	–1.060 –1.060 –1.060 –1.060	–0.890 –0.890 –0.890 –0.890	–0.960 –0.960 –0.960 –0.960		–0.810 –0.810 –0.810 –0.810	–0.890 –0.890 –0.890 –0.890	–0.700 –0.700 –0.700 –0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3 14 15	–1.890 –1.890 –1.890 –1.890	–1.675 –1.675 –1.675 –1.675	–1.850 –1.850 –1.850 –1.850		–1.650 –1.650 –1.650 –1.650	–1.825 –1.825 –1.825 –1.825	–1.615 –1.615 –1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3 14 15	–1.080 –1.080 –1.080 –1.080		–0.980 –0.980 –0.980 –0.980			–0.910 –0.910 –0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3 14 15		–1.655 –1.655 –1.655 –1.655			–1.630 –1.630 –1.630 –1.630		–1.595 –1.595 –1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Data Input	t_{5+14+} t_{5-14-} t_{7+3+} t_{11+15+} t_{13+2+}	14 14 3 15 2	2.0 2.0 2.0 2.0 2.0	7.0 7.0 7.0 7.0 7.0	3.0 3.0 3.0 3.0 3.0		7.0 7.0 7.0 7.0 7.0	2.0 2.0 2.0 2.0 2.0	8.0 8.0 8.0 8.0 8.0	
Clock Input	t_{4-3+} t_{4-3-} t_{4-14+} t_{4-14-}	3 (2.) 3 (3.) 14 (2.) 14 (3.)	1.5 1.5 1.5 1.5	4.5 4.5 4.5 4.5	2.0 2.0 2.0 2.0		4.0 4.0 4.0 4.0	1.5 1.5 1.5 1.5	4.5 4.5 4.5 4.5	
Setup Time	t_{setupH} t_{setupL}	3 3	6.0 6.0		6.0 6.0	3.4 3.0		6.0 6.0		
Hold Time	t_{holdH} t_{holdL}	3 3	1.0 1.0		1.0 1.0	–2.3 –2.7		1.0 1.0		
Rise Time (20 to 80%)	t_{3+}	3	1.1	3.5	1.1	2.0	3.3	1.1	3.5	
Fall Time (20 to 80%)	t_{3-}	3	1.1	3.5	1.1	2.0	3.3	1.1	3.5	

1. The same limit applies for all D type input pins. To test input currents for other D inputs, individually apply proper voltage to pin under test.
2. Output latched to low state prior to test.
3. Output latched to high state prior to test.

* To preserve reliable performance, the MC10165P (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500 lfpm blown air or equivalent heat sinking is provided.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8					8	1, 16
Input Current	I_{inH}	4	4				8	1, 16
		5	5 (1.)				8	1, 16
	I_{inL}	4		4			8	1, 16
		5		5 (1.)			8	1, 16
Output Voltage Logic 1	V_{OH}	2	6	4			8	1, 16
		3	6	4			8	1, 16
		14	6	4			8	1, 16
		15	6	4			8	1, 16
Output Voltage Logic 0	V_{OL}	2		4			8	1, 16
		3		4			8	1, 16
		14		4			8	1, 16
		15		4			8	1, 16
Threshold Voltage Logic 1	V_{OHA}	2		4	6		8	1, 16
		3		4	6		8	1, 16
		14		4	6		8	1, 16
		15		4	6		8	1, 16
Threshold Voltage Logic 0	V_{OLA}	2		4		6	8	1, 16
		3		4		6	8	1, 16
		14		4		6	8	1, 16
		15		4		6	8	1, 16
Switching Times (50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0**
Propagation Delay Data Input	t_{5+14+}	14		4	5	14	8	1, 16
	$t_{5–14–}$	14		4	5	14	8	1, 16
	t_{7+3+}	3		4	7	3	8	1, 16
	t_{11+15+}	15		4	11	15	8	1, 16
	t_{13+2+}	2		4	13	2	8	1, 16
Clock Input	$t_{4–3+}$	3 (2.)	7		4	3	8	1, 16
	$t_{4–3–}$	3 (3.)			4	3	8	1, 16
	$t_{4–14+}$	14 (2.)	7		4	14	8	1, 16
	$t_{4–14–}$	14 (3.)			4	14	8	1, 16
Setup Time	t_{setupH}	3			4,7	3	8	1, 16
	t_{setupL}	3			4,7	3	8	1, 16
Hold Time	t_{holdH}	3			4,7	3	8	1, 16
	t_{holdL}	3			4,7	3	8	1, 16
Rise Time (20 to 80%)	t_{3+}	3		4	7	3	8	1, 16
Fall Time (20 to 80%)	$t_{3–}$	3		4	7	3	8	1, 16

1. The same limit applies for all D type input pins. To test input currents for other D inputs, individually apply proper voltage to pin under test.
2. Output latched to low state prior to test.
3. Output latched to high state prior to test.

* To preserve reliable performance, the MC10165P (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500 lfpm blown air or equivalent heat sinking is provided.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

APPLICATION INFORMATION

A typical application of the MC10165 is the decoding of system status on a priority basis. A 64 line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64–LINE PRIORITY ENCODER