FAIRCHILD SEMICONDUCTOR™

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DM93S41
4-Bit Arithmetic Logic Unit

General Description

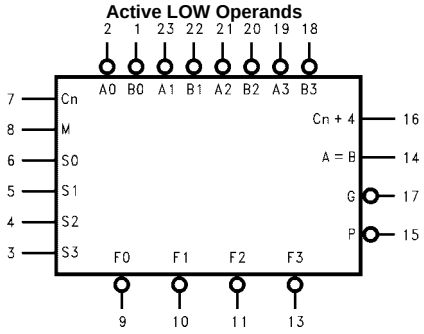
The DM93S41 4-bit arithmetic logic units can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important.

Ordering Code:

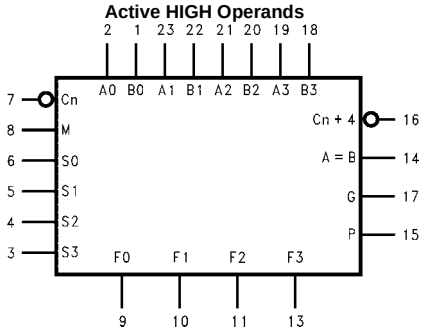
Order Number	Package Number	Package Description
DM93S41N	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600" Wide

Logic Symbols

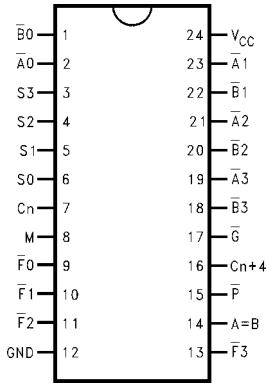
Active LOW Operands



Active HIGH Operands



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{A}0$–$\overline{A}3$, $\overline{B}0$–$\overline{B}3$	Operand Inputs (Active LOW)
S0–S3	Function Select Inputs
M	Mode Control Input
Cn	Carry Input
$\overline{F}0$–$\overline{F}3$	Function Outputs (Active LOW)
A = B	Comparator Output
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
C_{n+4}	Carry Output

Functional Description

The DM93S41 is a 4-bit high speed parallel arithmetic logic unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the DM93S41 can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For super high speed operation the Schottky DM93S41 should be used in conjunction with the '42 carry lookahead circuit.

The A = B output from the DM93S41 goes HIGH when all four $\overline{F}_n$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with the other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated the '41 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

Mode Select Inputs				Active LOW Inputs & Outputs		Active HIGH Inputs & Outputs	
				Logic Arithmetic (Note 2)		Logic Arithmetic (Note 2)	
S3	S2	S1	S0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A} + B$	A + B
L	L	H	L	$\overline{A} + \overline{B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A} + \overline{B}$	A plus $(A + \overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	(A +B) plus $A\overline{B}$
L	H	H	L	$\overline{A} \oplus \overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A} + B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	$(A + \overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A (Note 1)	Logic 1	A plus A (Note 1)
H	H	L	H	$A\overline{B}$	AB plus A	$A + \overline{B}$	(A + B) plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	$(A + \overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

H = HIGH Voltage Level
L = LOW Voltage Level

Note 1: Each bit is shifted to the next more significant position

Note 2: Arithmetic operations expressed in 2s complement notation

TABLE 1. SUM MODE TEST Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Input		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ to $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ to $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH}, t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH}, t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

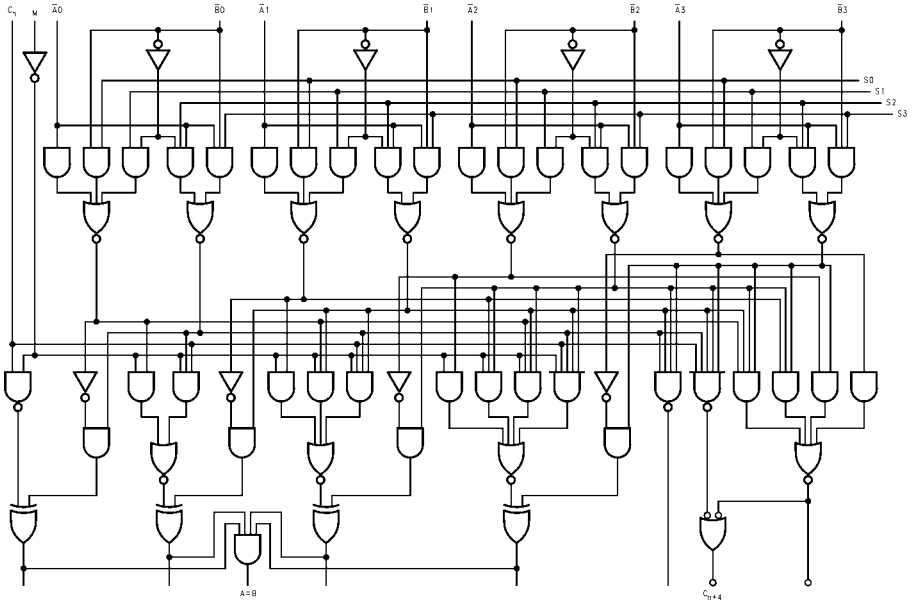
TABLE 2. DIFF MODE TEST Function Inputs: S1 = S2 = 4.5V,S0 = S3 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH}, t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH}, t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH}, t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH}, t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH}, t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$

TABLE 3. LOGIC MODE TEST Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH}, t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$

Logic Diagram



Absolute Maximum Ratings(Note 3)

Supply Voltage	7V
Input Voltage:	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−1	mA
I_{OL}	LOW Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA			−1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			50	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.5V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	−40		−100	mA
I_{CCL}	Supply Current	V_{CC} = Max M, S0–S3 = 4.5V All Other Inputs = 0V			150	mA
I_{CCH}	Supply Current	V_{CC} = Max C_n, $\overline{B}0$–$\overline{B}3$ = GND All Other Inputs = 4.5V			140	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

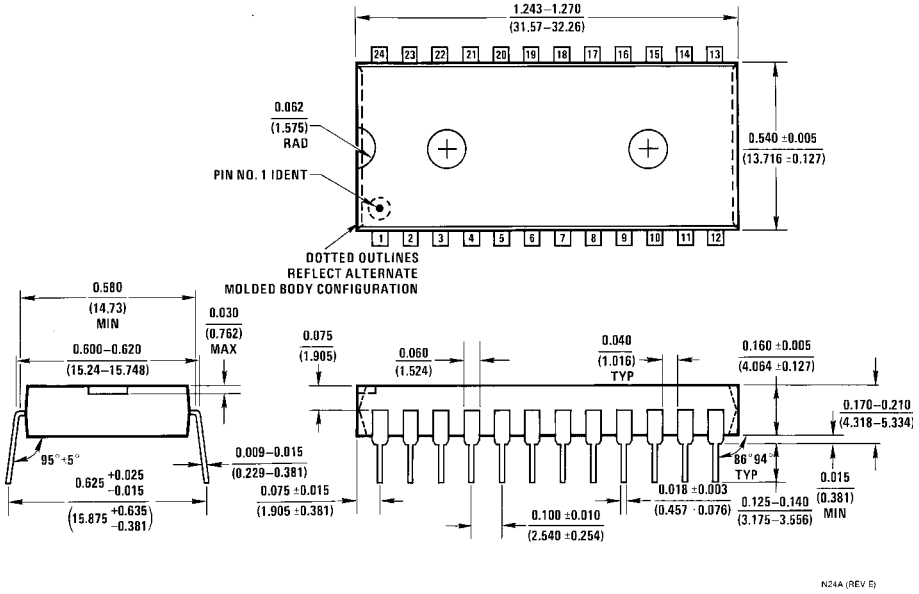
Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	Conditions	CL = 15 pF, R_L = 280Ω		Units
			Min	Max	
t_{PLH}	Propagation Delay	M = GND		12	ns
t_{PHL}	C_n to C_{n+4}			12	
t_{PLH}	Propagation Delay	M = GND		12	ns
t_{PHL}	C_n to $\overline{F}$			12	
t_{PLH}	Propagation Delay	M, S1, S2 = GND		14	ns
t_{PHL}	$\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	S0, S3 = 4.5V		14	
t_{PLH}	Propagation Delay	M, S0, S3 = GND		15	ns
t_{PHL}	$\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	S1, S2 = 4.5V		15	
t_{PLH}	Propagation Delay	M, S1, S2 = GND		14	ns
t_{PHL}	$\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	S0, S3 = 4.5V		14	
t_{PLH}	Propagation Delay	M, S0, S3 = GND		15	ns
t_{PHL}	$\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	S1, S2 = 4.5V		15	
t_{PLH}	Propagation Delay	M, S1, S3 = GND		20	ns
t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	S0, S3 = 4.5V		20	
t_{PLH}	Propagation Delay	M, S0, S3 = GND		21	ns
t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	S1, S2 = 4.5V		21	
t_{PLH}	Propagation Delay	M, S1, S2 = GND		24	ns
t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_{i+1}$	S0, S3 = 4.5V		24	
t_{PLH}	Propagation Delay	M, S0, S3 = GND		25	ns
t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_{i+1}$	S1, S2 = 4.5V		25	
t_{PLH}	Propagation Delay	M = 4.5V		20	ns
t_{PHL}	$\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}$			20	
t_{PLH}	Propagation Delay	M, S1, S2 = GND		18.5	ns
t_{PHL}	$\overline{A}_n$ or $\overline{B}_n$ to C_{n+1}	S0, S3 = 4.5V		18.5	
t_{PLH}	Propagation Delay	M, S0, S3 = GND		23	ns
t_{PHL}	$\overline{A}_n$ or $\overline{B}_n$ to C_{n+1}	S1, S2 = 4.5V		23	
t_{PLH}	Propagation Delay	M, S0, S3 = GND		23	ns
t_{PHL}	$\overline{A}_n$ or $\overline{B}_n$ to A = B	S1, S2 = 4.5V		23	
		R_L = 400Ω to 5.0V			

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600" Wide
Package Number N24A