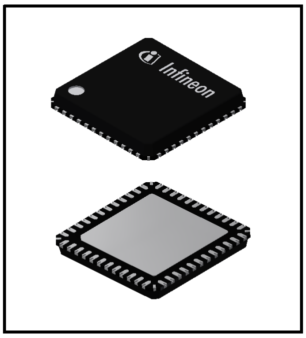
TLD5501-2QV

Dual SYNC Buck Controller with SPI Interface

Infineon LITIX™ Power Flex

AEC Qualified RoHS

Package	PG-VQFN-48
Marking	TLD55012QV
Sales Name	TLD5501-2QV



1 Overview

Features

- Dual-Channel synchronous DC/DC Controller for HIGH POWER LED drivers
- Wide LED forward voltage Range (2 V up to 50 V)
- Wide VIN Range (IC 4.5 V to 40 V, Power 4.5 V to 55 V)
- Switching Frequency Range from 200 kHz to 700 kHz
- SPI for diagnostics and control
- Maximum Efficiency in every condition (up to 96%)
- Constant Current (LED) and Constant Voltage Regulation
- Limp Home Function (Fail Safe Mode)
- EMC optimized device: Features an auto Spread Spectrum
- LED current sense with dedicated monitor Output
- Advanced protection features for device and load
- Enhanced Dimming features: Analog and PWM dimming
- LED current accuracy +/- 3%
- Available in a small thermally enhanced PG-VQFN-48 package
- Automotive AEC Q100 Grade 1 (-40°C to 125°C) qualified

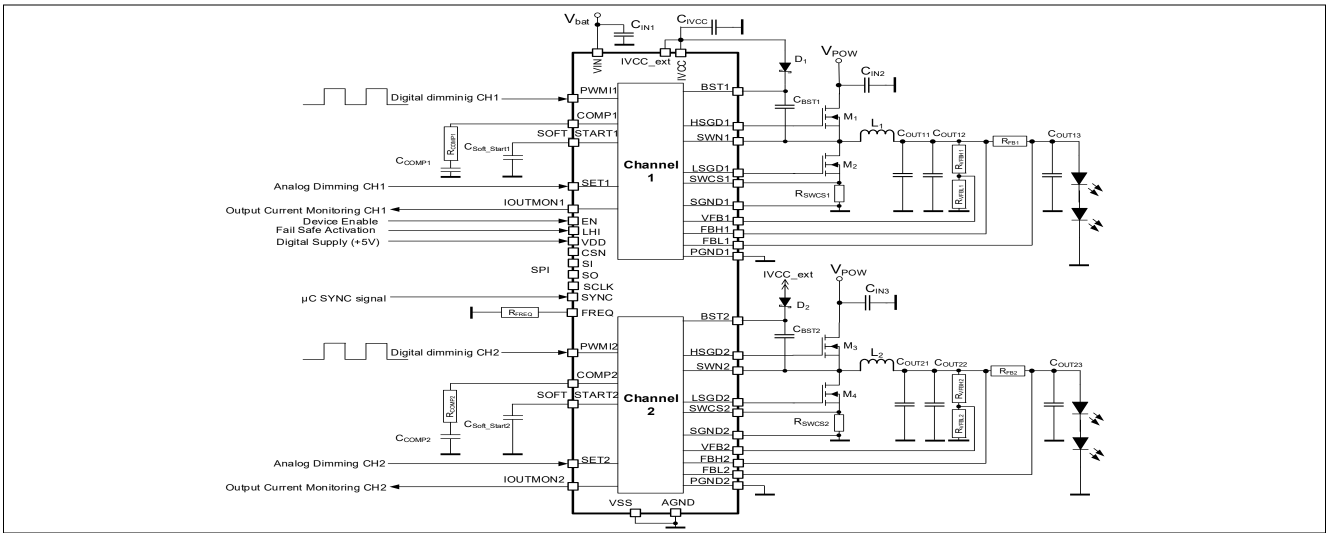


Figure 1 Application Drawing - TLD5501-2QV as current regulator

Description

The TLD5501-2QV is a synchronous DUAL Channel DC/DC buck controller with built in protection features and SPI interface. This concept is beneficial for driving high power LEDs with maximum system efficiency and minimum number of external components. The TLD5501-2QV offers both analog and digital (PWM) dimming. The switching frequency is adjustable in the range of 200 kHz to 700 kHz. It can be synchronized to an external clock source. A built in programmable Spread Spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. Furthermore the current mode regulation scheme provides a stable regulation loop maintained by small external compensation components. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The TLD5501-2QV is suitable for use in the harsh automotive environment.

Table 1 Product Summary

Power Stage input voltage range	V_{POW}	4.5 V … 55 V
Device Input supply voltage range	V_{VIN}	4.5 V … 40 V
Maximum output voltage (depending by the application conditions)	$V_{OUT(max)}$	50 V
Switching Frequency range	f_{SW}	200 kHz ... 700 kHz
Typical NMOS driver on-state resistance at T_j = 25°C (Gate Pull Up)	$R_{DS(ON\_PU)}$	2.3 Ω
Typical NMOS driver on-state resistance at T_j = 25°C (Gate Pull Down)	$R_{DS(ON\_PD)}$	1.2 Ω
SPI clock frequency	$f_{SCLK(MAX)}$	5 MHz

Protective Functions

- Over load protection of external MOSFETs
- Shorted load, output overvoltage and overcurrent protection
- Input undervoltage protection
- Thermal shutdown of device with autorestart behavior
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Latched diagnostic information via SPI
- Open load detection in ON-state
- Device Overtemperature shutdown and Temperature Prewarning
- Smart monitoring and advanced functions provide I_{LED} information

Limp Home Function

- Limp Home activation via LHI pin

Applications

- Especially designed for driving high power LEDs in automotive applications
- Automotive Exterior Lighting: full LED headlamp assemblies (Low Beam, High Beam, Matrix Beam, Pixel Light)
- General purpose current/voltage controlled DC/DC buck LED driver

2 Block Diagram

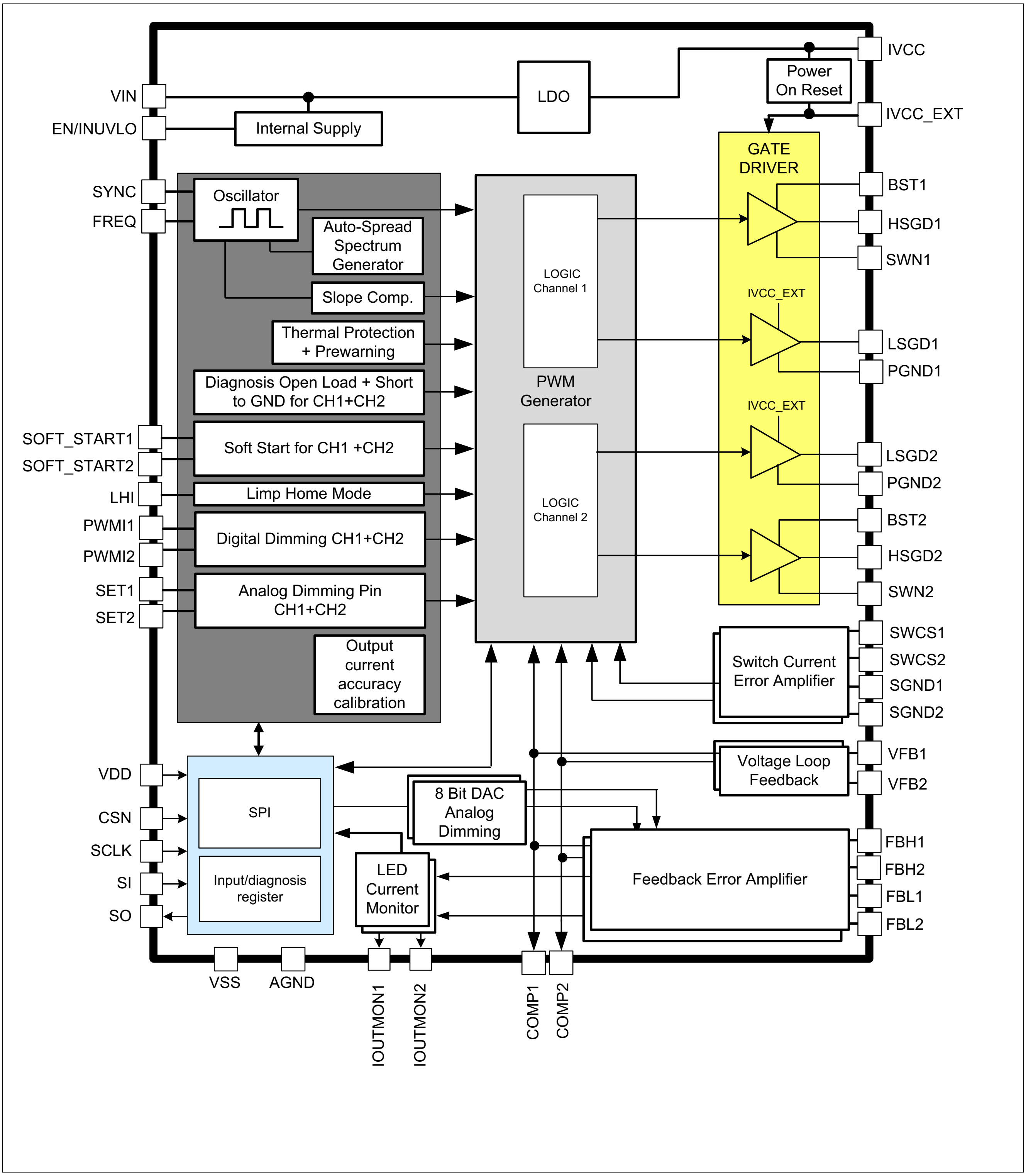


Figure 2 Block Diagram - TLD5501-2QV

3 Pin Configuration

3.1 Pin Assignment

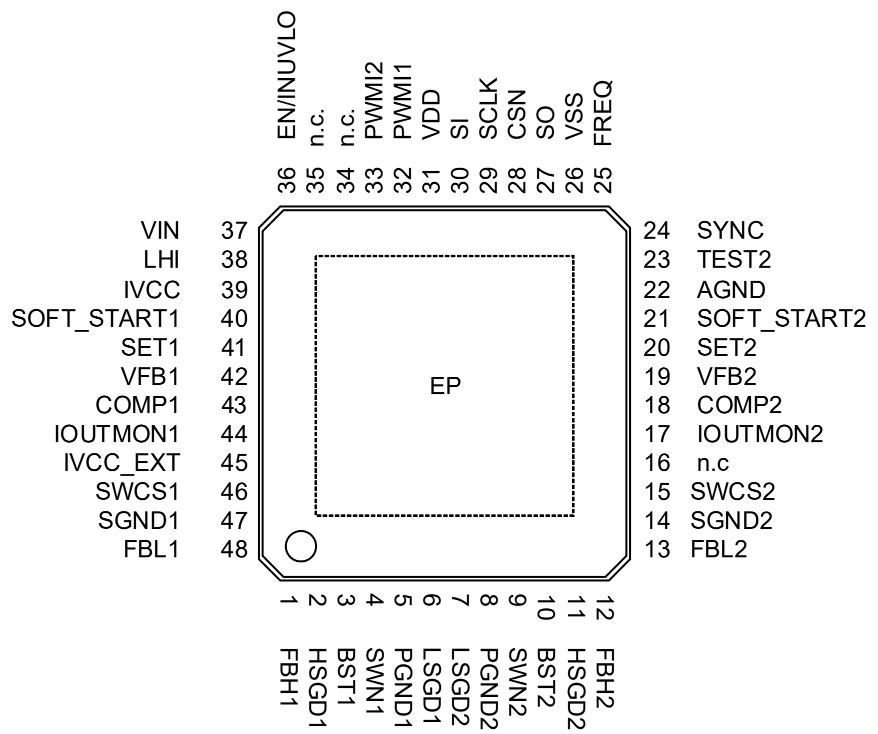


Figure 3 Pin Configuration - TLD5501-2QV

3.2 Pin Definitions and Functions

Table 2 Pin Definitions and Functions

Pin	Symbol	I/O	[1]	Function
Power Supply				
16,34, 35	n.c.	-		**Not connected** tie to AGND on the layout
37	VIN	-		**Power Supply Voltage** Supply for internal biasing
31	VDD	-		**Digital GPIO Supply Voltage** Connect to reverse voltage protected 5 V or 3.3 V supply
45	IVCC_EXT	I	PD	**External LDO input** Input to alternatively supply internal Gate Drivers via an external LDO. Connect to IVCC pin to use internal LDO to supply gate drivers. Must not be left open
5, 8	PGND1, 2	-		**Power Ground** Ground for power potential. Connect externally close to the chip
26	VSS	-		**Digital GPIO Ground** Ground for GPIO pins
22	AGND	-		**Analog Ground** Ground Reference
-	EP	-		**Exposed Pad** Connect to external heatspreading Cu area (e.g. inner GND layer of multilayer PCB with thermal vias)
Gate Driver Stages				
2	HSGD1	O		**Highside Gate Driver Output 1** Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN1. Connect to gate of external switching MOSFET
11	HSGD2	O		**Highside Gate Driver Output 2** Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN2. Connect to gate of external switching MOSFET
6	LSGD1	O		**Lowside Gate Driver Output 1** Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT}. Connect to gate of external switching MOSFET
7	LSGD2	O		**Lowside Gate Driver Output 2** Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT}. Connect to gate of external switching MOSFET
4	SWN1	IO		**Switch Node 1**
9	SWN2	IO		**Switch Node 2**
39	IVCC	O		**Internal LDO output** Used for internal biasing and gate driver supply. Bypass with external capacitor close to the pin. Pin must not be left open

Table 2 Pin Definitions and Functions

Pin	Symbol	I/O [1)]		Function
Inputs and Outputs				
38	LHI	I	PD	**Limp Home Input Pin** Used to enter in Limp Home state during Fail Safe condition.
23	TEST2	-		**Test Pin** Used for Infineon end of line test, connect to GND in application
36	EN/INUVLO	I	PD	**Enable/Input Under Voltage Lock Out** Used to put the device in a low current consumption mode, with additional capability to fix an undervoltage threshold via external components. Pin must not be left open
25	FREQ	I		**Frequency Select Input** Connect external resistor to GND to set frequency
24	SYNC	I	PD	**Synchronization Input** Apply external clock signal for synchronization
32	PWMI1	I	PD	**Control Input CH1** Digital input 5 V or 3.3 V
33	PWMI2	I	PD	**Control Input CH2** Digital input 5 V or 3.3 V
1	FBH1	I		**Output current Feedback Positive for CH1** Non inverting Input (+) CH1
12	FBH2	I		**Output current Feedback Positive for CH2** Non inverting Input (+) CH2
48	FBL1	I		**Output current Feedback Negative for CH1** Inverting Input (-) CH1
13	FBL2	I		**Output current Feedback Negative for CH2** Inverting Input (-) CH2
3	BST1	IO		**Bootstrap capacitor** Used for internal biasing and to drive the Highside Switch HSGD1. Bypass to SWN1 with external capacitor close to the pin. Pin must not be left open
10	BST2	IO		**Bootstrap capacitor** Used for internal biasing and to drive the Highside Switch HSGD2. Bypass to SWN2 with external capacitor close to the pin. Pin must not be left open
46	SWCS1	I		**Current Sense Input for CH1** Inductor current sense CH1 - Non Inverting Input (+)
15	SWCS2	I		**Current Sense Input for CH2** Inductor current sense CH2 - Non Inverting Input (+)
47	SGND1	I		**Current Sense Ground for CH1** Inductor current sense CH1 - Inverting Input (-). Route as Differential net with SWCS1 on the Layout
14	SGND2	I		**Current Sense Ground for CH2** Inductor current sense CH2 - Inverting Input (-). Route as Differential net with SWCS2 on the Layout

Table 2 Pin Definitions and Functions

Pin	Symbol	I/O	1)	Function
43	COMP1	O		**Compensation Network Pin for CH1** Connect R and C network to pin for stability phase margin adjustment for CH1
18	COMP2	O		**Compensation Network Pin for CH2** Connect R and C network to pin for stability phase margin adjustment for CH2
40	SOFT_START1	O		**Softstart configuration Pin for CH1** Connect a capacitor C_{SOFT_START1} to GND to fix a soft start ramp default time
21	SOFT_START2	O		**Softstart configuration Pin for CH2** Connect a capacitor C_{SOFT_START2} to GND to fix a soft start ramp default time
42	VFB1	I		**Voltage Feedback Pin for CH1** VFB is intended to set output protection functions for CH1
19	VFB2	I		**Voltage Feedback Pin for CH2** VFB is intended to set output protection functions for CH2
41	SET1	I		**Analog current sense adjustment Pin for CH1**
20	SET2	I		**Analog current sense adjustment Pin for CH2**
44	IOUTMON1	O	PD	**Output current monitor output 1** Monitor pin that produces a linear function of I_{OUT} as a voltage.
17	IOUTMON2	O	PD	**Output current monitor output 2** Monitor pin that produces a linear function of I_{OUT} as a voltage.
SPI				
30	SI	I	PD	**Serial data in;** Digital input 5 V or 3.3 V
29	SCLK	I	PD	**Serial clock;** Digital input 5 V or 3.3 V
28	CSN	I	PU	**SPI chip select;** Digital input 5 V or 3.3 V. Active LOW
27	SO	O		**Serial data out;** Digital output, referenced to V_{DD}

1) O: Output, I: Input,
PD: pull-down circuit integrated,
PU: pull-up circuit integrated

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings[1)]
T_J = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
VIN Supply Input	V_{VIN}	-0.3	–	60	V	–	P_4.1.1
VDD Digital supply voltage	V_{VDD}	-0.3	–	6	V	–	P_4.1.2
IVCC Internal Linear Voltage Regulator Output voltage	V_{IVCC}	-0.3	–	6	V	–	P_4.1.3
IVCC_EXT External Linear Voltage Regulator Input voltage	V_{IVCC_EXT}	-0.3	–	6	V	–	P_4.1.4
Gate Driver Stages							
LSGD1,2 - PGND1,2 Lowside Gatedriver voltage	$V_{LSGD1,2-PGND1,2}$	-0.3	–	5.5	V	–	P_4.1.54
HSGD1,2 - SWN1,2 Highside Gatedriver voltage	$V_{HSGD1,2-SWN1,2}$	-0.3	–	5.5	V	Differential signal (not referred to GND)	P_4.1.55
SWN1, SWN2 switching node voltage	$V_{SWN1,2}$	-1	–	60	V	–	P_4.1.6
(BST1-SWN1), (BST2-SWN2) Boostrap voltage	$V_{BST1,2-SWN1,2}$	-0.3	–	6	V	Differential signal (not referred to GND)	P_4.1.7
BST1, BST2 Boostrap voltage related to GND	$V_{BST1,2}$	-0.3	–	65	V	–	P_4.1.8
SWCS1,2 Switch Current Sense Input voltages	$V_{SWCS1,2}$	-0.3	–	0.3	V	–	P_4.1.42
SGND1,2 Switch Current Sense GND voltages	$V_{SGND1,2}$	-0.3	–	0.3	V	–	P_4.1.43
SWCS1,2-SGND1,2 Switch Current Sense differential voltages	$V_{SWCS1,2-SGND1,2}$	-0.5	–	0.5	V	–	P_4.1.44
PGND1,2 Power GND voltage	$V_{PGND1,2}$	-0.3	–	0.3	V	–	P_4.1.28

Table 3 Absolute Maximum Ratings[1] (cont'd)
T_J = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High voltage Pins							
FBH1,2; FBL1,2 Feedback Error Amplifier voltages	$V_{FBH1,2; FBL1,2}$	-0.3	–	60	V	–	P_4.1.45
FBH1,2-FBL1,2 Feedback Error Amplifier differential voltages	$V_{FBH1,2-FBL1,2}$	-0.5	–	0.5	V	Differential signal (not referred to GND)	P_4.1.47
EN/INUVLO Device enable/input undervoltage lockout	$V_{EN/INUVLO}$	-0.3	–	60	V	–	P_4.1.16
Digital (I/O) Pins							
PWMI1,2 Digital Input voltages	$V_{PWMI1,2}$	-0.3	–	5.5	V	–	P_4.1.49
CSN Voltage at Chip Select pin	V_{CSN}	-0.3	–	5.5	V	–	P_4.1.18
SCLK Voltage at Serial Clock pin	V_{SCLK}	-0.3	–	5.5	V	–	P_4.1.19
SI Voltage at Serial Input pin	V_{SI}	-0.3	–	5.5	V	–	P_4.1.20
SO Voltage at Serial Output pin	V_{SO}	-0.3	–	5.5	V	–	P_4.1.21
SYNC Synchronization Input voltage	V_{SYNC}	-0.3	–	5.5	V	–	P_4.1.22
LHI Limp Home Input Voltage	V_{LHI}	-0.3	–	5.5	V	–	P_4.1.58
LHI Limp Home Input Current	I_{LHI}	-5	–	–	mA	–	P_4.1.60
Analog Pins							
VFB1,2 Loop Input voltages	$V_{VFB1,2}$	-0.3	–	5.5	V	–	P_4.1.50
SET1,2 Analog dimming Input voltage	$V_{SET1,2}$	-0.3	–	5.5	V	–	P_4.1.56
COMP1,2 Compensation Input voltages	$V_{COMP1,2}$	-0.3	–	3.6	V	–	P_4.1.52
SOFT_START1,2 Softstart Voltages	$V_{SOFT\_START1,2}$	-0.3	–	3.6	V	–	P_4.1.53
FREQ Voltage at frequency selection pin	V_{FREQ}	-0.3	–	3.6	V	–	P_4.1.32
IOUTMON1,2 Voltages at output monitor pins	$V_{IOUTMON1,2}$	-0.3	–	5.5	V	–	P_4.1.59

Table 3 Absolute Maximum Ratings[1] (cont'd)
T_J = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.35
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.36
ESD Susceptibility							
ESD Resistivity of all Pins	$V_{ESD,HBM}$	-2	–	2	kV	HBM[2]	P_4.1.37
ESD Resistivity to GND	$V_{ESD,CDM}$	-500	–	500	V	CDM[3]	P_4.1.38
ESD Resistivity of corner Pins to GND	V_{ESD,CDM_corner}	-750	–	750	V	CDM[3]	P_4.1.39

1) Not subject to production test, specified by design.
2) ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002
3) ESD susceptibility, Charged Device Model "CDM" AECQ100-011

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 4 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Device Extended Supply Voltage Range	V_{VIN}	4.5	–	40	V	[1] (parameter deviations possible)	P_4.2.1
Device Nominal Supply Voltage Range	V_{VIN}	8	–	36	V	–	P_4.2.2
Power Stage Voltage Range	V_{POW}	4.5	–	55	V	[1]	P_4.2.5
Digital Supply Voltage	V_{DD}	3	–	5.5	V	–	P_4.2.3
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org***.

Table 5

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	0.9	–	K/W	[1] [2]	P_4.3.1
Junction to Ambient	R_{thJA}	–	25	–	K/W	[1] [3] 2s2p	P_4.3.2

1) Not subject to production test, specified by design.

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). Ta = 25°C; The IC is dissipating 1 W.

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layers (2 x 35 µm Cu). A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. Ta = 25°C; The IC is dissipating 1 W.

5 Power Supply

The TLD5501-2QV is supplied by the following pins:

- VIN (main supply voltage)
- VDD (digital supply voltage)
- IVCC_EXT (supply for internal gate driver stages)

The VIN supply, in combination with the VDD supply, provides internal supply voltages for the analog and digital blocks. In situations where VIN voltage drops below VDD voltage, an increased current consumption may be observed at the VDD pin.

The SPI and IO interfaces are supplied by the VDD pin.

IVCC_EXT is the supply for the low side driver stages. This supply is used also to charge, through external Schottky diodes, the bootstrap capacitors which provide supply voltages to the high side driver stages. If no external voltage is available this pin must be shorted to IVCC, which is the output of an internal 5 V LDO.

The supply pins VIN, VDD and IVCC_EXT have undervoltage detections.

Undervoltage on VDD supply voltage prevents the activation of the gate driver stages and any SPI communication (the SPI registers are reset). Undervoltage on IVCC_EXT or IVCC voltages forces a deactivation of the driver stages, thus stopping the switching activity, but has no effect on the SPI register settings.

Moreover the double function pin EN/INUVLO can be used as an input undervoltage protection by placing a resistor divider from VIN to GND .

If EN/INUVLO undervoltage is detected, it will turn-off the IVCC voltage regulator, stop switching, stop communications and reset all the registers.

Figure 4 shows a basic concept drawing of the supply domains and interactions among pins VIN, VDD and IVCC/IVCC_EXT.

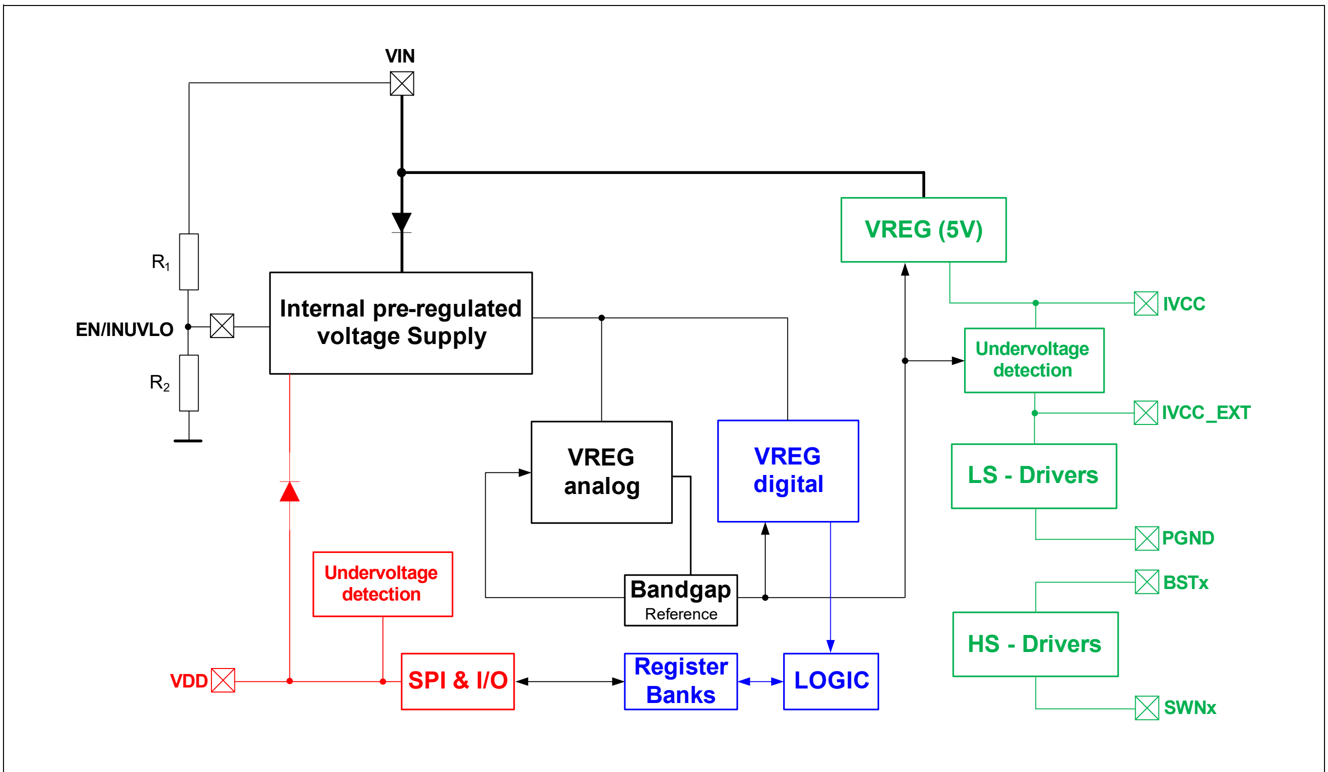


Figure 4 Power Supply Concept Drawing

Usage of EN/INUVLO pin in different applications

The pin EN/INUVLO is a double function pin and can be used to put the device into a low current consumption mode. An undervoltage threshold is fixed by placing an external resistor divider (A) in order to avoid low voltage operating conditions. This pin can be driven by a µC-port as shown in (B) (C).

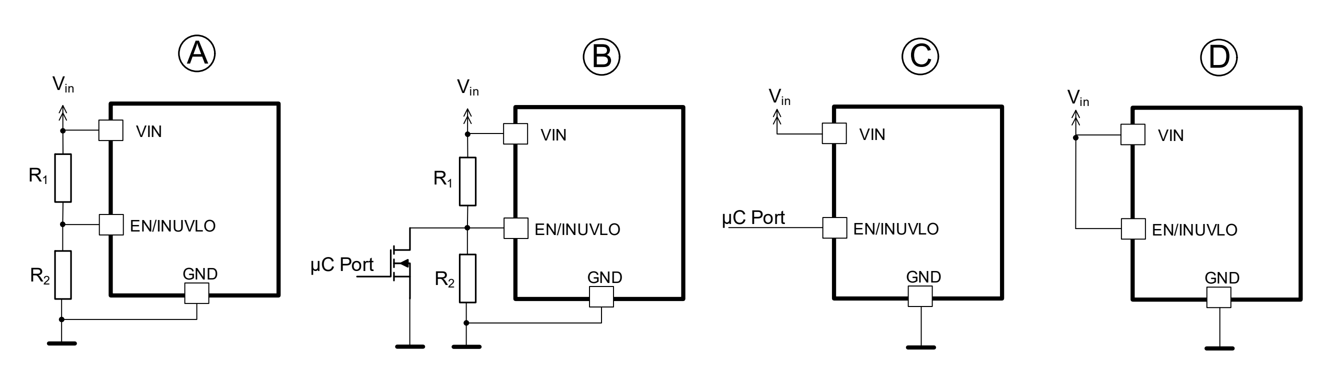


Figure 5 Usage of EN/INUVLO pin in different applications

5.1 Different Power States

TLD5501-2QV has the following power states:

- SLEEP state
- IDLE state
- LIMP HOME state
- ACTIVE state

The transition between the power states is determined according to these variables after a filter time of max. 3 clock cycles:

- VIN level
- EN/INUVLO level
- IVCC level
- IVCC_EXT level
- VDD level
- LHI level
- `DVCCTRL.IDLE` bit state

The state diagram including the possible transitions is shown in **Figure 6**.

The Power-up condition is entered when the supply voltage V_{VIN} exceed its minimum supply voltage threshold $V_{VIN(ON)}$.

SLEEP

When the device is powered it enters the SLEEP state, all outputs are OFF and the SPI registers are reset, independently from the supply voltages at the pins VIN , VDD, IVCC, and IVCC_EXT. The current consumption is low. Refer to parameters: $I_{VDD(SLEEP)}$, and $I_{VIN(SLEEP)}$.

The transition from SLEEP to ACTIVE state requires a specified time: t_{ACTIVE}.

IDLE

In IDLE state, the current consumption of the device can reach the limits given by parameter I_{VDD} (P_5.3.4). The internal voltage regulator is working. Not all diagnosis functions are available (refer to **Chapter 10** for additional informations). In this state there is no switching activity, independently from the supply voltages V_{IN}, V_{DD}, IVCC and IVCC_EXT. When V_{DD} is available, the SPI registers are working and SPI communication is possible.

Limp Home

The Limp Home state is beneficial to fulfill system safety requirements and provides the possibility to maintain a defined current/voltage level on the output via a backup control circuitry. The backup control circuitry turns on required loads during a malfunction of the µC. For detailed info, refer to **Chapter 8**.

When Limp Home state is entered, SPI registers are reset to their default values. In order to regulate the output current/voltage, it is necessary that V_{IN} and IVCC_EXT are present and above their undervoltage threshold. If also VDD is above its undervoltage threshold, SPI communication is possible but only in read mode.

ACTIVE

In active state the device will start switching activity to provide power at the output only when PWMI1,2 = HIGH or `LOOPCTRL_CH1,2.PWM_1,2` = HIGH. To start the Highside gate drivers HSGD1,2 the voltage level $V_{BST1,2}$ - $V_{SWN1,2}$ needs to be above the threshold $V_{BST1,2}$ - $V_{SWN1,2\_UVth}$. In order to recharge the bootstrap capacitor, sporadic switching activity could also be observed when PWMI1,2 = LOW and LOOPCTRL_CH1,2.PWM_1,2 =

LOW. In ACTIVE state the device current consumption via V_{IN} and V_{DD} is dependent on the external MOSFET used and the switching frequency f_{SW}.

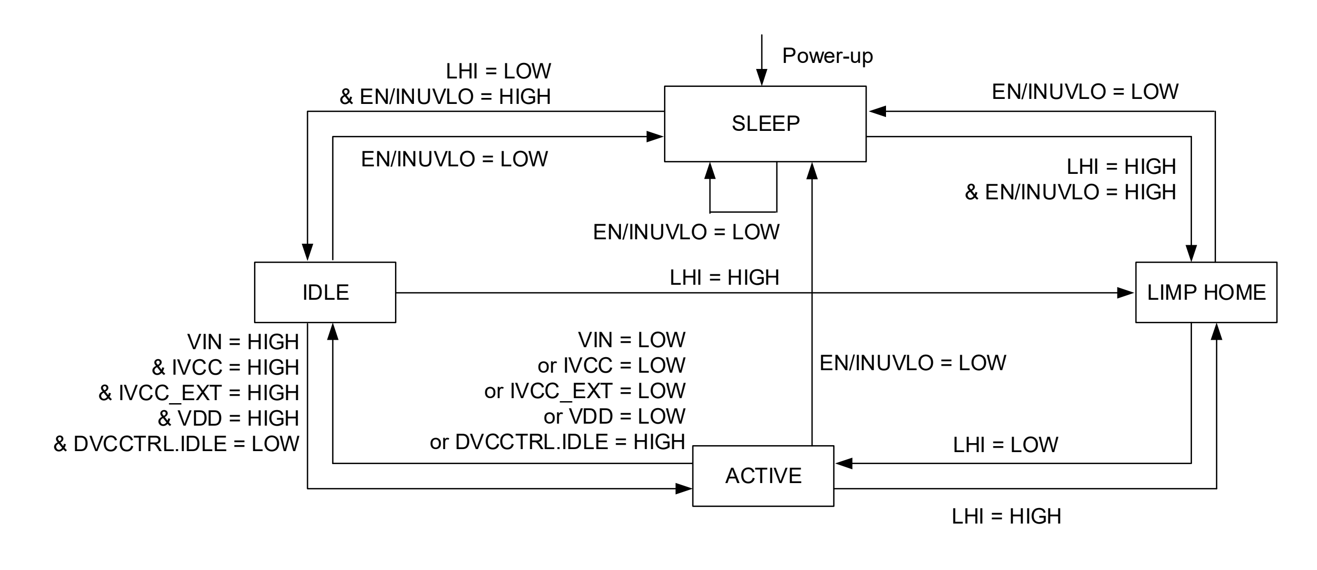


Figure 6 Simplified State Diagram

5.2 Different Possibilities to RESET the device

There are several reset triggers implemented in the device.

After any kind of reset, the Transmission Error Flag (`TER`) is set to HIGH.

Under Voltage Reset:

EN/INUVLO: When EN/INUVLO is below $V_{EN/INUVLOth}$ (P_5.3.7), the SPI interface is not working and all the registers are reset to their default values. In addition, the device enters SLEEP mode and the current consumption is minimized.

VDD: When V_{VDD} is below $V_{VDD(UV)}$ (P_5.3.6), the SPI interface is not working and all the registers are reset to their default values.

Reset via SPI command:

There is a command (`DVCCTRL.SWRST` = HIGH) available to RESET all writeable registers to their default values. Note that the result coming from the Calibration routine, which is readable by the SPI when `LOOPCTRL_CH1,2.ENCAL_CH1,2` = HIGH, is not reset by the SWRST.

Reset via Limp Home:

When Limp Home state is detected the registers are reset to the default values.

5.3 Electrical Characteristics

Table 6 EC Power Supply

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply V_{IN}							
Input Voltage Startup	$V_{VIN(ON)}$	–	–	4.7	V	V_{IN} increasing; $V_{EN/INUVLO}$ = HIGH; V_{DD} = 5 V; IVCC = IVCC_EXT = 10 mA	P_5.3.1
Input Undervoltage switch OFF	$V_{VIN(OFF)}$	–	–	4.5	V	V_{IN} decreasing; $V_{EN/INUVLO}$ = HIGH; V_{DD} = 5 V; IVCC = IVCC_EXT = 10 mA	P_5.3.14
Device operating current	$I_{VIN(ACTIVE)}$	–	6.2	9	mA	[1]ACTIVE mode; $V_{PWMI1,2}$ = 0 V	P_5.3.2
V_{IN} Sleep mode supply current	$I_{VIN(SLEEP)}$	–	–	1.5	µA	$V_{EN/INUVLO}$ = 0 V; V_{CSN} = V_{DD} = 5 V; V_{IN} = 13.5 V; V_{IVCC} = V_{IVCC_EXT}= 0 V	P_5.3.3
Digital Power Supply V_{DD}							
Digital supply current	I_{VDD}	–	–	0.5	mA	V_{IN} = 13.5 V; f_{SCLK} = 0 Hz; $V_{PWMI1,2}$ = 0 V; V_{EN} =V_{CSN} = V_{DD} = 5 V	P_5.3.4
Digital Supply Sleep mode current	$I_{VDD(SLEEP)}$	–	–	1.5	µA	$V_{EN/INUVLO}$ = 0 V; V_{CSN} = V_{DD} = 5 V; V_{IN} = 13.5 V; V_{IVCC} = V_{IVCC_EXT} = 0 V	P_5.3.5
Undervoltage shutdown threshold voltage	$V_{VDD(UV)}$	1	–	3	V	V_{CSN} = V_{DD}; V_{SI} = V_{SCLK} = 0 V; SO from LOW to HIGH impedance	P_5.3.6
EN/INUVLO Pin characteristics							
Input Undervoltage falling Threshold	$V_{EN/INUVLOth}$	1.64	1.75	1.86	V	–	P_5.3.7
EN/INUVLO Rising Hysteresis	$V_{EN/INUVLO(hyst)}$	–	90	–	mV	[1]	P_5.3.8
EN/INUVLO input Current LOW	$I_{EN/INUVLO(LOW)}$	0.45	0.89	1.34	µA	$V_{EN/INUVLO}$ = 0.8 V	P_5.3.9
EN/INUVLO input Current HIGH	$I_{EN/INUVLO(HIGH)}$	1.1	2.2	3.3	µA	$V_{EN/INUVLO}$ = 2 V	P_5.3.10

Table 6 EC Power Supply (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
LHI Pin characteristics							
LOW level	$V_{LHI(L)}$	0	-	0.8	V	–	P_5.3.16
HIGH level	$V_{LHI(H)}$	2.0	-	5.5	V	–	P_5.3.17
L-Input pull-down current	$I_{LHI(L)}$	6	12	18	µA	V_{LHI} = 0.8 V	P_5.3.18
H-Input pull-down current	$I_{LHI(H)}$	15	30	45	µA	V_{LHI} = 2.0 V	P_5.3.19
Timings							
SLEEP mode to ACTIVE time	t_{ACTIVE}	–	–	0.7	ms	[1] $V_{IVCC} = V_{IVCC\_EXT}$; C_{IVCC} = 10 µF; V_{IN} = 13.5 V; V_{DD} = 5 V	P_5.3.11

1) Not subject to production test, specified by design

6 Regulator Description

The TLD5501-2QV includes all of the functions necessary to provide constant current to the output as usually required to drive LEDs. A voltage mode regulation can also be implemented (Refer to **Chapter 6.5**).

In deep buck applications, due to duty cycle limitations (D_{BUCK_MIN}) the device will enter pulse skipping mode in order to keep regulating the average output current, the ouptut ripple may increase.

The minimum duty cycle is dependent by the f_{sw}.

6.1 Regulator Diagram Description

An analog current control loop (A5, A4 with complessive gain = $IFBx_{gm}$) connected to the sensing pins FBL1,2, FBH1,2 regulates the output current.

The regulator function is implemented by a pulse width modulated (PWM) current mode controller. The error in the output current loop is used to determine the appropriate duty cycle to get a constant output current.

An external compensation network (R_{COMP}, C_{COMP}) is used to adjust the control loop to various application boundary conditions.

The inductor current for the current mode loop is sensed by the R_{SWCS} resistor.

R_{SWCS} is used also to limit the maximum external switches / inductor current.

If the Voltage across R_{SWCS} exceeds its overcurrent threshold ($V_{SWCS1,2\_buck}$) the device reduces the duty cycle in order to bring the switches current below the imposed limit.

The current mode controller has a built-in slope compensation as well to prevent sub-harmonic oscillations.

The control loop logic block (LOGIC_CHx) provides a PWM signal to two internal gate drivers. The gate drivers (HSGD1,2 and LSGD1,2) are used to drive external MOSFETs. Once $V_{SOFT\_START1,2}$ exceeds $V_{Soft\_start1,2\_LOFF}$ or $V_{(FBH1,2\text{-}FBL1,2)}$ exceeds $V_{(FBH1,2\text{-}FBL1,2)\_VALID}$ thresholds, TLD5501-2QV forces CCM regulation mode.

The control loop block diagram displayed in **Figure 7** shows a typical constant current application. The voltage across R_{FB} sets the output current.

The output current is fixed via the SPI parameter (`LEDCURRADIM_CH1,2.ADIMVAL_CH1,2` = 11110000_B = default at 100%) plus an offset trimming (`LEDCURRCAL_CH1,2.CALIBVAL_CH1,2` = 0000_B = default in the middle of the range). Refer to **Chapter 8.1** for more details.

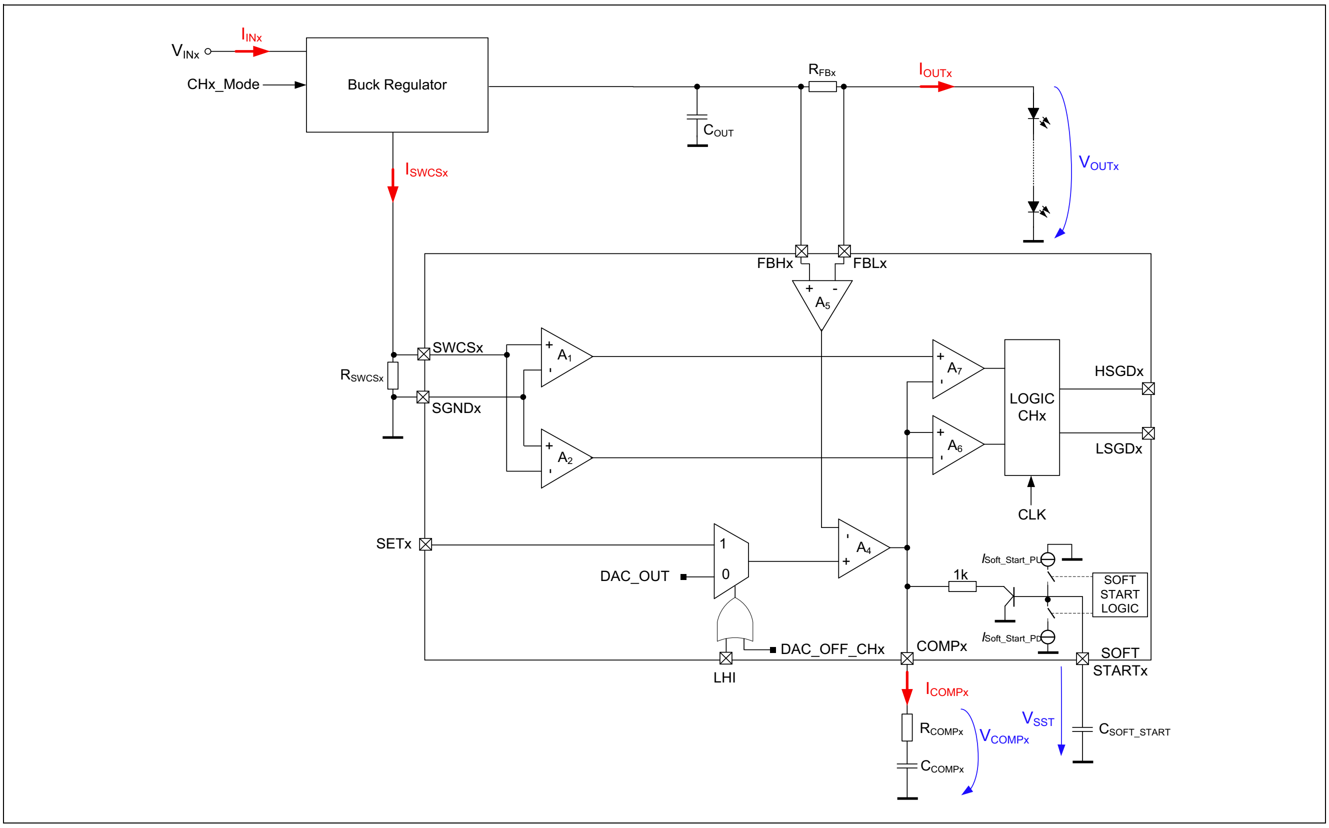


Figure 7 Regulator Block Diagram (similar for both Channels) - TLD5501-2QV

6.2 Adjustable Soft Start Ramp

The soft start routine has two functionalities:

- Fault management: fault mask and wait-before-retry time, on rising and falling edge of SOFT_START1,2 respectively (**Figure 8** and **Chapter 10.2**)
- To limit the current through the inductor and the external MOSFET switches during initialization to minimize potential overshoots at the output.

The soft start routine is applied:

- At startup (first PWM rise after IDLE to ACTIVE transition)
- After Output Short to GND detection
- After channel stop via low analog dimming value (See **Chapter 8**)

The soft start timing is defined by a capacitor placed at the SOFT_START pin and the pull-up and pull-down current sources ($I_{Soft\_Start1,2\_PU}$, $I_{Soft\_Start1,2\_PD}$).

Minimum value for soft start capacitor has to be designed such that, at startup, the output voltage exceeds the short to ground threshold before the soft start voltage reaches $V_{SOFT\_START1,2\_LOFF}$. Minimum temperature and minimum input voltage shall be considered as worst case condition for previously mentioned dimensioning.

Soft Start rising edge time is approximately:

$$t_{SOFT\_START1,2} = V_{Soft\_Start1,2\_LOFF} \cdot \frac{C_{Soft\_Start1,2}}{I_{Soft\_Start1,2\_PU}} \tag{6.1}$$

The Soft Start routine limits the inrush current by clamping the COMP pin through a buffer as in **Figure 7**. Therefore, this functionality is effective only when soft start capacitor is sufficiently larger than the COMP capacitor.

If a short on the output is detected, a pull-down current source $I_{SOFT\_START1,2\_PD}$ (P_6.4.59) is activated. This current brings down the $V_{SOFT\_START1,2}$ until $V_{SOFT\_START1,2\_RESET}$ (P_6.4.61) is reached, then the pull-up current source $I_{SOFT\_START1,2\_PU}$ (P_6.4.58) turns on again, if PWMI1,2 is high, see **Figure 8**. If the fault condition hasn't been removed until $V_{SOFT\_START1,2\_LOFF}$ (P_6.4.60) is reached, the pull-down current source turns back on again, initiating a new cycle. This will continue until the fault is removed.

During rising edge of soft start, the internal PWM is extended until one of the 2 following conditions is reached:

- Until $V_{SOFT\_START1,2}$ exceeds $V_{Soft\_Start1,2\_LOFF}$ (P_6.4.60)
- Until $V_{FBH1,2\text{-}FBL1,2}$ exceeds $V_{(FBH1,2\text{-}FBL1,2)\_VALID}$ (P_6.6.1)

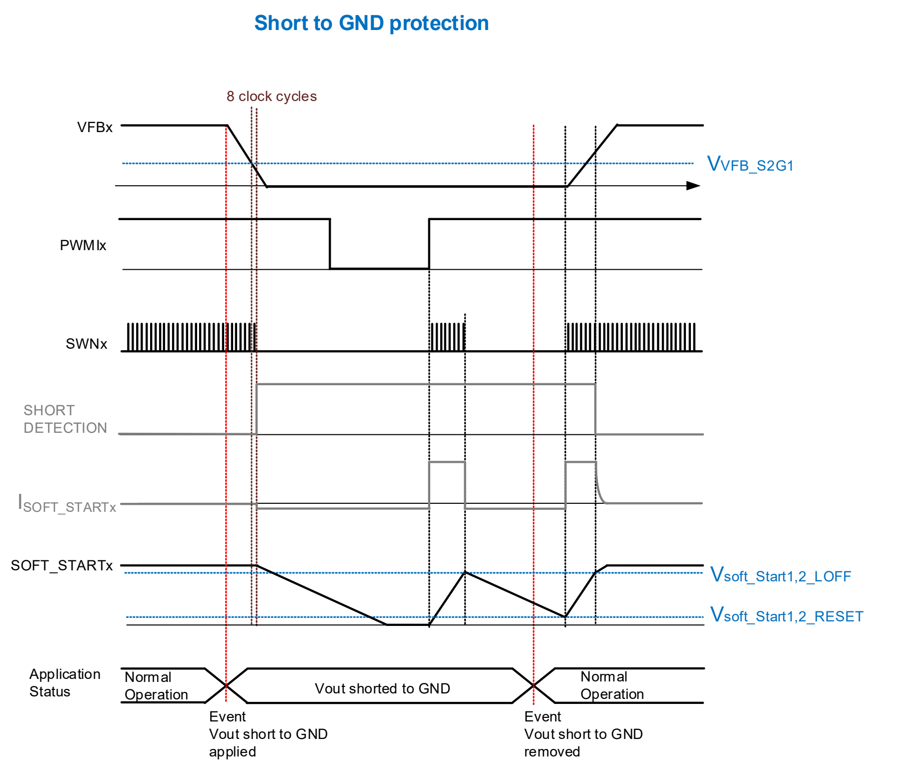


Figure 8 Soft Start timing diagram on a short to ground detected by the VFBx pin

6.3 Switching Frequency setup

The switching frequency can be set from 200 kHz to 700 kHz by an external resistor connected from the FREQ pin to GND or by supplying a sync signal as specified in chapter **Chapter 11.2**. Select the switching frequency with an external resistor according to the graph in **Figure 9** or the following approximate formulas.

$$f_{SW}\,[kHz] = 5375\ *\,(R_{FREQ}\,[k\Omega])^{-0.8} \tag{6.2}$$

$$R_{FREQ}[k\Omega] = 46023 * (f_{SW}[kHz])^{-1.25} \tag{6.3}$$

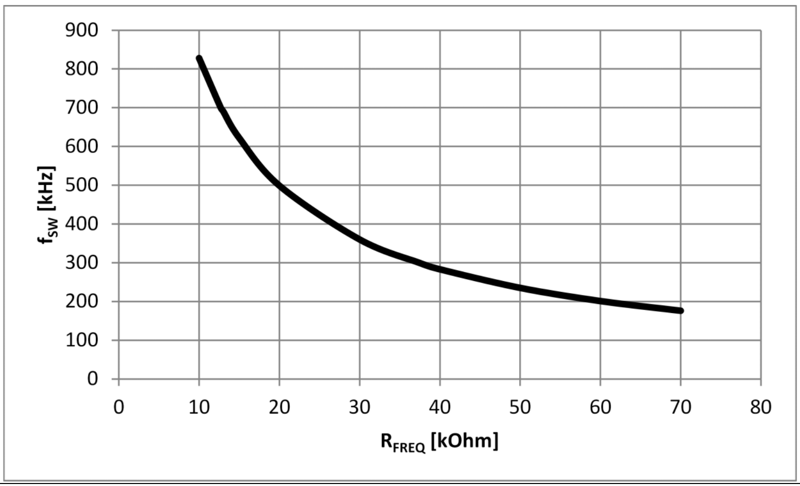


Figure 9 Switching Frequency f_{SW} versus Frequency Select Resistor to GND R_{FREQ}

6.4 Flexible current sense

The flexible current sense implementation enables highside and lowside current sensing.

The **Figure 10** displays the application examples for the highside and lowside current sense concept.

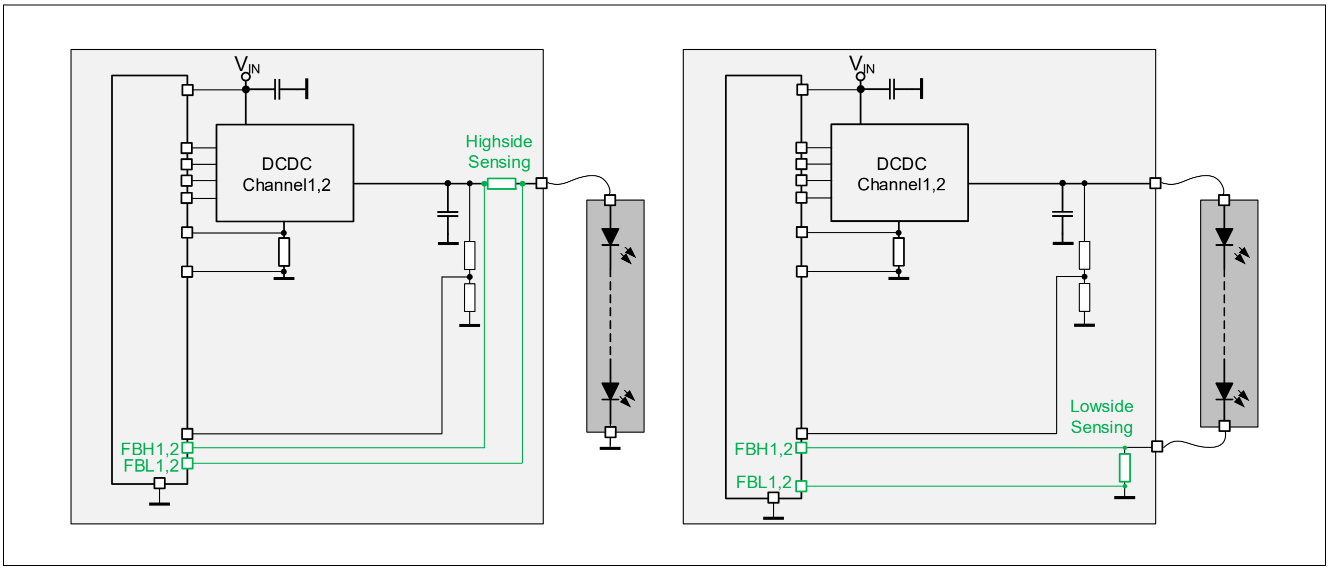


Figure 10 Highside and lowside current sensing - TLD5501-2QV

6.5 Programming Output Voltage (Constant Voltage Regulation)

For a voltage regulator, the output voltage can be set by selecting the values R_{FBx1}, R_{FBx2} and R_{FBx3} according to the following **Equation (6.4)**:

$$V_{OUT1,2} = \left(I_{FBH1,2} + \frac{V_{FBH1,2-FBL1,2}}{R_{FB21,2}} \right) \cdot R_{FB11,2} + \left(\frac{V_{FBH1,2-FBL1,2}}{R_{FB21,2}} - I_{FBL1,2} \right) \cdot R_{FB31,2} + V_{FBH1,2-FBL1,2} \tag{6.4}$$

After the output voltage is fixed via the resistor divider, the value can be changed via the Analog Dimming bits `ADIMVAL_CH1,2`.

If Analog dimming is performed, due to the variations on the I_{FBL} ($I_{FBL1,2\_HSS}$ (P_6.4.52) and $I_{FBL1,2\_LSS}$ (P_6.4.54)) or I_{FBH} ($I_{FBH1,2\_HSS}$ (P_6.4.51) and $I_{FBH1,2\_LSS}$ (P_6.4.53)) current on the entire voltage spanning, a non linearity on the output voltage may be observed. To minimize this effect RFBx resistors should be properly dimensioned.

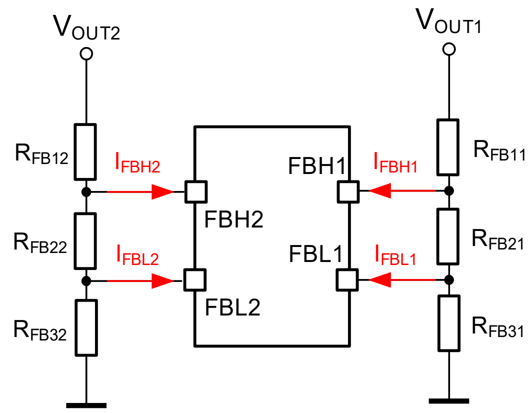


Figure 11 Programming Output Voltage (Constant Voltage Regulation)

*Note: In case of no load condition, if the voltage on the output is above $V_{(FBH1,2-FBL1,2)\_VALID}$ threshold, the output capacitor may be discharged during the soft-start sequence. Proper sizing of external components (e.g. increasing the output capacitor or decreasing the inductor values) is recommended to avoid negative output voltage. Alternatively it is recommended to add a clamping diode on the output as shown in **Figure 38**.*

6.6 Electrical Characteristics

Table 7 EC Regulator

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Regulator:							
$V_{(FBH1,2-FBL1,2)}$ thresholds	$V_{(FBH1,2-FBL1,2)}$	145.5	150	154.5	mV	ADIM.ADIMVAL_CH1,2 = *11110000*$_B$; Differential signal (not referred to GND	P_6.4.43
$V_{(FBH1,2-FBL1,2)}$ thresholds @ analog dimming 10%	$V_{(FBH1,2-FBL1,2)\_10}$	12	15	18	mV	ADIM.ADIMVAL_CH1,2 = *00011000*$_B$; Differential signal (not referred to GND) Calibration Procedure not performed	P_6.4.47
V(FBH-FBL) valid range threshold	$V_{(FBH1,2-FBL1,2)\_VALID}$	110	120	130	mV	V_{SET} = 1.4 V or ADIM.ADIMVAL_CH1,2 = 11110000$_B$	P_6.6.1
FBH1,2 Bias currents @ highside sensing setup	$I_{FBH1,2\_HSS}$	65	100	156	µA	$V_{FBL1,2}$ = 7 V; $V_{FBH1,2-FBL1,2}$ = 150 mV	P_6.4.51
FBL1,2 Bias currents @ highside sensing setup	$I_{FBL1,2\_HSS}$	17	30	45	µA	$V_{FBL1,2}$ = 7 V; $V_{FBH1,2-FBL1,2}$ = 150 mV	P_6.4.52
FBH1,2 Bias currents @ lowside sensing setup	$I_{FBH1,2\_LSS}$	-7.5	-4	-2.5	µA	$V_{FBL1,2}$ = 0 V; $V_{FBH1,2-FBL1,2}$ = 150 mV	P_6.4.53
FBL1,2 Bias currents @ lowside sensing setup	$I_{FBL1,2\_LSS}$	-45	-30	-20	µA	$V_{FBL1,2}$ = 0 V; $V_{FBH1,2-FBL1,2}$ = 150 mV	P_6.4.54
FBH-FBL High Side sensing entry threshold	$V_{FBH\_HSS\_inc}$	1.9	2	2.1	V	[1] $V_{FBH1,2}$ increasing	P_6.9.1
FBH-FBL High Side sensing exit threshold	$V_{FBH\_HSS\_dec}$	1.65	1.75	1.85	V	[1] $V_{FBH1,2}$ decreasing	P_6.9.2
OUT Current sense Amplifier g_m	$IFBx_{gm}$	–	890	–	µS	[1]	P_6.4.10
Output Monitor Voltages	$V_{IOUTMON1,2}$	1.33	1.4	1.47	V	$V_{FBH1,2-FBL1,2}$ = 150 mV	P_6.5.1
Minimum BUCK Duty Cycle	D_{BUCK_MIN}	–	4	5.5	%	[1] f_{sw} = 300 kHz	P_6.8.2
Maximum BUCK Duty Cycle	D_{BUCK_MAX}	90.5	92	94	%	[1] f_{sw} = 300 kHz	P_6.5.2
Switch Peak Over Current Thresholds - BUCK	$V_{SWCS1,2\_buck}$	-60	-50	-40	mV	[1]	P_10.8.25
Soft Start							
Soft Start1,2 pull up currents	$I_{Soft\_Start1,2\_PU}$	21	27	34	µA	$V_{Soft\_Start1,2}$ = 1 V	P_6.4.58

Table 7 EC Regulator (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Soft Start1,2 pull down currents	$I_{Soft\_Start1,2\_PD}$	2.1	2.7	3.4	µA	$V_{Soft\_Start1,2}$ = 1 V	P_6.4.59
Soft Start1,2 Latch-OFF Thresholds	$V_{Soft\_Start1,2\_LOFF}$	1.65	1.75	1.85	V	–	P_6.4.60
Soft Start1,2 Reset Thresholds	$V_{Soft\_Start1,2\_RESET}$	0.1	0.2	0.3	V	–	P_6.4.61
Soft Start1,2 Voltage during regulation	$V_{Soft\_Start1,2\_reg}$	1.9	2	2.1	V	[1]No Faults	P_6.9.3
Oscillator							
Switching Frequency	f_{SW}	285	300	315	kHz	T_j = 25°C; R_{FREQ}= 37.4 kΩ; ENSPREAD = LOW	P_6.4.23
SYNC Frequency	f_{SYNC}	200	–	700	kHz	–	P_6.4.24
SYNC Turn On Threshold	$V_{SYNC,ON}$	2	–	–	V	–	P_6.4.25
SYNC Turn Off Threshold	$V_{SYNC,OFF}$	–	–	0.8	V	–	P_6.4.26
SYNC High Input Current	$I_{SYNC,H}$	15	30	45	µA	V_{SYNC} = 2.0 V;	P_6.4.62
SYNC Low Input Current	$I_{SYNC,L}$	6	12	18	µA	V_{SYNC} = 0.8 V;	P_6.4.63
Gate Driver for external Switch							
Gate Driver undervoltage threshold VBST1,2-VSWN1,2_UVth	$V_{BST1,2}$-$V_{SWN1,2\_UVth}$	3.4	–	4	V	$V_{BST1,2}$ - $V_{SWN1,2}$ decreasing; Differential signal (not referred to GND)	P_6.4.64
HSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{DS(ON\_PU)HS}$	1.4	2.3	3.7	Ω	$V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V; I_{source} = 100 mA	P_6.4.28
HSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{DS(ON\_PD)HS}$	0.6	1.2	2.2	Ω	$V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V; I_{sink} = 100 mA	P_6.4.29
LSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{DS(ON\_PU)LS}$	1.4	2.3	3.7	Ω	V_{IVCC_EXT} = 5 V; I_{source} = 100 mA	P_6.4.30
LSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{DS(ON\_PD)LS}$	0.4	1.2	1.8	Ω	V_{IVCC_EXT} = 5 V; I_{sink} = 100 mA	P_6.4.31

Table 7 **EC Regulator** (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
HSGD1,2 Gate Driver peak sourcing current	$I_{HSGD1,2\_SRC}$	380	–	–	mA	[1] $V_{HSGD1,2} - V_{SWN1,2}$ = 1 V to 4 V; $V_{BST1,2} - V_{SWN1,2}$ = 5 V	P_6.4.32
HSGD1,2 Gate Driver peak sinking current	$I_{HSGD1,2\_SNK}$	410	–	–	mA	[1] $V_{HSGD1,2} - V_{SWN1,2}$ = 4 V to 1 V; $V_{BST1,2} - V_{SWN1,2}$ = 5 V	P_6.4.33
LSGD1,2 Gate Driver peak sourcing current	$I_{LSGD1,2\_SRC}$	370	–	–	mA	[1] $V_{LSGD1,2}$ = 1 V to 4 V; V_{IVCC_EXT} = 5 V	P_6.4.34
LSGD1,2 Gate Driver peak sinking current	$I_{LSGD1,2\_SNK}$	550	–	–	mA	[1] $V_{LSGD1,2}$ = 4 V to 1 V; V_{IVCC_EXT} = 5 V	P_6.4.35
LSGD1,2 OFF to HSGD1,2 ON delay	$t_{LSOFF\text{-}HSON\_delay}$	15	30	40	ns	[1]	P_6.4.36
HSGD1,2 OFF to LSGD1,2 ON delay	$t_{HSOFF\text{-}LSON\_delay}$	35	65	95	ns	[1]	P_6.4.37

1) Not subject to production test, specified by design

7 Digital Dimming Function

PWM dimming is adopted to vary LEDs brightness with greatly reduced chromaticity shift. PWM dimming achieves brightness reduction by varying the duty cycle of a constant current in the LED string.

7.1 Description

A PWM signal can be transmitted to the TLD5501-2QV in two manners, as described below.

An HIGH PWM value, communicated in either of the two ways, always overrides a possible LOW from the other with a resulting enable of the gate drivers.

PWM via direct interface

The PWMI1,2 pin can be fed with a pulse width modulated (PWM) signals, this enables when HIGH and disables when LOW the gate drivers of the main switches.

PWM via SPI

A pulse width modulated (PWM) signal can be sent via SPI interface by changing the value of the LOOPCTRL_CH1,2.PWM_1,2 bit.
LOOPCTRL_CH1,2.PWM_1,2=HIGH/LOW respectively enables/disables the gate drivers of the main switches.

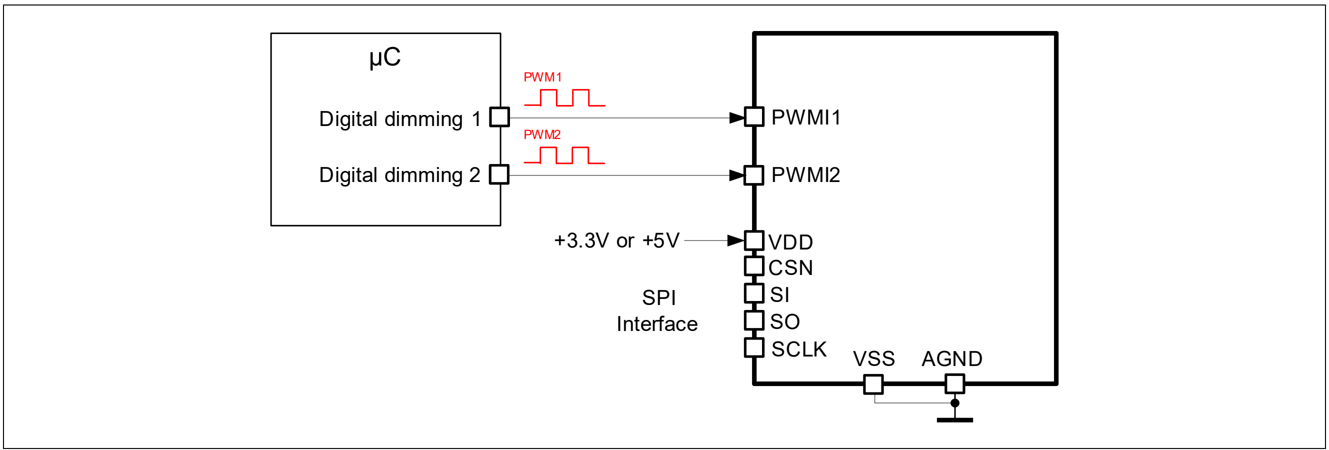


Figure 12 Digital Dimming Overview

To avoid unwanted output overshoots due to not soft start assisted startups, PWM dimming in LOW state should not be used to suspend the output current for long time intervals. To stop a single channel in a safe manner see **Chapter 8**. To stop both channels DVCCTRL.IDLE=HIGH or EN/INUVLO=LOW can be used.

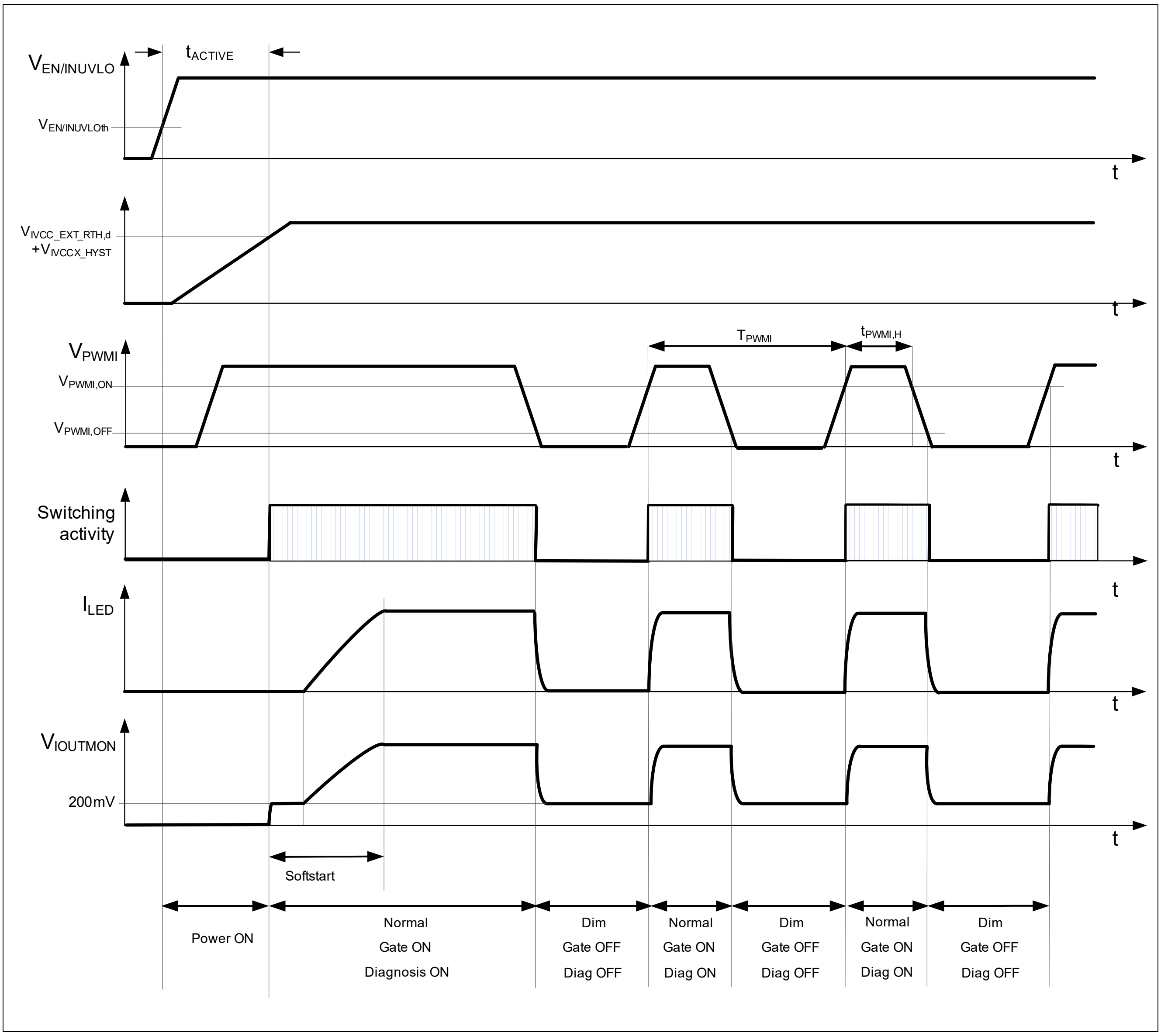


Figure 13 Timing Diagram LED Dimming and Start up behavior example (V_{VDD} and V_{VIN} stable in the functional range and not during startup)

7.2 Electrical Characteristics

Table 8 EC Digital Dimming

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMI Input:							
PWMI1,2 Turn On Thresholds	$V_{PWMI1,2,ON}$	2	–	–	V	–	P_7.2.6
PWMI1,2 Turn Off Thresholds	$V_{PWMI1,2,OFF}$	–	–	0.8	V	–	P_7.2.7
PWMI1,2 High Input Currents	$I_{PWMI1,2,H}$	15	30	45	µA	$V_{PWMI1,2}$ = 2.0 V	P_7.2.9
PWMI1,2 Low Input Currents	$I_{PWMI1,2,L}$	6	12	18	µA	$V_{PWMI1,2}$ = 0.8 V	P_7.2.10

8 Analog Dimming

The analog dimming feature allows further control of the output current. This approach is used to:

- Reduce the default current in a narrow range to adjust to different binning classes of the used LEDs.
- Adjust the load current to enable the usage of one hardware for several LED types where different current levels are required.
- Reduce the current at high temperatures (protect LEDs from overtemperature).

8.1 Description

The analog dimming feature is adjusting the average load current level via the control of the feedback error Amplifier voltage ($V_{FBH1,2-FBL1,2}$).

The `LEDCURRCAL_CH1,2.DAC_OFF_CH1,2` bit-field is used to switch the error amplifier reference from the internal DAC circuitry to the SET1,2 pin during the active state (refer to **Figure 7**). This provides customers higher dimming resolution via the µC and the SET1,2 pin (refer to picture 1 displayed in **Figure 17**).

When `LEDCURRCAL_CH1,2.DAC_OFF_CH1,2 = LOW` ,the current adjustment is done via a 8BIT SPI parameter (`LEDCURRADIM_CH1,2.ADIMVAL_CH1,2`). Refer to **Figure 14**.

If `LEDCURRADIM_CH1,2.ADIMVAL_CH1,2` is set to 00000000_B the channel stops the switching activity and will restart with a soft start routine as soon as a different value is programmed.

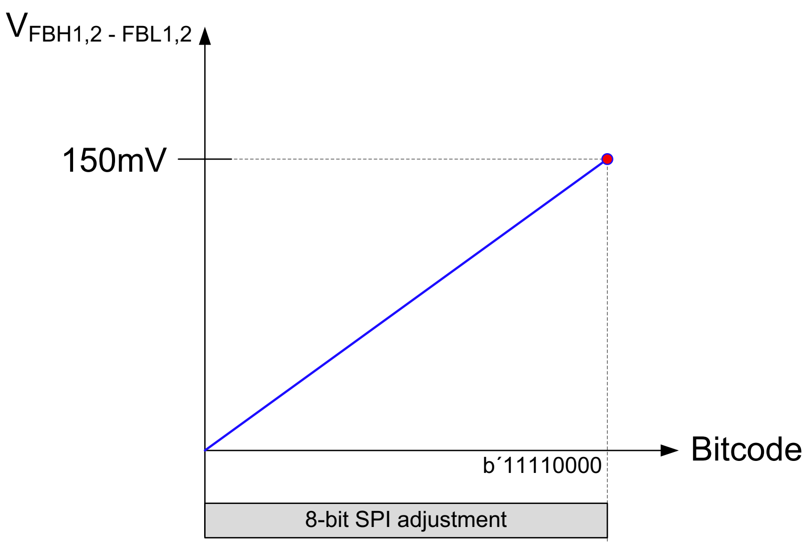


Figure 14 Analog Dimming Overview

Analog dimming adjustment during Limp Home state:

To enter in Limp Home state the LHI pin must be HIGH.

Note: *If the PWMI1,2 and the EN/INUVLO are not set to HIGH, it is not possible to enable switching during Limp Home state.*

In Limp Home state the analog dimming control is done via the SET1,2 pins. A Resistor divider between IVCC/IVCC_EXT, SET1,2 and GND is used to fix a default load current/voltage value (refer to **Figure 15** below).

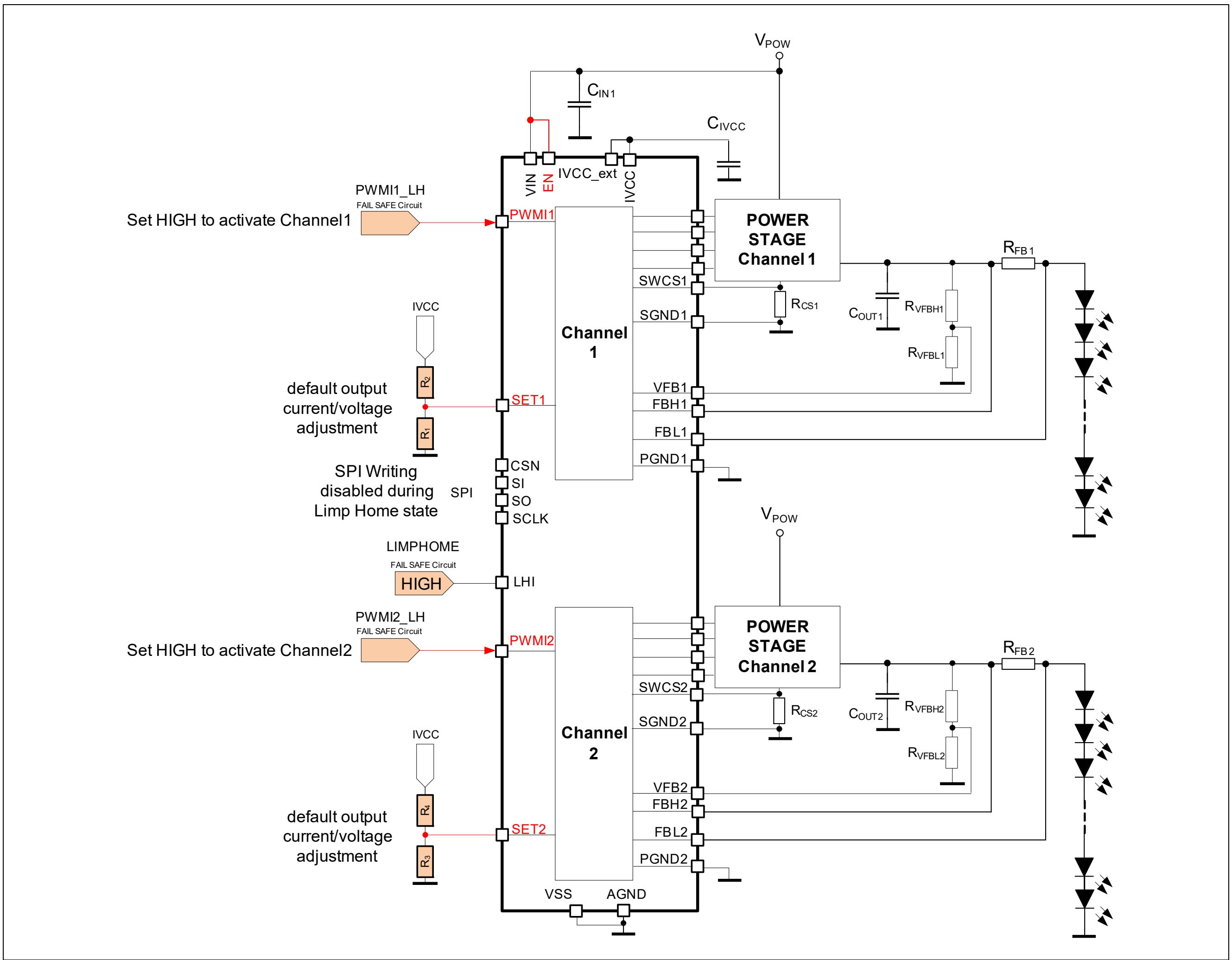


Figure 15 Limp Home state schematic overview

Using the SET1,2 pins to adjust the output currents:

For the calculation of the output current I_{OUT} the following **Equation (8.1)** is used:

$$I_{OUT\,1,2} = \frac{V_{FBH\,1,2} - V_{FBL\,1,2}}{R_{FB\,1,2}} \tag{8.1}$$

A decrease of the average output current can be achieved by controlling the voltage at the SET1,2 pin ($V_{SET1,2}$) between 0.2 V and 1.4 V. The mathematical relation is given in the **Equation (8.2)** below:

$$I_{OUT\,1,2} = \frac{V_{SET\,1,2} - 200\ mV}{R_{FB\,1,2} \cdot 8} \tag{8.2}$$

If $V_{SET1,2}$ is 200 mV (typ.) the LED current is only determined by the internal offset voltages of the comparators. To assure the switching activity is stopped and $I_{OUT} = 0$, $V_{SET1,2}$ has to be < 100 mV, see **Figure 16**.

The channel is then ready to restart with the soft start routine when VSET1,2 is pulled above 200 mV.

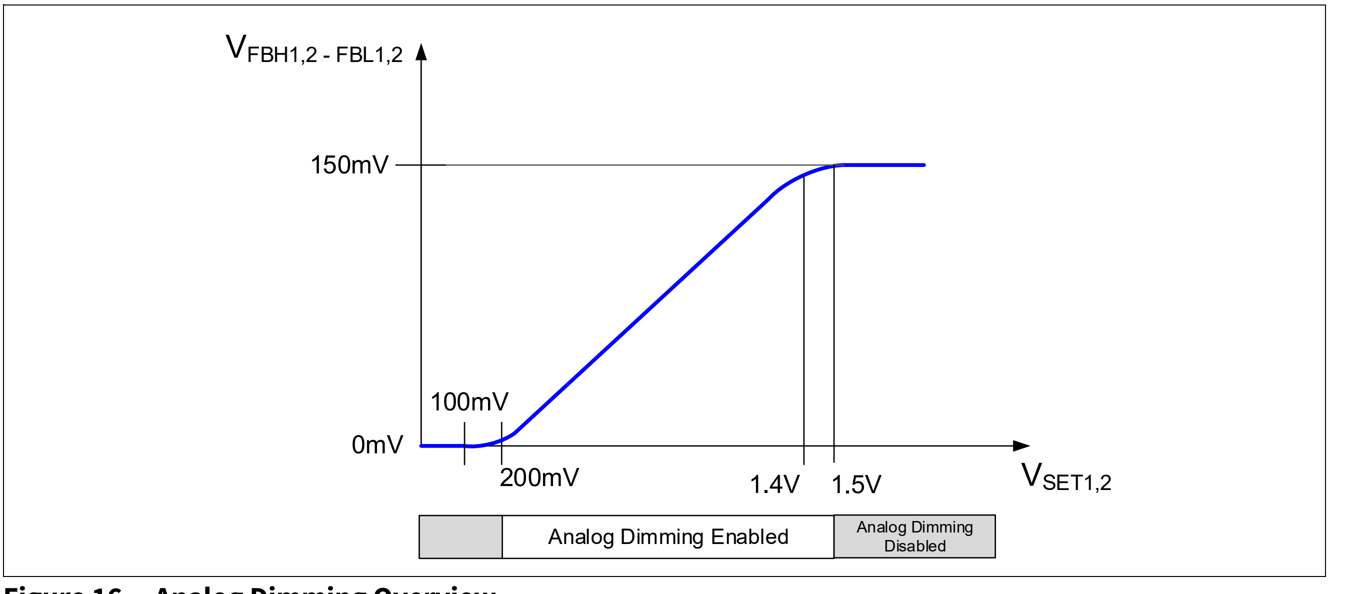


Figure 16 Analog Dimming Overview

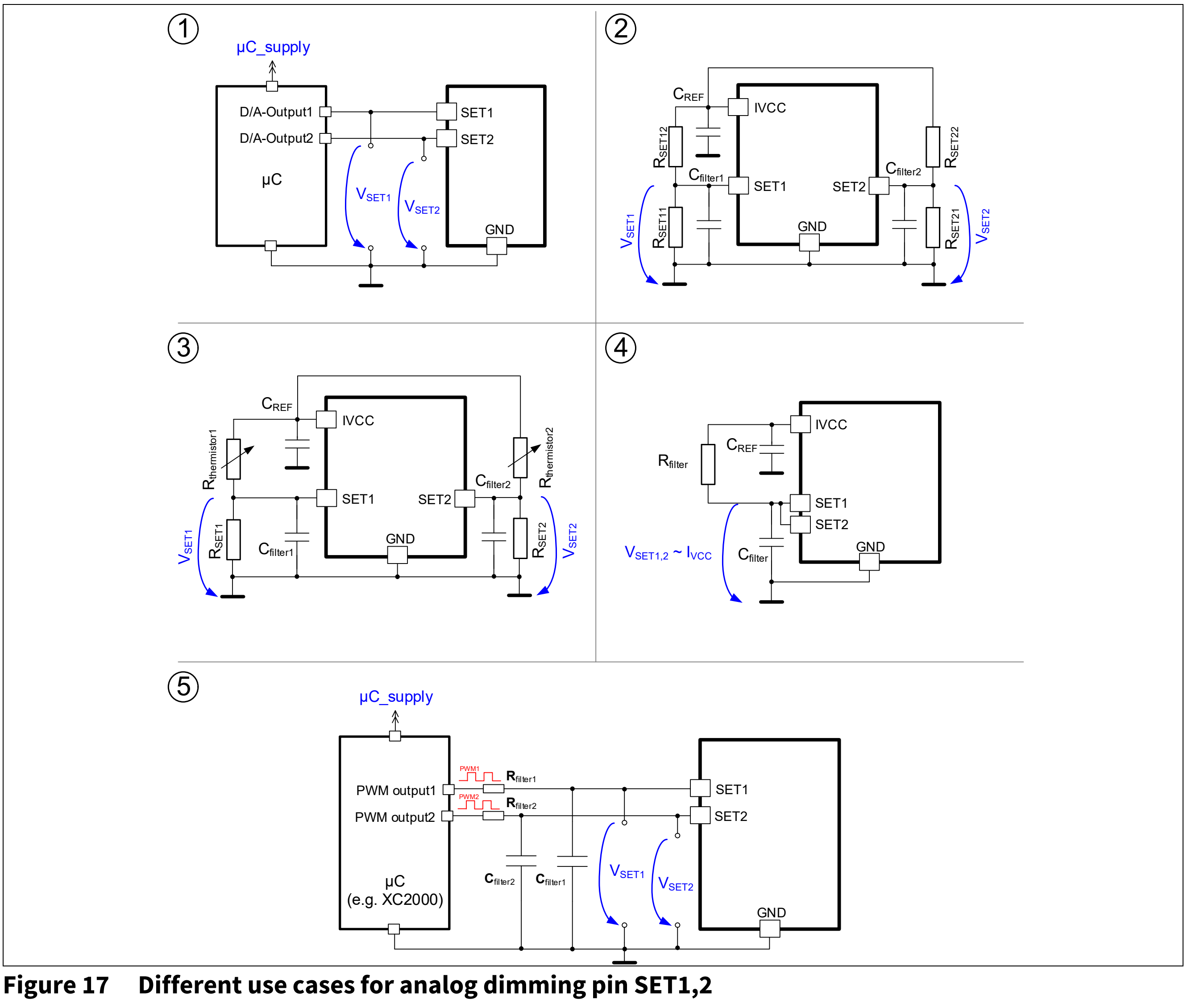


Figure 17 Different use cases for analog dimming pin SET1,2

The relation between the analog dimming and the $V_{(FBH1,2\text{-}FBL1,2)\_VALID}$ threshold is shown in **Figure 18**.

When SET1,2 pin is used to set the analog dimming, the $V_{(FBH1,2\text{-}FBL1,2)\_VALID}$ threshold is a direct partition of the SET voltage.

Thus, in case the voltage on SET pin is above 100% of analog dimming the $V_{(FBH1,2\text{-}FBL1,2)\_VALID}$ threshold could not be exceeded by the regulated voltage $V_{(FBH1,2\text{-}FBL1,2)}$ with the following implications:

- The forced CCM mode is applied only once the $V_{SOFT\_START1,2}$ exceeds the $V_{SOFT\_START1,2\_LOFF}$
- During rising edge of the soft start the internal PWM is extended always until the $V_{SOFT\_START1,2}$ exceeds the $V_{SOFT\_START1,2\_LOFF}$

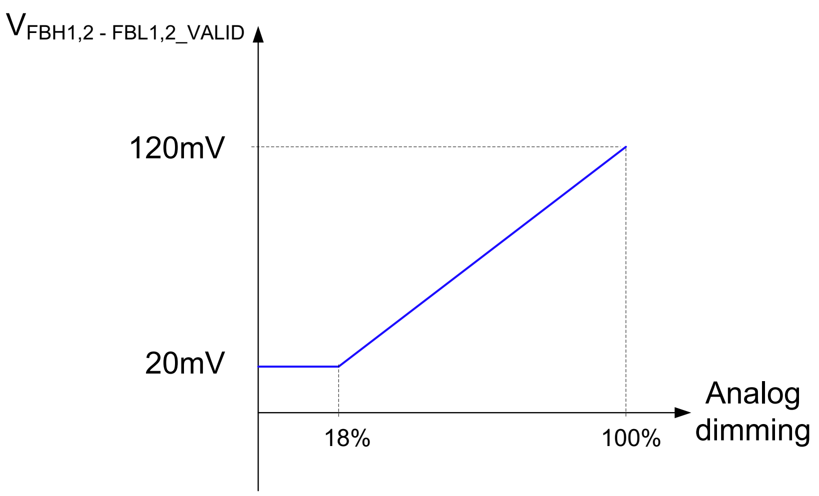


Figure 18 Relation between Analog Dimming $V_{(FBH1,2\text{-}FBL1,2)\_VALID}$

8.2 LED current calibration procedure

The LED current calibration procedure improves the accuracy during analog dimming. In order to be most effective, this routine has to be performed in the application, when the TLD5501-2QV temperature and the output voltage are the ones in which the driver has to be accurate. The output current must be 0 during the procedure run. The optimum should be to re-calibrate the output periodically every time the application has PWMI1,2=LOW for a sufficent long time .

Current calibration procedure:

- Power the Load with a low analog dimming value (for example 10%)
- Set PWMI1,2 = LOW and disconnect the Load at the same time (to avoid Vout drifts from operating conditions and bring the output current to 0)
- Quickly (to avoid Vout drifts) µC enables the calibration routine: `LOOPCTRL_CH1,2.ENCAL_CH1,2` = HIGH
- Quickly (to avoid Vout drifts) µC starts the calibration: `LEDCURRCAL_CH1,2.SOCAL_CH1,2` = HIGH
- Waiting time (needed to internally perform the calibration routine) → aprox. 200 µs
- TLD5501-2QV will set the FLAG: `LEDCURRCAL_CH1,2.EOCAL_CH1,2` = HIGH, when calibration routine has finished
- Reconnect the load
- The Output current is automatically adjusted to a low offset and more accurate analog dimming value

Once the Calibration routine is correctly performed, the output current accuracy with analog dimming = 10% (`LEDCURRADIM_CH1,2.ADIMVAL_CH1,2` = 24) is 10%.

The Calibration routine is not affecting the accuracy at 100% analog dimming.

The ENCAL_CH1,2 Bits affect both device operation and CALIBVAL_CH1,2 reading result:

- ENCAL_CH1,2 = HIGH: the calibration result coming from the routine is used by internal circuitry and can be read back from CALIBVAL_CH1,2
- ENCAL_CH1,2 = LOW: SPI value written in CALIBVAL_CH1,2 is used by internal circuitry and can be read back; calibration routine start is inhibited

As a result, µC can use a stored result from a previously performed calibration to directly impose the desired value without waiting for a new routine to finish.

8.3 Electrical Characteristics

Table 9 EC Analog Dimming

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Source currents on SET1,2 Pin	$I_{SET1,2\_source}$	–	–	1	µA	[1] $V_{SET1,2}$ = 0.2 V to 1.4 V	P_8.3.5

1) Specified by design: not subject to production test

9 Linear Regulator

The TLD5501-2QV features an integrated voltage regulator for the supply of the internal gate driver stages. Furthermore an external voltage regulator can be connected to the IVCC_EXT pin to achieve an alternative gate driver supply if required.

9.1 IVCC Description

When the IVCC pin is connected to the IVCC_EXT pin, the internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to I_{LIM} (P_9.2.2). An external output capacitor with low ESR is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor (**Figure 19**, drawing A). Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches. A minimum capacitance value is given in parameter C_{IVCC} (P_9.2.4).

Alternative IVCC_EXT Supply Concept:

The IVCC_EXT pin can be used for an external voltage supply to alternatively supply the MOSFET Gate drivers. This concept is beneficial in the high input voltage range to avoid power losses in the IC (**Figure 19**, drawing B).

Integrated undervoltage protection for the external switching MOSFET:

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage. This undervoltage reset threshold circuit will turn OFF the gate drivers in case the IVCC or IVCC_EXT voltage falls below their undervoltage Reset switch OFF Thresholds $V_{IVCC\_RTH,d}$ (P_9.2.9) and $V_{IVCC\_EXT\_RTH,d}$ (P_9.2.5).

In Limp Home state the Undervoltage Reset switch OFF threshold for the IVCC has no impact on the switching activity.

The Undervoltage Reset threshold for the IVCC and the IVCC_EXT pins help to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of the external logic level N-channel MOSFETs.

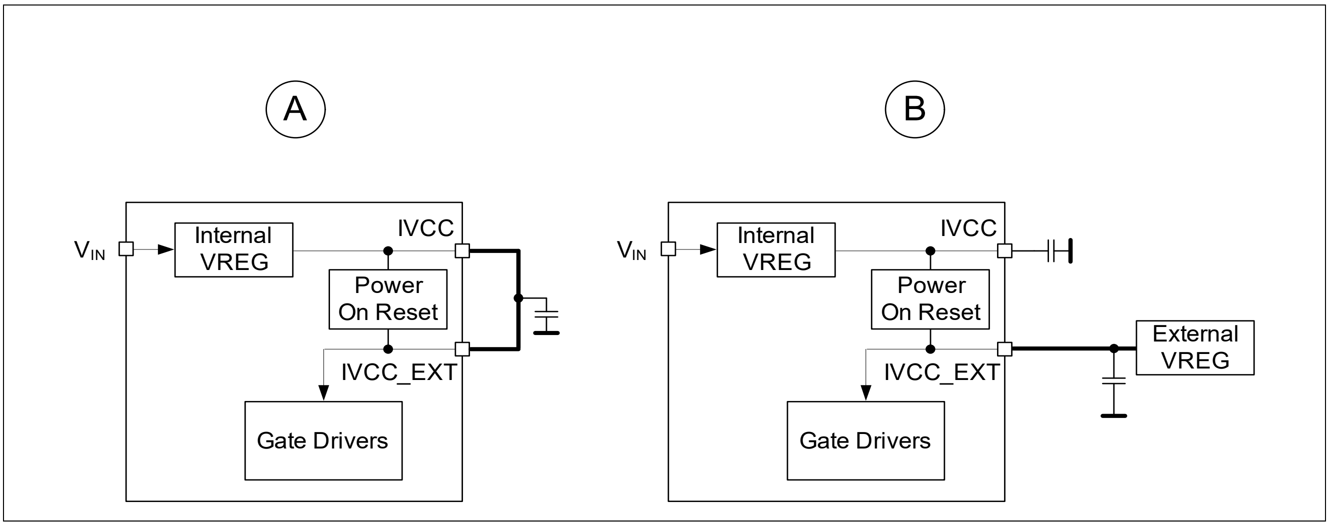


Figure 19 Voltage Regulator Configurations

9.2 Electrical Characteristics

Table 10 EC Line Regulator

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IVCC							
Output Voltage	V_{IVCC}	4.8	5	5.2	V	V_{IN} = 13.5 V; 0.1 mA ≤ I_{IVCC} ≤ 50 mA	P_9.2.1
Output Current Limitation	I_{LIM}	70	90	110	mA	[1] V_{IVCC} = 4 V	P_9.2.2
Drop out Voltage (V_{IN} - V_{IVCC})	V_{DR}	–	200	350	mV	V_{IN} = 5 V; I_{IVCC} = 10 mA	P_9.2.3
IVCC Buffer Capacitor	C_{IVCC}	10	–	–	µF	[1] [2]	P_9.2.4
IVCC_EXT Undervoltage Reset switch OFF Threshold	$V_{IVCC\_EXT\_RTH,d}$	3.7	3.9	4.1	V	[3] V_{IVCC_EXT} decreasing	P_9.2.5
IVCC Undervoltage Reset switch OFF Threshold	$V_{IVCC\_RTH,d}$	3.7	3.9	4.1	V	[3] V_{IVCC} decreasing	P_9.2.9
IVCC and IVCC_EXT Undervoltage Hysterisis	V_{IVCCX_HYST}	0.335	0.365	0.395	V	V_{IVCC} increasing; V_{IVCC_EXT} increasing	P_9.2.6

1) Not subject to production test, specified by design
2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum. Use capacitors with LOW ESR
3) Selection of external switching MOSFET is crucial. $V_{IVCC\_EXT\_RTH,d}$ and $V_{IVCC\_RTH,d}$ min. as worst case V_{GS} must be considered

10 Protection and Diagnostic Functions

10.1 Description

The TLD5501-2QV has integrated circuits to diagnose and protect against overcurrent, overvoltage, open load, short circuits of the load and overtemperature faults. Furthermore, the device provides a 2 Bit information of $I_{LED1,2}$ by the SPI to the µC.

In IDLE state, only the Over temperature Shut Down, Over Temperature Warning, IVCC or IVCC_EXT Undervoltage Monitor, V_{DD} or $V_{EN/INUVLO}$ Undervoltage Monitor are reported according to specifications.

In **Figure 20** a summary of the protection, diagnostic and monitor functions is displayed.

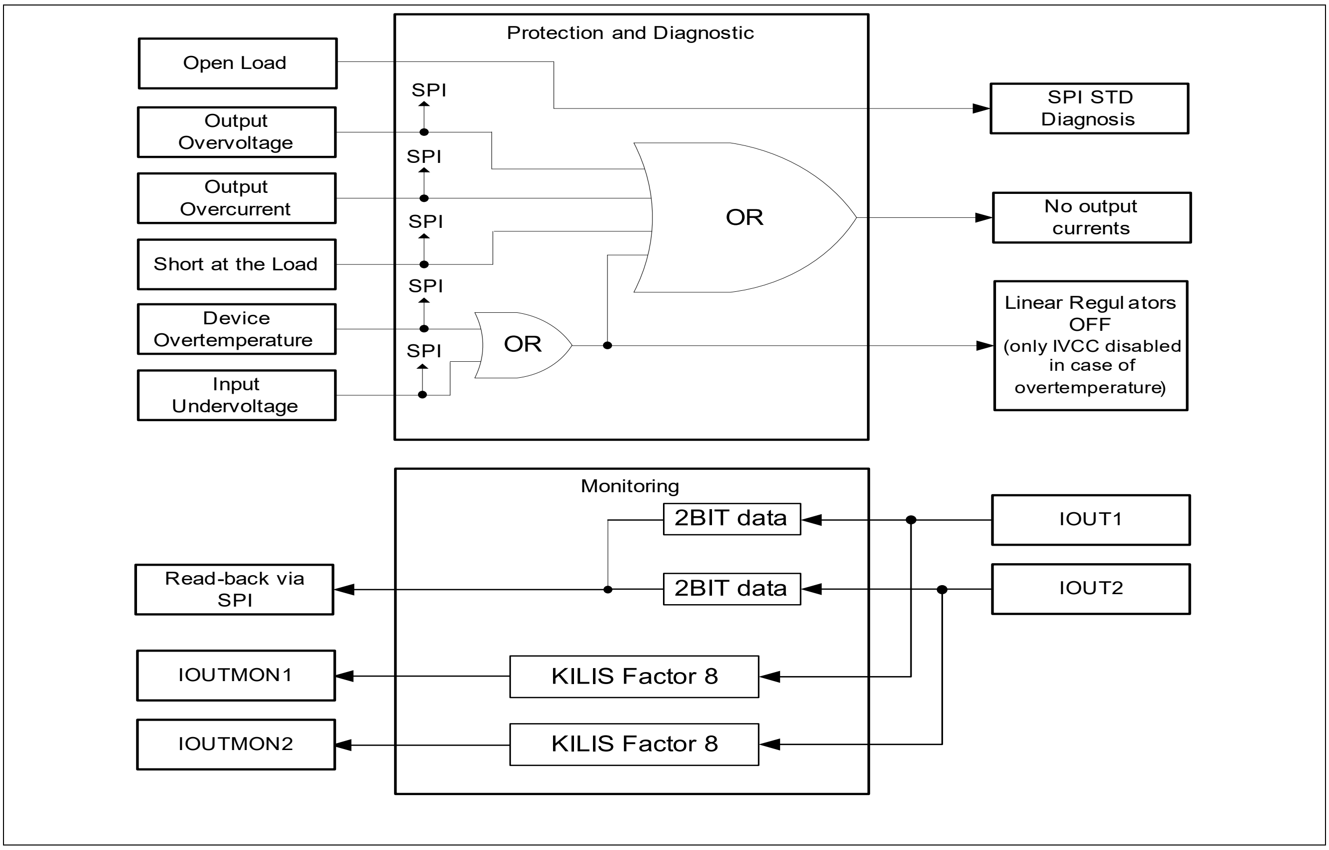


Figure 20 Protection, Diagnostic and Monitoring Overview

Note: A device Overtemperature event overrules all other fault events!

10.2 Output Overvoltage, Overcurrent, Open Load, Short circuit protection

The VFB pin measures the voltage on the application output and in accordance with the populated resistor divider, short to ground, open load and output overvoltage thresholds are set. Refer to **Figure 22** and **Figure 21** for more details.

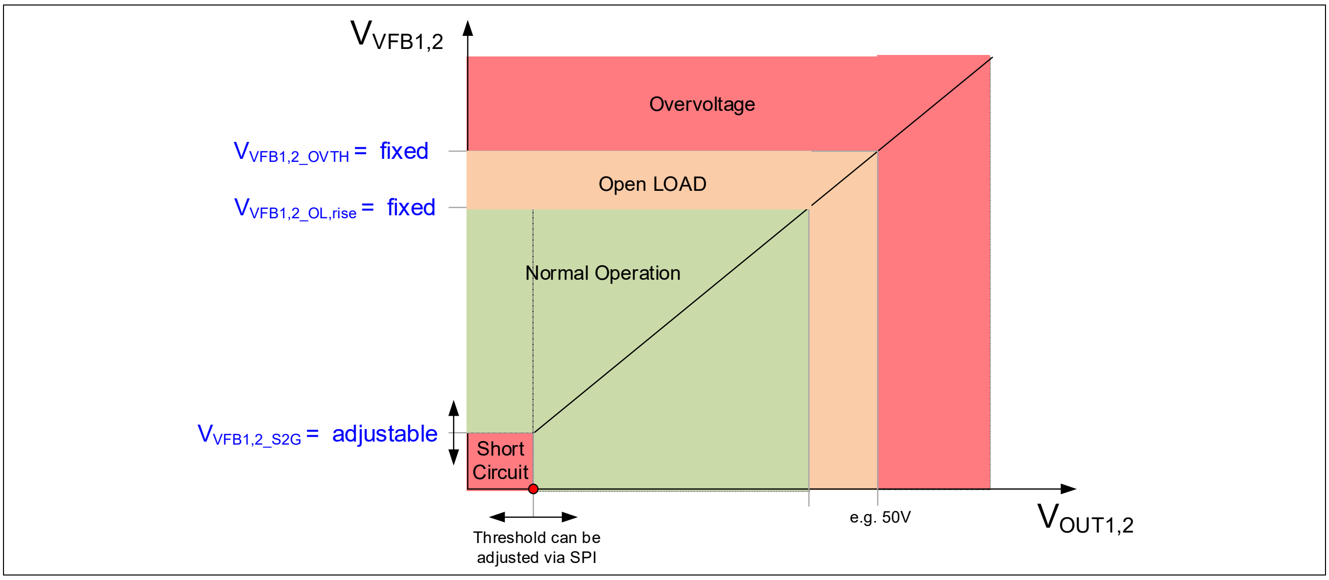


Figure 21 Definition of Protection Ranges

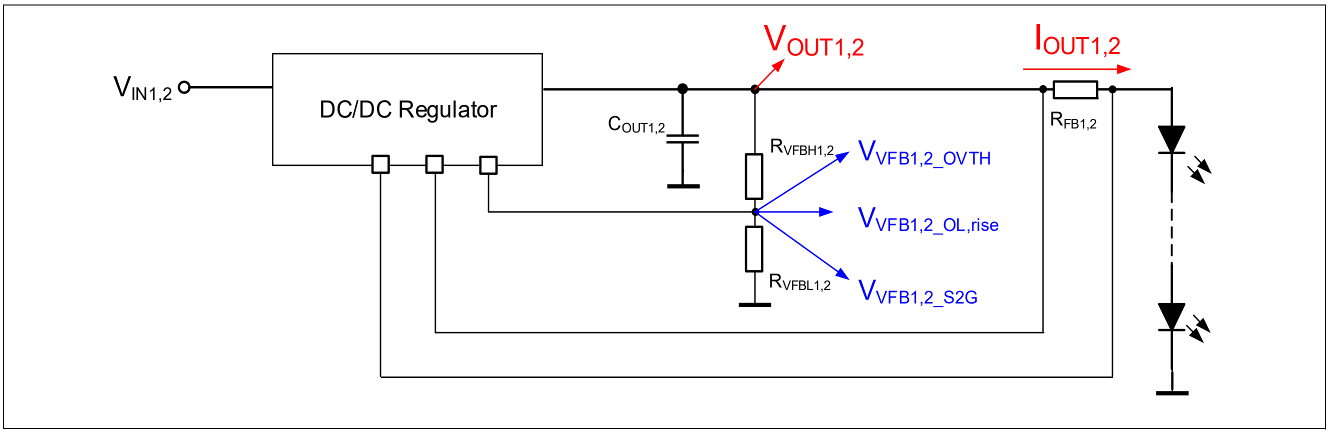


Figure 22 VFB Protection Pin - Overview

10.2.1 Short Circuit protection

The device detects a short circuit at the output if this condition is verified:

- The pin VFB1,2 falls below the threshold voltage $V_{VFB1,2\_S2G}$ for at least 8 clock cycles

During the rising edge of the Soft Start the short circuit detection via VFB1,2 is ignored until $V_{SOFT\_START1,2\_LOFF}$ (see **Figure 8**).

After a short circuit detection, the SPI flag (`SHRTLED_CH1,2`) in the `FAULTS_CH1,2` register is set to HIGH and the gate drivers stop delivering output current. The Device will auto restart with the soft start routine described in **Chapter 6.2**.

Voltage dividers between $V_{OUT1,2}$, VFB1,2 pins and AGND are used to adjust the application short circuit thresholds $V_{short\_led1,2}$ following **Equation (10.1)**.

$$V_{short\_led1,2} = V_{VFB1,2\_S2G} \cdot \frac{R_{VFBH1,2} + R_{VFBL1,2}}{R_{VFBL1,2}} \tag{10.1}$$

The short circuit threshold voltage $V_{VFB1,2\_S2G}$ (P_10.8.17) is set by 4-Bits in the SPI register `MFSSETUP1_CH1,2.LEDCHAIN_CH1,2` as shown in **Table 11**.

The adjustable short circuit threshold $V_{VFB1,2\_S2G}$ enables applications with a large V_{OUT} operation range.

The MFSSETUP1_CH1,2.LEDCHAIN_CH1,2 register allows configuration of the short circuit threshold in 16 Steps.

The step size depends on the sizing of the $R_{VFBH1,2}$ and $R_{VFBL1,2}$ resistors.

In order to have proper short circuit detection MFSSETUP1_CH1,2.LEDCHAIN_CH1,2 should be calculated as shown in **Equation (10.2)**.

$$LEDCHAIN\_CH1,2 = \frac{V_{short\_led} \cdot K_{VFB1,2}}{45mV} \tag{10.2}$$

Where $K_{VFB}=R_{VFBL1,2}/(R_{VFBH1,2} + R_{VFBL1,2})$ and V_{short_led} is the desired short circuit threshold value at $V_{OUT1,2}$.

The **Table 11** below displays the relationship between the bitcode and the short circuit threshold voltage $V_{VFB1,2\_S2G}$ based on an example (resistor divider R_{VFBH} = 56 kΩ, $R_{VFBL1,2}$ = 1.5 kΩ).

The application overvoltage protection is instead not dependent by LEDCHAIN_CH1,2 and, based on the **Equation (10.3)** for this particular resistor divider is fixed to 56 V.

Table 11 Adjustable Short Circuit threshold overview

LEDCHAIN_CH1,2	V_{OUT_OVLO}	k = R_{VFBL} / (R_{VFBH} + R_{VFBL})	V_{open_load}	V_{short_led} (V) ($V_{FB1,2\_S2G}$ / k)	$V_{VFB1,2\_S2G}$(V)
1	56.0	0.026	51.4	1.7	0.045
2 (default)	56.0	0.026	51.4	3.5	0.091
3	56.0	0.026	51.4	5.2	0.136
4	56.0	0.026	51.4	7.0	0.182
5	56.0	0.026	51.4	8.7	0.227
6	56.0	0.026	51.4	10.4	0.272
7	56.0	0.026	51.4	12.2	0.318
8	56.0	0.026	51.4	13.9	0.363
9	56.0	0.026	51.4	15.7	0.409
10	56.0	0.026	51.4	17.4	0.454
11	56.0	0.026	51.4	19.2	0.499
12	56.0	0.026	51.4	20.9	0.545
13	56.0	0.026	51.4	22.6	0.590
14	56.0	0.026	51.4	24.4	0.636
15	56.0	0.026	51.4	26.1	0.681
0	56.0	0.026	51.4	27.9	0.726

Note: If the short circuit condition disappears, the device will re-start with the soft start routine as described in ***Chapter 6.2***

10.2.2 Overvoltage Protection

Voltage dividers between $V_{OUT1,2}$, VFB1,2 pins and AGND are used to adjust the overvoltage protection thresholds (refer to **Figure 22**).

To fix the overvoltage protection thresholds the following **Equation (10.3)** is used:

$$V_{OUT1,2\_OV\_protected} = V_{VFB1,2\_OVTH} \cdot \frac{R_{VFBH1,2} + R_{VFBL1,2}}{R_{VFBL1,2}} \tag{10.3}$$

If $V_{VFB1,2}$ gets higher than its overvoltage thresholds $V_{VFB1,2\_OVTH}$, the SPI flags (OUTOV_CH1,2) in the FAULTS_CH1,2 registers are set to HIGH and the gate drivers stop switching for output regulation (High Impedance, both MOS are OFF). When $V_{VFB1,2\_OVTH}$- $V_{VFB1,2\_OVTH,HYS}$ threshold is reached the device will auto restart.

If the FAULTS_CH1,2.OUTOVLAT_CH1,2 bits are set to HIGH the overvoltage protection is changed into latched behavior and the µC has to set the DVCCTRL.CLRLAT bit to reset the OUTOV flag and restart the switching activities.

10.2.3 Overcurrent on Load Protection

If the output current I_{OUT} (or the voltage V_{OUT} for voltage regulators) exceeds the nominal value, driving $V_{(FBH1,2-FBL1,2)} > V_{FBHL\_OCTH,rise}$, the SPI flag OUTOC_CH1,2 in the FAULTS_CH1,2 register is set to HIGH and the output stage is set to High Impedance (both MOS are OFF), reducing the risk of load damage. I_{OUT} and V_{OUT} are shown in **Figure 22**

The device recovers automatically from the overcurrent protection when $V_{(FBH1,2-FBL1,2)} < V_{FBHL\_OCTH,fall}$.

10.2.4 Open Load Detection

To reliably detect an open load event, two conditions need to be observed for at least 8 clock cycles:

1) Voltage threshold: $V_{VFB1,2} > V_{VFB1,2\_OL,rise}$

2) Output current information: $V_{(FBH1,2-FBL1,2)} < V_{FBH1,2\_FBL1,2\_OL}$

During the rising edge of the Soft Start the open load detection is ignored until $V_{SOFT\_START1,2\_LOFF}$.

After an open load detection, the SPI flag (OL_CH1,2) in the FAULTS_CH1,2 register is set to HIGH without affecting the gate drivers activity.

An Open Load error causes an increase of the output voltage as well. An Overvoltage condition could be reported in combination with an Open Load error.

10.3 Output current Monitoring

The output current can be monitored through an analog output pin and an SPI routine.

The IOUTMON1,2 pin provides a linear indication of the current flowing through the LEDs. The following **Equation (10.4)** is applicable:

$$V_{IOUTMON\ 1,2} = 200\,mV + I_{OUT\ 1,2} \cdot R_{FB\ 1,2} \cdot 8 \tag{10.4}$$

The nominal output impedence of the IOUTMON1,2 is 24 kΩ.

Purpose of the SPI current monitor routine is to verify if the system is in loop.

- The output of the Led Current Sense is compared to the output of the Analog Dimming DAC
- The comparator works like a 2 bit window ADC around 8 bit DAC output

To execute the current monitor routine the CURRMON_CH1,2.SOMON_CH1,2 bit has to be set HIGH and the result is ready when CURRMON_CH1,2.EOMON_CH1,2 is read HIGH.

The result of the monitor routine for the output current is reported on the CURRMON_CH1,2.LEDCURR_CH1,2 bits.

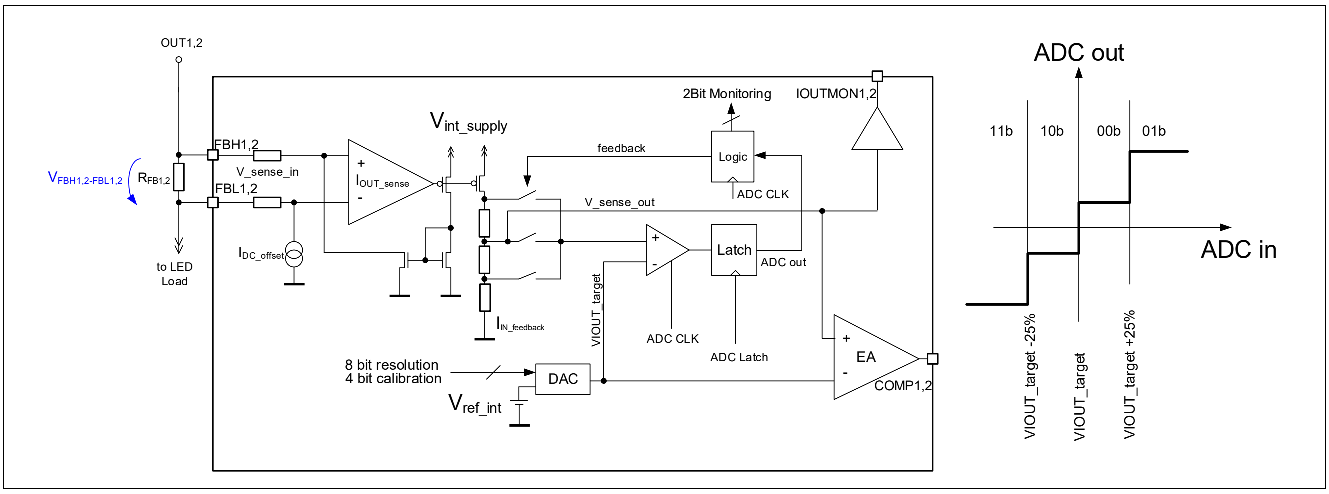


Figure 23 Output Current Monitoring General Overview

10.4 Device Temperature Monitoring

A temperature sensor is integrated on the chip. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds. If the internal temperature sensor reaches the warning temperature, the temperature warning bit `TW` is set to HIGH. This bit is not latched (i.e. if the temperature falls below the warning threshold (with hysteresis), the `TW` bit is reset to LOW again).

If the internal temperature sensor reaches the shut-down temperature, the Gate Drivers plus the IVCC regulator are shut down as described in **Figure 24** and the temperature shut-down bit: `TSD` is set to HIGH. The `TSD` bit is latched while the Gate Drivers plus the IVCC regulator have an auto restart behavior.

Note: The Device will start up with a soft start routine after a TSD condition disappear.

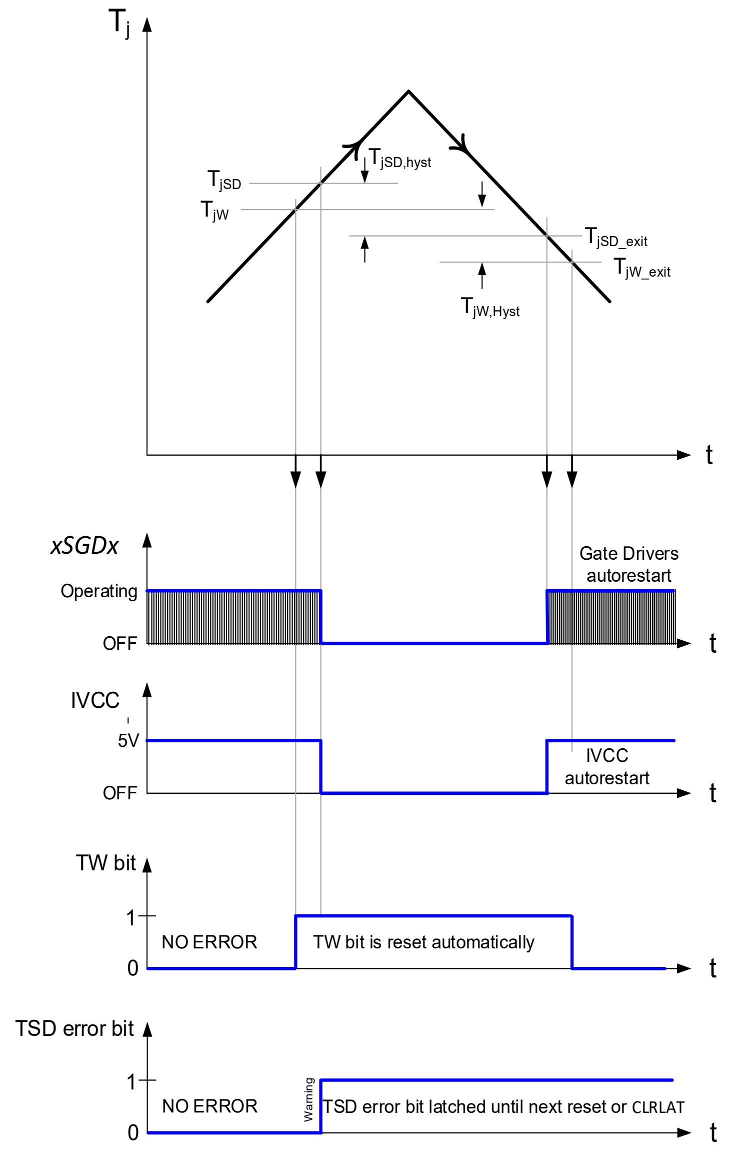


Figure 24 Device Overtemperature Protection Behavior

10.5 Electrical Characteristics

Table 12 EC Protection and Diagnosis

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Short Circuit Protection							
Short to GND thresholds by VFB1,2 voltage (default)	$V_{VFB1,2\_S2G}$	0.081	0.091	0.101	V	$V_{VFB1,2}$ decreasing; MFSSETUP1_CH1,2.LEDCHAIN_CH1,2 = 0010_B	P_10.8.17
Temperature Protection:							
Thermal Warning junction temperature	$T_{j,W}$	125	140	155	°C	[1]	P_10.8.2
Temperature warning Hysteresis	$T_{j,W,hyst}$	–	10	–	°C	[1]	P_10.8.3
Over Temperature Shutdown	$T_{j,SD}$	160	175	190	°C	[1]	P_10.8.4
Over Temperature Shutdown Hysteresis	$T_{j,SD,hyst}$	–	10	–	°C	[1]	P_10.8.5
Overvoltage Protection:							
VFB1,2 Over Voltage Feedback Threshold	$V_{VFB1,2\_OVTH}$	1.42	1.46	1.50	V		P_10.8.18
Output Over Voltage Feedback Hysteresis	$V_{VFB1,2\_OVTH,HYS}$	25	40	58	mV	[1] Output Voltage decreasing	P_10.8.19
Overcurrent Protection							
I_{OUT} Overcurrent rising Threshold	$V_{FBHL\_OCTH,rise}$	185	205	225	mV	Differential signal (not referred to GND)	P_10.8.30
I_{OUT} Overcurrent falling Threshold	$V_{FBHL\_OCTH,fall}$	165	185	205	mV	Differential signal (not referred to GND)	P_10.8.31
Open Load and Open Feedback Diagnostics							
Open Load rising Thresholds	$V_{VFB1,2\_OL,rise}$	1.29	1.34	1.39	V	$V_{FBH1,2-FBL1,2}$ = 0 V	P_10.8.20
Open Load reference Voltages $V_{FBH1,2-FBL1,2}$	$V_{FBH1,2\_FBL1,2\_OL}$	–	15	24	mV	$V_{VFB1,2}$ = 1.4 V; Differential signal (not referred to GND)	P_10.8.21
Open Load falling Thresholds	$V_{VFB1,2\_OL,fall}$	1.23	1.28	1.33	V	$V_{FBH1,2-FBL1,2}$ = 0 V	P_10.8.22

1) Specified by design; not subject to production test

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation

11 Infineon FLAT SPECTRUM Feature set

11.1 Description

The Infineon FLAT SPECTRUM feature set has the target to minimize external additional filter circuits. The goal is to provide several beneficial concepts to provide easy adjustments for EMC improvements after the layout is already done and the HW designed.

11.2 Synchronization Function

The gate driver switching behavior of the TLD5501-2QV are per default 180° phase shifted between the two channels. Synchronization and Spread Spectrum modulation will be done on top of the 180° phase shift between the two channels.

The TLD5501-2QV features a SYNC input pin which can be used by a µC pin to define an oscillator switching frequency. The µC is responsible to synchronize with various devices by applying appropriate SYNC signals to the dedicated DC/DC devices in the system. Refer to **Figure 25**

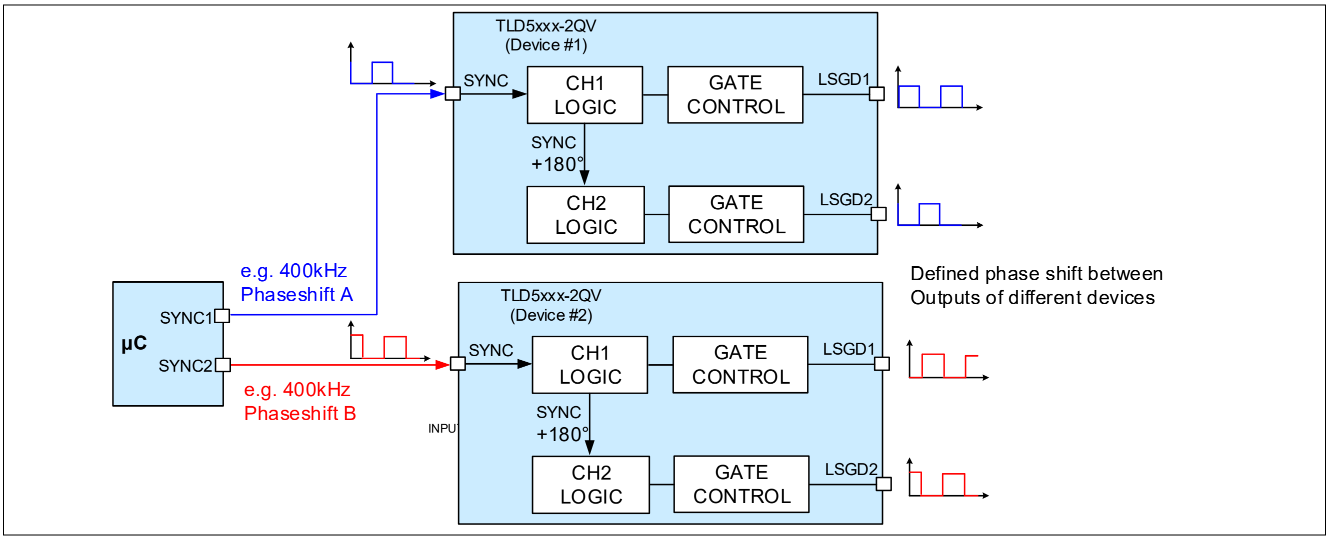


Figure 25 Synchronization Overview

11.3 Spread Spectrum

The Spread Spectrum modulation technique significantly improves the lower frequency range of the spectrum (f < 30 MHz).

By using the spread spectrum technique, it is possible to optimize the input filter only for the peak limits, and also pass the average limits (average emission limits are -20dB lower than the peak emission limits). By using spread spectrum, the need for low ESR input capacitors is relaxed because the input capacitor series resistor is important for the low frequency filter characteristic. This can be an economic benefit if there is a strong requirement for average limits.

The TLD5501-2QV features a built in Spread Spectrum function which can be disabled (`SWTMOD.ENSPREAD`) and adjusted via the SPI interface. Dedicated SPI-Bits are used to adjust the modulation frequency f_{FM}, (P_11.6.3) and (P_11.6.4) (`SWTMOD.FMSPREAD`) and the deviation frequency f_{dev}, (P_11.6.1) and (P_11.6.2) (`SWTMOD.FDEVSPREAD`) accordingly to specific application needs. Refer to **Figure 26** for more details.

The following adjustments can be programmed when `SWTMOD.ENSPREAD` **= HIGH:**

`SWTMOD.FMSPREAD` = LOW: 12 kHz

`SWTMOD.FMSPREAD` = HIGH: 18 kHz

`SWTMOD.FDEVSPREAD` = HIGH: ±10% of f_{SW}

`SWTMOD.FDEVSPREAD` = LOW: ±20% of f_{SW}

Note: The Spread Spectrum function can not be used when the synchronization pin is used.

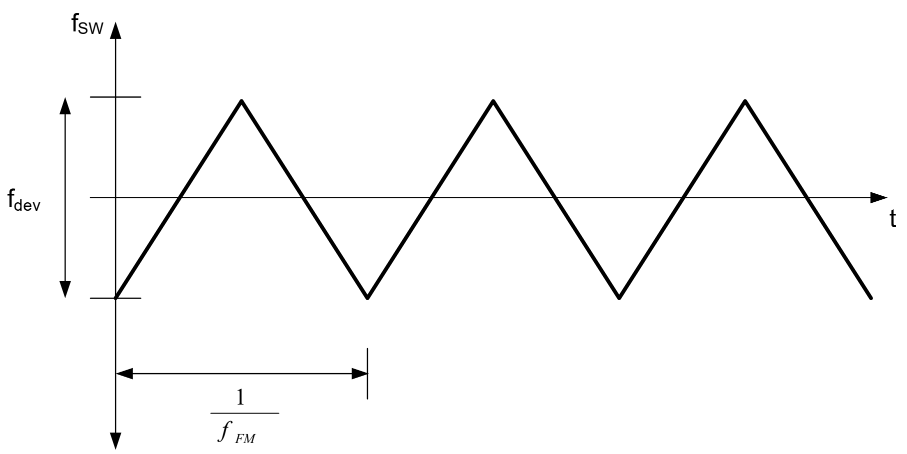


Figure 26 Spread Spectrum Overview

11.4 EMC optimized schematic

Figure 27 below displays the Application circuit with additional external components for improved EMC behavior.

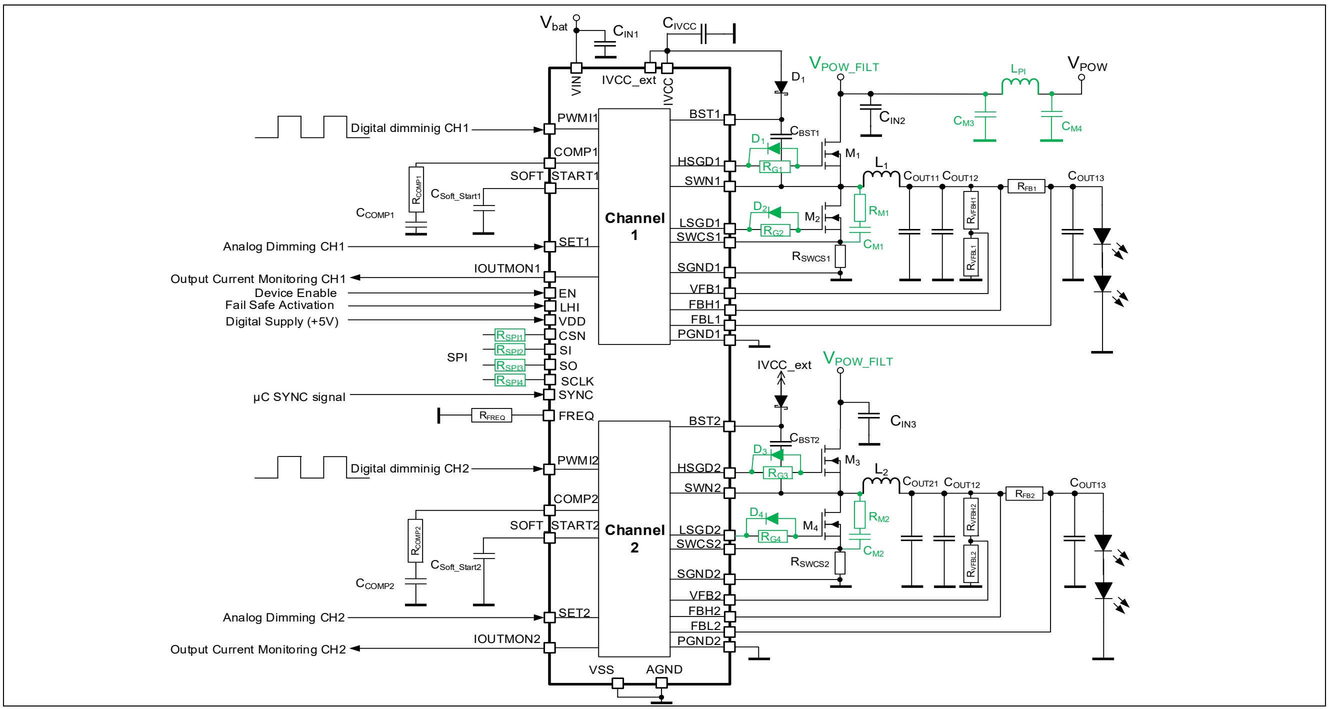


Figure 27 Application Drawing Including Additional Components for an Improved EMC Behavior - TLD5501-2QV

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

11.5 Electrical Characteristics

Table 13 EC Spread Spectrum

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Spread Spectrum Parameters							
Frequency Deviation	f_{dev}	–	±10	–	%	1) SWTMOD.FDEVSPREAD = HIGH	P_11.6.1
Frequency Deviation	f_{dev}	–	±20	–	%	1) SWTMOD.FDEVSPREAD = LOW	P_11.6.2
Frequency Modulation	f_{FM}	–	12	–	kHz	1) SWTMOD.FMSPREAD = LOW	P_11.6.3
Frequency Modulation	f_{FM}	–	18	–	kHz	1) SWTMOD.FMSPREAD = HIGH	P_11.6.4

1) Specified by design; not subject to production test

12 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CSN. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of CSN indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CSN. A modulo 8/16 counter ensures that data is taken only when a multiple of 8 bit has been transferred after the first 16 bits. Otherwise, a TER (i.e. Transmission Error) bit is asserted. In this way the interface provides daisy chain capability with 16 bit as well as with 8 bit SPI devices.

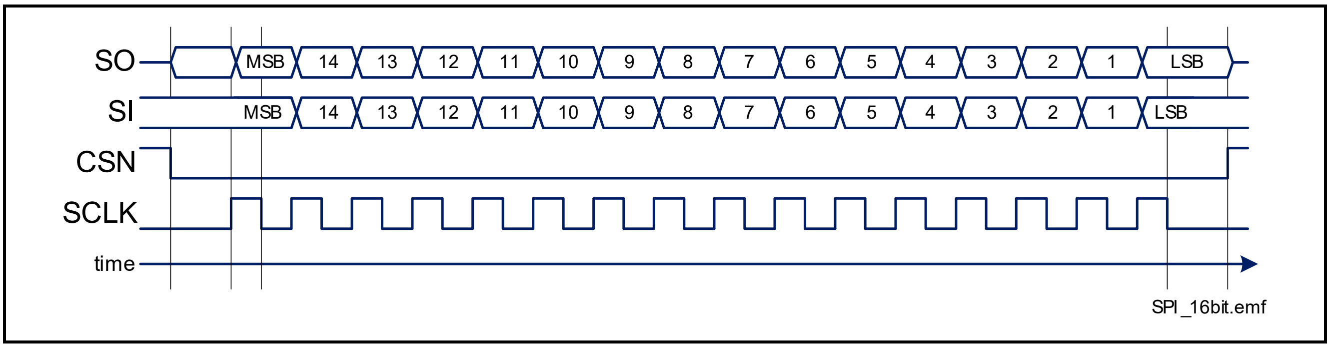


Figure 28 Serial Peripheral Interface

12.1 SPI Signal Description

CSN - Chip Select

The system microcontroller selects the TLD5501-2QV by means of the CSN pin. Whenever the pin is in LOW state, data transfer can take place. When CSN is in HIGH state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

CSN HIGH to LOW Transition

- The requested information is transferred into the shift register.
- SO changes from high impedance state to HIGH or LOW state depending on the signal level at pin SI.
- If the device is in SLEEP mode, the SO pin remains in high impedance state and no SPI transmission will occur.
- TER Flag will set the Bit number 10 in the STD diagnosis Frame. This Bit is set to HIGH after an undervoltage contition, reset via SPI command, on Limp Home state entering or after an incorrect SPI transmission. TER Flag can be read also direcly on the SO line between the falling edge of the CSN and the first rising edge of the SCLK according to the **Figure 29**.

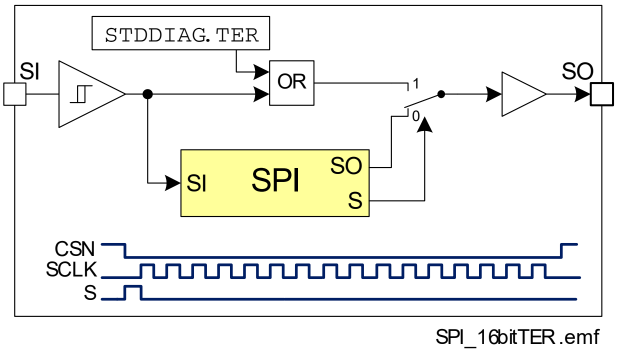


Figure 29 Combinatorial Logic for TER bit

CSN LOW to HIGH Transition

- Command decoding is only done, when after the falling edge of CSN exactly a multiple (0,1, 2, 3, ...) of eight SCLK signals have been detected after the first 16 SCLK pulses. In case of faulty transmission, the transmission error bit (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in LOW state whenever chip select CSN makes any transition, otherwise the command may be not accepted.

SI - Serial Input

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Chapter 12.5** for further information.

SO Serial Output

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CSN pin goes to LOW state. New data will appear at the SO pin following the rising edge of SCLK.

Please refer to **Chapter 12.5** for further information.

12.2 Daisy Chain Capability

The SPI of the TLD5501-2QV provides daisy chain capability. In this configuration several devices are activated by the same CSN signal MCSN. The SI line of one device is connected with the SO line of another device (see **Figure 30**), in order to build a chain. The end of the chain is connected to the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

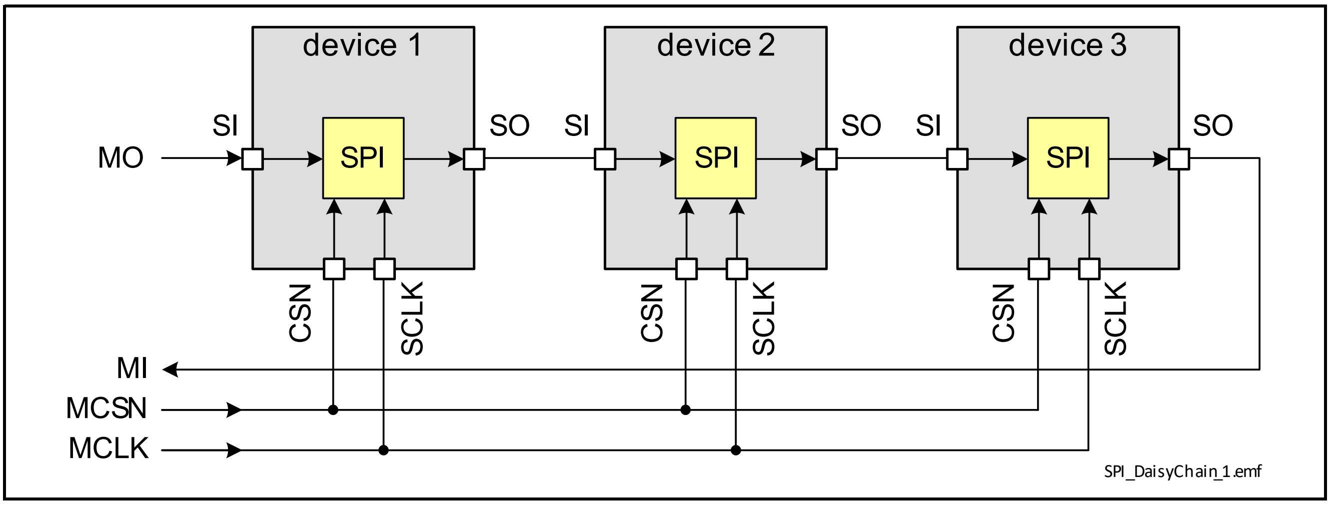


Figure 30 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where each bit from the SI line is shifted in with each SCLK. The bit shifted out occurs at the SO pin. After sixteen SCLK cycles, the data transfer for one device is finished. In single chip configuration, the CSN line must turn HIGH to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, several multiples of 8 bits have to be shifted through the devices (depending on how many devices with 8 bit SPI and how many with 16 bit SPI). After that, the MCSN line must turn HIGH (see **Figure 31**).

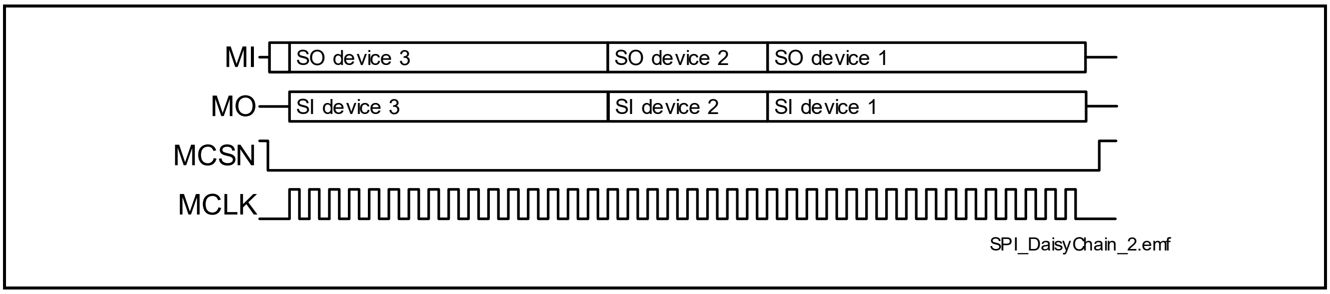


Figure 31 Data Transfer in Daisy Chain Configuration

12.3 Timing Diagrams

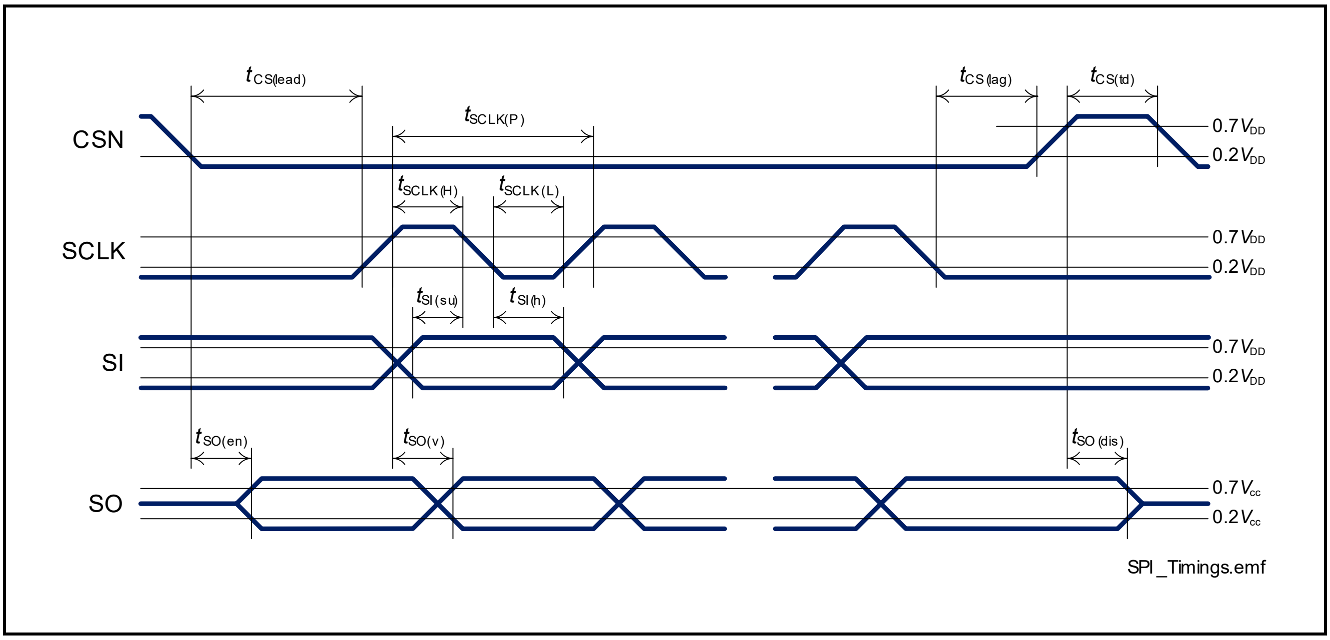


Figure 32 Timing Diagram SPI Access

12.4 Electrical Characteristics

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, V_{DD}= 3 V to 5.5 V, all voltages with respect to ground; (unless otherwise specified)

Table 14 EC Serial Peripheral Interface (SPI)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Characteristics (CSN, SCLK, SI) - LOW level of pin							
CSN	$V_{CSN(L)}$	0	–	0.8	V	–	P_12.4.1
SCLK	$V_{SCLK(L)}$	0	–	0.8	V	–	P_12.4.2
SI	$V_{SI(L)}$	0	–	0.8	V	–	P_12.4.3
Input Characteristics (CSN, SCLK, SI) - HIGH level of pin							
CSN	$V_{CSN(H)}$	2	–	V_{DD}	V	–	P_12.4.4
SCLK	$V_{SCLK(H)}$	2	–	V_{DD}	V	–	P_12.4.5
SI	$V_{SI(H)}$	2	–	V_{DD}	V	–	P_12.4.6
L-input pull-up current at CSN pin	$-I_{CSN(L)}$	31	63	94	µA	V_{DD} = 5 V; V_{CSN} = 0.8 V	P_12.4.7
H-input pull-up current at CSN pin	$-I_{CSN(H)}$	22	45	67	µA	V_{DD} = 5 V; V_{CSN} = 2 V	P_12.4.8
L-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(L)}$	6	12	18	µA	V_{SCLK} = 0.8 V;	P_12.4.9
SI	$I_{SI(L)}$	6	12	18	µA	V_{SI} = 0.8 V	P_12.4.10
H-Input Pull-Down Current at Pin							
SCLK	$I_{SCLK(H)}$	15	30	45	µA	V_{SCLK} = 2 V;	P_12.4.11
SI	$I_{SI(H)}$	15	30	45	µA	V_{SI} = 2 V	P_12.4.12
Output Characteristics (SO)							
L level output voltage	$V_{SO(L)}$	0	–	0.4	V	I_{SO} = -2 mA	P_12.4.13
H level output voltage	$V_{SO(H)}$	V_{DD} - 0.4 V	–	V_{DD}	V	I_{SO} = 2 mA; V_{DD} = 5 V	P_12.4.14
Output tristate leakage current	$I_{SO(OFF)}$	-1	–	1	µA	V_{CSN} = V_{DD}; V_{SO} = 0 V or V_{SO} = V_{DD}	P_12.4.15
Timings							
Enable lead time (falling CSN to rising SCLK)	$t_{CSN(lead)}$	200	–	–	ns	[1]	P_12.4.17
Enable lag time (falling SCLK to rising CSN)	$t_{CSN(lag)}$	200	–	–	ns	[1]	P_12.4.18
Transfer delay time (rising CSN to falling CSN)	$t_{CSN(td)}$	250	–	–	ns	[1]	P_12.4.19
Output enable time (falling CSN to SO valid)	$t_{SO(en)}$	–	–	200	ns	[1] C_L = 20 pF at SO pin	P_12.4.20

Table 14 EC Serial Peripheral Interface (SPI) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output disable time (rising CSN to SO tristate)	$t_{SO(dis)}$	–	–	200	ns	[1] C_L = 20 pF at SO pin	P_12.4.21
Serial clock frequency	f_{SCLK}	–	–	5	MHz	[1]	P_12.4.22
Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	[1]	P_12.4.24
Serial clock HIGH time	$t_{SCLK(H)}$	75	–	–	ns	[1]	P_12.4.25
Serial clock LOW time	$t_{SCLK(L)}$	75	–	–	ns	[1]	P_12.4.26
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	–	–	ns	[1]	P_12.4.27
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	20	–	–	ns	[1]	P_12.4.28
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	100	ns	[1] C_L = 20 pF	P_12.4.29

1) Not subject to production test, specified by design

12.5 SPI Protocol

The relationship between SI and SO content during SPI communication is shown in **Figure 33**. The SI line represents the frame sent from the µC and the SO line is the answer provided by the TLD5501-2QV. The first SO response is the response from the previous command.

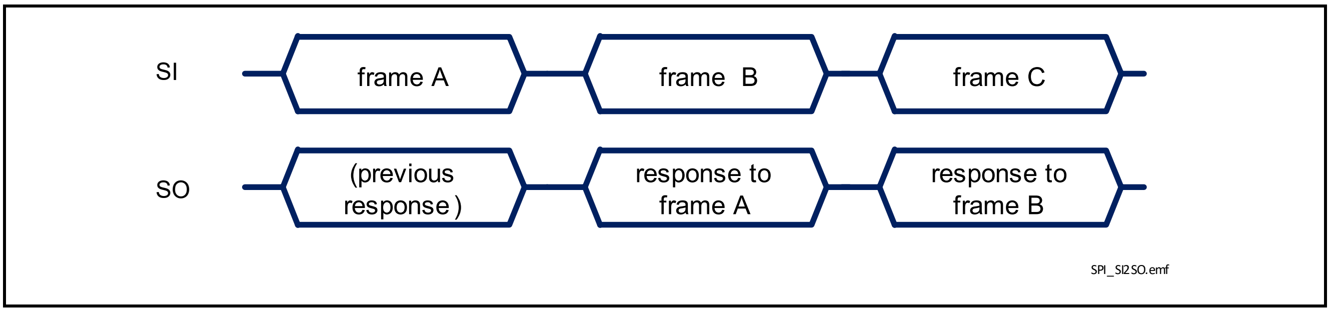


Figure 33 Relationship between SI and SO during SPI communication

The SPI protocol will provide the answer to a command frame only with the next transmission triggered by the µC. Although the biggest majority of commands and frames implemented in TLD5501-2QV can be decoded without the knowledge of what happened before, it is advisable to consider what the µC sent in the previous transmission to decode TLD5501-2QV response frame completely.

More in detail, the sequence of commands to “read” and “write” the content of a register will look as follows:

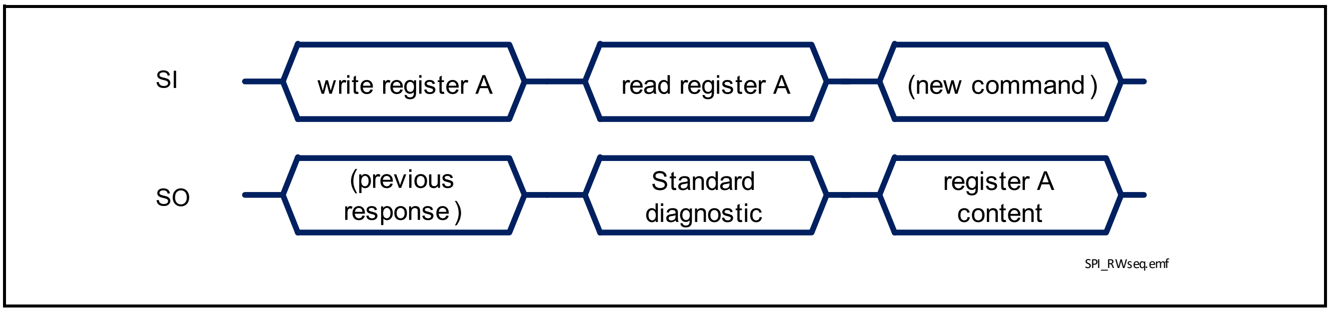


Figure 34 Register content sent back to µC

There are 3 special situations where the frame sent back to the µC doesn't depend on the previously received frame:

- in case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8 with a minimum of 16 bits), shown in **Figure 35**
- when TLD5501-2QV logic supply comes out of an Undervoltage reset condition ($V_{DD} < V_{DD(UV)}$ as shown in **Figure 36** or EN/INUVLO < $V_{EN/INUVLOth}$)
- in case of a read or write command for a “not used” or “reserved” register (in this case TLD5501-2QV answers with Standard Diagnosis at the next SPI transmission)

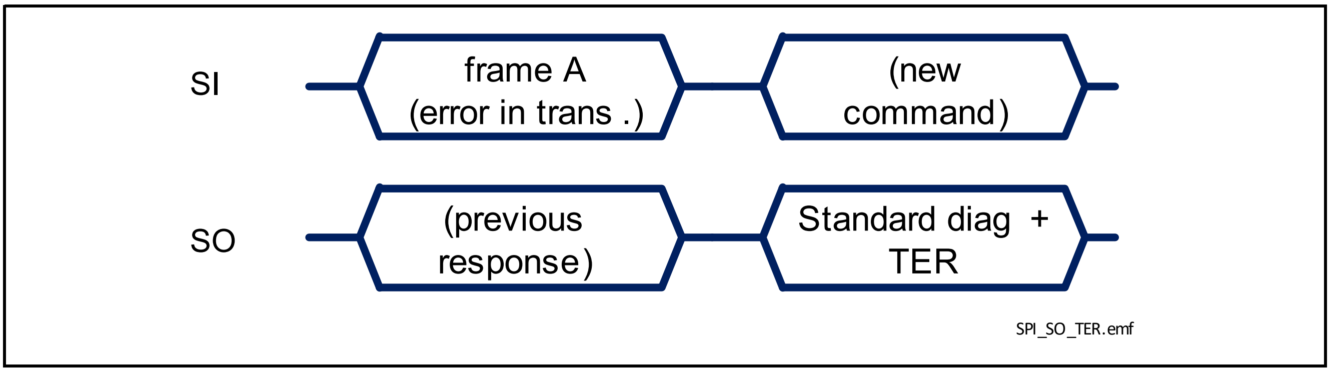


Figure 35 TLD5501-2QV response after an error in transmission

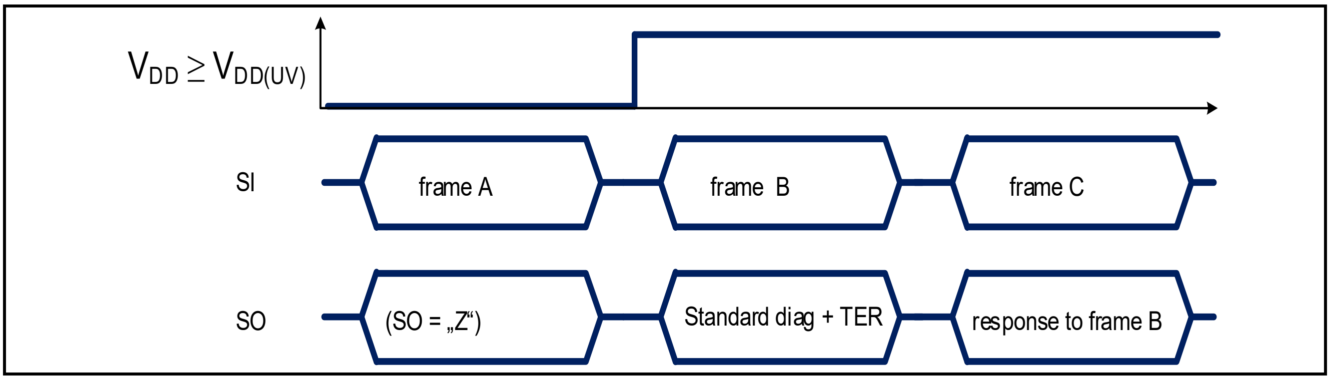


Figure 36 TLD5501-2QV response after coming out of Power-On reset at V_{DD}

12.6 SPI Registers Overview

Reading a register needs two SPI frames. In the first frame the read command is sent. In the second frame the output at SPI signal SO will contain the requested information. The MSB will be HIGH (while in case of standard diagnosis is LOW). A new command can be executed in the second frame.

Table 15 SPI Command Summary[1)]

Requested Operation	Frame sent to TLD5501-2QV (SI pin)	Frame received from TLD5501-2QV (SO pin) with the next command
Read Standard Diagnosis	0xxxxxxxxxxxxxx1$_B$ ("xxxxxxxxxxxx$_B$" = don't care)	0ddddddddddddddd$_B$ (Standard Diagnosis)
Write 8-bit register	Bank 0: 10aaaaaacccccccc$_B$ Bank 1: 11aaaaaacccccccc$_B$ where: "aaaaaa$_B$" = register address "cccccccc$_B$" = new register content	0ddddddddddddddd$_B$ (Standard Diagnosis)
Read 8-bit registers	Bank 0: 00aaaaaaxxxxxxx0$_B$ Bank 1: 01aaaaaaxxxxx$_B$ where: "aaaaaa$_B$" = register address "xxxxxxx$_B$" = don't care	Bank 0: 10aaaaaacccccccc$_B$ Bank 1: 11aaaaaacccccccc$_B$ where: "aaaaaa$_B$" = register address "cccccccc$_B$" = register content

1) "a" = address bits, "c" = register content, "d" = diagnostic bit

12.6.1 Standard Diagnosis

The Standard Diagnosis reports several diagnostic informations and the status of the device and the utility routines. The bits SWRST, UVLORST, TER, CAPUV_CH1, CAPUV_CH2, and IVCCUVLO are latched and automatically cleared after a STD diagnosis reading.

The bit TSD is latched and clearable only via explicit CLRLAT command.

The bits STATE and TW are real time status flags.

The bits EOMON, EOCAL, FAULT_CH1 and FAULT_CH2 are mirrors of internal registers.

A CLRLAT command resets the diagnostic Latched Flags and Latched protections for the OUTOV_CH1,2, TSD bits, restarting the switching activity if this was halted due the previously mentioned faults.

In standard operating condition (active state, no Limp Home), if no special routines have been executed and no faults have been detected, the readout of the STD should be 1000$_H$.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SWRST	UVLORST	STATE		TER	EOMON	x	EOCAL	CAPUV_CH2	CAPUV_CH1	IVCCUVLO	FAULT_CH2	FAULT_CH1	TSD	TW

Field	Bits	Type	Description
SWRST	14	r	**SWRST Monitor** 0_B , no SWRST occured 1_B , there was at least one SWRST since last readout
UVLORST	13	r	**V_{DD} OR $V_{EN/INUVLO}$ Undervoltage Monitor** 0_B , there was no V_{DD} OR $V_{EN/INUVLO}$ undervoltage since last readout 1_B , there was at least one V_{DD} undervoltage OR $V_{EN/INUVLO}$ undervoltage condition since last readout
STATE	12:11	r	**Operative State Monitor** 00_B , (reserved) 01_B , Limp Home Mode 10_B , Active Mode 11_B , Idle Mode
TER	10	r	**Transmission Error** 0_B , Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1_B , Previous transmission failed or first transmission after reset
EOMON	9	r	**Mirror of EOMON_CH1,2** This bit is the mirror of EOMON_CH1 or EOMON_CH2 bits, according to the last SOMON_CH1,2 command received.
EOCAL	7	r	**Mirror of EOCAL_CH1,2** This bit is the mirror of EOCAL_CH1 or EOCAL_CH2 bits, according to the last SOCAL_CH1,2 command received.
CAPUV_CH2	6	r	**Undervoltage at High Side Drivers monitor bit for CH2:** 0_B , V_{BST2} - V_{SWN2} voltage difference is above the Gate Driver undervoltage threshold V_{BST2}-V_{SWN2_UVth} = no undervoltage at Gate Drivers detected 1_B , V_{BST2} - V_{SWN2} voltage is below the Gate Driver undervoltage threshold V_{BST2}-V_{SWN2_UVth} = undervoltage at Gate Drivers detected
CAPUV_CH1	5	r	**Undervoltage at High Side Drivers monitor bit for CH1:** 0_B , V_{BST1} - V_{SWN1} voltage difference is above the Gate Driver undervoltage threshold V_{BST1}-V_{SWN1_UVth} = no undervoltage at Gate Drivers detected 1_B , V_{BST1} - V_{SWN1} voltage is below the Gate Driver undervoltage threshold V_{BST1}-V_{SWN1_UVth} = undervoltage at Gate Drivers detected
IVCCUVLO	4	r	**IVCC or IVCC_EXT Undervoltage Lockout Monitor** 0_B , IVCC and IVCC_EXT above $V_{IVCC\_RTH,d}$ or $V_{IVCC\_EXT\_RTH,d}$ threshold since last readout 1_B , Undervoltage on IVCC or IVCC_EXT occurred since last readout
FAULT_CH2	3	r	**Fault Diagnosis Flag of CH2** This bit is the mirror of SHRTLED_CH2, OL_CH2, OUTOV_CH2 combined in logic OR

Field	Bits	Type	Description
FAULT_CH1	2	r	**Fault Diagnosis Flag of CH1** This bit is the mirror of SHRTLED_CH1, OL_CH1, OUTOV_CH1 combined in logic OR
TSD	1	r	**Over Temperature Shutdown** 0_B , T_j below temperature shutdown threshold 1_B , Overtemperature condition detected since last readout
TW	0	r	**Over Temperature Warning** 0_B , T_j below temperature warning threshold 1_B , T_j exceeds temperature warning threshold

12.6.2 Register structure

Table 18 describes in detail the available registers with their bit-fields function, size and position
Table 16 and **Table 17** show register addresses and summarize bit-field position inside each register

Table 16 Register Bank 0

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**W/R**	**RB**	**ADDR**						**Data**							
LEDCURRADIM_CH1	W/R	0	0	0	0	0	0	0	ADIMVAL_CH1							
LEDCURRCAL_CH1	W/R	0	0	0	0	0	1	1	x	DAC_OFF_CH1	SOCAL_CH1	EOCAL_CH1	CALIBVAL_CH1			
SWTMOD	W/R	0	0	0	0	1	0	1	x	x	x	x	x	ENSPREAD	FMSPREAD	FDEVSPREAD
DVCCTRL	W/R	0	0	0	0	1	1	0	x	x	x	x	x	CLRLAT	SWRST	IDLE
MFSSETUP1_CH1	W/R	0	0	0	1	0	0	1	x	x	x	x	LEDCHAIN_CH1			
CURRMON_CH1	W/R	0	0	0	1	1	0	0	x	x	x	x	SOMON_CH1	EOMON_CH1	LEDCURR_CH1	
FAULTS_CH1	W/R	0	0	0	1	1	1	1	OUTOC_CH1	x	x	OUTOVLAT_CH1	x	OUTOV_CH1	OL_CH1	SHRTLED_CH1
LOOPCTRL_CH1	W/R	0	0	1	0	0	0	1	PWM_1	x	x	x	x	x	x	ENCAL_CH1

Table 17 Register Bank 1

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**W/R**	**RB**	**ADDR**						**Data**							
LEDCURRADIM_CH2	W/R	1	0	0	0	0	0	1	ADIMVAL_CH2							
LEDCURRCAL_CH2	W/R	1	0	0	0	0	1	0	x	DAC_OFF_CH2	SOCAL_CH2	EOCAL_CH2	CALIBVAL_CH2			
MFSSETUP1_CH2	W/R	1	0	0	1	0	0	0	x	x	x	x	LEDCHAIN_CH2			
CURRMON_CH2	W/R	1	0	0	1	1	0	1	x	x	x	x	SOMON_CH2	EOMON_CH2	LEDCURR_CH2	

Table 17 Register Bank 1 (cont'd)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULTS_CH2	W/R	1	0	0	1	1	1	0	OUTOC_CH2	x	x	OUTOVLAT_CH2	x	OUTOV_CH2	OL_CH2	SHRTLED_CH2
LOOPCTRL_CH2	W/R	1	0	1	0	0	0	0	PWM_2	x	x	x	x	x	x	ENCAL_CH2

A write to a non existing address is ignored, a read to a non existing register is ignored and the STD Diagnosis Frame is send out.

Table 18 Register description

Register name	Field	Bits	Type	Purpose
LEDCURRADIM_CH1,2	ADIMVAL_CH1,2	7:0	r/w	**LED Current Configuration Register** 00000000_B, analog dimming @ 0% of LED current fixed via $R_{FB1,2}$ 11110000_B, (default) analog dimming @ 100% of LED current fixed via $R_{FB1,2}$
LEDCURRCAL_CH1,2	CALIBVAL_CH1,2	3:0	r/w	**LED Current Accuracy Trimming Configuration Register** LED current calibration value definition, the first bit is the calibration sign: 0000_B, (default) Initial state in the middle of the range 0111_B, maximum calibration value positive 1111_B, maximum calibration value negative
	EOCAL_CH1,2	4	r	End of calibration routine signalling bit: 0_B, (default) calibration routine not completed, not successfully performed or never run. 1_B, calibration successfully performed (is reset to 0_B when SOCAL_CH1,2 is set to 1_B)
	SOCAL_CH1,2	5	r/w	Start of calibration routine signalling bit: 0_B, (default) no calibration routine started 1_B, calibration routine start (autoclear)
	DAC_OFF_CH1,2	6	r/w	Switch OFF internal analog dimming DAC bit: 0_B, (default) internal DAC active 1_B, internal DAC inactive and analog dimming error amplifier reference mapped to SET1,2 pin

Table 18 Register description (cont'd)

Register name	Field	Bits	Type	Purpose
SWTMOD	FDEVSPREAD	0	r/w	**Switching Mode Configuration Register** Deviation Frequency f_{DEV} definition: 0_B , (default) ±20% of f_{SW} 1_B , ±10% of f_{SW}
	FMSPREAD	1	r/w	Frequency Modulation Frequency f_{FM} definition: 0_B , (default) 12 kHz 1_B , 18 kHz
	ENSPREAD	2	r/w	Enable Spread Spectrum feature: 0_B , Spread Spectrum modulation disabled 1_B , (default) Spread Spectrum modulation enabled
DVCCTRL	IDLE	0	r/w	**Device Control Register** IDLE mode configuration bit: 0_B , ACTIVE mode (default) 1_B , IDLE mode
	SWRST	1	r/w	Software reset bit: 0_B , (default) normal operation 1_B , execute reset command
	CLRLAT	2	r/w	Clear Latch bit: 0_B , (default) normal operation 1_B , execute CLRLAT command
MFSSETUP1_CH1,2	LEDCHAIN_CH1,2	3:0	r/w	**Short Circuit configuration Register** Short circuit threshold and MFS ratio bits: change the $V_{VFB1,2\_S2G}$ threshold 0001_B, smallest Value 1 Step 0010_B, (default) 2 Steps 1000_B, 8 Steps 1111_B, 15 Steps 0000_B, largest Value 16 Steps
CURRMON_CH1,2	LEDCURR_CH1,2	1:0	r	**Current Monitor Register** Status of the LED Current bits: 00_B , (default) LED current between Target and +25% 01_B , LED current above +25% of Target 10_B , LED current between Target and -25% 11_B , LED current below -25% of Target
	EOMON_CH1,2	2	r	End of LED/Input Current Monitoring bits: 0_B , (default) Current monitoring routine not completed, not successfully performed or never run. 1_B , Current Monitor routine successfully performed (is reset to 0_B when SOMON_CH1,2 is set to 1_B)
	SOMON_CH1,2	3	r/w	Start of LED/Input Current Monitoring bits: 0_B , (default) Current monitor routine not started 1_B , Start of the current monitor routine

Table 18 Register description (cont'd)

Register name	Field	Bits	Type	Purpose
FAULTS_CH1,2	SHRTLED_CH1,2	0	r	**Detailed Fault and Diagnosis Registers** Shorted Load Diagnosis Bit: 0_B , Short circuit condition not detected since last readout 1_B , Short circuit condition detected since last readout This bit is latched and automatically cleared after a FAULTS_CH1,2 register reading
	OL_CH1,2	1	r	Open Load in ON state Diagnosis Bit: 0_B , Open load condition not detected since last readout 1_B , Open load condition detected since last readout This bit is latched and automatically cleared after a FAULTS_CH1,2 register reading
	OUTOV_CH1,2	2	r	Output overvoltage Monitor Bit: 0_B , Output overvoltage not detected since last readout 1_B , Output overvoltage detected since last readout This bit is latched and automatically cleared after a FAULTS_CH1,2 register reading (default condition if OUTOVLAT_CH1,2 is not set). See **Chapter 10.2.2** for further details.
	OUTOVLAT_CH1,2	4	r/w	Output latch after overvoltage error enable Bit: 0_B , (default) gate driver outputs are autorestarting after an overvoltage event 1_B , gate drivers are latched low (output Mos are High Impedance) and bit OUTOV_CH1,2 is latched after an overvoltage event until a CLRLAT command
	OUTOC_CH1,2	7	r	Output overcurrent Monitor Bit: 0_B , Output overcurrent not detected since last readout 1_B , Output overcurrent detected since last readout This bit is latched and automatically cleared after a FAULTS_CH1,2 register reading
LOOPCTRL_CH1,2	ENCAL_CH1,2	0	r/w	**Loop Control Register** Enable automatic output current calibration Bits of CH1,2: 0_B , (default) DAC of CH1,2 takes CALIBVAL_CH1,2 from SPI registers 1_B , DAC of CH1,2 takes CALIBVAL_CH1,2 from last completed automatic calibration procedure; SOCAL_CH1,2 bits can be set.
	PWM_1,2	7	r/w	Bits to enable/disable the gate drivers of the main switches (gate driver resulting status is the OR function with the PWMI1,2 pins value): 0_B , (default) disable 1_B , enable

13 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

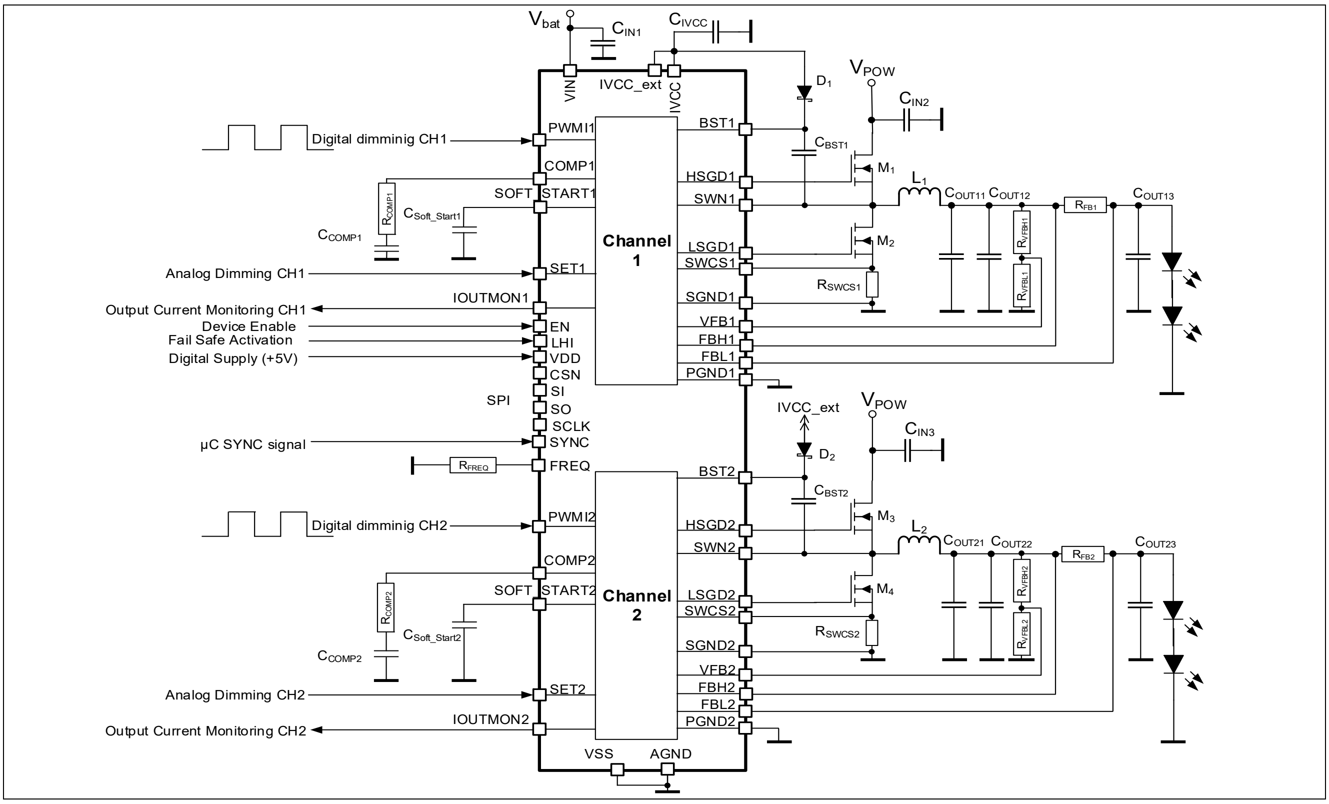


Figure 37 Application Drawing - TLD5501-2QV as BUCK current Regulator, Separate Channels

Table 19 BOM - TLD5501-2QV as BUCK current regulator

Reference Designator	Value	Manufacturer	Part Number	Type
D_1 , D_2	BAT46WJ	--	BAT46WJ	Diode
C_{IN2}, C_{IN3}	4.7 µF, 100 V	TDK	X7R	Capacitor
C_{COMP1}, C_{COMP2}	22n F, 16 V	TDK	X7R	Capacitor
C_{SOFT_START1} , C_{SOFT_START2}	22 nF, 16 V	TDK	X7R	Capacitor
C_{OUT11}, C_{OUT21}, $C_{OUT12,}$ C_{OUT22}	4.7 µF, 60 V	TDK	X7R	Capacitor
C_{IN1}, C_{OUT13} , C_{OUT23}	100 nF, 60 V	TDK	X7R	Capacitor
C_{OUT23}	100 µF, 80 V	TDK	Tantalum	Capacitor
C_{IVCC}	10 µF, 16 V	TDK	X7R	Capacitor
C_{BST1} , C_{BST2}	100 nF, 16 V	TDK	X7R	Capacitor
IC_1	--	Infineon	TLD5501-2QV	IC
L_1 , L_2	10 µH	Coilcraft	XAL1010-103MEC	Inductor
R_{FB1}, R_{FB2}	0.50 Ω, 1%	Panasonic	--	Resistor

Table 19 BOM - TLD5501-2QV as BUCK current regulator

Reference Designator	Value	Manufacturer	Part Number	Type
R_{VFBL1} , R_{VFBL2}	1.5 kΩ, 1%	Panasonic	--	Resistor
R_{VFBH1}, R_{VFBH2}	56 kΩ, 1%	Panasonic	--	Resistor
R_{COMP1},R_{COMP2}	0 Ω, 5%	Panasonic	--	Resistor
R_{FREQ}	37.4 kΩ, 1%	Panasonic	--	Resistor
R_{SWCS1} , R_{SWCS2}	0.005 Ω, 1%	Panasonic	ERJB1CFR05U	Resistor
M_1 , M_2, M_3 , M_4	Dual MOSFET: 100 V / 26 mΩ N-ch	Infineon	IPG20N06S4L-26	Transistor

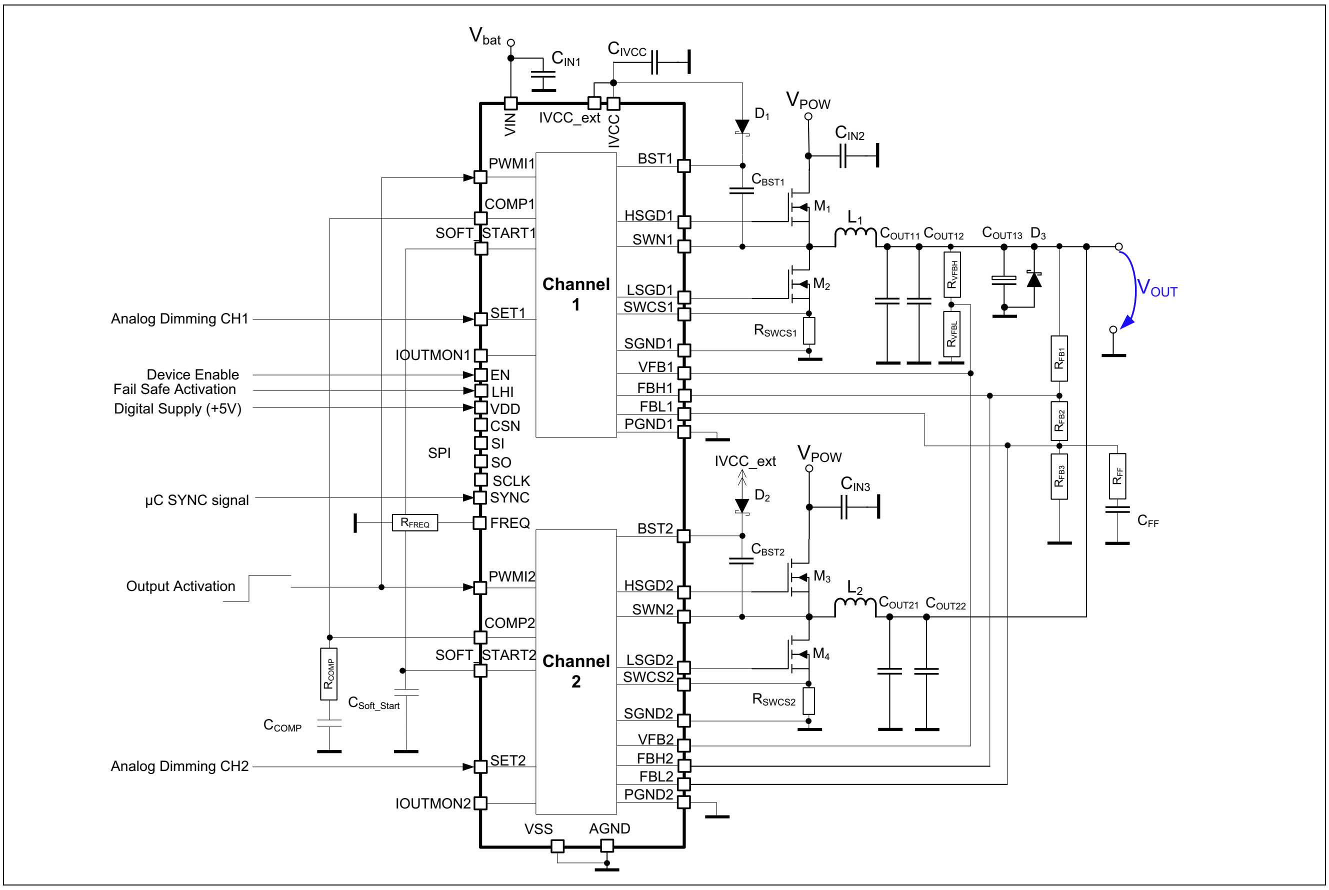


Figure 38 Application Drawing - TLD5501-2QV as BUCK voltage regulator parallel channels

Table 20 BOM - TLD5501-2QV as BUCK voltage regulator with parallel channels

Reference Designator	Value	Manufacturer	Part Number	Type
D_1 , D_2	BAT46WJ	--	--	Diode
C_{IN2} , C_{IN3}	4.7 µF, 50 V	TDK	X7R	Capacitor
C_{COMP}	39 nF, 16 V	TDK	X7R	Capacitor
C_{SOFT_START}	47 nF, 16 V	TDK	X7R	Capacitor
C_{FF}	68nF, 50V	TDK	X7R	Capacitor
C_{OUT11}, C_{OUT21}, C_{OUT12}, C_{OUT22}	4.7 µF, 60 V	TDK	X7R	Capacitor

Table 20 BOM - TLD5501-2QV as BUCK voltage regulator with parallel channels

Reference Designator	Value	Manufacturer	Part Number	Type
C_{OUT13}	100 µF, 80 V	--	Electrolytic	Capacitor
C_{IVCC}	10 µF, 16 V	TDK	X7R	Capacitor
C_{BST1} , C_{BST2}	100 nF, 16 V	TDK	X7R	Capacitor
IC_1	--	Infineon	TLD5501-2QV	IC
L_{OUT1} , L_{OUT2}	10 µH	Coilcraft	XAL1010-103MEC	Inductor
R_{FB1} , R_{FB2} , R_{FB3}	0, 150Ω, 48kΩ 1%	Panasonic	--	Resistor
R_{VFBL} , R_{VFBH}	1.5 kΩ, 56 kΩ, 1%	Panasonic	--	Resistor
R_{COMP}	1 kΩ	Panasonic	--	Resistor
R_{FF}	470Ω 1%	Panasonic	--	Resistor
R_{FREQ}	37.4 kΩ, 1%	Panasonic	--	Resistor
R_{SWCS1} , R_{SWCS2}	0.005 Ω, 1%	Panasonic	ERJB1CFR05U	Resistor
M_1 , M_2 , M_3 , M_4	Dual MOSFET: 100 V / 14 mΩ N-ch	Infineon	IPG20N06S4L-14	Transistor

13.1 Further Application Information

- For further information you may contact **http://www.infineon.com/**

14 Package Outlines

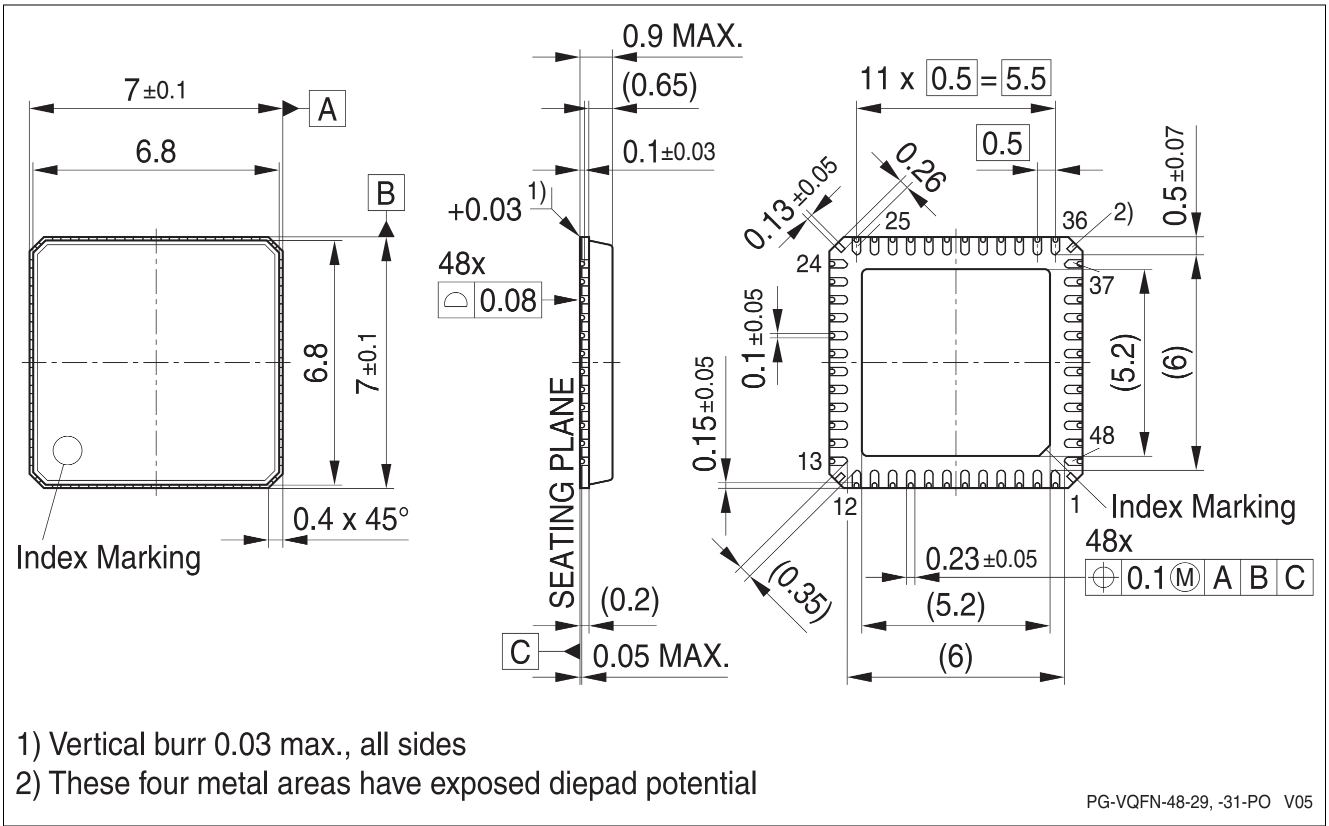


Figure 39 PG-VQFN-48 (with LTI)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

15 Revision History

Revision	Date	Changes
Rev. 2.00	2021-03-26	Editorial changes and typos
Rev. 2.00	2021-03-26	Change package name and updated product validation AEC Q100
Rev. 2.00	2021-03-26	Update **Figure 2**
Rev. 2.00	2021-03-26	Update footnotes of **Table 3**
Rev. 2.00	2021-03-26	P_4.2.1, P_4.3.2, P_6.4.43, P_6,4,47, P_6.4.64, P_10.8.30, P_10.8.31, P_10.8.21: added notes
Rev. 2.00	2021-03-26	P_5.3.7 min: 1.64 → 1.6, max: 1.86 → 1.9
Rev. 2.00	2021-03-26	Update **Chapter 6.1**
Rev. 2.00	2021-03-26	Update **Figure 7**
Rev. 2.00	2021-03-26	Improved description of **Adjustable Soft Start Ramp Chapter 6.2**
Rev. 2.00	2021-03-26	Update **Figure 8**
Rev. 2.00	2021-03-26	Improved description of Programming Output Voltage (Constant Voltage Regulation **Chapter 6.5**)
Rev. 2.00	2021-03-26	Added P_6.6.1
Rev. 2.00	2021-03-26	Update **Chapter 8**
Rev. 2.00	2021-03-26	Update **Chapter 8.1**
Rev. 2.00	2021-03-26	Improved description of **Output current Monitoring Chapter 10.3**
Rev. 2.00	2021-03-26	Added note in **Spread Spectrum** description **Chapter 11.3**
Rev. 2.00	2021-03-26	Removed introduction table in **Chapter 12.6**
Rev. 2.00	2021-03-26	Added **Table 15**
Rev. 2.00	2021-03-26	Update **Chapter 12.6.1**
Rev. 2.00	2021-03-26	Update **Table 16** and **Table 17**
Rev. 2.00	2021-03-26	Update BOM **Table 19** and **Table 20**
Rev. 2.00	2021-03-26	Update **Figure 38**
Rev. 1.00	2017-07-11	Initial Datasheet

Table of Content

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Document reference
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