5-Bit Adjustable, Wide Operating Range, No R_{SENSE}™ Step-Down Controller

FEATURES

- **5-Bit Programmable Output Voltage: 0.925V to 2V**
- **No Sense Resistor Required**
- **True Current Mode Control**
- **2% to 90% Duty Cycle at 200kHz**
- **$t_{ON(MIN)}$ < 100ns**
- **Supports Active Voltage Positioning**
- **Extremely Fast Transient Response**
- **Stable with Ceramic C_{OUT}**
- Dual N-Channel MOSFET Synchronous Drive
- Power Good Output Voltage Monitor
- Wide V_{IN} Range: 4V to 36V
- ±1% 0.8V Reference
- Adjustable Current Limit
- Adjustable Switching Frequency
- Programmable Soft-Start
- Output Overvoltage Protection
- Optional Short-Circuit Shutdown Timer
- Micropower Shutdown: I_Q < 30µA
- Available in 24-Lead Narrow SSOP Package

APPLICATIONS

- Power Supplies for Mobile Pentium® Processors
- Notebook and Palmtop Computers, PDAs

DESCRIPTION

The LTC®3711 is a synchronous step-down switching regulator controller for CPU power. An output voltage between 0.925V and 2.000V is selected by a 5-bit code (Intel mobile VID specification). The controller uses a valley current control architecture to deliver very low duty cycles without requiring a sense resistor. Operating frequency is selected by an external resistor and is compensated for variations in V_{IN} and V_{OUT}.

Discontinuous mode operation provides high efficiency operation at light loads. A forced continuous control pin reduces noise and RF interference and can assist secondary winding regulation by disabling discontinuous mode operation when the main output is lightly loaded.

Fault protection is provided by internal foldback current limiting, an output overvoltage comparator and optional short-circuit shutdown timer. Soft-start capability for supply sequencing is accomplished using an external timing capacitor. The regulator current limit level is user programmable. Wide supply range allows operation from 4V to 36V at the input.

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No R_{SENSE} is a trademark of Linear Technology Corporation.
Pentium is a registered trademark of Intel Corporation.

TYPICAL APPLICATION

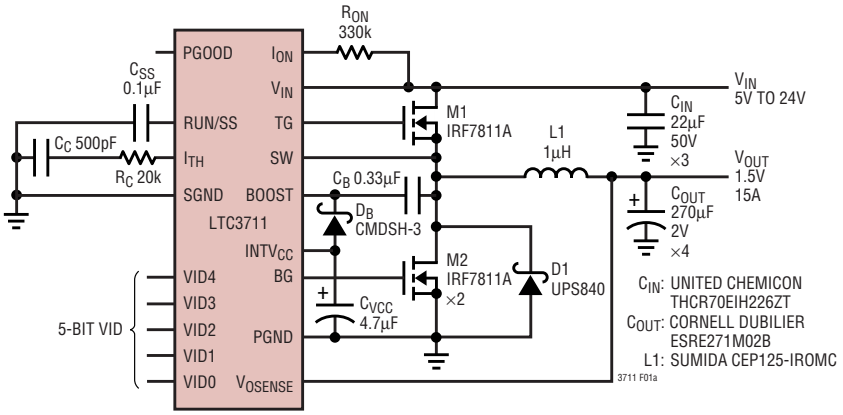
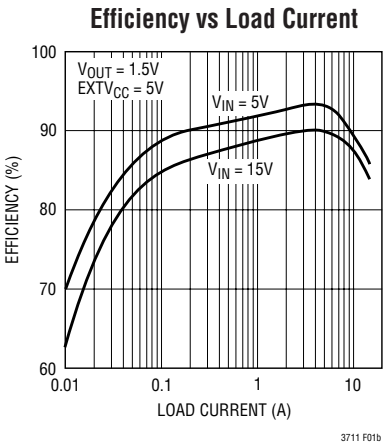


Figure 1. High Efficiency Step-Down Converter

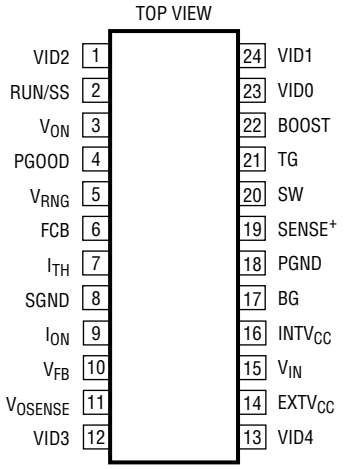


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage
V_{IN}, I_{ON} ..... 36V to –0.3V
Boosted Topside Driver Supply Voltage
BOOST ..... 42V to –0.3V
SW, SENSE+ Voltages ..... 36V to –5V
$EXTV_{CC}$, (BOOST – SW), RUN/SS,
VID0-VID4, PGOOD Voltages ..... 7V to –0.3V
FCB, V_{ON}, V_{RNG} Voltages ..... $INTV_{CC}$ + 0.3V to –0.3V
I_{TH}, V_{FB}, V_{OSENSE} Voltages ..... 2.7V to –0.3V
TG, BG, $INTV_{CC}$, $EXTV_{CC}$ Peak Currents 2A
TG, BG, $INTV_{CC}$, $EXTV_{CC}$ RMS Currents 50mA
Operating Ambient Temperature Range
LTC3711EGN (Note 2) ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC3711EGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
I_Q	Input DC Supply Current Normal Shutdown Supply Current				 900 15	 2000 30	 µA µA
V_{FB}	Feedback Reference Voltage	I_{TH} = 1.2V (Note 4)	●	0.792	0.800	0.808	V
$\Delta V_{FB(LINEREG)}$	Feedback Voltage Line Regulation	V_{IN} = 4V to 30V, I_{TH} = 1.2V (Note 4)			0.002		%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	I_{TH} = 0.5V to 1.9V (Note 4)	●		–0.05	–0.3	%
I_{FB}	Feedback Input Current	V_{FB} = 0.8V			–5	±50	nA
$g_{m(EA)}$	Error Amplifier Transconductance	I_{TH} = 1.2V (Note 4)	●	1.4	1.7	2	mS
V_{FCB}	Forced Continuous Threshold		●	0.76	0.8	0.84	V
I_{FCB}	Forced Continuous Pin Current	V_{FCB} = 0.8V			–1	–2	µA
t_{ON}	On-Time	I_{ON} = 60µA, V_{ON} = 1.5V I_{ON} = 30µA, V_{ON} = 1.5V		212 425	250 500	288 575	ns ns
$t_{ON(MIN)}$	Minimum On-Time	I_{ON} = 180µA, V_{ON} = 0V			50	100	ns
$t_{OFF(MIN)}$	Minimum Off-Time	I_{ON} = 60µA, V_{ON} = 1.5V			250	400	ns
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold $V_{PGND} – V_{SENSE^+}$	V_{RNG} = 1V, V_{FB} = 0.76V V_{RNG} = 0V, V_{FB} = 0.76V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.76V	 ●	113 79 158	133 93 186	153 107 214	mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold $V_{PGND} – V_{SENSE^+}$	V_{RNG} = 1V, V_{FB} = 0.84V V_{RNG} = 0V, V_{FB} = 0.84V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.84V			–67 –47 –93		mV mV mV
$\Delta V_{FB(OV)}$	Output Overvoltage Fault Threshold			5.5	7.5	9.5	%
$V_{FB(UV)}$	Output Undervoltage Fault Threshold			520	600	680	mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{RUN/SS(ON)}$	RUN Pin Start Threshold		●	0.8	1.5	2	V
$V_{RUN/SS(LE)}$	RUN Pin Latchoff Enable Threshold	RUN/SS Pin Rising			4	4.5	V
$V_{RUN/SS(LT)}$	RUN Pin Latchoff Threshold	RUN/SS Pin Falling			3.5	4.2	V
$I_{RUN/SS(C)}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 0V		–0.5	–1.2	–3	µA
$I_{RUN/SS(D)}$	Soft-Start Discharge Current	$V_{RUN/SS}$ = 4.5V, V_{FB} = 0V		0.8	1.8	3	µA
$V_{IN(UVLO)}$	Undervoltage Lockout	V_{IN} Falling	●		3.4	3.9	V
$V_{IN(UVLOR)}$	Undervoltage Lockout Release	V_{IN} Rising	●		3.5	4	V
TG R_{UP}	TG Driver Pull-Up On Resistance	TG High			2	3	Ω
TG R_{DOWN}	TG Driver Pull-Down On Resistance	TG Low			2	3	Ω
BG R_{UP}	BG Driver Pull-Up On Resistance	BG High			3	4	Ω
BG R_{DOWN}	BG Driver Pull-Down On Resistance	BG Low			1	2	Ω
TG t_r	TG Rise Time	C_{LOAD} = 3300pF			20		ns
TG t_f	TG Fall Time	C_{LOAD} = 3300pF			20		ns
BG t_r	BG Rise Time	C_{LOAD} = 3300pF			20		ns
BG t_f	BG Fall Time	C_{LOAD} = 3300pF			20		ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V	●	4.7	5	5.3	V
$\Delta V_{LDO(LOADREG)}$	Internal V_{CC} Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 4V			–0.1	±2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, V_{EXTVCC} Rising	●	4.5	4.7		V
ΔV_{EXTVCC}	$EXTV_{CC}$ Switch Drop Voltage	I_{CC} = 20mA, V_{EXTVCC} = 5V			150	300	mV
$\Delta V_{EXTVCC(HYS)}$	$EXTV_{CC}$ Switchover Hysteresis				200		mV
PGOOD Output							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		5.5	7.5	9.5	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		–5.5	–7.5	–9.5	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning			1	2	%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.15	0.4	V
VID DAC							
$V_{VID(T)}$	VID0-VID4 Logic Threshold Voltage			0.4	1.2	2	V
$I_{VID(PULLUP)}$	VID0-VID4 Pull-Up Current	V_{VID0} to V_{VID4} = 0V			–2.5		µA
$V_{VID(PULLUP)}$	VID0-VID4 Pull-Up Voltage	V_{VID0} to V_{VID4} Open			4.5		V
$I_{VID(LEAK)}$	VID0-VID4 Leakage Current	V_{VID0} to V_{VID4} = 5V, $V_{RUN/SS}$ = 0V			0.01	1	µA
R_{VID}	Resistance from V_{OSENSE} to V_{FB}			6	10	14	KΩ
ΔV_{OSENSE}	DAC Output Accuracy	V_{OSENSE} Programmed from 0.925V to 2V (Note 5)		–0.25	0	0.25	%

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3711E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

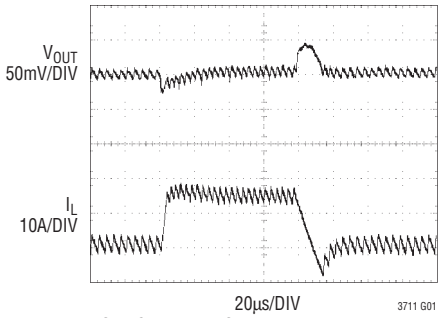
LTC3711EGN: $T_J = T_A + (P_D \bullet 130°C/W)$

Note 4: The LTC3711 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

Note 5: The LTC3711 VID DAC is tested in a feedback loop that adjusts V_{OSENSE} to achieve a specified feedback voltage (V_{FB} = 0.8V) for each DAC VID code.

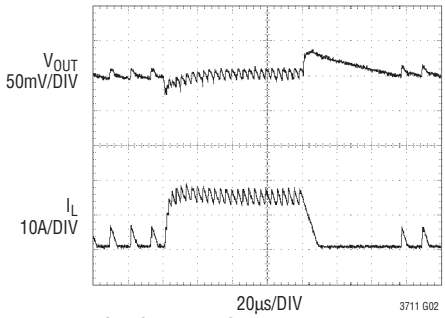
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response



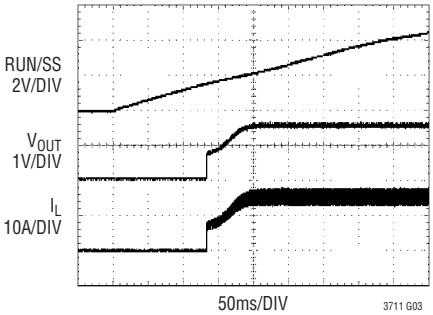
LOAD STEP = 0A TO 15A
V_{IN} = 15V
V_{OUT} = 1.5V
FCB = 0V
FIGURE 9 CIRCUIT

Transient Response (Discontinuous Mode)



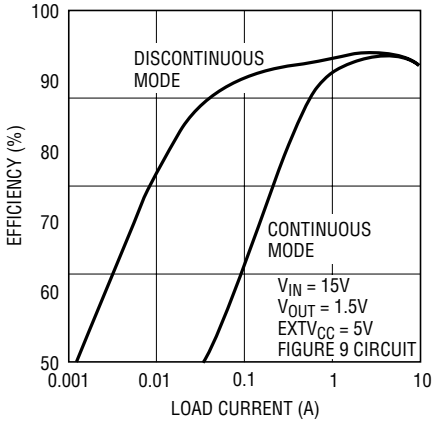
LOAD STEP = 1A TO 15A
V_{IN} = 15V
V_{OUT} = 1.5V
FCB = $INTV_{CC}$
FIGURE 9 CIRCUIT

Start-Up

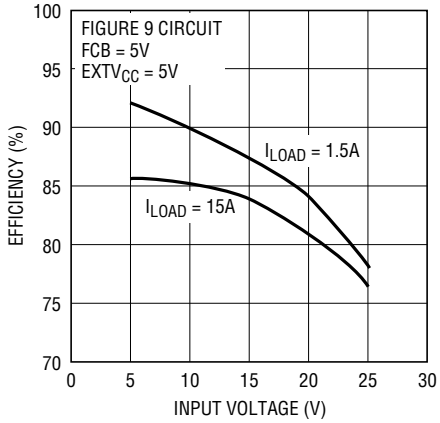


V_{IN} = 15V
V_{OUT} = 1.5V
R_{LOAD} = 0.1Ω
FIGURE 9 CIRCUIT

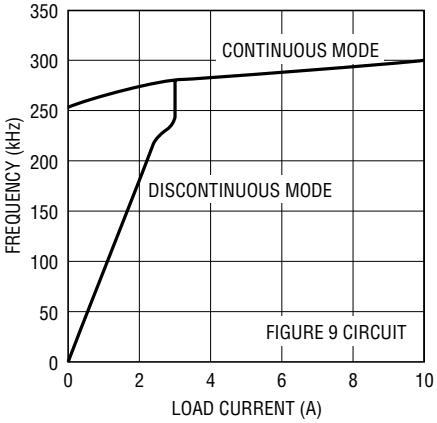
Efficiency vs Load Current



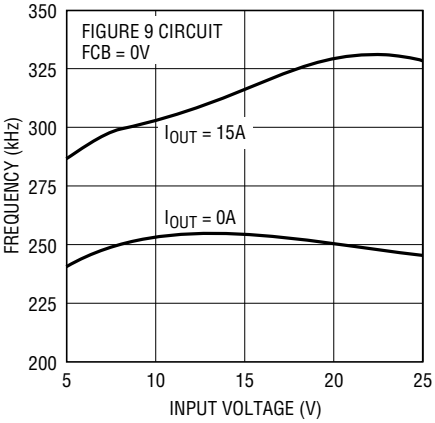
Efficiency vs Input Voltage



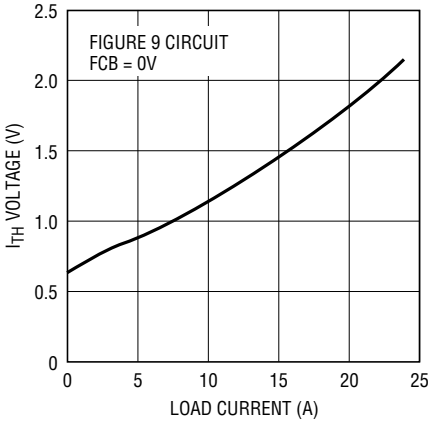
Frequency vs Load Current



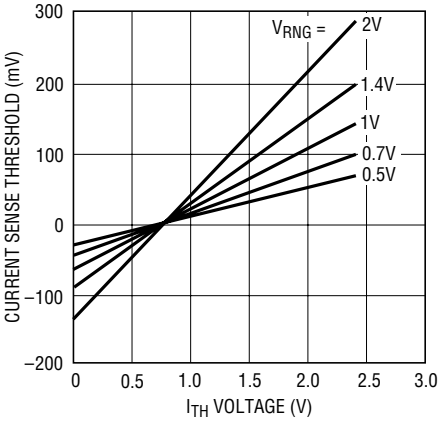
Frequency vs Input Voltage



I_{TH} Voltage vs Load Current

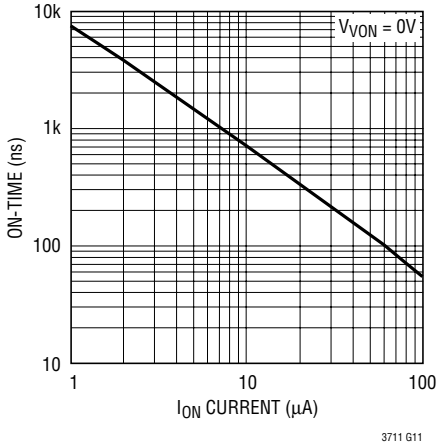


Current Sense Threshold vs I_{TH} Voltage

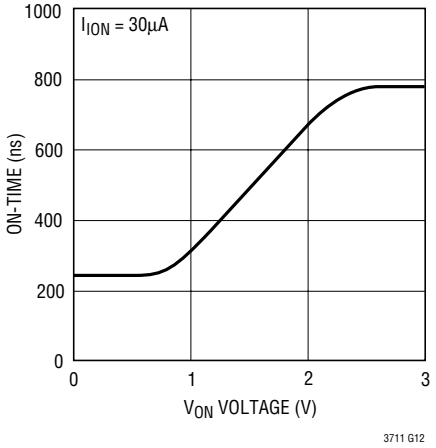


TYPICAL PERFORMANCE CHARACTERISTICS

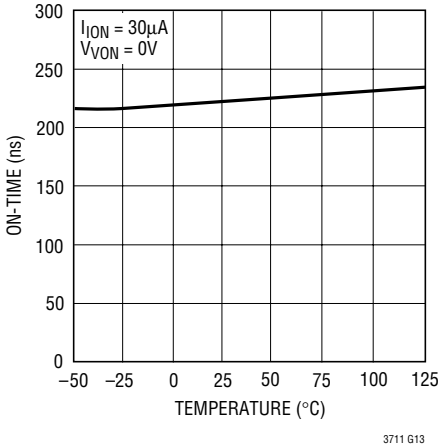
On-Time vs I_{ON} Current



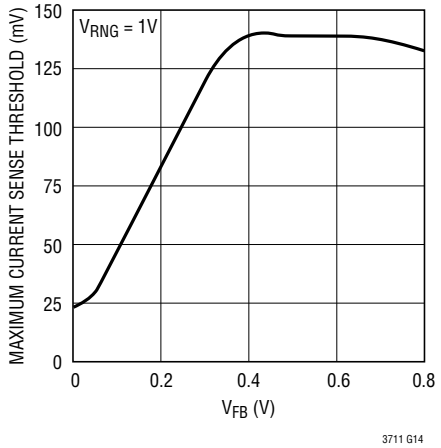
On-Time vs V_{ON} Voltage



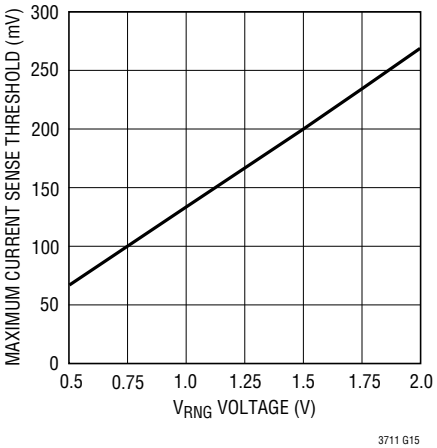
On-Time vs Temperature



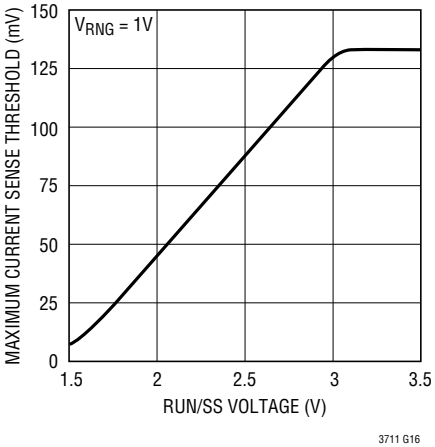
Current Limit Foldback



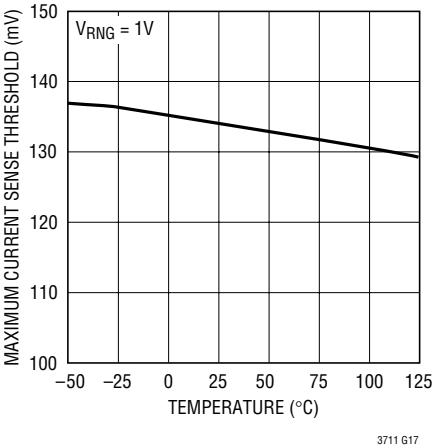
Maximum Current Sense Threshold vs V_{RNG} Voltage



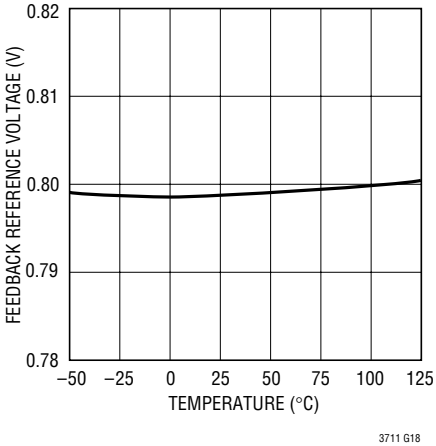
Maximum Current Sense Threshold vs RUN/SS Voltage



Maximum Current Sense Threshold vs Temperature

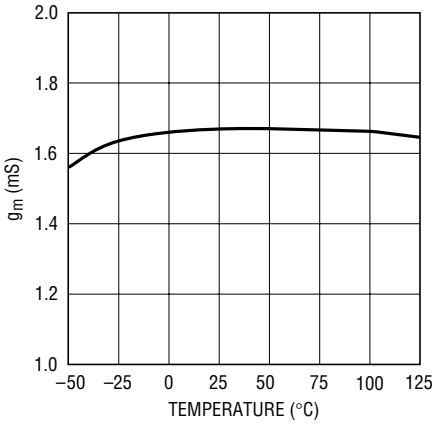


Feedback Reference Voltage vs Temperature



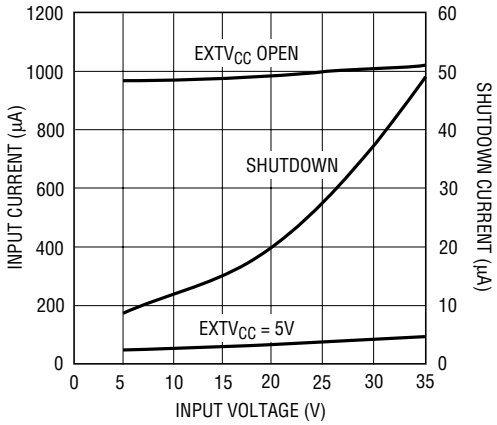
TYPICAL PERFORMANCE CHARACTERISTICS

Error Amplifier g_m vs Temperature



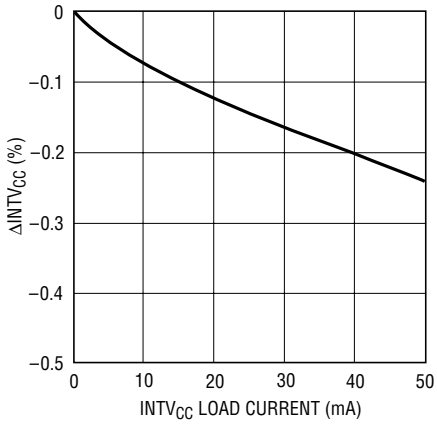
3711 G19

Input and Shutdown Currents vs Input Voltage



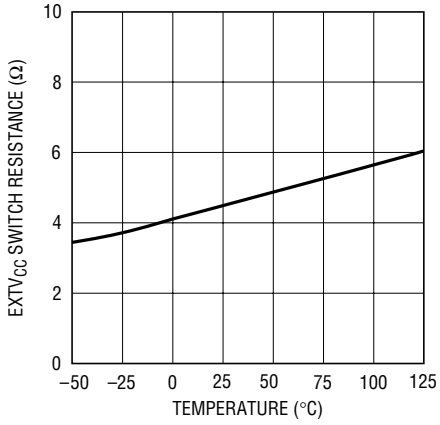
3711 G20

$INTV_{CC}$ Load Regulation



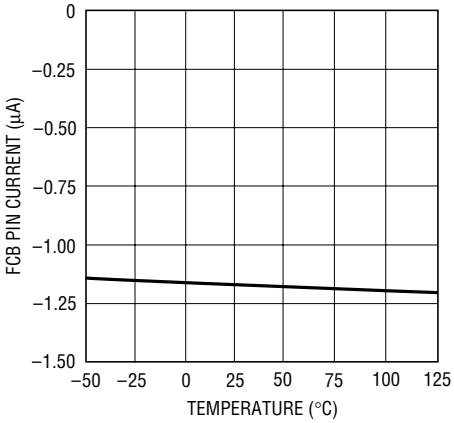
3711 G21

$EXTV_{CC}$ Switch Resistance vs Temperature



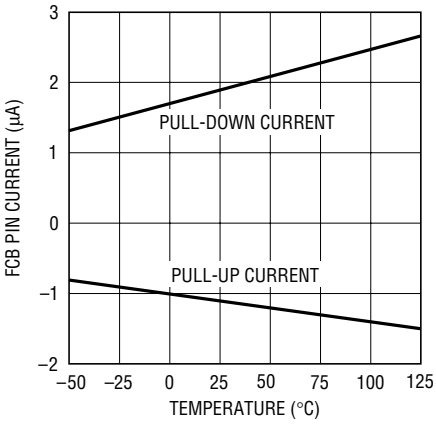
3711 G22

FCB Pin Current vs Temperature



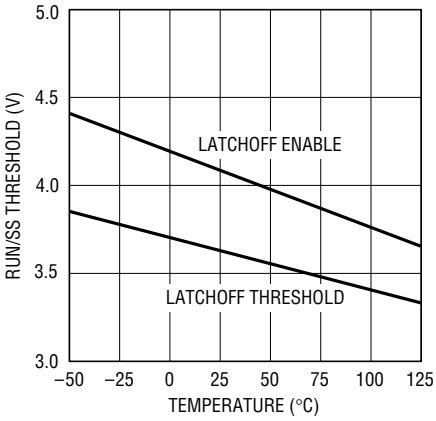
3711 G23

RUN/SS Pin Current vs Temperature



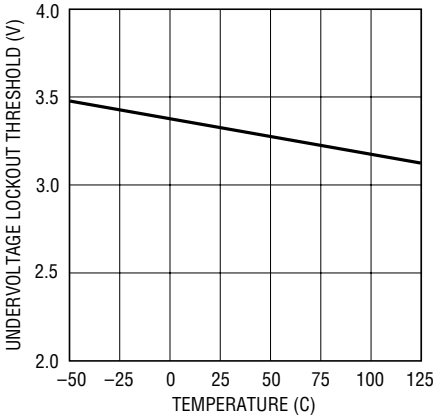
3711 G24

RUN/SS Latchoff Thresholds vs Temperature



3711 G25

Undervoltage Lockout Threshold vs Temperature



3711 G26

PIN FUNCTIONS

VID0-VID4 (Pins 23, 24, 1, 12, 13): VID Digital Inputs. The voltage identification (VID) code sets the internal feedback resistor divider ratio for different output voltages as shown in Table 1. If unconnected, the pins are pulled high by internal 2.5μA current sources.

RUN/SS (Pin 2): Run Control and Soft-Start Input. A capacitor to ground at this pin sets the ramp time to full output current (approximately 3s/μF) and the time delay for overcurrent latchoff (see Applications Information). Forcing this pin below 0.8V shuts down the device.

V_{ON} (Pin 3): On-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to V_{OUT}. The comparator input defaults to 0.7V when the pin is grounded, 2.4V when the pin is tied to $INTV_{CC}$.

PGOOD (Pin 4): Power Good Output. Open drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

V_{RNG} (Pin 5): Sense Voltage Range Input. The voltage at this pin is ten times the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from $INTV_{CC}$. The nominal sense voltage defaults to 70mV when this pin is tied to ground, 140mV when tied to $INTV_{CC}$.

FCB (Pin 6): Forced Continuous Input. Tie this pin to ground to force continuous synchronous operation at low load, to $INTV_{CC}$ to enable discontinuous mode operation at low load or to a resistive divider from a secondary output when using a secondary winding.

I_{TH} (Pin 7): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.8V corresponding to zero sense voltage (zero current).

SGND (Pin 8): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

I_{ON} (Pin 9): On-Time Current Input. Tie a resistor from V_{IN} to this pin to set the one-shot timer current and thereby set the switching frequency.

V_{FB} (Pin 10): Error Amplifier Feedback Input. This pin connects to both the error amplifier input and to the output of the internal resistive divider. It can be used to attach additional compensation components if desired.

V_{OSENSE} (Pin 11): Output Voltage Sense. The output voltage connects here to the input of the internal resistive feedback divider.

$EXTV_{CC}$ (Pin 14): External V_{CC} Input. When $EXTV_{CC}$ exceeds 4.7V, an internal switch connects this pin to $INTV_{CC}$ and shuts down the internal regulator so that controller and gate drive power is drawn from $EXTV_{CC}$. Do not exceed 7V at this pin and ensure that $EXTV_{CC} < V_{IN}$.

V_{IN} (Pin 15): Main Input Supply. Decouple this pin to PGND with an RC filter (1Ω, 0.1μF).

$INTV_{CC}$ (Pin 16): Internal 5V Regulator Output. The driver and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7μF low ESR tantalum capacitor.

BG (Pin 17): Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and $INTV_{CC}$.

PGND (Pin 18): Power Ground. Connect this pin closely to the source of the bottom N-channel MOSFET, the (–) terminal of C_{VCC} and the (–) terminal of C_{IN}.

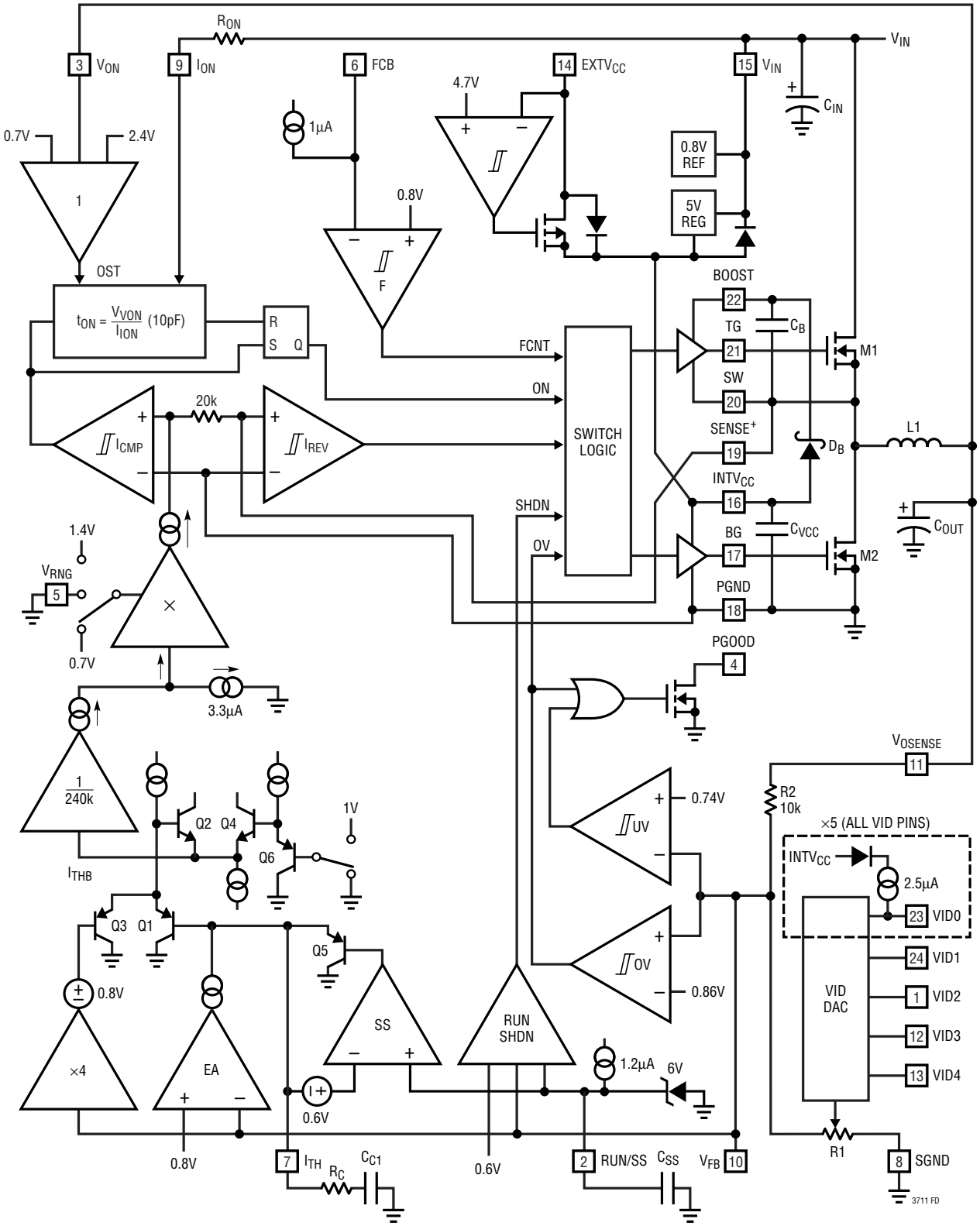
$SENSE^+$ (Pin 19): Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the SW node unless using a sense resistor (see Applications Information).

SW (Pin 20): Switch Node. The (–) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below ground up to V_{IN}.

TG (Pin 21): Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

BOOST (Pin 22): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below $INTV_{CC}$ up to $V_{IN} + INTV_{CC}$.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3711 is a current mode controller for DC/DC step-down converters. In normal operation, the top MOSFET is turned on for a fixed interval determined by a one-shot timer OST. When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator I_{CMP} trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage between the PGND and SENSE$^+$ pins using either the bottom MOSFET on-resistance or an optional sense resistor. The voltage on the I_{TH} pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this voltage by comparing the feedback signal V_{FB} from the output voltage with an internal 0.8V reference. The feedback voltage is derived from the output voltage by a resistive divider DAC that is set by the VID code pins VID0-VID4. If the load current increases, it causes a drop in the feedback voltage relative to the reference. The I_{TH} voltage then rises until the average inductor current again matches the load current.

At low load currents, the inductor current can drop to zero and become negative. This is detected by current reversal comparator I_{REV} which then shuts off M2, resulting in discontinuous operation. Both switches will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current level (0.8V) to initiate another cycle. Discontinuous mode operation is disabled by comparator F when the FCB pin is brought below 0.8V, forcing continuous synchronous operation.

The operating frequency is determined implicitly by the top MOSFET on-time and the duty cycle required to maintain regulation. The one-shot timer generates an on-time that is proportional to the ideal duty cycle, thus holding frequency approximately constant with changes in V_{IN} and V_{OUT}. The nominal frequency can be adjusted with an external resistor R_{ON}.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a ±7.5% window around the regulation point. Furthermore, in an overvoltage condition, M1 is turned off and M2 is turned on and held on until the overvoltage condition clears.

Foldback current limiting is provided if the output is shorted to ground. As V_{FB} drops, the buffered current threshold voltage I_{THB} is pulled down by clamp Q3 to a 1V level set by Q4 and Q6. This reduces the inductor valley current level to one sixth of its maximum value as V_{FB} approaches 0V.

Pulling the RUN/SS pin low forces the controller into its shutdown state, turning off both M1 and M2. Releasing the pin allows an internal 1.2μA current source to charge up an external soft-start capacitor C_{SS}. When this voltage reaches 1.5V, the controller turns on and begins switching, but with the I_{TH} voltage clamped at approximately 0.6V below the RUN/SS voltage. As C_{SS} continues to charge, the soft-start current limit is removed.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the internal controller circuitry is derived from the $INTV_{CC}$ pin. The top MOSFET driver is powered from a floating bootstrap capacitor C_B. This capacitor is recharged from $INTV_{CC}$ through an external Schottky diode D_B when the top MOSFET is turned off. When the $EXTV_{CC}$ pin is grounded, an internal 5V low dropout regulator supplies the $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ rises above 4.7V, the internal regulator is turned off, and an internal switch connects $EXTV_{CC}$ to $INTV_{CC}$. This allows a high efficiency source connected to $EXTV_{CC}$, such as an external 5V supply or a secondary output from the converter, to provide the $INTV_{CC}$ power. Voltages up to 7V can be applied to $EXTV_{CC}$ for additional gate drive. If the input voltage is low and $INTV_{CC}$ drops below 3.5V, undervoltage lockout circuitry prevents the power switches from turning on.

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The basic LTC3711 application circuit is shown in Figure 1. External component selection is primarily determined by the maximum load current and begins with the selection of the sense resistance and power MOSFET switches. The LTC3711 can use either a sense resistor or the on-resistance of the synchronous power MOSFET for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification.

Maximum Sense Voltage and V_{RNG} Pin

Inductor current is determined by measuring the voltage across a sense resistance that appears between the PGND and SENSE$^+$ pins. The maximum sense voltage is set by the voltage applied to the V_{RNG} pin and is equal to approximately $(0.133)V_{RNG}$. The current mode control loop will not allow the inductor current valleys to exceed $(0.133)V_{RNG}/R_{SENSE}$. In practice, one should allow some margin for variations in the LTC3711 and external component values and a good guide for selecting the sense resistance is:

$$R_{SENSE} = \frac{V_{RNG}}{10 \bullet I_{OUT(MAX)}}$$

An external resistive divider from $INTV_{CC}$ can be used to set the voltage of the V_{RNG} pin between 0.5V and 2V resulting in nominal sense voltages of 50mV to 200mV. Additionally, the V_{RNG} pin can be tied to SGND or $INTV_{CC}$ in which case the nominal sense voltage defaults to 70mV or 140mV, respectively. The maximum allowed sense voltage is about 1.33 times this nominal value.

Connecting the SENSE$^+$ Pin

The LTC3711 can be used with or without a sense resistor. When using a sense resistor, it is placed between the source of the bottom MOSFET M2 and ground. Connect the SENSE$^+$ pin to the source of the bottom MOSFET so that the resistor appears between the SENSE$^+$ and PGND pins. Using a sense resistor provides a well defined current limit, but adds cost and reduces efficiency. Alternatively, one can eliminate the sense resistor and use the bottom MOSFET as the current sense element by simply connecting the SENSE$^+$ pin to the switch node SW at the drain of the bottom MOSFET. This improves efficiency, but one must carefully choose the MOSFET on-resistance as discussed below.

Power MOSFET Selection

The LTC3711 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, threshold voltage $V_{(GS)TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

The gate drive voltage is set by the 5V $INTV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LTC3711 applications. If the input voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be considered.

When the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho_T}$$

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C as shown in Figure 2. For a maximum temperature of 100°C, using a value $\rho_T = 1.3$ is reasonable.

The power dissipated by the top and bottom MOSFETs strongly depends upon their respective duty cycles and the load current. When the LTC3711 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$D_{TOP} = \frac{V_{OUT}}{V_{IN}}$$

$$D_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

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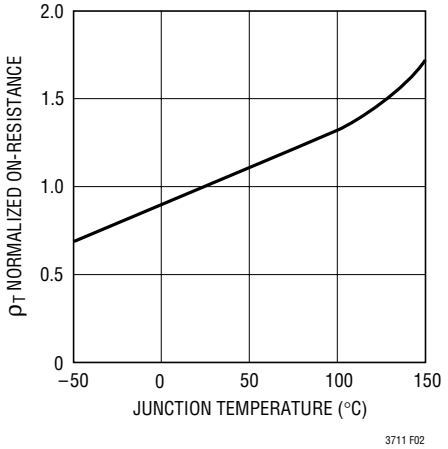

Figure 2. $R_{DS(ON)}$ vs. Temperature

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{TOP} = D_{TOP}\, I_{OUT(MAX)}^2\, \rho_{T(TOP)}\, R_{DS(ON)(MAX)} + k\, V_{IN}^2\, I_{OUT(MAX)}\, C_{RSS}\, f$$

$$P_{BOT} = D_{BOT}\, I_{OUT(MAX)}^2\, \rho_{T(BOT)}\, R_{DS(ON)(MAX)}$$

Both MOSFETs have I^2R losses and the top MOSFET includes an additional term for transition losses, which are largest at high input voltages. The constant $k = 1.7A^{-1}$ can be used to estimate the amount of transition loss. The bottom MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage.

Operating Frequency

The choice of operating frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance in order to maintain low output ripple voltage.

The operating frequency of LTC3711 applications is determined implicitly by the one-shot timer that controls the on-time t_{ON} of the top MOSFET switch. The on-time is set by the current into the I_{ON} pin and the voltage at the V_{ON} pin according to:

$$t_{ON} = \frac{V_{VON}}{I_{ION}}(10pF)$$

Tying a resistor R_{ON} from V_{IN} to the I_{ON} pin yields an on-time inversely proportional to V_{IN}. For a step-down converter, this results in approximately constant frequency operation as the input supply varies:

$$f = \frac{V_{OUT}}{V_{VON}\, R_{ON}(10pF)} \quad [Hz]$$

To hold frequency constant during output voltage changes, tie the V_{ON} pin to V_{OUT}. Figure 3 shows how frequency varies with R_{ON} in this case. The V_{ON} pin has internal clamps that limit its input to the one-shot timer. If the pin is tied below 0.7V, the input to the one-shot is clamped at 0.7V. Similarly, if the pin is tied above 2.4V, the input is clamped at 2.4V.

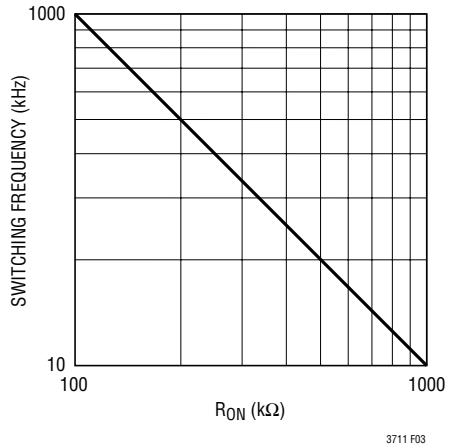

Figure 3. Switching Frequency vs R_{ON} with V_{ON} Tied to V_{OUT}

Because the voltage at the I_{ON} pin is about 0.7V, the current into this pin is not exactly inversely proportional to V_{IN}, especially in applications with lower input voltages. To correct for this error, an additional resistor R_{ON2} connected from the I_{ON} pin to the 5V $INTV_{CC}$ supply will further stabilize the frequency.

$$R_{ON2} = \frac{5V}{0.7V} R_{ON}$$

Changes in the load current magnitude will also cause frequency shift. Parasitic resistance in the MOSFET switches and inductor reduce the effective voltage across the inductance, resulting in increased duty cycle as the load current increases. By lengthening the on-time slightly

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(4a) (4b)

Figure 4. Correcting Frequency Shift with Load Current Changes

as current increases, constant frequency operation can be maintained. This is accomplished with a resistive divider from the I_{TH} pin to the V_{ON} pin and V_{OUT}. The values required will depend on the parasitic resistances in the specific application. A good starting point is to feed about 25% of the voltage change at the I_{TH} pin to the V_{ON} pin as shown in Figure 4a. Place capacitance on the V_{ON} pin to filter out the I_{TH} variations at the switching frequency. The resistor load on I_{TH} reduces the DC gain of the error amp and degrades load regulation, which can be avoided by using the PNP emitter follower of Figure 4b.

Minimum Off-time and Dropout Operation

The minimum off-time $t_{OFF(MIN)}$ is the smallest amount of time that the LTC3711 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 250ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON}+t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT}\frac{t_{ON}+t_{OFF(MIN)}}{t_{ON}}$$

A plot of maximum duty cycle vs frequency is shown in Figure 5.

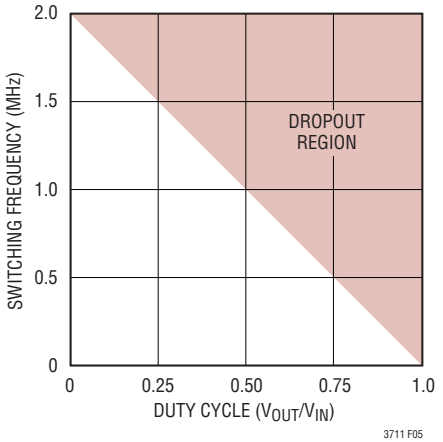

Figure 5. Maximum Switching Frequency vs Duty Cycle

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{fL}\right)\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces cores losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

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$$L = \left(\frac{V_{OUT}}{f\,\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

Schottky Diode D1 Selection

The Schottky diode D1 shown in Figure 1 conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half to one fifth of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently. The diode can be omitted if the efficiency loss is tolerable.

C_{IN} and C_{OUT} Selection

The input capacitance C_{IN} is required to filter the square wave current at the drain of the top MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \le \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications providing that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller. To dampen input voltage transients, add a small 5μF to 50μF aluminum electrolytic capacitor with an ESR in the range of 0.5Ω to 2Ω. High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of their lead inductance.

Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from $INTV_{CC}$ when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises

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to approximately V_{IN} + $INTV_{CC}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications a 0.1µF to 0.47µF X5R or X7R dielectric capacitor is adequate.

Discontinuous Mode Operation and FCB Pin

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 0.8V threshold enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. The load current at which current reverses and discontinuous operation begins depends on the amplitude of the inductor ripple current and will vary with changes in V_{IN}. Tying the FCB pin below the 0.8V threshold forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation.

In addition to providing a logic input to force continuous operation, the FCB pin provides a means to maintain a flyback winding output when the primary is operating in discontinuous mode. The secondary output V_{SEC} is normally set as shown in Figure 6 by the turns ratio N of the transformer. However, if the controller goes into discontinuous mode and halts switching due to a light primary load current, then V_{OUT2} will droop. An external resistor divider from V_{OUT2} to the FCB pin sets a minimum voltage $V_{OUT2(MIN)}$ below which continuous operation is forced until V_{OUT2} has risen above its minimum.

$$V_{OUT2(MIN)} = 0.8V\left(1+\frac{R4}{R3}\right)$$

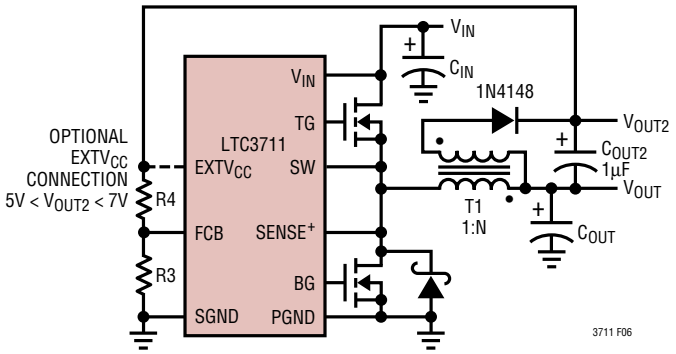

Figure 6. Secondary Output Loop and $EXTV_{CC}$ Connection

Fault Conditions: Current Limit and Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3711, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SNS(MAX)}}{R_{DS(ON)}\,\rho_T} + \frac{1}{2}\Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of I_{LIMIT} which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same amount below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

To further limit current in the event of a short circuit to ground, the LTC3711 includes foldback current limiting. If the output falls by more than 25%, then the maximum sense voltage is progressively lowered to about one sixth of its full value.

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Output Voltage Programming

The output voltage is digitally set to levels between 0.900V and 2.000V using the voltage identification (VID) inputs VID0-VID4. An internal 5-bit DAC configured as a precision resistive voltage divider sets the output voltage in increments according to Table 1. The VID codes are compatible with Intel Mobile Pentium III processor specifications. Each VID input is pulled up by an internal 2.5μA current source from the $INTV_{CC}$ supply and includes a series diode to prevent damage from VID inputs that exceed the supply.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces the 5V supply that powers the drivers and internal circuitry within the LTC3711. The $INTV_{CC}$ pin can supply up to 50mA RMS and must be bypassed to ground with a minimum of 4.7μF low ESR tantalum capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers. Applications using large MOSFETs with a high input voltage and high frequency of operation may cause the LTC3711 to exceed its maximum junction temperature rating or RMS current rating. Most of the supply current drives the MOSFET gates unless an external $EXTV_{CC}$ source is used. In continuous mode operation, this current is $I_{GATECHG} = f(Q_{g(TOP)} + Q_{g(BOT)})$. The junction temperature can be estimated from the equations given in Note 2 of the Electrical Characteristics. For example, the LTC3711CGN is limited to less than 14mA from a 30V supply:

$$T_J = 70°C + (14mA)(30V)(130°C/W) = 125°C$$

For larger currents, consider using an external supply with the $EXTV_{CC}$ pin.

Table 1. VID Output Voltage Programming

VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
0	0	0	0	0	2.000V
0	0	0	0	1	1.950V
0	0	0	1	0	1.900V
0	0	0	1	1	1.850V
0	0	1	0	0	1.800V
0	0	1	0	1	1.750V
0	0	1	1	0	1.700V
0	0	1	1	1	1.650V
0	1	0	0	0	1.600V
0	1	0	0	1	1.550V
0	1	0	1	0	1.500V
0	1	0	1	1	1.450V
0	1	1	0	0	1.400V
0	1	1	0	1	1.350V
0	1	1	1	0	1.300V
0	1	1	1	1	*
1	0	0	0	0	1.275V
1	0	0	0	1	1.250V
1	0	0	1	0	1.225V
1	0	0	1	1	1.200V
1	0	1	0	0	1.175V
1	0	1	0	1	1.150V
1	0	1	1	0	1.125V
1	0	1	1	1	1.100V
1	1	0	0	0	1.075V
1	1	0	0	1	1.050V
1	1	0	1	0	1.025V
1	1	0	1	1	1.000V
1	1	1	0	0	0.975V
1	1	1	0	1	0.950V
1	1	1	1	0	0.925V
1	1	1	1	1	**

Note: *, ** represent codes without a defined output voltage as specified by Intel. The LTC3711 interprets these codes as valid inputs and produces output voltages as follows: [01111] = 1.250V, [11111] = 0.900V.

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$EXTV_{CC}$ Connection

The $EXTV_{CC}$ pin can be used to provide MOSFET gate drive and control power from the output or another external source during normal operation. Whenever the $EXTV_{CC}$ pin is above 4.7V the internal 5V regulator is shut off and an internal 50mA P-channel switch connects the $EXTV_{CC}$ pin to $INTV_{CC}$. $INTV_{CC}$ power is supplied from $EXTV_{CC}$ until this pin drops below 4.5V. Do not apply more than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$. The following list summarizes the possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. $INTV_{CC}$ is always powered from the internal 5V regulator.

2. $EXTV_{CC}$ connected to an external supply. A high efficiency supply compatible with the MOSFET gate drive requirements (typically 5V) can improve overall efficiency.

3. $EXTV_{CC}$ connected to an output derived boost network. The low voltage output can be boosted using a charge pump or flyback winding to greater than 4.7V. The system will start-up using the internal linear regulator until the boosted output supply is available.

External Gate Drive Buffers

The LTC3711 drivers are adequate for driving up to about 30nC into MOSFET switches with RMS currents of 50mA. Applications with larger MOSFET switches or operating at frequencies requiring greater RMS currents will benefit from using external gate drive buffers such as the LTC1693. Alternately, the external buffer circuit shown in Figure 7 can be used. Note that the bipolar devices reduce the signal swing at the MOSFET gate and benefit from an increased $EXTV_{CC}$ voltage of about 6V.

Soft-Start and Latchoff with the RUN/SS Pin

The RUN/SS pin provides a means to shut down the LTC3711 as well as a timer for soft-start and overcurrent latchoff. Pulling the RUN/SS pin below 0.8V puts the LTC3711 into a low quiescent current shutdown (I_Q < 30μA). Releasing the pin allows an internal 1.2μA current source to charge up the external timing capacitor C_{SS}. If RUN/SS has been pulled all the way to ground, there is a delay before starting of about:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = \left(1.3s/\mu F\right) C_{SS}$$

When the voltage on RUN/SS reaches 1.5V, the LTC3711 begins operating with a clamp on I_{TH} of approximately 0.9V. As the RUN/SS voltage rises to 3V, the clamp on I_{TH} is raised until its full 2.4V range is available. This takes an additional 1.3s/μF, during which the load current is folded back until the output reaches 75% of its final value. The pin can be driven from logic as shown in Figure 8. Diode D1 reduces the start delay while allowing C_{SS} to charge up slowly for the soft-start function.

After the controller has been started and given adequate time to charge up the output capacitor, C_{SS} is used as a short-circuit timer. After the RUN/SS pin charges above 4V, if the output voltage falls below 75% of its regulated value, then a short-circuit fault is assumed. A 1.8μA current then begins discharging C_{SS}. If the fault condition persists until the RUN/SS pin drops to 3.5V, then the controller turns off both power MOSFETs, shutting down the converter permanently. The RUN/SS pin must be actively pulled down to ground in order to restart operation.

The overcurrent protection timer requires that the soft-start timing capacitor C_{SS} be made large enough to guarantee that the output is in regulation by the time C_{SS} has reached the 4V threshold. In general, this will depend upon the size of the output capacitance, output voltage and load current characteristic. A minimum soft-start capacitor can be estimated from:

$$C_{SS} > C_{OUT}\ V_{OUT}\ R_{SENSE}\ (10^{-4}\ [F/V\ s])$$

Generally 0.1μF is more than sufficient.

Overcurrent latchoff operation is not always needed or desired. Load current is already limited during a short-circuit by the current foldback circuitry and latchoff operation can prove annoying during troubleshooting. The feature can be overridden by adding a pull-up current greater than 5μA to the RUN/SS pin. The additional current prevents the discharge of C_{SS} during a fault and also shortens the soft-start period. Using a resistor to V_{IN} as shown in Figure 8a is simple, but slightly increases shutdown current. Connecting a resistor to $INTV_{CC}$ as shown in Figure 8b eliminates the additional shutdown

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current, but requires a diode to isolate C_{SS}. Any pull-up network must be able to pull RUN/SS above the 4.2V maximum threshold of the latchoff circuit and overcome the 4μA maximum discharge current.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3711 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)} = 0.01\Omega$ and $R_L = 0.005\Omega$, the loss will range from 1% up to 10% as the output current varies from 1A to 10A for a 1.5V output.

2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

$$\text{Transition Loss} \cong (1.7A^{-1})\ V_{IN}^2\ I_{OUT}\ C_{RSS}\ f$$

3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents. This loss can be reduced by supplying $INTV_{CC}$ current through the $EXTV_{CC}$ pin from a high efficiency source, such as an output derived boost network or alternate supply if available.

4. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including C_{OUT} ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin external components shown in

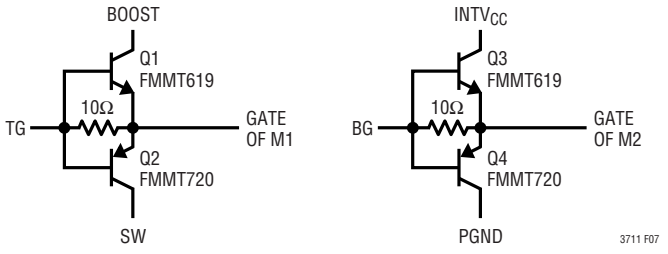

Figure 7. Optional External Gate Driver

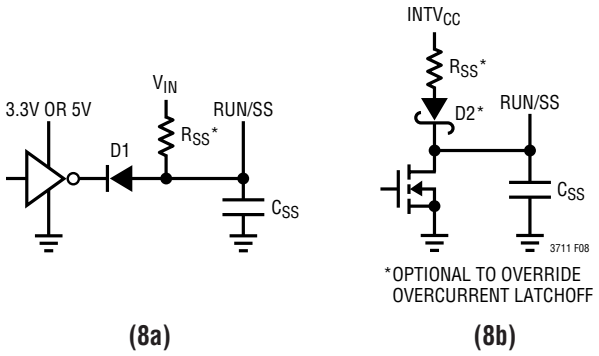

Figure 8. RUN/SS Pin Interfacing with Latchoff Defeated

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Figure 9 will provide adequate compensation for most applications. For a detailed explanation of switching control loop theory see Application Note 76.

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 7V to 24V (15V nominal), V_{OUT} = 1.5V ±100mV, $I_{OUT(MAX)}$ = 15A, f = 300kHz. First, calculate the timing resistor with $V_{ON} = V_{OUT}$:

$$R_{ON} = \frac{1}{(300kHz)(10pF)} = 330k$$

and choose the inductor for about 40% ripple current at the maximum V_{IN}:

$$L = \frac{1.5V}{(300kHz)(0.4)(15A)}\left(1 - \frac{1.5V}{24V}\right) = 0.8\mu H$$

Selecting a standard value of 1μH results in a maximum ripple current of:

$$\Delta I_L = \frac{1.5V}{(300kHz)(1\mu H)}\left(1 - \frac{1.5V}{24V}\right) = 4.7A$$

Next, choose the synchronous MOSFET switch. Because of the narrow duty cycle and large current, a single SO-8 MOSFET will have difficulty dissipating the power lost in the switch. Choosing two IRF7811A ($R_{DS(ON)}$ = 0.013Ω, C_{RSS} = 60pF, θ_{JA} = 50°C/W) yields a nominal sense voltage of:

$$V_{SNS(NOM)} = (15A)(0.5)(1.3)(0.012\Omega) = 117mV$$

Tying V_{RNG} to $INTV_{CC}$ will set the current sense voltage range for a nominal value of 140mV with current limit occurring at 186mV. To check if the current limit is acceptable, assume a junction temperature of about 100°C above a 50°C ambient with $\rho_{150°C}$ = 1.6:

$$I_{LIMIT} \geq \frac{186mV}{(0.5)(1.6)(0.012\Omega)} + \frac{1}{2}(4.7A) = 18A$$

and double check the assumed T_J in the MOSFET:

$$P_{BOT} = \frac{24V - 1.5V}{24V}\left(\frac{21.7A}{2}\right)^2(1.6)(0.012\Omega) = 2.12W$$

$$T_J = 50°C + (2.12W)(50°C/W) = 156°C$$

Because the top MOSFET is on for such a short time, a single IRF7811A will be sufficient. Checking its power dissipation at current limit with $\rho_{90°C}$ = 1.3:

$$P_{BOT} = \frac{1.5V}{24V}(21.7A)^2(1.3)(0.012\Omega) + (1.7)(24V)^2(21.7A)(60pF)(300kHz) = 0.46W + 0.38W = 0.84W$$

$$T_J = 50°C + (0.84W)(50°C/W) = 92°C$$

The junction temperatures will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking will be necessary in this circuit.

C_{IN} is chosen for an RMS current rating of about 6A at temperature. The output capacitors are chosen for a low ESR of 0.005Ω to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$$\Delta V_{OUT(RIPPLE)} = \Delta I_{L(MAX)}\,(ESR) = (4.7A)\,(0.005\Omega) = 24mV$$

However, a 0A to 15A load step will cause an output change of up to:

$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD}\,(ESR) = (15A)\,(0.005\Omega) = 75mV$$

The complete circuit is shown in Figure 9.

Active Voltage Positioning

Active voltage positioning (also termed load "deregulation" or droop) describes a technique where the output voltage varies with load in a controlled manner. It is useful in applications where rapid load steps are the main cause of error in the output voltage. By positioning the output voltage above the regulation point at zero load, and below the regulation point at full load, one can use more of the error budget for the load step. This allows one to reduce the number of output capacitors by relaxing the ESR requirement.

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In the design example, Figure 9, five 0.025Ω capacitors are required in parallel to keep the output voltage within tolerance. Using active voltage positioning, the same specification can be met with only three capacitors. In this case, the load step will cause an output voltage change of:

$$\Delta V_{OUT(STEP)} = (15A)\left(\frac{1}{3}\right)(0.025\Omega) = 125mV$$

By positioning the output voltage 60mV above the regulation point at no load, it will only drop 65mV below the regulation point after the load step, well within the ±100mV tolerance.

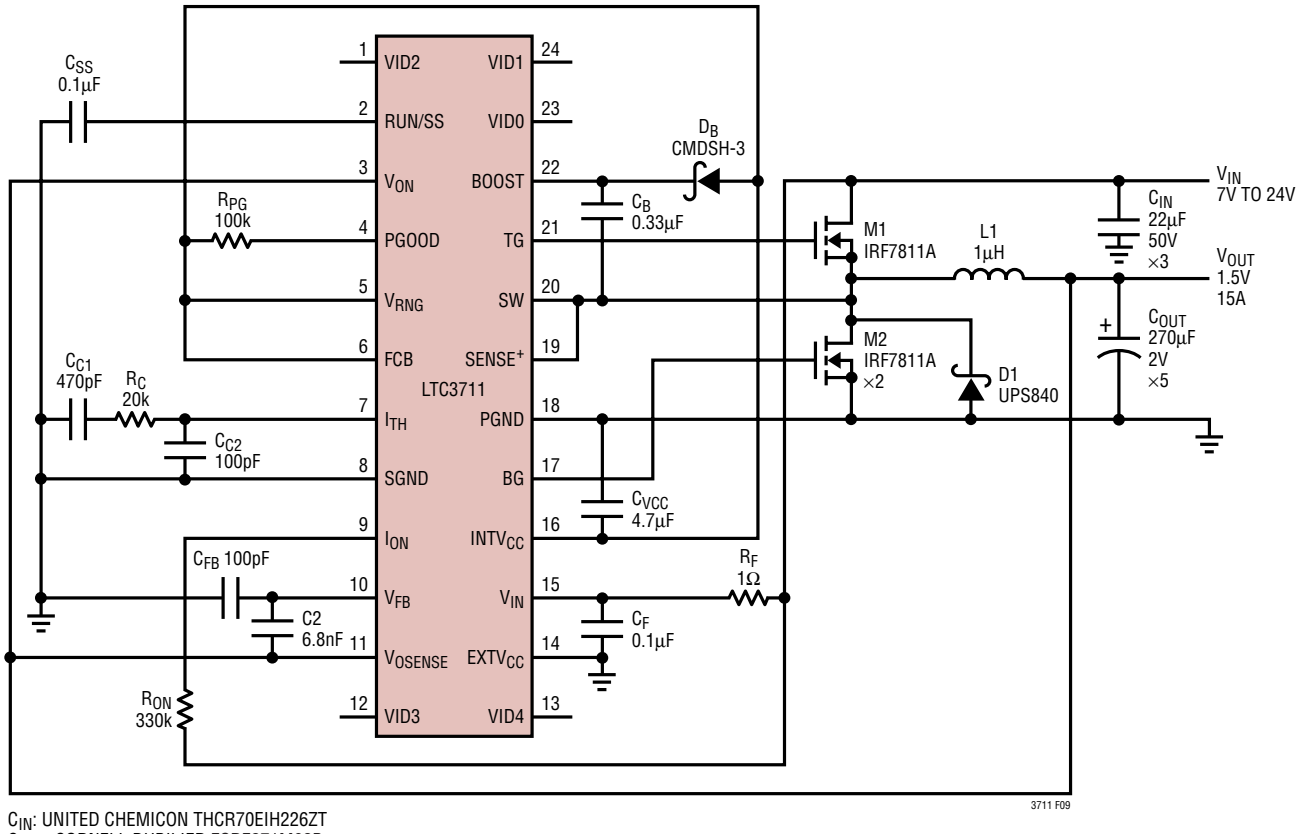
Implementing active voltage positioning requires setting a precise gain between the sensed current and the output voltage. Because of the variability of MOSFET on-resistance, it is prudent to use a sense resistor with active voltage positioning. In order to minimize power lost in this resistor, a low value is chosen of 0.003Ω. The nominal sense voltage will now be:

$$V_{SNS(NOM)} = (0.003\Omega)(15A) = 45mV$$

To maintain a reasonable current limit, the voltage on the V_{RNG} pin is reduced to its minimum value of 0.5V, corresponding to a 50mV nominal sense voltage.

Next, the gain of the LTC3711 error amplifier must be determined. The change in I_{TH} voltage for a corresponding change in the output current is:

$$\Delta I_{TH} = \left(\frac{12V}{V_{RNG}}\right) R_{SENSE}\, \Delta I_{OUT}$$
$$= (24)(0.003\Omega)(15A) = 1.08V$$



C_{IN}: UNITED CHEMICON THCR70EIH226ZT
C_{OUT}: CORNELL DUBILIER ESRE271M02B
L1: SUMIDA CEP125-IR0MC-H

Figure 9. CPU Core Voltage Regulator 1.5V/15A at 300kHz

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The corresponding change in the output voltage is determined by the gain of the error amplifier and feedback divider. The LTC3711 error amplifier has a transconductance g_m that is constant over both temperature and a wide ± 40mV input range. Thus, by connecting a load resistance R_{VP} to the I_{TH} pin, the error amplifier gain can be precisely set for accurate active voltage positioning.

$$\Delta I_{TH} = g_m R_{VP}\left(\frac{0.8V}{V_{OUT}}\right)\Delta V_{OUT}$$

Solving for this resistance value:

$$R_{VP} = \frac{V_{OUT}\,\Delta I_{TH}}{(0.8V)\,g_m\,\Delta V_{OUT}} = \frac{(1.5V)(1.08V)}{(0.8V)(1.7mS)(125mV)} = 9.53k$$

The gain setting resistance R_{VP} is implemented with two resistors, R_{VP1} connected from I_{TH} to ground and R_{VP2} connected from I_{TH} to $INTV_{CC}$. The parallel combination of these resistors must equal R_{VP} and their ratio determines nominal value of the I_{TH} pin voltage when the error amplifier input is zero. To center the load line around the regulation point, the I_{TH} pin voltage must be set to correspond to half the output current. The relation between I_{TH} voltage and the output current is:

$$I_{TH(NOM)} = \left(\frac{12V}{V_{RNG}}\right)R_{SENSE}\left(I_{OUT} - \frac{1}{2}\Delta I_L\right) + 0.8V = \left(\frac{12V}{0.5V}\right)(0.003\Omega)\left(7.5A - \frac{1}{2}4.7A\right) + 0.8V = 1.17V$$

Solving for the required values of the resistors:

$$R_{VP1} = \frac{5V}{5V - I_{TH(NOM)}}R_{VP} = \frac{5V}{5V - 1.17V}9.53k = 12.44k$$

$$R_{VP2} = \frac{5V}{I_{TH(NOM)}}R_{VP} = \frac{5V}{1.17V}9.53k = 40.73k$$

The modified circuit is shown in Figure 10. Figures 11 and 12 show the transient response without and with active voltage positioning. Both circuits easily stay within ±100mV of the 1.5V output. However, the circuit with active voltage positioning accomplishes this with only three output capacitors rather than five. Refer to Design Solutions 10 for additional information about active voltage positioning.

PC Board Layout Checklist

When laying out the printed circuit board, use the following checklist to ensure proper operation of the controller. These items are also illustrated in Figure 11.

- Segregate the signal and power grounds. All small signal components should return to the SGND pin at one point which is then tied to the PGND pin close to the source of M2.
- Place M2 as close to the controller as possible, keeping the PGND, BG and $SENSE^+$ traces short.
- Connect the input capacitor(s) C_{IN} close to the power MOSFETs. This capacitor carries the MOSFET AC current.
- Keep the high dV/dT SW, BOOST and TG nodes away from sensitive small-signal nodes.
- Connect the $INTV_{CC}$ decoupling capacitor C_{VCC} closely to the $INTV_{CC}$ and PGND pins.
- Connect the top driver boost capacitor C_B closely to the BOOST and SW pins.
- Connect the V_{IN} pin decoupling capacitor C_F closely to the V_{IN} and PGND pins.
- VID0-VID4 interface circuitry must return to SGND.

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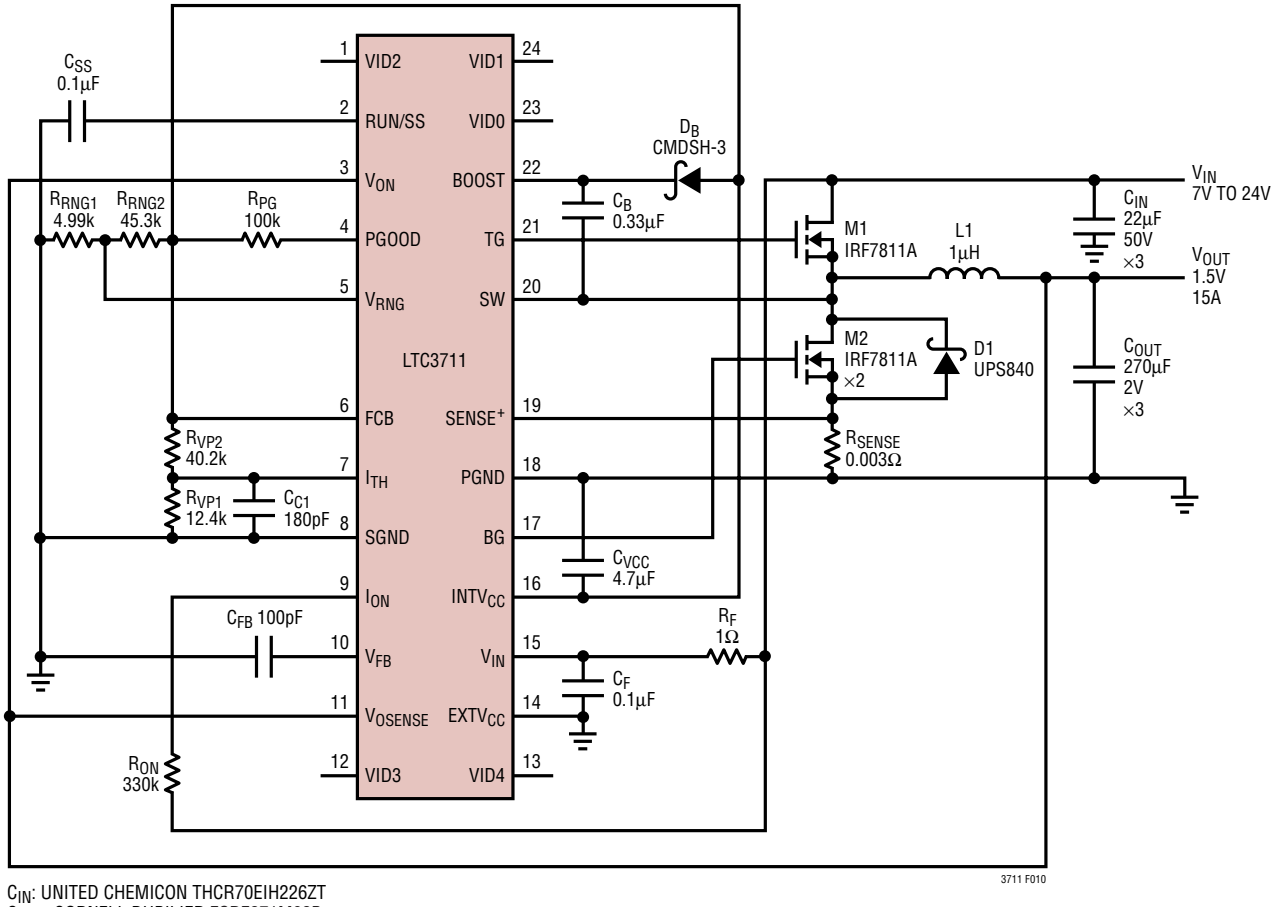


C_{IN}: UNITED CHEMICON THCR70EIH226ZT
C_{OUT}: CORNELL DUBILIER ESRE271M02B
L1: SUMIDA CEP125-IR0MC-H

Figure 10. CPU Core Voltage Regulator with Active Voltage Positioning 1.5V/15A at 300kHz

APPLICATIONS INFORMATION

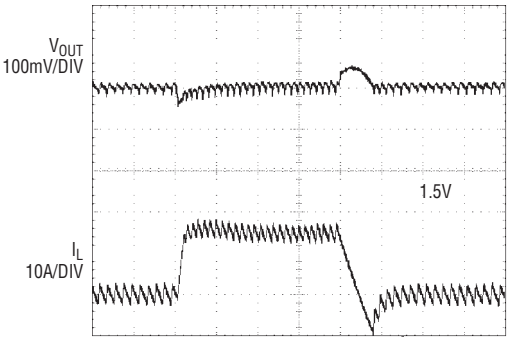


Figure 11. Normal Transient Response

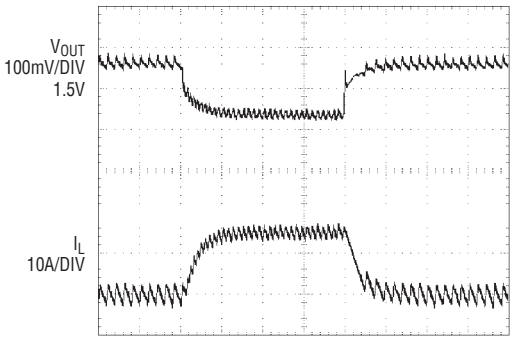


Figure 12. Transient Response with Active Voltage Positioning

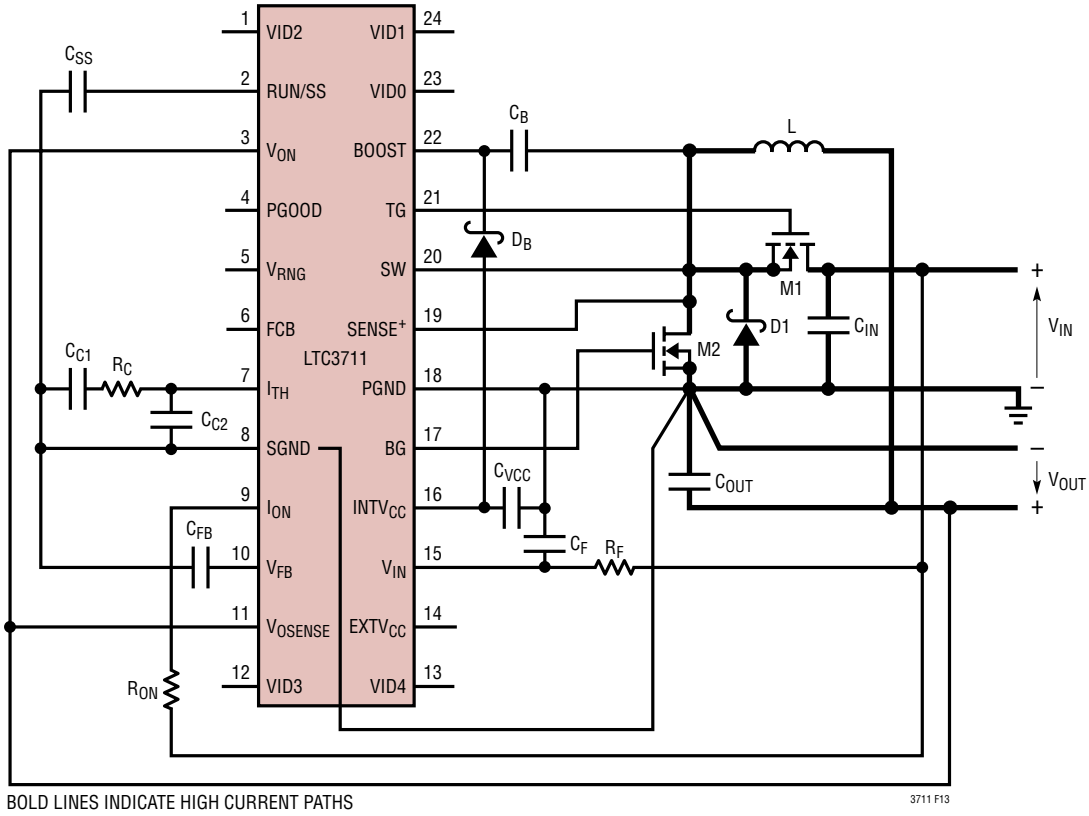
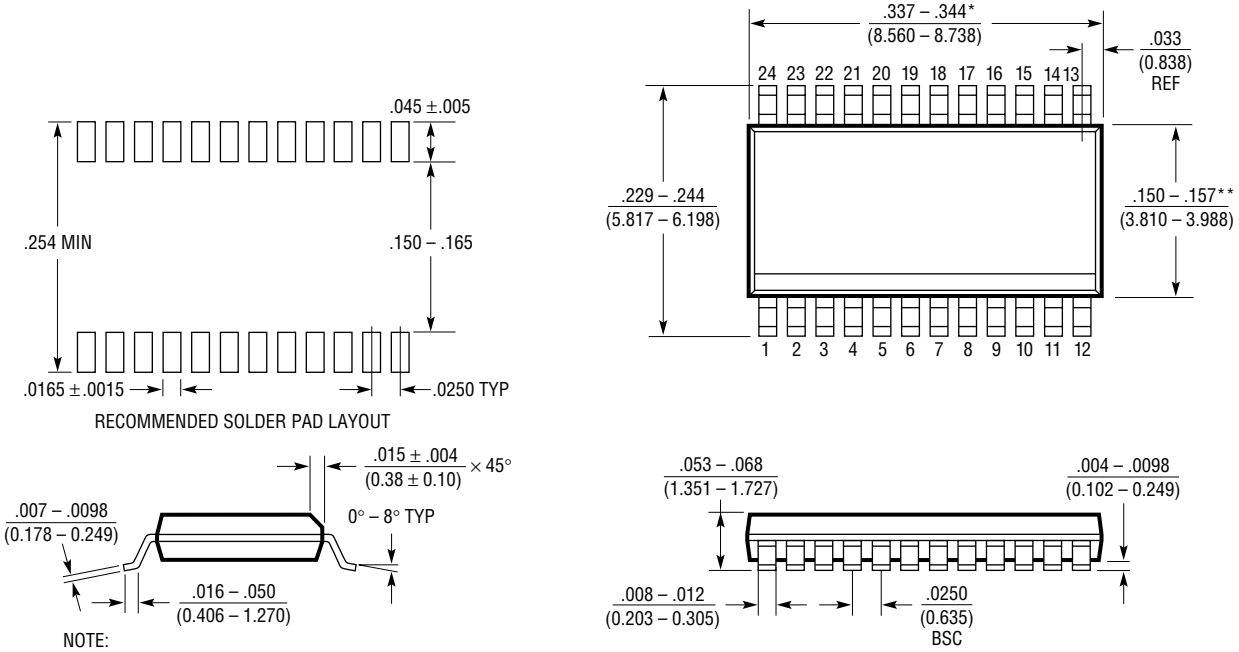


Figure 13. LTC3711 Layout Diagram

PACKAGE DESCRIPTION

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

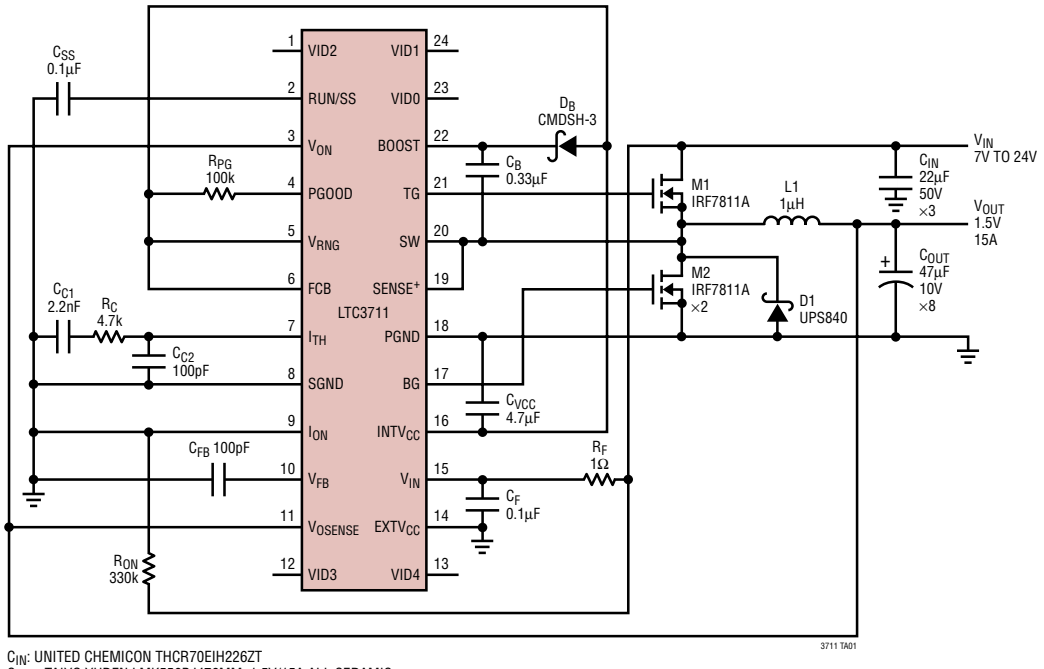


NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE
   *DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
   **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

1.5V/15A All Ceramic C_{OUT}



C_{IN}: UNITED CHEMICON THCR70EIH226ZT
C_{OUT}: TAIYO YUDEN LMK550BJ476MM, 1.5V/15A ALL CERAMIC
L1: SUMIDA CEP125-IR0MC-H

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1625/ LTC1775	No R_{SENSE} Current Mode Synchronous Step-Down Controller	97% Efficiency, No Sense Resistor, 16-Pin SSOP
LTC1628-PG	Dual, 2-Phase Synchronous Step-Down Controller	Power Good Output, Minimum Input/Output Capacitors, $3.5V \le V_{IN} \le 36V$
LTC1628-SYNC	Dual, 2-Phase Synchronous Step-Down Controller	Synchronizable 150kHz to 300kHz
LTC1709-7	High Efficiency, 2-Phase Synchronous Step-Down Controller with 5-Bit VID	Up to 42A Output, $0.925V \le V_{OUT} \le 2V$
LTC1709-8	High Efficiency, 2-Phase Synchronous Step-Down Controller	Up to 42A Output, VRM 8.4, $1.3V \le V_{OUT} \le 3.5V$
LTC1735	High Efficiency, Synchronous Step-Down Controller	Burst Mode® Operation, 16-Pin Narrow SSOP, $3.5V \le V_{IN} \le 36V$
LTC1736	High Efficiency, Synchronous Step-Down Controller with 5-Bit VID	Mobile VID, $0.925V \le V_{OUT} \le 2V$, $3.5V \le V_{IN} \le 36V$
LTC1772	SOT-23 Step-Down Controller	Current Mode, 550kHz, Very Small Solution Size
LTC1773	Synchronous Step-Down Controller	Up to 95% Efficiency; 550kHz, $2.65V \le V_{IN} \le 8.5V$, $0.8V \le V_{OUT} \le V_{IN}$, Synchronizable to 750kHz
LTC1778	No R_{SENSE} Synchronous Step-Down Controller	No Sense Resistor Required, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le (0.9)\ V_{IN}$
LTC1874	Dual, Step-Down Controller	Current Mode; 550kHz; Small 16-Pin SSOP, $V_{IN} < 9.8V$
LTC1876	2-Phase, Dual Synchronous Step-Down Controller with Step-Up Regulator	$3.5V \le V_{IN} \le 36V$, Power Good Output, 300kHz Operation
LTC3714	Intel and Transmeta Compatible DC/DC Controller with V20 and Internal Op Amp	$0.6V \le V_{OUT} \le 1.75V$, $4V \le V_{IN} \le 36V$, ±1% 0.6V Reference
LTC3732	3-Phase, VRM 9.0/9.1 Synchronous Step-Down Controller	600kHz per Phase, ±5% Output Current Matching, Integrated Drivers, SSOP-36

Burst Mode is a registered trademark of Linear Technology Corporation.

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