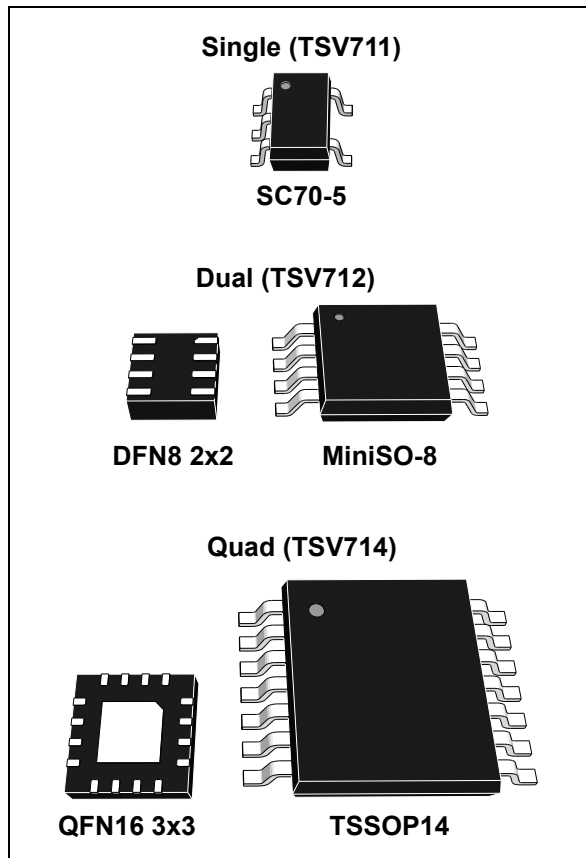


High accuracy (200 μ V) micropower 14 μ A, 150 kHz
5 V CMOS operational amplifiers

Datasheet - preliminary data



Features

- Low offset voltage: 200 μ V max.
- Low power consumption: 10 μ A at 5 V
- Low supply voltage: 1.5 V to 5.5 V
- Gain bandwidth product: 150 kHz typ.
- Low input bias current: 1 pA typ.
- Rail-to-rail input and output
- EMI hardened operational amplifiers
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 to +125 °C

Benefits

- Higher accuracy without calibration
- Energy saving
- Guaranteed operation on low-voltage battery

Related products

- See the TSV73 series (900 kHz for 60 μ A) for higher gain bandwidth products

Applications

- Battery powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

Description

The TSV71x series of single, dual, and quad operational amplifiers offer low-voltage operation, rail-to-rail input and output, and excellent accuracy (V_{io} lower than 200 μ V at 25 °C).

These devices benefit from STMicroelectronics® 5 V CMOS technology and offer an excellent speed/power consumption ratio (150 kHz typical gain bandwidth) while consuming less than 14 μ A at 5 V. The TSV71x series also feature an ultra-low input bias current.

The single version (TSV711), the dual version (TSV712), and the quad version (TSV714) are housed in the smallest industrial packages.

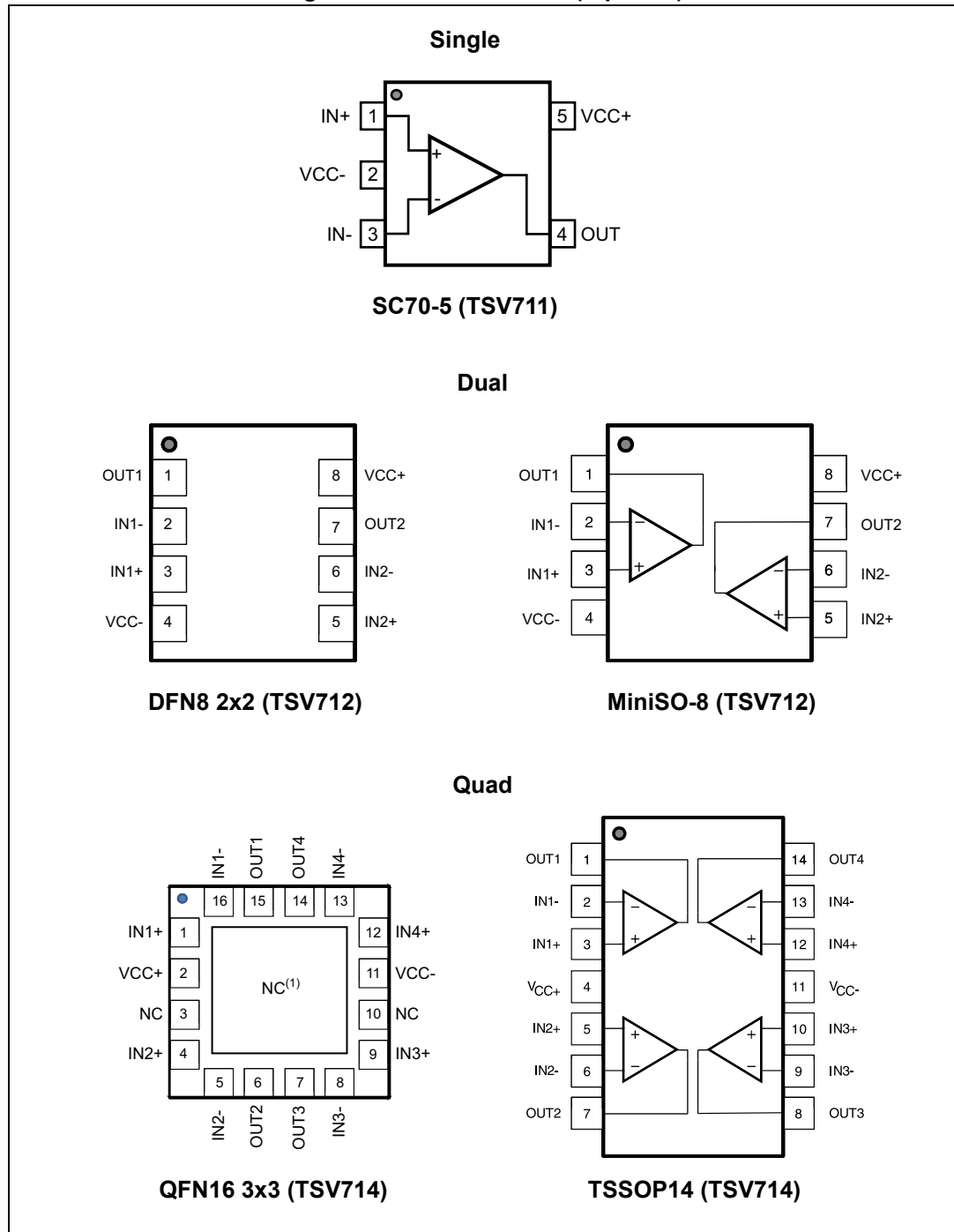
These characteristics make the TSV71x family ideal for sensor interfaces, battery-powered and portable applications, and active filtering.

Contents

1	Pin connections	3
2	Absolute maximum ratings and operating conditions	4
3	Electrical characteristics	6
4	Application information	16
4.1	Operating voltages	16
4.2	Rail-to-rail input	16
4.3	Rail-to-rail output	16
4.4	Input offset voltage drift over temperature	16
4.5	Long-term input offset voltage drift	17
4.6	Initialization time	19
4.7	PCB layouts	19
4.8	Macromodel	20
5	Package information	21
5.1	SC70-5 package information	22
5.2	DFN8 2x2 package information	23
5.3	MiniSO-8 package information	24
5.4	QFN16 3x3 package information	25
5.5	TSSOP14 package information	27
6	Ordering information	28
7	Revision history	28

1 Pin connections

Figure 1. Pin connections (top view)



1. The exposed pads of the QFN16 3x3 can be connected to VCC- or left floating.

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_{id}	Differential input voltage ⁽²⁾	$\pm V_{CC}$	
V_{in}	Input voltage ⁽³⁾	$V_{CC-} - 0.2$ to $V_{CC+} + 0.2$	
I_{in}	Input current ⁽⁴⁾	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction-to-ambient ⁽⁵⁾⁽⁶⁾		°C/W
	SC70-5	205	
	DFN8 2x2	120	
	MiniSO8	190	
	QFN16 3x3	45	
	TSSOP14	100	
R_{thjc}	Thermal resistance junction-to-case DFN8 2x2	33	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model ⁽⁷⁾	4	kV
	MM: machine model for TSV711 ⁽⁸⁾	150	V
	MM: machine model for TSV712 ⁽⁸⁾	200	
	MM: machine model for TSV714 ⁽⁸⁾	300	
	CDM: charged device model except MiniSO8 ⁽⁹⁾	1.5	kV
	CDM: charged device model for MiniSO8 ⁽⁹⁾	1.3	
	Latchup immunity	200	mA

1. All voltage values, except the differential voltage are with respect to the network ground terminal.
2. The differential voltage is a non-inverting input terminal with respect to the inverting input terminal. The TSV712 and TSV714 devices include an internal differential voltage limiter that clamps internal differential voltage at 0.5 V.
3. $V_{CC} - V_{in}$ must not exceed 6 V, V_{in} must not exceed 6 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: 100 pF discharged through a 1.5 k Ω resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common mode input voltage range	$V_{CC-} - 0.1$ to $V_{CC+} + 0.1$	
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 3. Electrical characteristics at $V_{CC+} = 1.8\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ °C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage ($V_{icm} = 0\text{ V}$)	$T = 25\text{ °C}$			200	μV
		$-40\text{ °C} < T < 85\text{ °C}$			850	
		$-40\text{ °C} < T < 125\text{ °C}$			1200	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	$-40\text{ °C} < T < 125\text{ °C}^{(1)}$			10	$\mu\text{V}/\text{°C}$
I_{io}	Input offset current ($V_{out} = V_{CC}/2$)	$T = 25\text{ °C}$		1	$10^{(2)}$	pA
		$-40\text{ °C} < T < 125\text{ °C}$		1	$300^{(2)}$	
I_{ib}	Input bias current ($V_{out} = V_{CC}/2$)	$T = 25\text{ °C}$		1	$10^{(2)}$	
		$-40\text{ °C} < T < 125\text{ °C}$		1	$300^{(2)}$	
CMR	Common mode rejection ratio $20 \log (\Delta V_{icm}/\Delta V_{io})$ $V_{icm} = 0\text{ V to } V_{CC}$, $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$	$T = 25\text{ °C}$	69	88		dB
		$-40\text{ °C} < T < 125\text{ °C}$	61			
A_{vd}	Large signal voltage gain $V_{out} = 0.5\text{ V to } (V_{CC} - 0.5\text{ V})$	$T = 25\text{ °C}$	95			
		$-40\text{ °C} < T < 125\text{ °C}$	85			
V_{OH}	High level output voltage ($V_{OH} = V_{CC} - V_{out}$)	$T = 25\text{ °C}$			75	mV
		$-40\text{ °C} < T < 125\text{ °C}$			80	
V_{OL}	Low level output voltage	$T = 25\text{ °C}$			40	
		$-40\text{ °C} < T < 125\text{ °C}$			60	
I_{out}	I_{sink} ($V_{out} = V_{CC}$)	$T = 25\text{ °C}$	6	12		mA
		$-40\text{ °C} < T < 125\text{ °C}$	4			
	I_{source} ($V_{out} = 0\text{ V}$)	$T = 25\text{ °C}$	5	7		
		$-40\text{ °C} < T < 125\text{ °C}$	3			
I_{CC}	Supply current (per channel, $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$)	$T = 25\text{ °C}$		9	14	μA
		$-40\text{ °C} < T < 125\text{ °C}$			16	

Table 3. Electrical characteristics at $V_{CC+} = 1.8\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ °C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	100	120		kHz
F_u	Unity gain frequency			100		
Φ_m	Phase margin			45		Degrees
G_m	Gain margin			19		dB
SR	Slew rate ⁽³⁾	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$		0.04		V/ μ s
e_n	Equivalent input noise voltage	$f = 1\text{ kHz}$		100		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
		$f = 10\text{ kHz}$		96		
t_{init}	Initialization time ⁽⁴⁾	$T = 25\text{ °C}$			5	ms
		$-40\text{ °C} < T < 125\text{ °C}$			60	

1. See [Section 4.4: Input offset voltage drift over temperature](#).
2. Guaranteed by characterization.
3. Slew rate value is calculated as the average between positive and negative slew rates.
4. Initialization time is defined as the delay after power-up to guarantee operation within specified performances. Guaranteed by design. See [Section 4.6: Initialization time](#).

Table 4. Electrical characteristics at $V_{CC+} = 3.3$ V with $V_{CC-} = 0$ V, $V_{icm} = V_{CC}/2$, $T = 25$ °C, and $R_L = 10$ k Ω connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	$T = 25$ °C			200	μ V
		-40 °C $< T < 85$ °C			850	
		-40 °C $< T < 125$ °C			1200	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C $< T < 125$ °C ⁽¹⁾			10	μ V/°C
ΔV_{io}	Long-term input offset voltage drift	$T = 25$ °C ⁽²⁾		0.3		$\frac{\mu V}{\sqrt{\text{month}}}$
I_{io}	Input offset current ($V_{out} = V_{CC}/2$)	$T = 25$ °C		1	10 ⁽³⁾	pA
		-40 °C $< T < 125$ °C		1	300 ⁽³⁾	
I_{ib}	Input bias current ($V_{out} = V_{CC}/2$)	$T = 25$ °C		1	10 ⁽³⁾	
		-40 °C $< T < 125$ °C		1	300 ⁽³⁾	
CMR	Common mode rejection ratio $20 \log (\Delta V_{icm}/\Delta V_{io})$ $V_{icm} = 0$ V to V_{CC} , $V_{out} = V_{CC}/2$, $R_L > 1$ M Ω	$T = 25$ °C	80	100		dB
		-40 °C $< T < 125$ °C	69			
A_{vd}	Large signal voltage gain $V_{out} = 0.5$ V to $(V_{CC} - 0.5$ V)	$T = 25$ °C	95			
		-40 °C $< T < 125$ °C	85			mV
V_{OH}	High level output voltage ($V_{OH} = V_{CC} - V_{out}$)	$T = 25$ °C			75	
		-40 °C $< T < 125$ °C			80	
V_{OL}	Low level output voltage	$T = 25$ °C			40	
		-40 °C $< T < 125$ °C			60	
I_{out}	I_{sink} ($V_{out} = V_{CC}$)	$T = 25$ °C	20	34		mA
		-40 °C $< T < 125$ °C	15			
	I_{source} ($V_{out} = 0$ V)	$T = 25$ °C	20	26		
		-40 °C $< T < 125$ °C	15			
I_{CC}	Supply current (per channel, $V_{out} = V_{CC}/2$, $R_L > 1$ M Ω)	$T = 25$ °C		9	14	μ A
		-40 °C $< T < 125$ °C			16	

Table 4. Electrical characteristics at $V_{CC+} = 3.3\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ °C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ $C_L = 100\text{ pF}$	100	120		kHz
F_u	Unity gain frequency			100		
Φ_m	Phase margin			45		Degrees
G_m	Gain margin			19		dB
SR	Slew rate ⁽⁴⁾	$R_L = 10\text{ k}\Omega$ $C_L = 100\text{ pF}$, $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$		0.05		V/ μ s
e_n	Equivalent input noise voltage	$f = 1\text{ kHz}$		100		$\frac{nV}{\sqrt{Hz}}$
		$f = 10\text{ kHz}$		96		
t_{init}	Initialization time ⁽⁵⁾	$T = 25\text{ °C}$			5	ms
		$-40\text{ °C} < T < 125\text{ °C}$			50	

1. See [Section 4.4: Input offset voltage drift over temperature](#).
2. Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV . The operational amplifier is aged in follower mode configuration. See [Section 4.5: Long-term input offset voltage drift](#).
3. Guaranteed by characterization.
4. Slew rate value is calculated as the average between positive and negative slew rates.
5. Initialization time is defined as the delay after power-up which guarantees operation within specified performances. Guaranteed by design. See [Section 4.6: Initialization time](#).

Table 5. Electrical characteristics at $V_{CC+} = 5\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	$T = 25\text{ }^{\circ}\text{C}$			200	μV
		$-40\text{ }^{\circ}\text{C} < T < 85\text{ }^{\circ}\text{C}$			850	
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			1200	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}^{(1)}$			10	$\mu\text{V}/^{\circ}\text{C}$
ΔV_{io}	Long-term input offset voltage drift	$T = 25\text{ }^{\circ}\text{C}^{(2)}$		0.7		$\frac{\mu\text{V}}{\sqrt{\text{month}}}$
I_{io}	Input offset current ($V_{out} = V_{CC}/2$)	$T = 25\text{ }^{\circ}\text{C}$		1	$10^{(3)}$	pA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$		1	$300^{(3)}$	
I_{ib}	Input bias current ($V_{out} = V_{CC}/2$)	$T = 25\text{ }^{\circ}\text{C}$		1	$10^{(3)}$	pA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$		1	$300^{(3)}$	
CMR	Common mode rejection ratio $20 \log (\Delta V_{icm}/\Delta V_{io})$ $V_{icm} = 0\text{ V to } V_{CC}$, $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$	$T = 25\text{ }^{\circ}\text{C}$	74	94		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	73			
SVR	Supply voltage rejection ratio $20 \log (\Delta V_{CC}/\Delta V_{io})$ $V_{CC} = 1.5\text{ to } 5.5\text{ V}$, $V_{ic} = 0\text{ V}$, $R_L > 1\text{ M}\Omega$	$T = 25\text{ }^{\circ}\text{C}$	71	90		
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	71			
A_{vd}	Large signal voltage gain $V_{out} = 0.5\text{ V to } (V_{CC} - 0.5\text{ V})$	$T = 25\text{ }^{\circ}\text{C}$	95			
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	85			
EMIRR	EMI rejection ratio $\text{EMIRR} = 20 \log (V_{RFpeak}/\Delta V_{io})$	$V_{RF} = 100\text{ mV}_{RFpeak}$, $f = 400\text{ MHz}$		$38^{(4)}$		
		$V_{RF} = 100\text{ mV}_{RFpeak}$, $f = 900\text{ MHz}$		$50^{(4)}$		
		$V_{RF} = 100\text{ mV}_{RFpeak}$, $f = 1800\text{ MHz}$		$60^{(4)}$		
		$V_{RF} = 100\text{ mV}_{RFpeak}$, $f = 2400\text{ MHz}$		$63^{(4)}$		
V_{OH}	High level output voltage ($V_{OH} = V_{CC} - V_{out}$)	$T = 25\text{ }^{\circ}\text{C}$			75	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			80	
V_{OL}	Low level output voltage	$T = 25\text{ }^{\circ}\text{C}$			40	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			60	
I_{out}	I_{sink} ($V_{out} = V_{CC}$)	$T = 25\text{ }^{\circ}\text{C}$	35	56		mA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	20			
	I_{source} ($V_{out} = 0\text{ V}$)	$T = 25\text{ }^{\circ}\text{C}$	35	45		
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	20			
I_{CC}	Supply current (per channel, $V_{out} = V_{CC}/2$, $R_L > 1\text{ M}\Omega$)	$T = 25\text{ }^{\circ}\text{C}$		10	14	μA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			16	

Table 5. Electrical characteristics at $V_{CC+} = 5\text{ V}$ with $V_{CC-} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T = 25\text{ °C}$, and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	110	150		kHz
F_u	Unity gain frequency			120		
Φ_m	Phase margin			45		Degrees
G_m	Gain margin			19		dB
SR	Slew rate ⁽⁵⁾	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$		0.06		V/ μ s
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: $f = 0.1$ to 10 Hz		10		μV_{pp}
e_n	Equivalent input noise voltage	$f = 1\text{ kHz}$		100		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
		$f = 10\text{ kHz}$		96		
THD+N	Total harmonic distortion + noise	$f_{in} = 1\text{ kHz}$, $A_{CL} = 1$, $R_L = 100\text{ k}\Omega$, $V_{icm} = (V_{CC} - 1\text{ V})/2$, $BW = 22\text{ kHz}$, $V_{out} = 0.5\text{ V}_{pp}$		0.008		%
t_{init}	Initialization time ⁽⁶⁾	$T = 25\text{ °C}$			5	ms
		$-40\text{ °C} < T < 125\text{ °C}$			50	

1. See [Section 4.4: Input offset voltage drift over temperature](#).
2. Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV . The operational amplifier is aged in follower mode configuration. See [Section 4.5: Long-term input offset voltage drift](#).
3. Guaranteed by characterization.
4. Tested on SC70-5 package.
5. Slew rate value is calculated as the average between positive and negative slew rates.
6. Initialization time is defined as the delay after power-up to guarantee operation within specified performances. Guaranteed by design. See [Section 4.6: Initialization time](#).

Figure 2. Supply current vs. supply voltage
at $V_{icm} = V_{CC}/2$

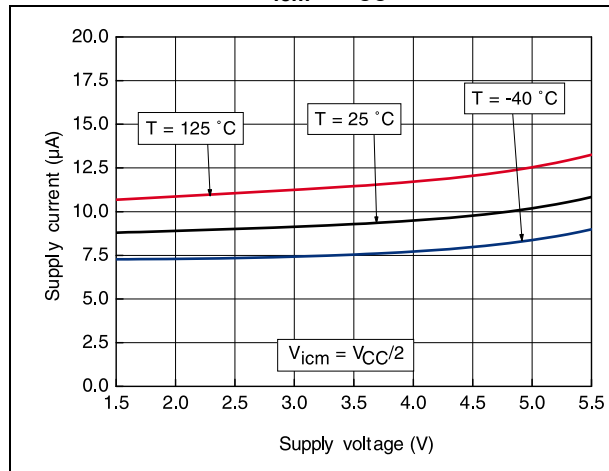


Figure 3. Input offset voltage distribution
at $V_{CC} = 5\text{ V}$, $V_{icm} = V_{CC}/2$

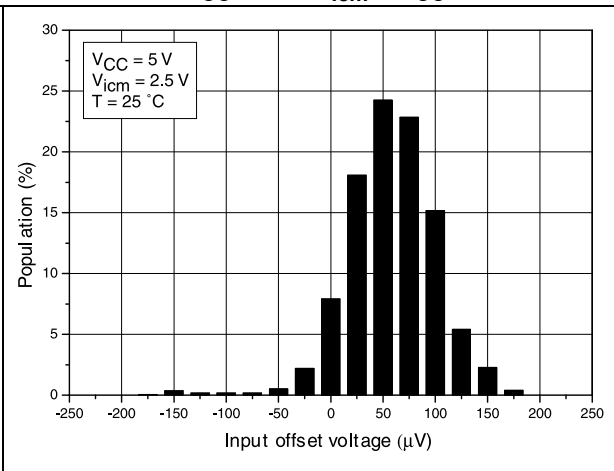


Figure 4. Input offset voltage distribution
at $V_{CC} = 3.3\text{ V}$, $V_{icm} = V_{CC}/2$

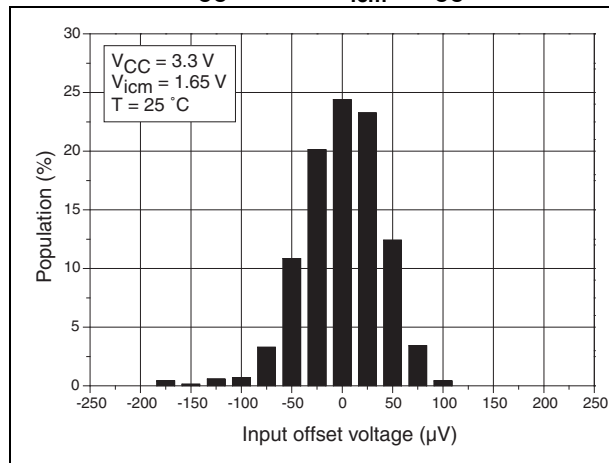


Figure 5. Input offset voltage temperature coefficient distribution

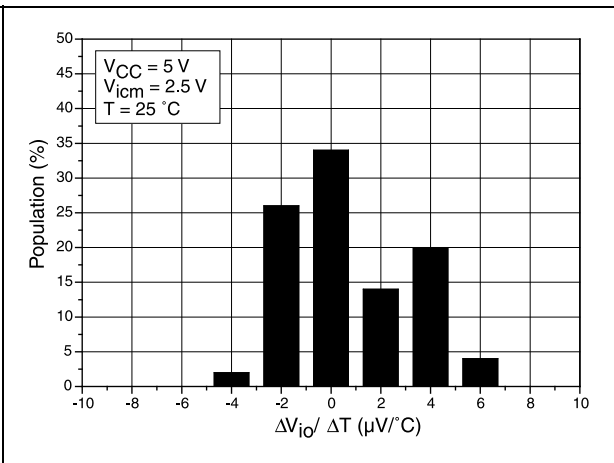


Figure 6. Input offset voltage vs. input common mode voltage

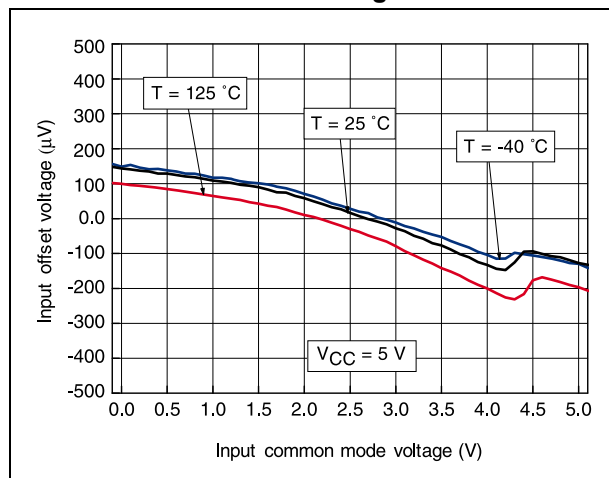


Figure 7. Input offset voltage vs. temperature

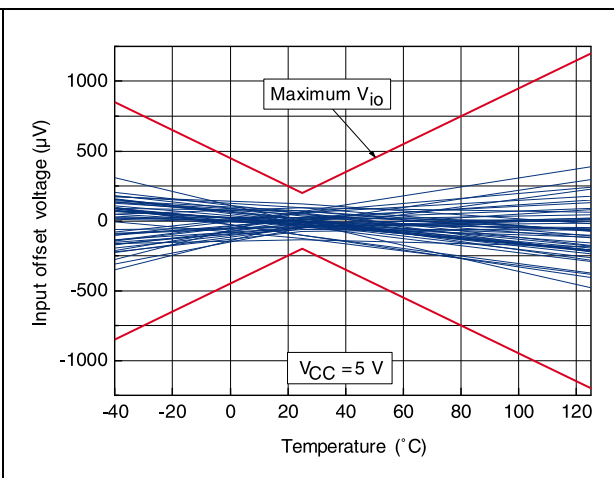


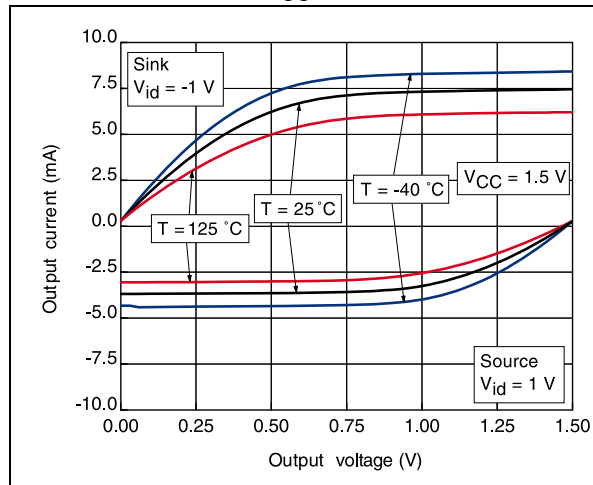
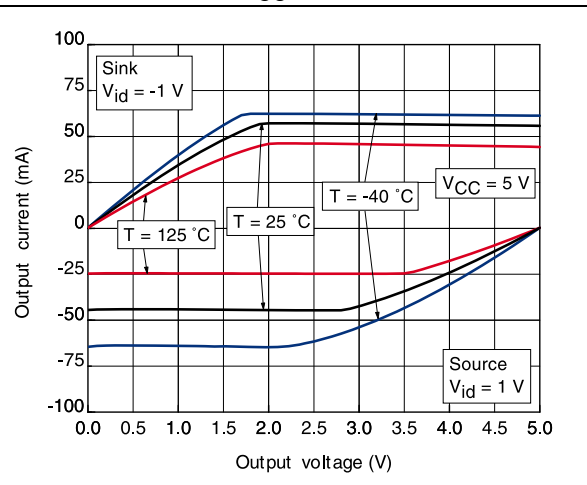
Figure 8. Output current vs. output voltage at $V_{CC} = 1.5\text{ V}$ Figure 9. Output current vs. output voltage at $V_{CC} = 5\text{ V}$ 

Figure 10. Output current vs. supply voltage

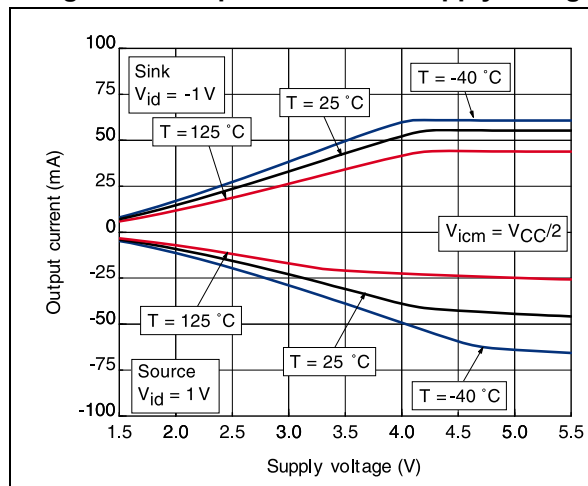
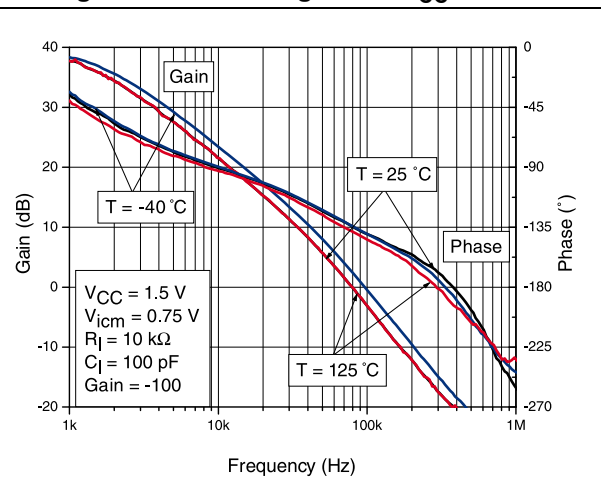
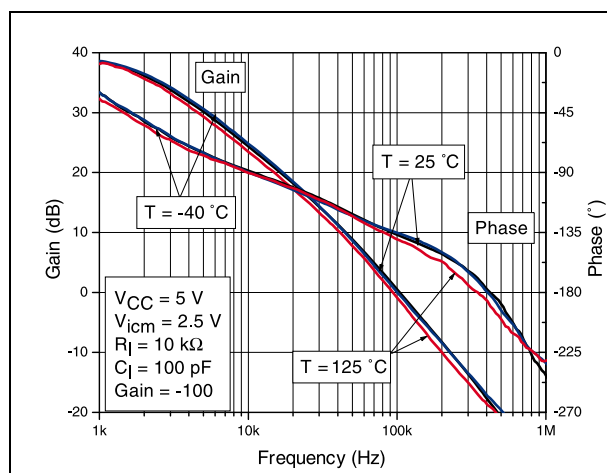
Figure 11. Bode diagram at $V_{CC} = 1.5\text{ V}$ Figure 12. Bode diagram at $V_{CC} = 5\text{ V}$ 

Figure 13. Closed-loop gain diagram vs. capacitive load

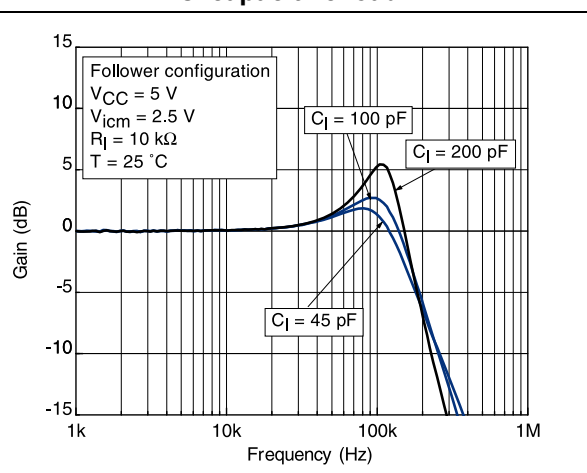


Figure 14. Positive slew rate

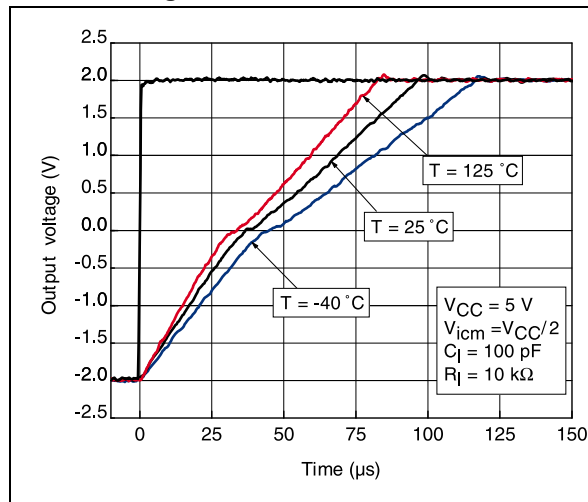


Figure 15. Negative slew rate

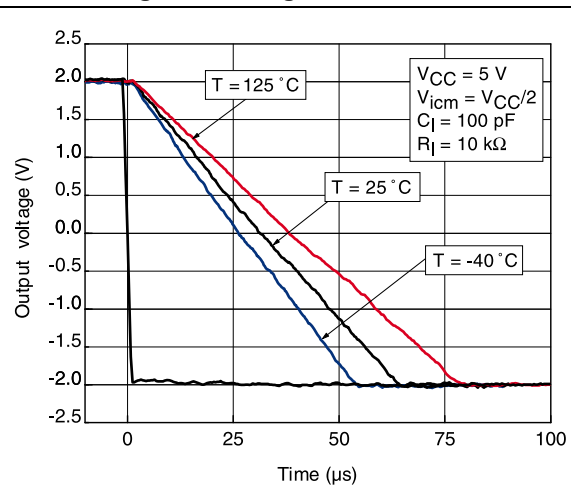


Figure 16. Slew rate vs. supply voltage

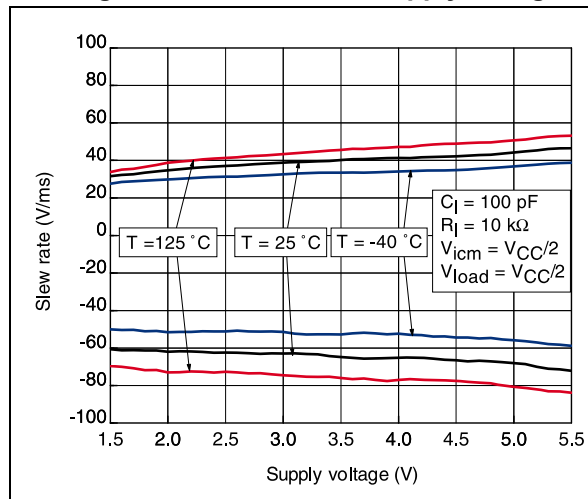


Figure 17. Noise vs. frequency

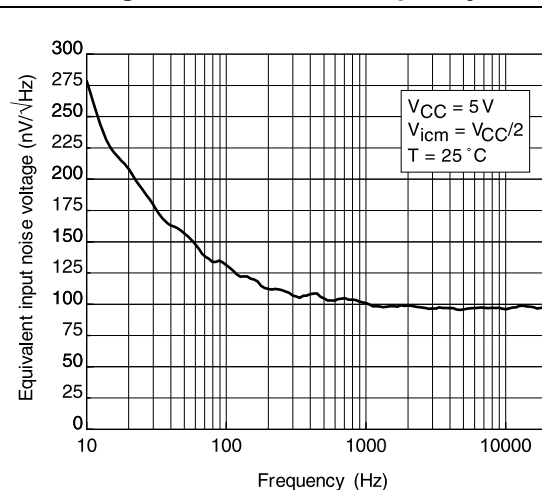


Figure 18. 0.1 Hz to 10 Hz noise

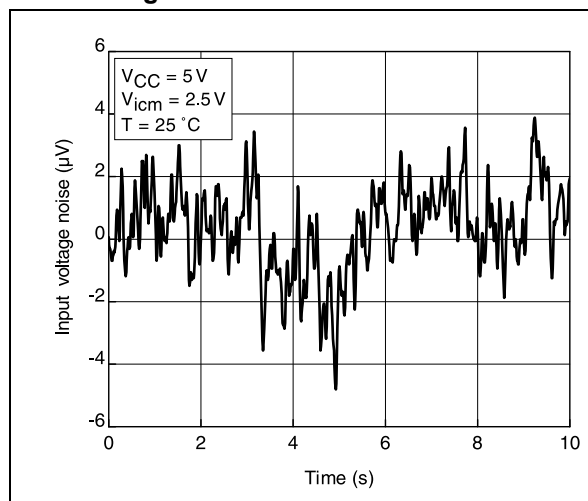


Figure 19. THD+N vs. frequency

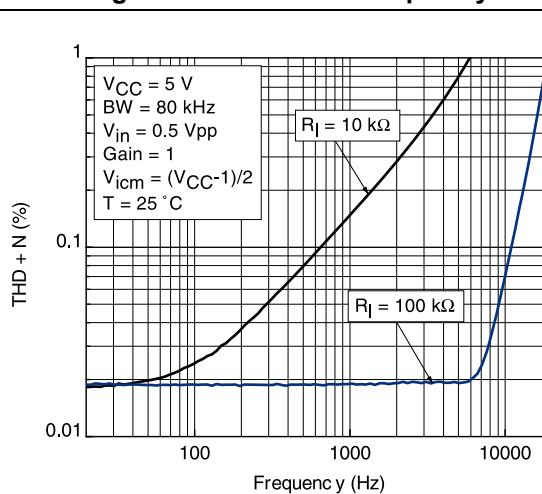


Figure 20. THD+N vs. output voltage

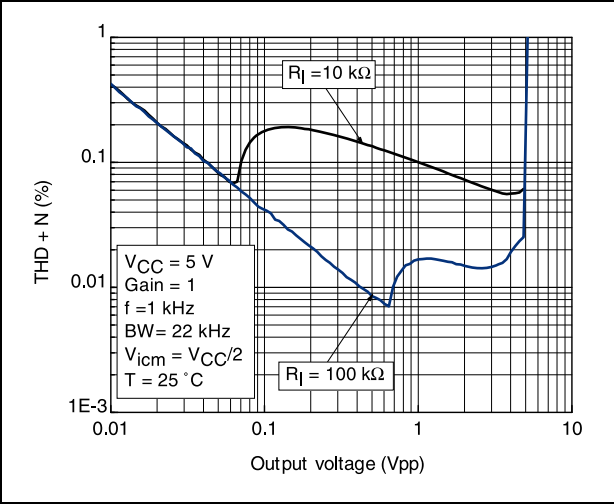
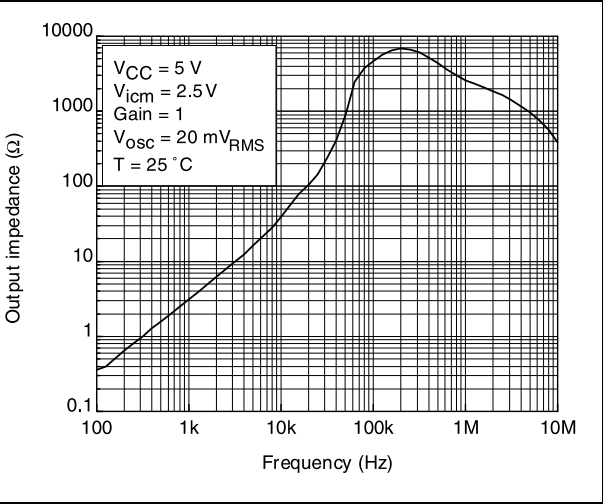


Figure 21. Output impedance vs. frequency in closed-loop configuration



4 Application information

4.1 Operating voltages

The TSV71x series of devices can operate from 1.5 V to 5.5 V. The parameters are fully specified for 1.8 V, 3.3 V, and 5 V power supplies. However, they are very stable in the full V_{CC} range and several characterization curves show TSV71x device characteristics at 1.5 V. In addition, the main specifications are guaranteed in the extended temperature range from -40 °C to +125 °C.

4.2 Rail-to-rail input

The TSV711, TSV712, and TSV714 devices have a rail-to-rail input, and the input common mode range is extended from $V_{CC-} - 0.1$ V to $V_{CC+} + 0.1$ V.

4.3 Rail-to-rail output

The output levels of the TSV71x operational amplifiers can go close to the rails: to a maximum of 40 mV below the upper rail and to a maximum of 75 mV above the lower rail when a 10 kΩ resistive load is connected to $V_{CC}/2$.

4.4 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using [Equation 1](#).

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max \left| \frac{V_{io}(T) - V_{io}(25^\circ \text{C})}{T - 25^\circ \text{C}} \right|$$

with $T = -40$ °C and 125 °C.

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.33.

4.5 Long-term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using [Equation 2](#).

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter ($\beta = 1$)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in [Equation 3](#).

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S} \right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant ($8.6173 \times 10^{-5} \text{ eV.K}^{-1}$)

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F , is the multiplication of the voltage acceleration factor and the temperature acceleration factor ([Equation 4](#)).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in [Equation 5](#) to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$\text{Months} = A_F \times 1000 \text{ h} \times 12 \text{ months} / (24 \text{ h} \times 365.25 \text{ days})$$

To evaluate the op-amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in μV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see [Equation 6](#)).

Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months ([Equation 7](#)).

Equation 7

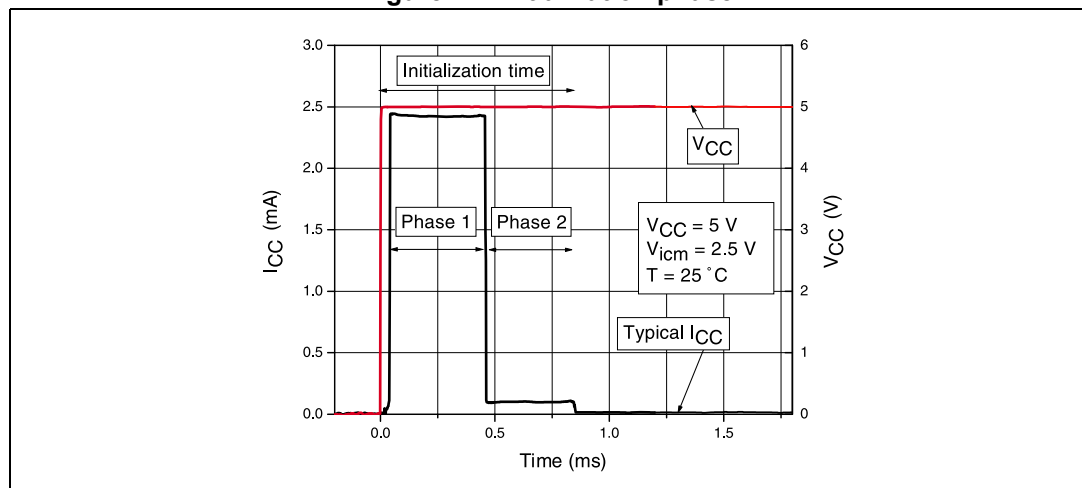
$$\Delta V_{io} = \frac{V_{io} \text{ drift}}{\sqrt{(\text{months})}}$$

where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

4.6 Initialization time

The TSV71x series of devices use a proprietary trimming topology that is initiated at each device power-up and allows excellent V_{io} performance to be achieved. The initialization time is defined as the delay after power-up which guarantees operation within specified performances. During this period, the current consumption (I_{CC}) and the input offset voltage (V_{io}) can be different to the typical ones.

Figure 22. Initialization phase



The initialization time is V_{CC} and temperature dependent. [Table 6](#) sums up the measurement results for different supply voltages and for temperatures varying from $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$.

Table 6. Initialization time measurement results

V_{CC} (V)	Temperature: $-40\text{ }^{\circ}\text{C}$		Temperature: $25\text{ }^{\circ}\text{C}$		Temperature: $125\text{ }^{\circ}\text{C}$	
	T_{init} (ms)	I_{CC} phase 1 (mA)	T_{init} (ms)	I_{CC} phase 1 (mA)	T_{init} (ms)	I_{CC} phase 1 (mA)
1.8	37	0.33	3.2	0.40	0.35	0.46
3.3	2.9	1.4	0.95	1.3	0.34	1.2
5	2.4	3.2	0.85	2.4	0.31	2.9

4.7 PCB layouts

For correct operation, it is advised to add a 10 nF decoupling capacitors as close as possible to the power supply pins.

4.8 Macromodel

Accurate macromodels of the TSV71x devices are available on the STMicroelectronics' website at www.st.com. These model are a trade-off between accuracy and complexity (that is, time simulation) of the TSV71x operational amplifiers. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, *but they do not replace on-board measurements*.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

5.1 SC70-5 package information

Figure 23. SC70-5 package mechanical drawing

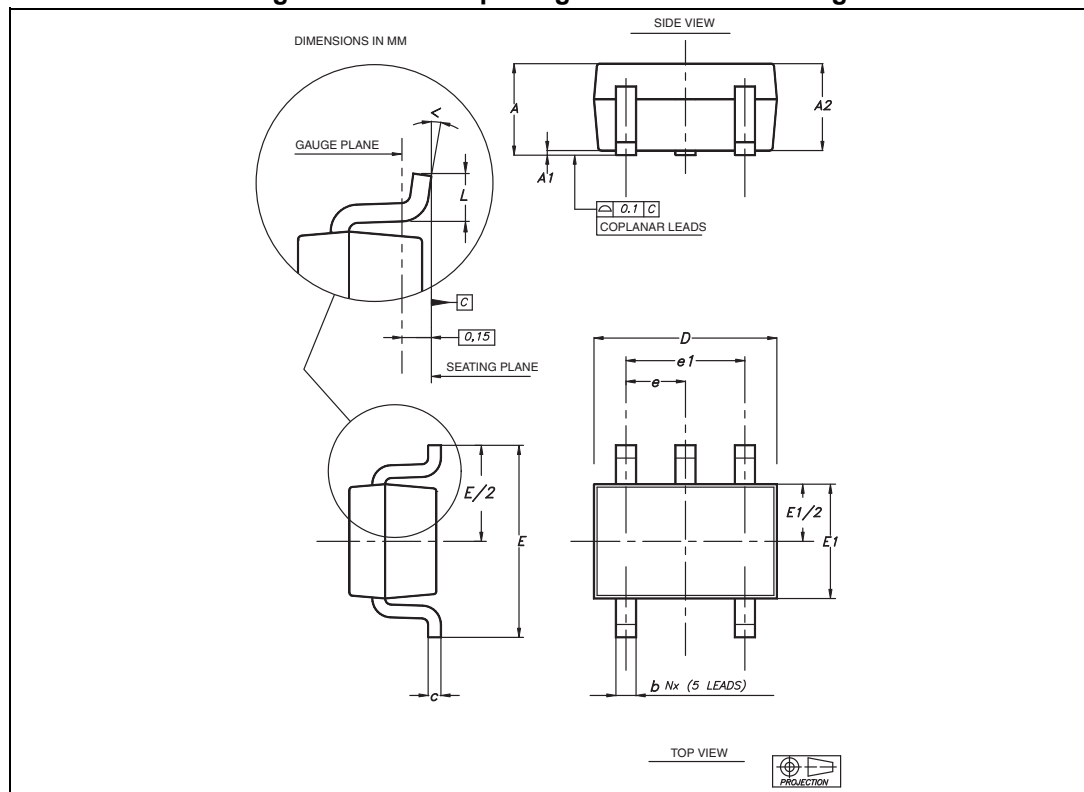


Table 7. SC70-5 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1	0		0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

5.2 DFN8 2x2 package information

Figure 24. DFN8 2x2 package mechanical drawing

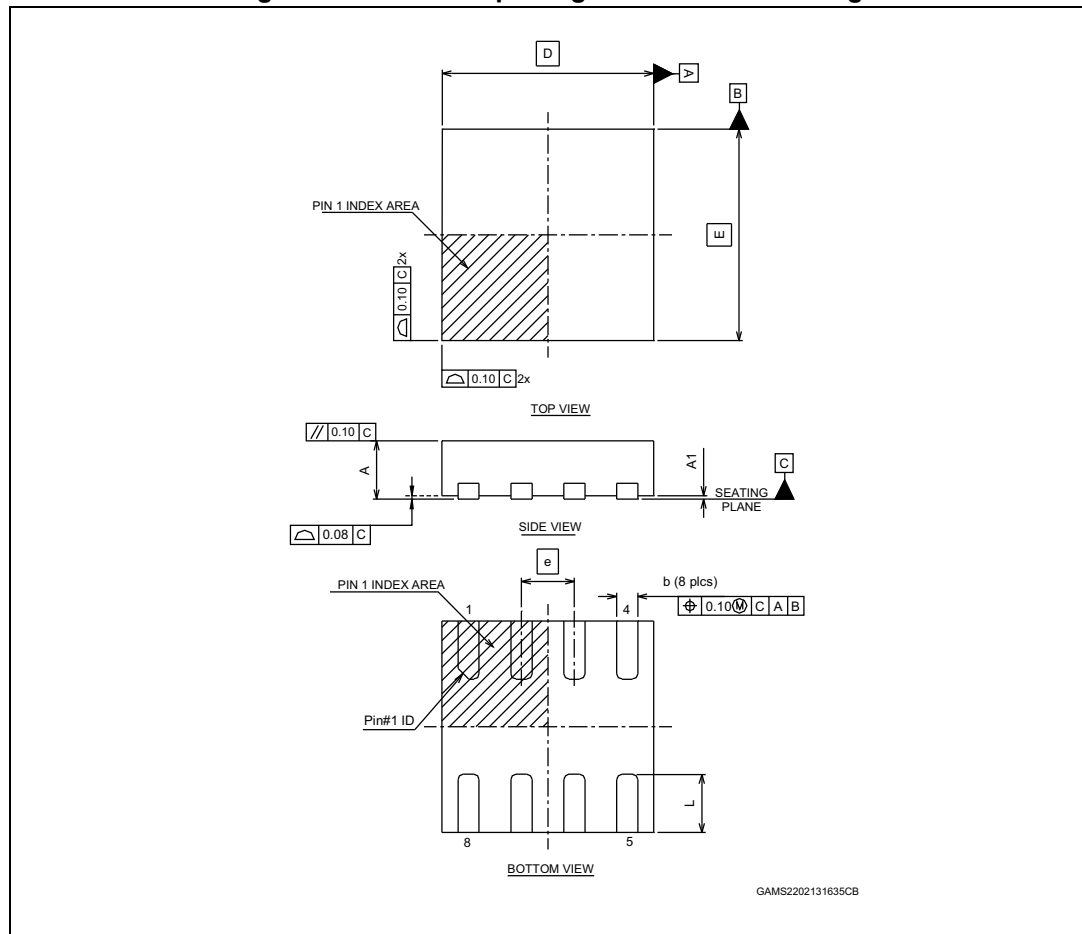


Table 8. DFN8 2x2 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		2.00			0.079	
E		2.00			0.079	
e		0.50			0.020	
L	0.045	0.55	0.65	0.018	0.022	0.026
N	8			8		

5.3 MiniSO-8 package information

Figure 25. MiniSO-8 package mechanical drawing

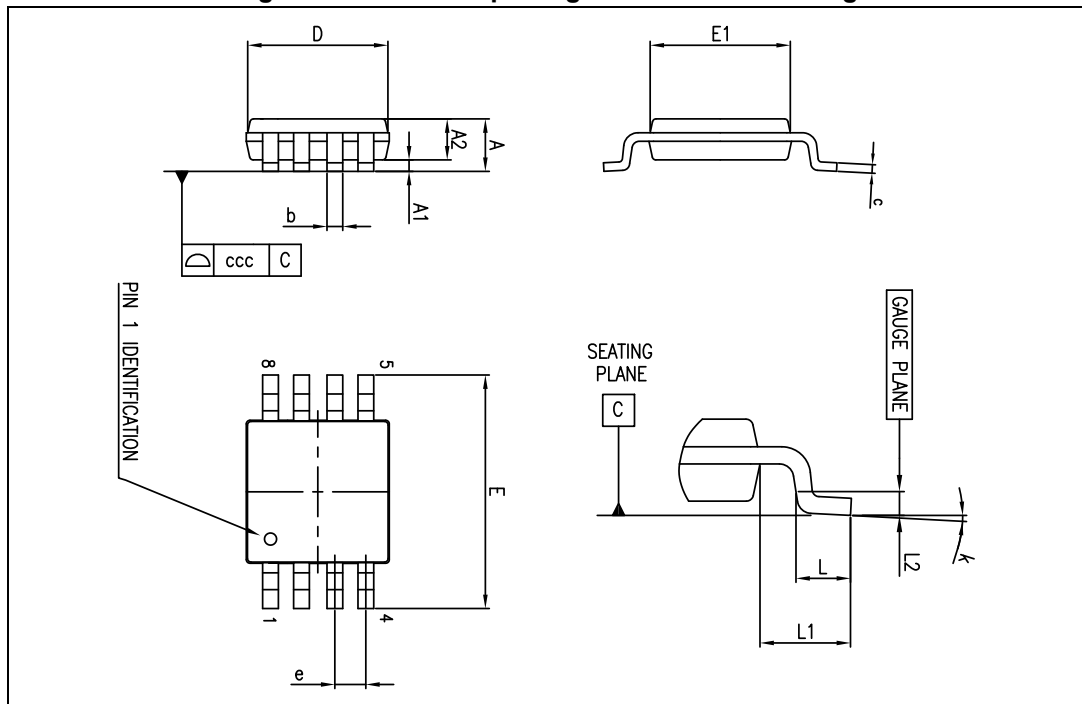


Table 9. MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0 °		8 °	0 °		8 °
ccc			0.10			0.004

5.4 QFN16 3x3 package information

Figure 26. QFN16 3x3 package mechanical drawing

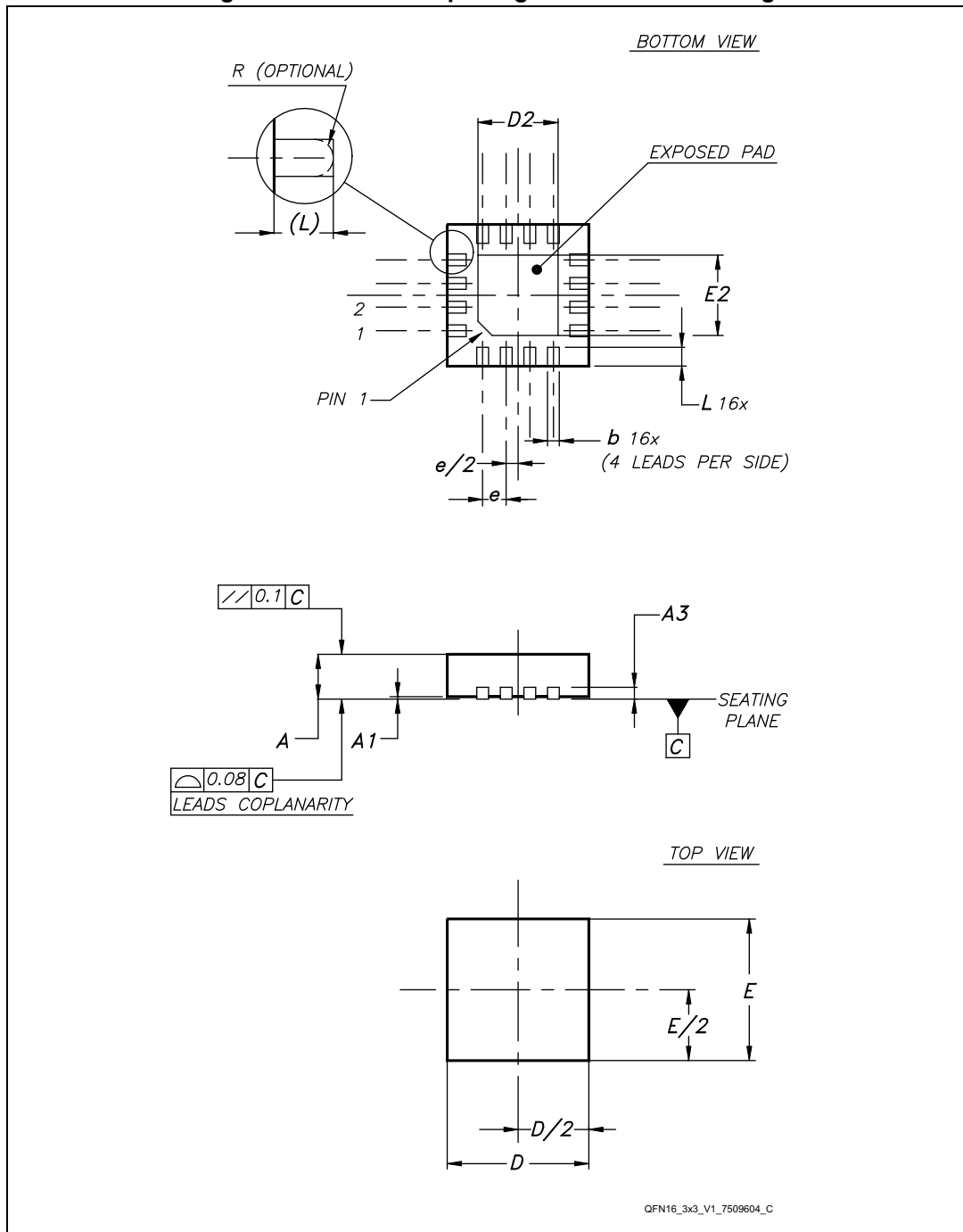
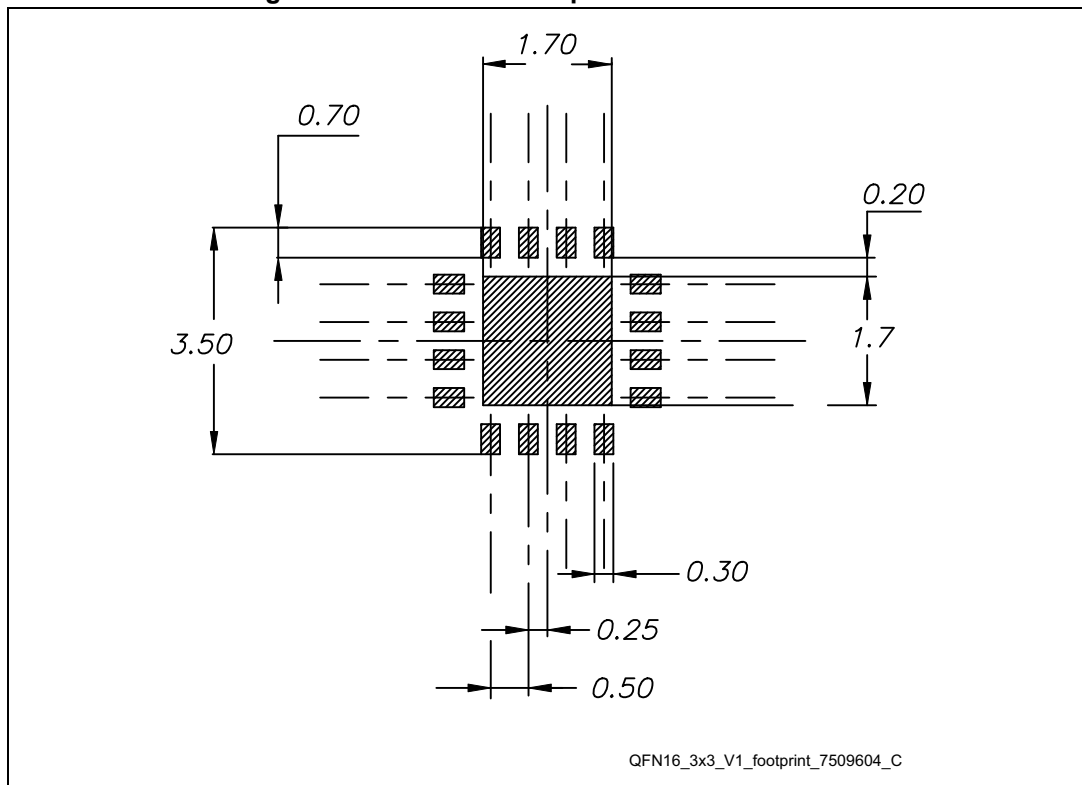


Table 10. QFN16 3x3 mm package mechanical data (pitch 0.5 mm)

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0		0.05	0		0.002
A3		0.20			0.008	
b	0.18		0.30	0.007		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.50		1.80	0.059		0.071
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.80	0.059		0.071
e		0.50			0.020	
L	0.30		0.50	0.012		0.020

Figure 27. QFN16 3x3 footprint recommendation



5.5 TSSOP14 package information

Figure 28. TSSOP14 package mechanical drawing

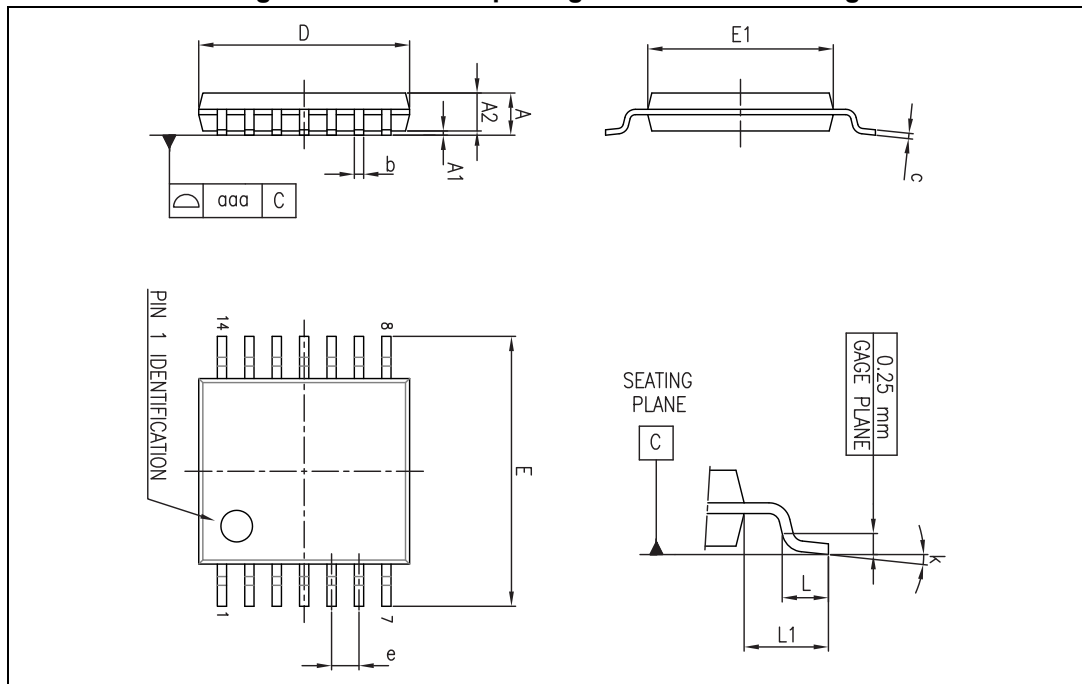


Table 11. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0 °		8 °	0 °		8 °
aaa			0.10			0.004

6 Ordering information

Table 12. Order codes

Order code	Temperature range	Package	Packaging	Marking
TSV711ICT	-40° C to +125° C	SC70-5	Tape and reel	K1W
TSV712IQ2T		DFN8 2x2		K1W
TSV712IST		MiniSO8		V712
TSV714IQ4T		QFN16 3x3		K1W
TSV714IPT		TSSOP14		TSV714IP

7 Revision history

Table 13. Document revision history

Date	Revision	Changes
26-Sep-2012	1	Initial internal release
26-Mar-2013	2	Initial public release. Datasheet updated for two new products: TSV712 and TSV714. Four new packages added: DFN8 2x2, MiniSO-8, QFN16 3x3, and TSSOP14. Updated Table 3 , Table 4 , and Table 5 . Section 4: Application information : re-written

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT AUTHORIZED FOR USE IN WEAPONS. NOR ARE ST PRODUCTS DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

