

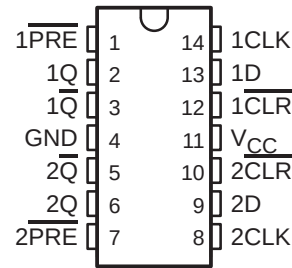
74AC11074

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS499A – DECEMBER 1986 – REVISED APRIL 1996

- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (D) and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic 300-mil DIPs (N)

D, N, OR PW PACKAGE
(TOP VIEW)



description

This device contains two independent positive-edge-triggered D-type flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input that meets the setup-time requirements are transferred to the outputs on the low-to-high transition of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The 74AC11074 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\overline{Q}_0$

[†] This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

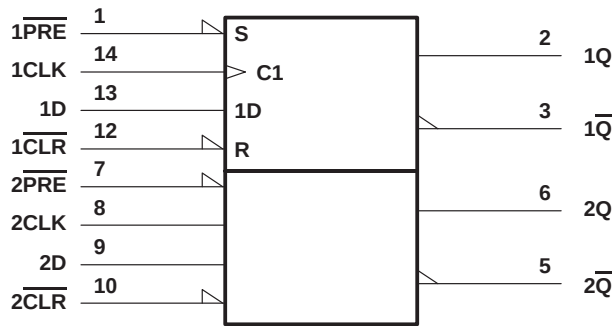
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated

74AC11074
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH CLEAR AND PRESET

SCAS499A – DECEMBER 1986 – REVISED APRIL 1996

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
N package	1.1 W
PW package	0.5 W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

74AC11074

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS499A – DECEMBER 1986 – REVISED APRIL 1996

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1		V
		$V_{CC} = 4.5\text{ V}$	3.15		
		$V_{CC} = 5.5\text{ V}$	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3\text{ V}$		0.9	V
		$V_{CC} = 4.5\text{ V}$		1.35	
		$V_{CC} = 5.5\text{ V}$		1.65	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3\text{ V}$		–4	mA
		$V_{CC} = 4.5\text{ V}$		–24	
		$V_{CC} = 5.5\text{ V}$		–24	
I_{OL}	Low-level output current	$V_{CC} = 3\text{ V}$		12	mA
		$V_{CC} = 4.5\text{ V}$		24	
		$V_{CC} = 5.5\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
		5.5 V				3.85		
V_{OL}	$I_{OL} = 50\text{ }\mu\text{A}$	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	$I_{OL} = 12\text{ mA}$	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
	$I_{OL} = 24\text{ mA}$	5.5 V			0.36		0.44	
		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS499A – DECEMBER 1986 – REVISED APRIL 1996

timing requirements over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Figure 1)

			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4		4		ns
		CLK low or high	5		5		
t_{su}	Setup time before CLK $\uparrow$	Data high or low	5		5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	1		1		
t_h	Hold time after CLK $\uparrow$		0		0		ns

timing requirements over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see Figure 1)

			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	125	0	125	MHz
t_w	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4		4		ns
		CLK low or CLK high	4		4		
t_{su}	Setup time before CLK $\uparrow$	Data high or low	3.5		3.5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	1		1		
t_h	Hold time after CLK $\uparrow$		0		0		ns

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100	125		100		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	1.5	5.8	9.3	1.5	10	ns
t_{PHL}			1.5	6.5	11.4	1.5	12.2	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	1.5	7.7	10.5	1.5	11.3	ns
t_{PHL}			1.5	7.3	9.7	1.5	10.6	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			125	150		125		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	1.5	4.2	6.6	1.5	7.1	ns
t_{PHL}			1.5	4.7	8.2	1.5	9	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$	1.5	5.4	7.5	1.5	8.2	ns
t_{PHL}			1.5	5	6.9	1.5	7.5	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

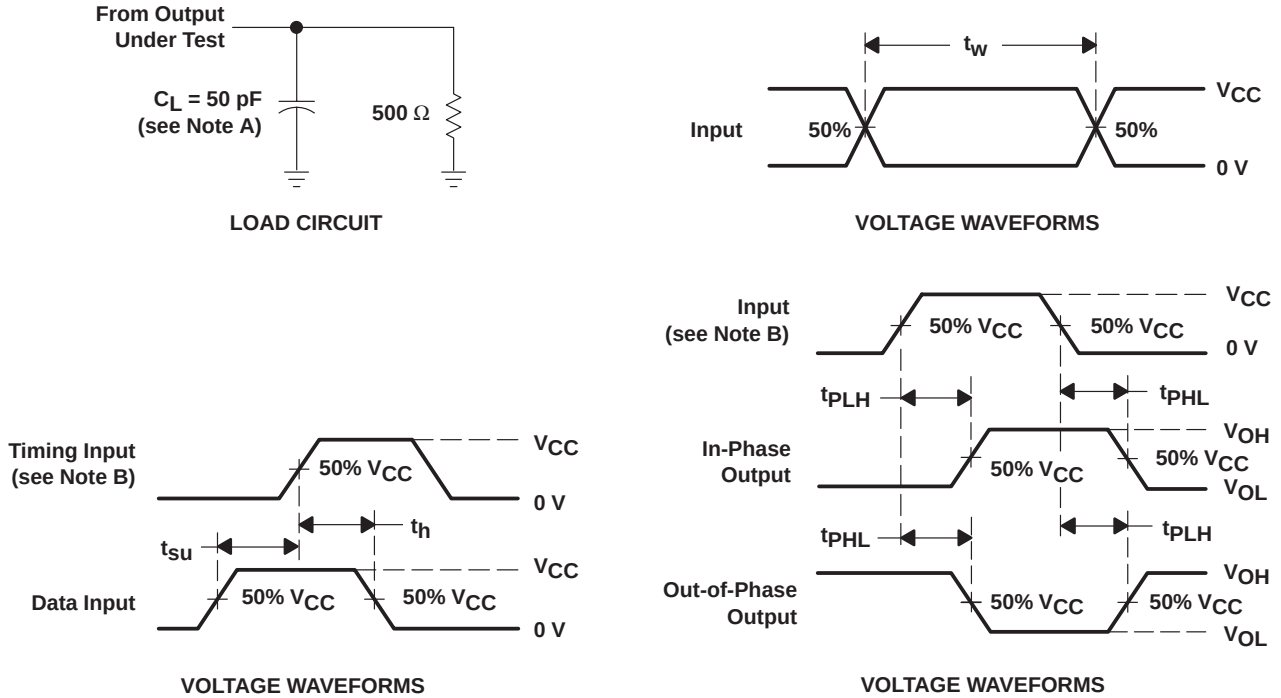
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$		30	pF

74AC11074

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS499A – DECEMBER 1986 – REVISED APRIL 1996

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.