PIC16(L)F183XX

Full-Featured, Low Pin Count Microcontrollers with XLP Product Brief

Description

PIC16(L)F183XX microcontrollers feature Analog, Core Independent Peripherals and communication peripherals, combined with eXtreme Low Power (XLP) for a wide range of general purpose and low-power applications. The Peripheral Pin Select (PPS) functionality enables pin mapping when using the digital peripherals (CLC, CWG, CCP, PWM and communications) to add flexibility to the application design.

Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-Bit Timers
- Up to Three 16-Bit Timers
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Extended Watchdog Timer (WDT) with Dedicated On-Chip Oscillator for Reliable Operation
- Programmable Code Protection

Memory

- Up to 28 KB Program Flash Memory (PFM)
- Up to 2 KB Data SRAM Memory
- 256B of EEPROM Data Flash Memory (DFM)
- Direct, Indirect and Relative Addressing modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF183XX)
  - 2.3V to 5.5V (PIC16F183XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

eXtreme Low-Power (XLP) Features

- Sleep mode: 40 nA @ 1.8V, typical
- Watchdog Timer: 250 nA @ 1.8V, typical
- Secondary Oscillator: 300 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 37 uA/MHz @ 1.8V, typical

Power-Saving Functionality

- Doze mode: Ability to run the CPU core slower than the system clock used by the internal peripherals
- Idle mode: Ability to put the CPU core to sleep while internal peripherals continue operating from the system clock
- Sleep mode: Lowest Power Consumption
- Peripheral Module Disable: Peripheral power disable hardware module to minimize power consumption of unused peripherals

Digital Peripherals

- Configurable Logic Cell (CLC):
  - Up to four CLCs
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Up to two CWGs
  - Multiple signal sources
- Up to Four Capture/Compare/PWM (CCP) modules
- PWM: Two 10-bit Pulse-Width Modulators
- Numerically Controlled Oscillator (NCO):
  - Precision linear frequency generator (@50% duty cycle) with 0.0001% step size of source input clock
  - Input Clock: 0 Hz < F_{NCO} < 32 MHz
  - Resolution: $F_{NCO}/2^{20}$
- Serial Communications:
  - SPI, I^2C, EUSART
  - RS-232, RS-485, LIN compatible
- Data Signal Modulator (DSM):
  - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms

- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals
- Up to 18 I/O Pins:
  - Individually programmable pull ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable

Analog Peripherals

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 17 external channels
  - Conversion available during Sleep
- Comparator:
  - Up to two comparators
  - Low and High-Speed modes
  - Fixed Voltage Reference at inverting/ noninverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

Clocking Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 32 MHz
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOCS)
- External High-Speed Crystal Oscillators

TABLE 1: PIC16(L)F183XX Family Types

Device	Data Sheet Index	Program Memory (KB)	Program Memory (KW)	EEPROM (B)	RAM (B)	I/Os(1)	10-bit ADCs	Comparators	5-bit DAC	Timers 0/1/2	CCP/PWM	CWG	EUSART	SPI	I^2C	CLC	NCO	PPS	ICD(2)
PIC16(L)F18313	(A)	3.5	2	256	256	6	5	1	1	1/1/1	2/2	1	1	1	1	2	1	Y	I
PIC16(L)F18323	(A)	3.5	2	256	256	12	11	2	1	1/1/1	2/2	1	1	1	1	2	1	Y	I
PIC16(L)F18324	(B)	7	4	256	512	12	11	2	1	1/3/3	4/2	2	1	1	1	4	1	Y	I
PIC16(L)F18325	(C)	14	8	256	1K	12	11	2	1	1/3/3	4/2	2	1	2	2	4	1	Y	I
PIC16(L)F18326	(D)	28	16	256	2K	12	11	2	1	1/3/3	4/2	2	1	2	2	4	1	Y	I
PIC16(L)F18344	(B)	7	4	256	512	18	17	2	1	1/3/3	4/2	2	1	1	1	4	1	Y	I
PIC16(L)F18345	(C)	14	8	256	1K	18	17	2	1	1/3/3	4/2	2	1	2	2	4	1	Y	I
PIC16(L)F18346	(D)	28	16	256	2K	18	17	2	1	1/3/3	4/2	2	1	2	2	4	1	Y	I

Note 1: One pin is input-only.
2: Debugging Methods: (I) – Integrated on Chip; E – using Emulation Header.

Data Sheet Index: (Unshaded devices are described in this document.)

A) DS40001799 PIC16(L)F18313/18323 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP
B) DS40001800 PIC16(L)F18324/18344 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP
C) DS40001795 PIC16(L)F18325/18345 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP
D) Future Release PIC16(L)F18326/18346 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

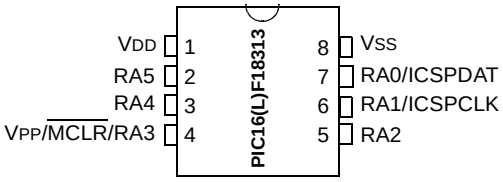
TABLE 2: PACKAGES

Packages	PDIP	SOIC	UDFN	TSSOP	UQFN	SSOP
PIC16(L)F18313	X	X	X			
PIC16(L)F18323	X	X		X	X	
PIC16(L)F18324	X	X		X	X	
PIC16(L)F18325	X	X		X	X	
PIC16(L)F18326	X	X		X	X	
PIC16(L)F18344	X	X			X	X
PIC16(L)F18345	X	X			X	X
PIC16(L)F18346	X	X			X	X

Note: Pin details are subject to change.

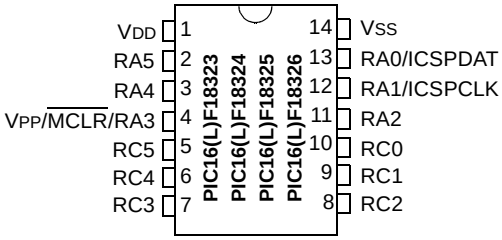
PIN DIAGRAMS

Pin Diagram – 8-Pin PDIP, SOIC, UDFN



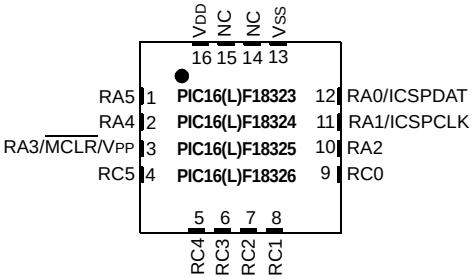
Note: See Table 3 for location of all peripheral functions.

Pin Diagram – 14-Pin PDIP, SOIC, TSSOP



Note: See Table 4, Table 5, Table 6 and Table 7 for location of all peripheral functions.

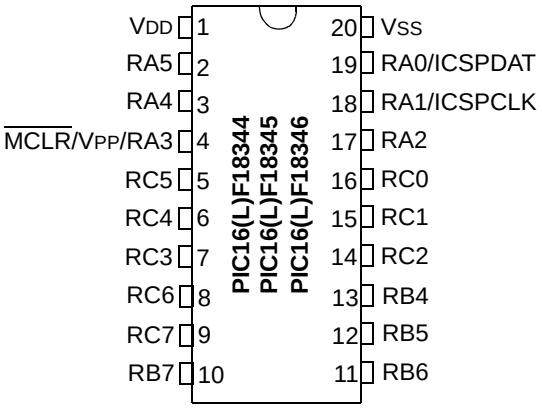
Pin Diagram – 16-Pin UQFN (4x4)



Note 1: See Table 4, Table 5, Table 6 and Table 7 for location of all peripheral functions.

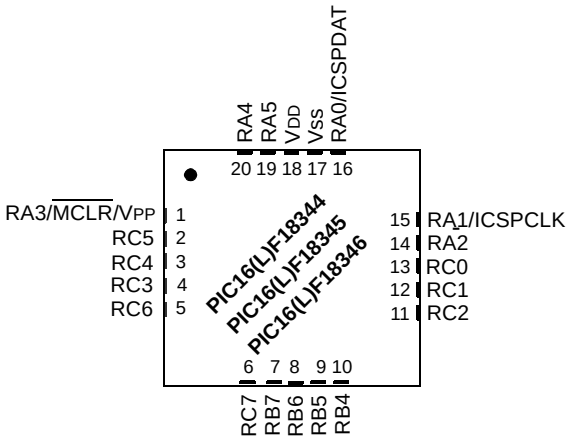
2: It is recommended that the exposed bottom pad be connected to VSS.

Pin Diagram – 20-Pin PDIP, SOIC, SSOP



Note: See Table 8, Table 9 and Table 10 for location of all peripheral functions.

Pin Diagram – 20-Pin UQFN (4x4)



Note 1: See Table 8, Table 9 and Table 10 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to VSS.

PIN ALLOCATION TABLES

TABLE 3: 8-PIN ALLOCATION TABLE (PIC16(L)F18313)

I/O(2)	8-Pin PDIP/SOIC/UDFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	7	ANA0	—	C1IN0+	—	DAC1OUT	MDCIN1(1)	—	—	—	—	—	TX(1) CK(1)	CLCIN3(1)	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	6	ANA1	VREF+	C1IN0-	—	DAC1REF+	MDMIN(1)	—	—	—	—	SCK(1) SCL(1,3,4)	RX(1) DT(1,3)	CLCIN2(1)	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	5	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	—	—	CWG1(1)	SDA(1,3,4) SDO(1)	—	—	—	INT(1) IOCA2	Y	—
RA3	4	—	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	CLCIN0(1)	—	IOCA3	Y	$\overline{MCLR}$ VPP
RA4	3	ANA4	—	C1IN1-	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	ANA5	—	—	—	—	MDCIN2(1)	T1CKI(1) SOSCIN SOSCI	CCP1(1) CCP2(1)	—	—	—	—	CLCIN1(1)	—	IOCA5	Y	CLKIN OSC1
VDD	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A	SDA(3)	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	—	—	—	—	CCP2	PWM6	CWG1B	SCL(3)	DT(3)	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	CWG1C	SDO	TX	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	CWG1D	SCK	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to the other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ ST as selected by the INLVL register.

TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18323)

I/O(2)	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	—	—	CWG1(1)	—	—	—	—	INT(1) IOCA2	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{\text{MCLR}}$ VPP
RA4	3	2	ANA4	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI(1) SOSCIN SOSCI	—	—	—	—	—	CLCIN3(1)	—	IOCA5	Y	CLKIN OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	—	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	CLCIN2(1)	—	IOCC1	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	—	CCP2(1)	—	—	$\overline{\text{SS}}$(1)	—	CLCIN0(1)	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	—	—	—	—	—	TX(1) CK(1)	CLCIN1(1)	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCIN2(1)	—	CCP1(1)	—	—	—	RX(1) DT(1,3)	—	—	IOCC5	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18323) (CONTINUED)

I/O(2)	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT(2)	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A	SDA(3)	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B	SCL(3)	DT(3)	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	CWG1C	SDO	TX	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	CWG1D	SCK	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

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TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324)

I/O(2)	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1(1) CWG2(1)	—	—	—	—	INT(1) IOCA2	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{\text{MCLR}}$ VPP
RA4	3	2	ANA4	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI(1) SOSCIN SOSCI	—	—	—	—	—	CLCIN3(1)	—	IOCA5	Y	CLKIN OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI(1)	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4(1)	—	—	SDI(1) SDA(1,3,4)	—	CLCIN2(1)	—	IOCC1	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	T5G(1)	CCP2(1)	—	—	$\overline{\text{SS}}$(1)	—	CLCIN0(1)	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	T3G(1)	—	—	—	—	TX(1) CK(1)	CLCIN1(1)	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCIN2(1)	T3CKI(1)	CCP1(1)	—	—	—	RX(1) DT(1,3)	—	—	IOCC5	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324) (CONTINUED)

I/O[2]	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT[2]	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA[3]	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL[3]	DT[3]	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK	—	CLC4OUT	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325)

I/O(2)	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	$\overline{SS2}$(1)	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1(1) CWG2(1)	—	—	—	—	INT(1) IOCA2	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{MCLR}$ VPP
RA4	3	2	ANA4	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI(1) SOSCIN SOSCI	—	—	—	—	—	CLCIN3(1)	—	IOCA5	Y	CLKIN OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI(1)	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4(1)	—	—	SDI1(1) SDA1(1,3,4)	—	CLCIN2(1)	—	IOCC1	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	T5G(1)	CCP2(1)	—	—	$\overline{SS1}$(1)	—	CLCIN0(1)	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	T3G(1)	—	—	—	SCK2(1) SCL2(1,3,4)	TX(1) CK(1)	CLCIN1(1)	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCIN2(1)	T3CKI(1)	CCP1(1)	—	—	SDI2(1) SDA2(1,3,4)	RX(1) DT(1,3)	—	—	IOCC5	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325) (CONTINUED)

I/O[2]	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT[2]	—	—	—	—	C1OUT	DDS	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA1[3] SDA2[3]	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL1[3] SCL2[3]	DT[3]	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO1 SDO2	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK1 SCK2	—	CLC4OUT	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 7: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18326)

I/O(2)	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	$\overline{SS2}$(1)	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1(1) CWG2(1)	—	—	—	—	INT(1) IOCA2	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{MCLR}$ VPP
RA4	3	2	ANA4	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI(1) SOSCIN SOSCI	—	—	—	—	—	CLCIN3(1)	—	IOCA5	Y	CLKIN OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI(1)	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4(1)	—	—	SDI1(1) SDA1(1,3,4)	—	CLCIN2(1)	—	IOCC1	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	T5G(1)	CCP2(1)	—	—	$\overline{SS1}$(1)	—	CLCIN0(1)	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	T3G(1)	—	—	—	SCK2(1) SCL2(1,3,4)	TX(1) CK(1)	CLCIN1(1)	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCIN2(1)	T3CKI(1)	CCP1(1)	—	—	SDI2(1) SDA2(1,3,4)	RX(1) DT(1,3)	—	—	IOCC5	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 7: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18326) (CONTINUED)

I/O[2]	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT[2]	—	—	—	—	C1OUT	DDS	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA1[3] SDA2[3]	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL1[3] SCL2[3]	DT[3]	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO1 SDO2	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK1 SCK2	—	CLC4OUT	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18344)

I/O(2)	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	18	15	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1(1) CWG2(1)	—	—	CLCIN0(1)	—	INT(1) IOCA2	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{MCLR}$ VPP
RA4	3	20	ANA4	—	—	—	—	—	T1G(1) T3G(1) T5G(1) SOSCO	CCP4(1)	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI(1) T3CKI(1) T5CKI(1) SOSCIN SOSCI	—	—	—	—	—	—	—	IOCA5	Y	CLKIN OSC1
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3,4)	—	CLCIN2(1)	—	IOCB4	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	—	RX(1) DT(1)	CLCIN3(1)	—	IOCB5	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK(1) SCL(1,3,4)	—	—	—	IOCB6	Y	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	—	TX(1) CK(1)	—	—	IOCB7	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOCC2	Y	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18344) (CONTINUED)

I/O(2)	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	—	CCP2(1)	—	—	—	—	CLCIN1(1)	—	IOCC3	Y	—
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC4	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2(1)	—	CCP1(1)	—	—	—	—	—	—	IOCC5	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	—	—	IOCC6	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO	DT(3)	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL(3)	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA(3)	—	CLC4OUT	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 9: 20-PIN ALLOCATION TABLE (PIC16(L)F18345)

I/O(2)	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	18	15	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	$\overline{SS2}$(1)	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1(1) CWG2(1)	—	—	CLCIN0(1)	—	INT(1) IOCA2	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{MCLR}$ VPP
RA4	3	20	ANA4	—	—	—	—	—	T1G(1) T3G(1) T5G(1) SOSCO	CCP4(1)	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI(1) T3CKI(1) T5CKI(1) SOSCIN SOSCI	—	—	—	—	—	—	—	IOCA5	Y	CLKIN OSC1
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SDI1(1) SDA1(1,3,4)	—	CLCIN2(1)	—	IOCB4	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	SDI2(1) SDA2(1,3,4)	RX(1) DT(1)	CLCIN3(1)	—	IOCB5	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	IOCB6	Y	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	SCK2(1) SCL2(1,3,4)	TX(1) CK(1)	—	—	IOCB7	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	—	CCP2(1)	—	—	—	—	CLCIN1(1)	—	IOCC3	Y	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 9: 20-PIN ALLOCATION TABLE (PIC16(L)F18345) (CONTINUED)

I/O(2)	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC4	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2(1)	—	CCP1(1)	—	—	—	—	—	—	IOCC5	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	—	—	IOCC6	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO1 SDO2	DT(3)	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK1 SCK2	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL1(3) SCL2(3)	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA1(3) SDA2(3)	—	CLC4OUT	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 10: 20-PIN ALLOCATION TABLE (PIC16(L)F18346)

I/O(2)	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	18	15	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	$\overline{SS}2$(1)	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1(1) CWG2(1)	—	—	CLCIN0(1)	—	INT(1) IOCA2	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{MCLR}$ VPP
RA4	3	20	ANA4	—	—	—	—	—	T1G(1) T3G(1) T5G(1) SOSCO	CCP4(1)	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI(1) T3CKI(1) T5CKI(1) SOSCIN SOSCI	—	—	—	—	—	—	—	IOCA5	Y	CLKIN OSC1
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SDI1(1) SDA1(1,3,4)	—	CLCIN2(1)	—	IOCB4	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	SDI2(1) SDA2(1,3,4)	RX(1) DT(1)	CLCIN3(1)	—	IOCB5	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	IOCB6	Y	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	SCK2(1) SCL2(1,3,4)	TX(1) CK(1)	—	—	IOCB7	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOCC2	Y	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 10: 20-PIN ALLOCATION TABLE (PIC16(L)F18346) (CONTINUED)

I/O(2)	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	—	CCP2(1)	—	—	—	—	CLCIN1(1)	—	IOCC3	Y	—
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC4	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2(1)	—	CCP1(1)	—	—	—	—	—	—	IOCC5	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	—	—	—	IOCC6	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO1 SDO2	DT(3)	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK1 SCK2	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL1(3) SCL2(3)	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA1(3) SDA2(3)	—	CLC4OUT	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

Note the following details of the code protection feature on Microchip devices:

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