DS36C280 Slew Rate Controlled CMOS EIA-RS-485 Transceiver

Check for Samples: DS36C280

FEATURES

- **100% RS-485 Compliant**
  - **Guaranteed RS-485 Device Interoperation**
- **Low Power CMOS Design: I_{CC} 500 µA max**
- **Adjustable Slew Rate Control**
  - **Minimizes EMI Effects**
- **Built-In Power Up/Down Glitch-Free Circuitry**
  - **Permits Live Transceiver Insertion/Displacement**
- **SOIC Packages**
- **Industrial Temperature Range: −40°C to +85°C**
- **On-board Thermal Shutdown Circuitry**
  - **Prevents Damage to the Device in the Event of Excessive Power Dissipation**
- **Wide Common Mode Range: −7V to +12V**
- **Receiver Open Input Fail-safe (1)**
- **¼ unit load (DS36C280): ≥128 nodes**
- **½ unit load (DS36C280T): ≥64 nodes**
- **ESD (human body model): ≥2 kV**

(1) Non-terminated, Open Inputs only

DESCRIPTION

The DS36C280 is a low power differential bus/line transceiver designed to meet the requirements of RS-485 Standard for multipoint data transmission. In addition, it is compatible with TIA/EIA-422-B.

The slew rate control feature allows the user to set the driver rise and fall times by using an external resistor. Controlled edge rates can reduce switching EMI.

The CMOS design offers significant power savings over its bipolar and ALS counterparts without sacrificing ruggedness against ESD damage. The device is ideal for use in battery powered or power conscious applications. I_{CC} is specified at 500 µA maximum.

The driver and receiver outputs feature TRI-STATE capability. The driver outputs operate over the entire common mode range of −7V to +12V. Bus contention or fault situations are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

The receiver incorporates a fail safe circuit which guarantees a high output state when the inputs are left open (1).

Connection and Logic Diagram

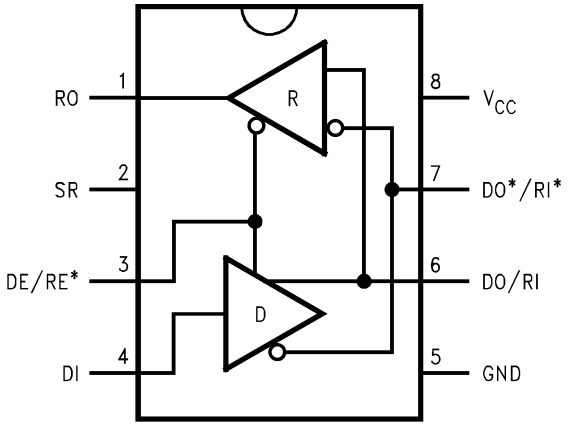


Figure 1. See Package Number D (R-PDSO-G8)

Truth Table(1)

DRIVER SECTION			
DE/RE*	**DI**	**DO/RI**	**DO*/RI***
H	H	H	L
H	L	L	H
L	X	Z	Z
RECEIVER SECTION			
DE/RE*	**RI-RI***		**RO**
L	≥+0.2V		H
L	≤−0.2V		L
H	X		Z
L	OPEN (1)		H

(1) Non-terminated, Open Inputs only

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})	+12V
Input Voltage (DE/RE*, & DI)	−0.5V to (V_{CC} +0.5V)
Common Mode (V_{CM})	
Driver Output/Receiver Input	±15V
Input Voltage (DO/RI, DO*/RI*)	±14V
Receiver Output Voltage	−0.5V to (V_{CC} +0.5V)
Maximum Package Power Dissipation @ +25°C	
M Package 1190 mV, derate	9.5 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	+260°C
(Soldering 4 sec.)	

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	**Typ**	**Max**	**Units**
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Bus Voltage	−7		+12	V
Operating Free Air Temperature (T_A)				
DS36C280T	−40	+25	+85	°C
DS36C280	0	+25	+70	°C

Electrical Characteristics[1][2]

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Reference		Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS									
V_{OD1}	Differential Output Voltage	I_O = 0 mA (No Load)		(422) (485)		1.5		5.0	V
V_{OD0}	Output Voltage	I_O = 0 mA				0		5.0	V
V_{OD0*}	Output Voltage	(Output to GND)				0		5.0	V
V_{OD2}	Differential Output Voltage (Termination Load)	R_L = 50Ω		(422)	Figure 2	2.0	2.8		V
		R_L = 27Ω		(485)		1.5	2.3	5.0	V
ΔV_{OD2}	Balance of V_{OD2}	R_L = 27Ω or 50Ω		[3]		−0.2	0.1	+0.2	V
	$\lvert V_{OD2} - V_{OD2*} \rvert$			(422, 485)					
V_{OD3}	Differential Output Voltage (Full Load)	R1 = 54Ω, R2 = 375Ω		*Figure 3*		1.5	2.0	5.0	V
		V_{TEST} = −7V to +12V							
V_{OC}	Driver Common Mode Output Voltage	R_L = 27Ω		(485)	*Figure 2*	0		3.0	V
		R_L = 50Ω		(422)		0		3.0	V
ΔV_{OC}	Balance of V_{OC}	R_L = 27Ω or		[3]		−0.2		+0.2	V
	$\lvert V_{OC} - V_{OC*} \rvert$	R_L = 50Ω		(422, 485)					
I_{OSD}	Driver Output Short-Circuit Current	V_O = +12V		(485)			200	+250	mA
		V_O = −7V		(485)			−190	−250	mA
RECEIVER CHARACTERISTICS									
V_{TH}	Differential Input High Threshold Voltage	$V_O = V_{OH}$, I_O = −0.4 mA		[4] (422, 485)			+0.035	+0.2	V
		−7V ≤ V_{CM} ≤ +12V							
V_{TL}	Differential Input Low Threshold Voltage	$V_O = V_{OL}$, I_O = 0.4 mA				−0.2	−0.035		V
		−7V ≤ V_{CM} ≤ +12V							
V_{HST}	Hysteresis[5]	V_{CM} = 0V					70		mV
R_{IN}	Input Resistance	−7V ≤ V_{CM} ≤ +12V		DS36C280T		24	68		kΩ
R_{IN}	Input Resistance	−7V ≤ V_{CM} ≤ +12V		DS36C280		48	68		kΩ
I_{IN}	Line Input Current [6]	Other Input = 0V	DS36C280	V_{IN} = +12V		0	0.19	0.25	mA
		DE = V_{IL}, RE* = V_{IL}		V_{IN} = −7V		0	−0.1	−0.2	mA
		V_{CC} = 4.75 to 5.25	DS36C280T	V_{IN} = +12V		0	0.19	0.5	mA
		or 0V		V_{IN} = −7V		0	−0.1	−0.4	mA
I_{ING}	Line Input Current Glitch [6]	Other Input = 0V	DS36C280	V_{IN} = +12V		0	0.19	0.25	mA
		DE = V_{IL}, RE* = V_{IL}		V_{IN} = −7V		0	−0.1	−0.2	mA
		V_{CC} = +3.0V	DS36C280T	V_{IN} = +12V		0	0.19	0.5	mA
		or 0V T_A = 25°C		V_{IN} = −7V		0	−0.1	−0.4	mA
I_B	Input Balance Test	RS = 500Ω		(422) [7]				±400	mV
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA, V_{ID} = +0.2V		RO *Figure 12*		3.5	4.6		V
V_{OL}	Low Level Output Voltage	I_{OL} = +4 mA, V_{ID} = −0.2V					0.3	0.5	V
I_{OSR}	Short Circuit Current	V_O = GND		RO		7	35	85	mA
I_{OZR}	TRI-STATE Leakage Current	V_O = 0.4V to 2.4V						±1	µA
DEVICE CHARACTERISTICS									

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD1} and V_{OD2}.
(2) All typicals are given for: V_{CC} = +5.0V, T_A = + 25°C.
(3) Delta $\lvert V_{OD2} \rvert$ and Delta $\lvert V_{OC} \rvert$ are changes in magnitude of V_{OD2} and V_{OC}, respectively, that occur when input changes state.
(4) Threshold parameter limits specified as an algebraic value rather than by magnitude.
(5) Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.
(6) I_{IN} includes the receiver input current and driver TRI-STATE leakage current.
(7) For complete details of test, see RS-485.

Electrical Characteristics[1][2] (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Reference	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			DE/RE*, DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{CC}$					2	µA
I_{IL}	Low Level Input Current	V_{CC} = 5.0V	V_{IL} = 0V				−2	µA
		V_{CC} = +3.0V					−2	µA
		SR = 0V		SR			−1	mA
I_{CCR}	Power Supply Current (No Load)	Driver OFF, Receiver ON		V_{CC}		200	500	µA
I_{CCD}		Driver ON, Receiver OFF				200	500	µA

Switching Characteristics[1][2][3]

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 54Ω, C_L = 100 pF	Figure 6, Figure 7	10	399	1000	ns
t_{PLHD}	Differential Propagation Delay Low to High			10	400	1000	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			0	1	10	ns
t_r	Rise Time	SR = Open			2870		ns
t_f	Fall Time				3070		ns
t_r	Rise Time	SR = 100 kΩ			1590		ns
t_f	Fall Time				1640		ns
t_r	Rise Time	SR = Short		100	337	1000	ns
t_f	Fall Time			100	348	1000	ns
t_{PHZ}	Disable Time High to Z	C_L = 15 pF	Figure 8, Figure 9		1100	2000	ns
t_{PLZ}	Disable Time Low to Z		Figure 10, Figure 11		500	800	ns
t_{PZH}	Enable Time Z to High	C_L = 100 pF	Figure 8, Figure 9		300	500	ns
t_{PZL}	Enable Time Z to Low		Figure 10, Figure 11		300	500	ns
RECEIVER CHARACTERISTICS							
t_{PHL}	Propagation Delay High to Low	C_L = 15 pF	Figure 13, Figure 14	30	210	400	ns
t_{PLH}	Propagation Delay Low to High			30	190	400	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$			0	20	50	ns
t_{PLZ}	Output Disable Time	C_L = 15 pF	Figure 15, Figure 16, Figure 17		50	150	ns
t_{PHZ}					55	150	ns
t_{PZL}	Output Enable Time				40	150	ns
t_{PZH}					45	150	ns

(1) All typicals are given for: V_{CC} = +5.0V, T_A = + 25°C.
(2) C_L includes probe and jig capacitance.
(3) SR = GND for all Switching Characteristics unless otherwise specified.

PARAMETER MEASUREMENT INFORMATION

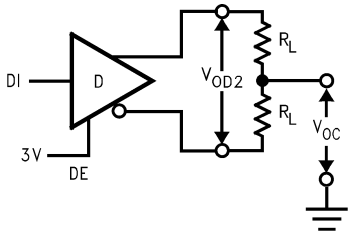


Figure 2. Driver V_{OD2} and V_{OC}

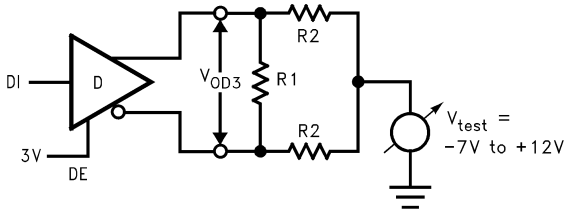


Figure 3. Driver V_{OD3}

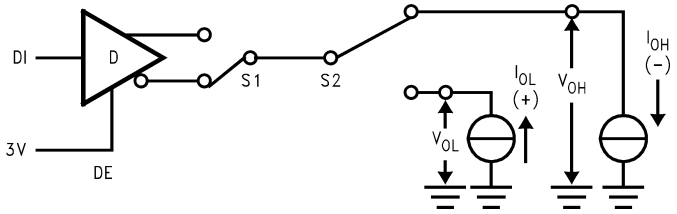
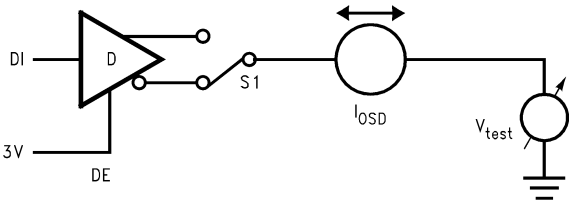


Figure 4. Driver V_{OH} and V_{OL}



Vtest = −7V to +12V

Figure 5. Driver I_{OSD}

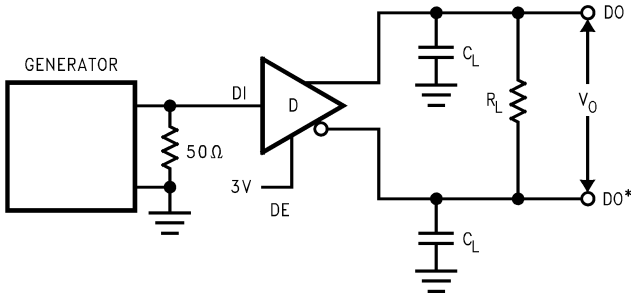


Figure 6. Driver Differential Propagation Delay Test Circuit

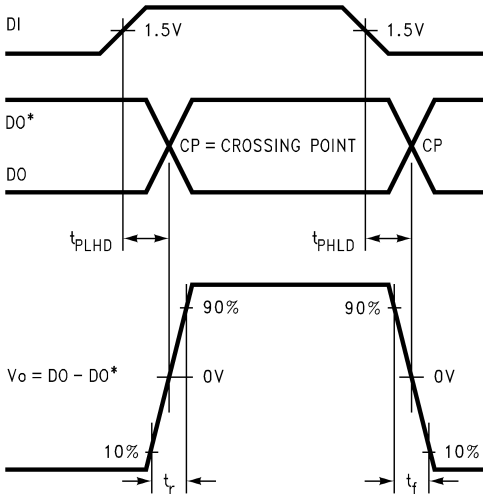


Figure 7. Driver Differential Propagation Delays and Differential Rise and Fall Times

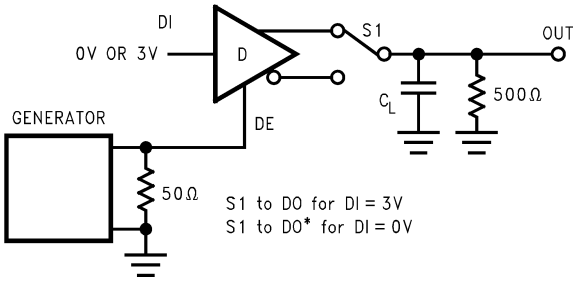


Figure 8. TRI-STATE Test Circuit (t_{PZH} , t_{PHZ})

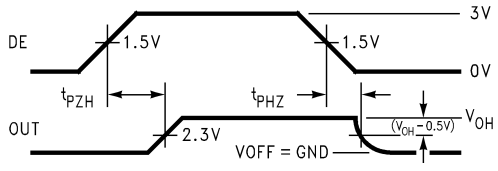


Figure 9. TRI-STATE Waveforms (t_{PZH}, t_{PHZ})

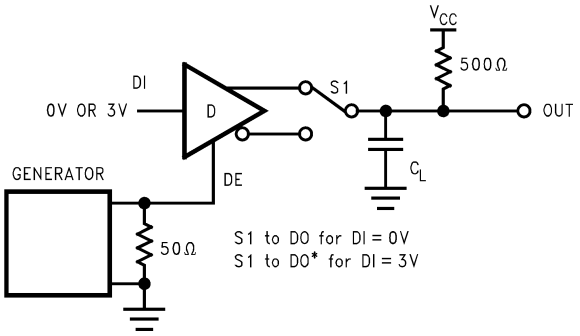


Figure 10. TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})

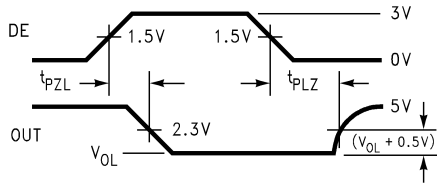


Figure 11. TRI-STATE Waveforms (t_{PZL}, t_{PLZ})

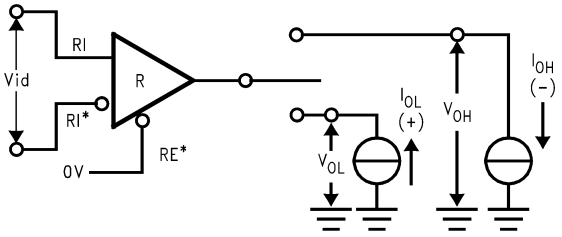


Figure 12. Receiver V_{OH} and V_{OL}

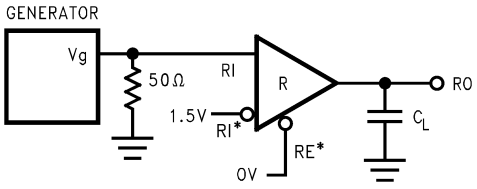


Figure 13. Receiver Differential Propagation Delay Test Circuit

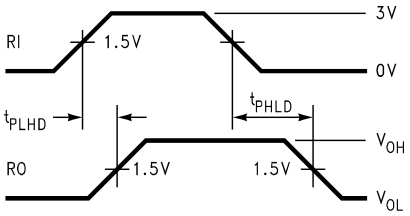


Figure 14. Receiver Differential Propagation Delay Waveforms

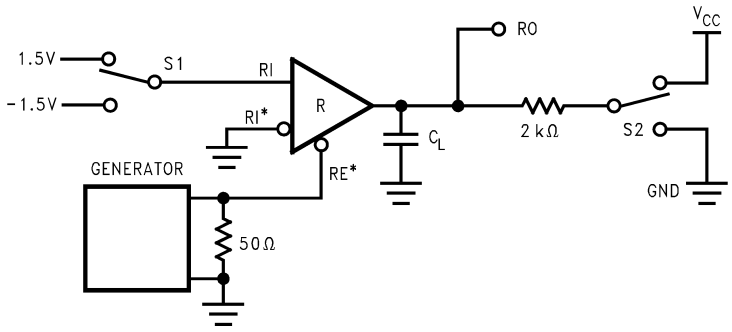


Figure 15. Receiver TRI-STATE Test Circuit

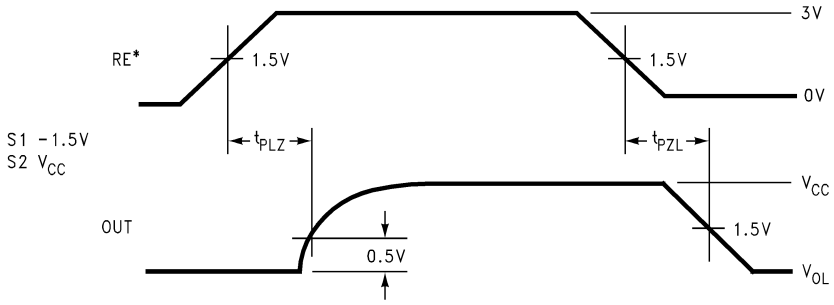


Figure 16. Receiver Enable and Disable Waveforms (t_{PLZ}, t_{PZL})

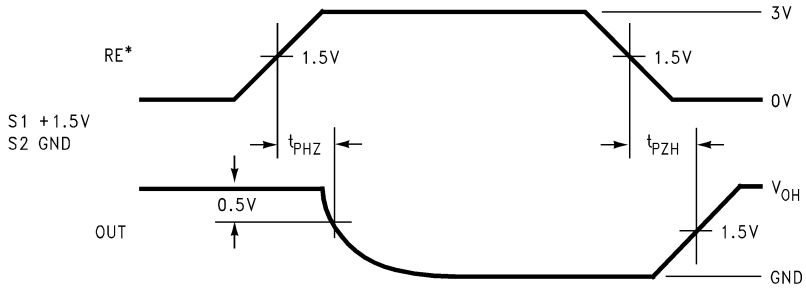


Figure 17. Receiver Enable and Disable Waveforms (t_{PHZ}, t_{PZH})

Typical Application Information

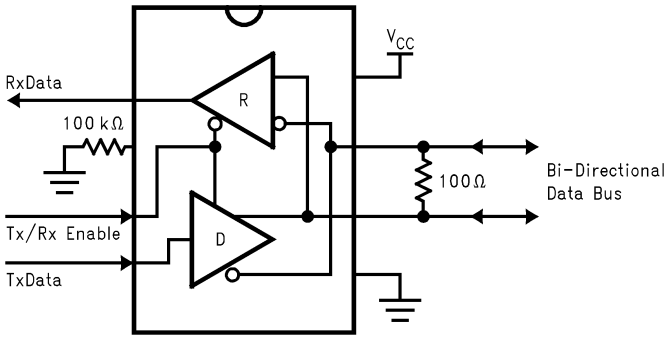


Figure 18. Typical Pin Connection

Table 1. DEVICE PIN DESCRIPTIONS

Pin #	Name	Description
1	RO	Receiver Output: When DE/RE* (Receiver Enable) is LOW, the receiver is enabled (ON), if DO/RI ≥ DO*/RI* by 200 mV, RO will be HIGH. If DO/RI ≤ DO*/RI* by 200 mV, RO will be LOW. Additionally RO will be HIGH for OPEN (Non-terminated) inputs.
2	SR	Slew Rate Control: A resistor connected to Ground controls the Driver Output rising and falling edge rates.
3	DE/RE*	Combined Driver and Receiver Output Enable: When signal is LOW the receiver output is enabled and the driver outputs are in TRI-STATE (OFF). When signal is HIGH, the receiver output is in TRI-STATE (OFF) and the driver outputs are enabled.
4	DI	Driver Input: When DE/RE* is HIGH, the driver is enabled, if DI is LOW, then DO/RI will be LOW and DO*/RI* will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO*/RI* is LOW.
5	GND	Ground Connection
6	DO/RI	Driver Output/Receiver Input, 485 Bus Pin.
7	DO*/RI*	Driver Output/Receiver Input, 485 Bus Pin.
8	V_{CC}	Positive Power Supply Connection: Recommended operating range for V_{CC} is +4.75V to +5.25V.

Unit Load

A unit load for a RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from −7V to +12V. The top border extending from −3V at 0 mA to +12V at +1 mA is defined as one unit load. Likewise, the bottom border extending from +5V at 0 mA to −7V at −0.8 mA is also defined as one unit load (see Figure 19). A RS-485 driver is capable of driving up to 32 unit loads. This allows upto 32 nodes on a single bus. Although sufficient for many applications, it is sometime desirable to have even more nodes. For example an aircraft that has 32 rows with 4 seats per row could benefit from having 128 nodes on one bus. This would allow signals to be transferred to and from each individual seat to 1 main station. Usually there is one or two less seats in the last row of the aircraft near the restrooms and food storage area. This frees the node for the main station.

The DS36C278, the DS36C279, and the DS36C280 all have ½ unit load and ¼ unit load (UL) options available. These devices will allow upto 64 nodes or 128 nodes guaranteed over temperature depending upon which option is selected. The ½ UL option is available in industrial temperature and the ¼ UL is available in commercial temperature.

First, for a ½ UL device the top and bottom borders shown in Figure 19 are scaled. Both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.5 mA for the top border and −7V at −0.4 mA for the bottom border (see Figure 19). Second, for a ¼ UL device the top and bottom borders shown in Figure 19 are scaled also. Again, both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.25 mA for the top border and −7V at −0.2 mA for the bottom border (see Figure 19).

The advantage of the ½ UL and ¼ UL devices is the increased number of nodes on one bus. In a single master multi-slave type of application were the number of slaves exceeds 32, the DS36C278/279/280 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.

The DS36C279 and DS36C280 have addition feature which offer more advantages. The DS36C279 has an automatic sleep mode function for power conscious applications. The DS36C280 has a slew rate control for EMI conscious applications. Refer to the sleep mode and slew rate control portion of the application information section in the corresponding datasheet for more information on these features.

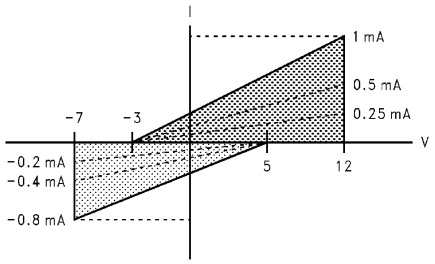


Figure 19. Input Current vs Input Voltage Operating Range

Slew Rate Control

The DS36C280 features an adjustable slew rate control. This feature allows more control over EMI levels than tradition fixed edge rate devices. The slew rate control may be adjusted with or without any external components. The DS36C280 offers both low power (I_{CC} 500 µA max) and low EMI for an RS-485 interface.

The slew rate control is located at pin two of the device and only controls the driver output edges. The slew rate control pin (SR) may be left open or shorted to ground, with or without a resistor. When the SR pin is shorted to ground without a resistor, the driver output edges will transition typically 350 ns. When the SR pin is left open, the driver output edges will transition typically 3 µs. When the SR pin is shorted to ground with a resistor, the driver output edges will transition between 350 ns and 3 µs depending on the resistor value. Refer to the slew rate versus resistor value curve in this datasheet for determining resistor values and expected typical slew rate value. Please note, when slowing the edge rates of the device will decrease the maximum data rate also.

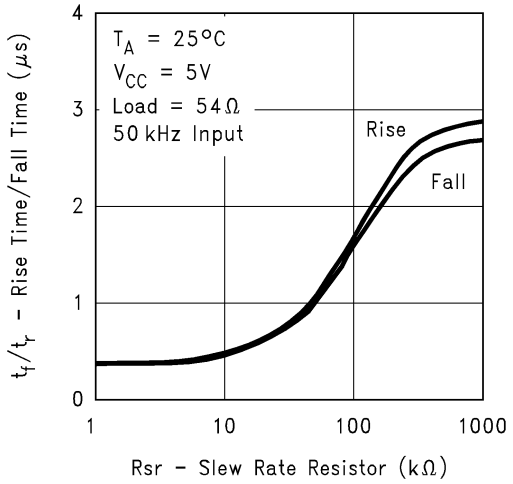


Figure 20. Slew Rate Resistor vs Differential Rise/Rise/Fall Time

REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS36C280M/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	36C28 0M	
DS36C280MX/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	36C28 0M	
DS36C280TM/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	36C28 0TM	
DS36C280TMX/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	36C28 0TM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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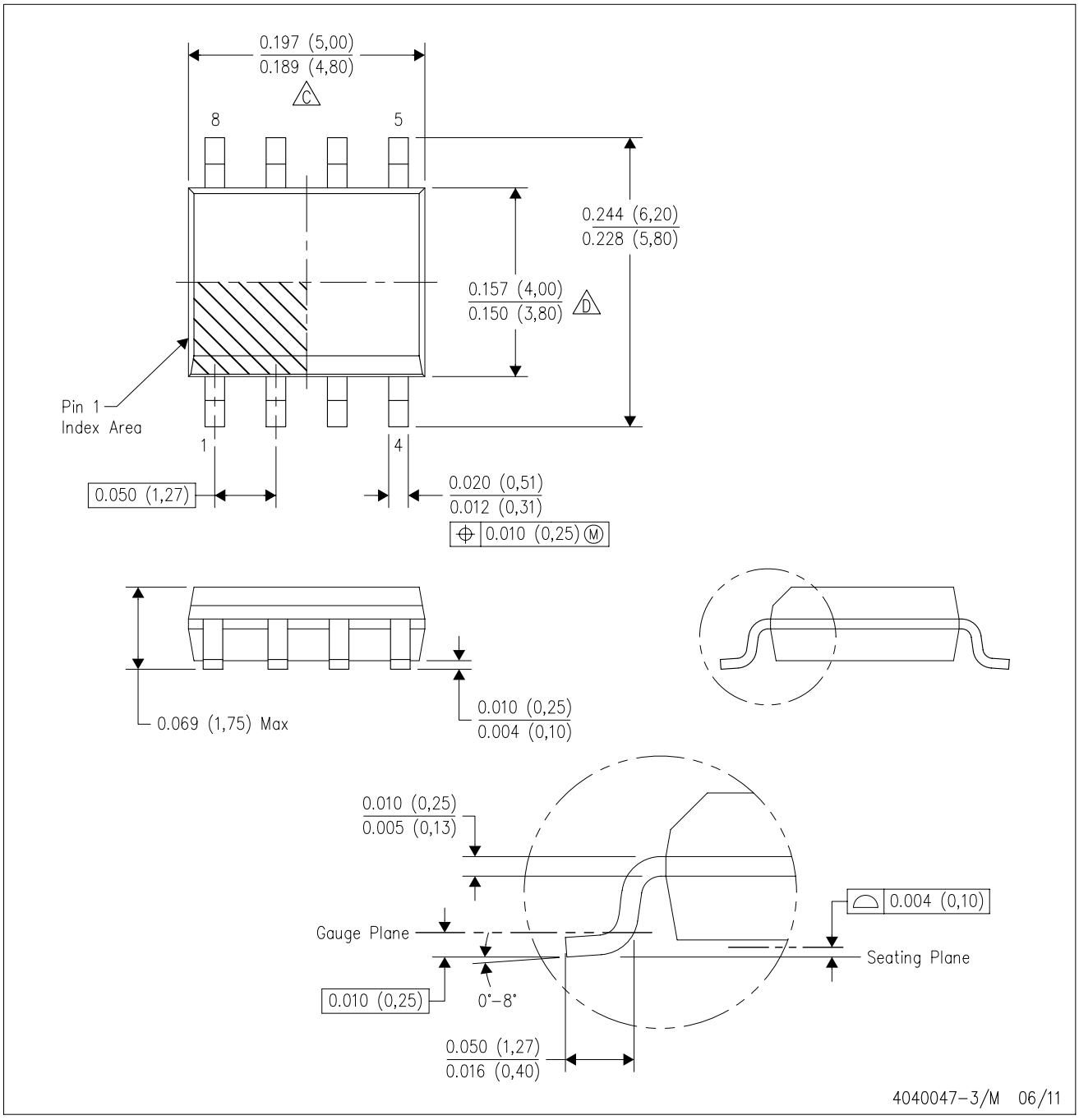
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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