LM4852 Boomer® Audio Power Amplifier Series Integrated Audio Amplifier System

Check for Samples: LM4852

FEATURES

- **1.1W (typ) Output Power with 8Ω Mono BTL Load**
- **60mW (typ) Output Power with Stereo 32Ω SE Loads**
- **I^2C Programmable 32 Step Digital Volume Control (-40.5dB to +6dB)**
- **Eight Distinct Output Modes**
- **DSBGA and WQFN Surface Mount Packaging**
- **"Click and Pop" Suppression Circuitry**
- **Thermal Shutdown Protection**
- **Low Shutdown Current (0.1uA, Typ)**

APPLICATIONS

- **Moblie Phones**
- **PDAs**

KEY SPECIFICATIONS

- **THD+N at 1kHz, 1.1W into 8Ω BTL, 1.0% (Typ)**
- **THD+N at 1kHz, 60mW into 32Ω SE, 0.5% (Typ)**
- **Single Supply Operation, 2.6 to 5.0V**

DESCRIPTION

The LM4852 is an audio power amplifier system capable of delivering 1.1W (typ) of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N and 60mW (typ) per channel of continuous average power into stereo 32Ω single-ended (SE) loads with 0.5% THD+N, using a 5V power supply.

The LM4852 features a 32 step digital volume control and eight distinct output modes. The digital volume control and output modes are programmed through a two-wire I^2C compatible control interface, that allows flexibility in routing and mixing audio channels. The LM4852 has 3 channels: one pair for a two-channel stereo signal and the third for a single-channel mono input.

The LM4852 is designed for cellular phone, PDA, and other portable handheld applications. It delivers high quality output power from a surface-mount package and requires only seven external components.

The industry leading DSBGA package only utilizes 2mm x 2.3mm of PCB space, making the LM4852 the most space efficient audio sub system available today.

Typical Application

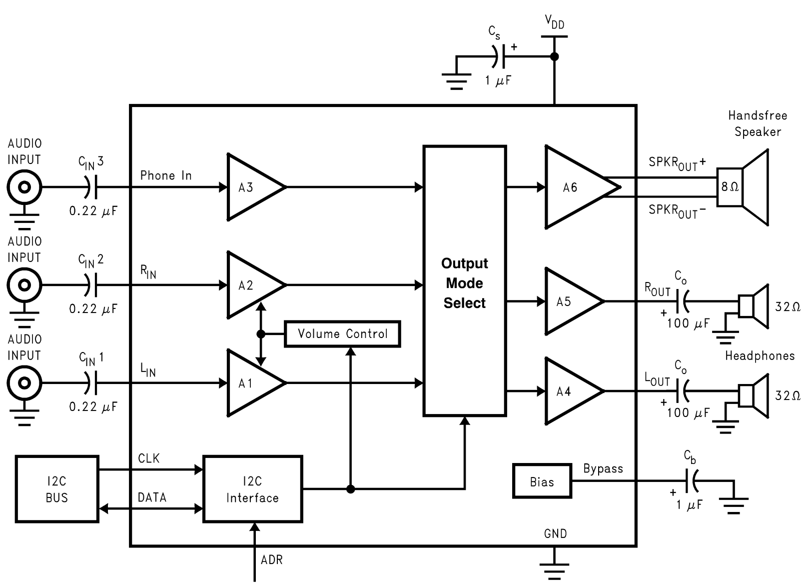

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

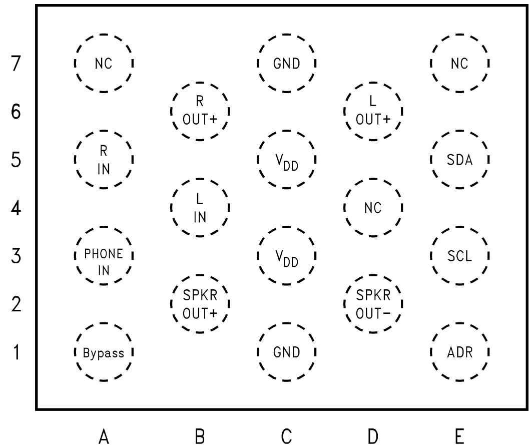

Figure 2. Top View (Bump-side down) See Package Number YZR0018

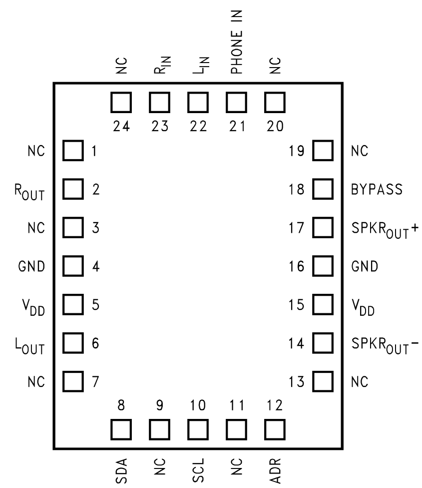

Figure 3. WQFN Package Top View See Package Number NHW0024B for WQFN

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
ESD Susceptibility[3]		2.0kV
ESD Machine model[4]		200V
Junction Temperature (T_J)		150°C
Vapor Phase (60 sec.)		215°C
Infrared (15 sec.)		220°C
Thermal Resistance	θ_{JA} (typ) - NHW0024B	42°C/W
	θ_{JC} (typ) - NHW0024B	3.0°C/W
	θ_{JA} (typ) - YZR0018	48°C/W[5]
	θ_{JC} (typ) - YZR0018	23°C/W[5]

(1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).
(5) The given θ_{JA} and θ_{JC} are for an LM4852 mounted on a demonstration board with a 4in^2 area of 1oz printed circuit board copper ground plane.

Operating Ratings[1]

Temperature Range	−40°C to 85°C
Supply Voltage V_{DD}	$2.6V \le V_{DD} \le 5.5V$

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics 5.0 V[(1)(2)]

The following specifications apply for V_{DD}= 5.0V, T_A= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4852		Units (Limits)
			Typical[(3)]	Limits[(4)(5)]	
I_{DD}	Supply Current	Output modes 2, 4, 6 V_{IN} = 0V; No loads	5	9	mA (max)
		Output modes 2, 4, 6 V_{IN} = 0V; Loaded (Figure 1)	6	10	mA (max)
		Output modes 1, 3, 5, 7 V_{IN} = 0V; No loads	7.5	11	mA (max)
		Output modes 1, 3, 5, 7 V_{IN} = 0V; Loaded (Figure 1)	8.5	12	mA (max)
I_{SD}	Shutdown Current	Output mode 0	0.1	2.0	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5.0	40	mV (max)
P_O	Output Power	$SPKR_{OUT}$; R_L = 4Ω THD+N = 1%; f = 1kHz, LM4852LQ	1.5		W
		$SPKR_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz	1.1	0.8	W (min)
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 0.5%; f = 1kHz	60	45	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	$SPKR_{OUT}$ f = 20Hz to 20kHz P_{OUT} = 400mW; R_L = 8Ω	0.5		%
		R_{OUT} and L_{OUT} f = 20Hz to 20kHz P_{OUT} = 15mW; R_L = 32Ω	0.5		%
N_{OUT}	Output Noise	A-weighted[(6)]	26		µV
PSRR	Power Supply Rejection Ratio $SPKR_{OUT}$	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 1.0µF All audio inputs terminated into 50Ω; Output referred Gain (BTL) = 6dB			
		Output Mode 1,7	64	57	dB (min)
		Output Mode 3	58		dB
		Output Mode 5	55		dB
	Power Supply Rejection Ratio $R_{OUT}$and L_{OUT}	V_{RIPPLE} = 200mV_{PP}; f = 217Hz C_B = 1.0µF All audio inputs terminated into 50Ω; Output referred Maximum gain setting			
		Output Mode 2	68	59	dB (min)
		Output Mode 4	60	54	dB (min)
		Output Mode 6, 7	56	51	dB (min)
V_{IH}	Logic High Input Voltage			0.7 x V_{DD} V_{DD}	V (min) V (max)
V_{IL}	Logic Low Input Voltage			0.4 GND	V (max) V (min)

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are ensured to Texas Instruments AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specifications are ensured by design, test, or statistical analysis.
(6) Please refer to the Output Noise vs Output Mode table in the Typical Performance Characteristics section for more details.

Electrical Characteristics 5.0 V(1)(2) (continued)

The following specifications apply for V_{DD}= 5.0V, T_A= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4852		Units (Limits)
			Typical (3)	Limits (4) (5)	
	Digital Volume Range (R_{IN} and L_{IN})	Input referred minimum gain	-40.5	-41.1 -39.9	dB (min) dB (max)
		Input referred maximum gain	6.0	5.4 6.6	dB (min) dB (max)
	Digital Volume Stepsize		1.5		dB
	Digital Volume Stepsize Error		±0.1	±0.6	dB (max)
	Phone In Volume	BTL gain from Phone In to $SPKR_{OUT}$	6	5.4 6.6	dB (min) dB (max)
	Mute Attenuation	Output Mode 1, 3, 5	100		dB
	Phone In Input Impedance		20	15 25	kΩ (min) kΩ (max)
	R_{IN} and L_{IN} Input Impedance	Maximum gain setting	30	22.5 37.5	kΩ (min) kΩ (max)
		Mininum gain setting	100	75 125	kΩ (min) kΩ (max)
T_{SD}	Thermal Shutdown Temperature		170	150	°C (min)
t_1	SCL (Clock) Period			2.5	µs (min)
t_2	SDA to SCL Set-up Time			100	ns (min)
t_3	Data Out Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)

Electrical Characteristics 3.0V(1)(2)

The following specifications apply for V_{DD}= 3.0V, T_A= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4852		Units (Limits)
			Typical(3)	Limits(4)(5)	
I_{DD}	Supply Current	Output modes 2, 4, 6 V_{IN} = 0V; No loads	4	7	mA (max)
		Output modes 2, 4, 6 V_{IN} = 0V; Loaded (Figure 1)	5	8	mA (max)
		Output modes 1, 3, 5, 7 V_{IN} = 0V; No loads	6.5	10	mA (max)
		Output modes 1, 3, 5, 7 V_{IN} = 0V; Loaded (Figure 1)	7	11	mA (max)
I_{SD}	Shutdown Current	Output mode 0	0.1	2.0	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5.0	40	mV (max)
P_O	Output Power	$SPKR_{OUT}$; R_L = 4Ω THD+N = 1%; f = 1kHz, LM4852LQ	430		mW
		$SPKR_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz	340	300	mW (min)
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 0.5%; f = 1kHz	22	18	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	$SPKR_{OUT}$ f = 20Hz to 20kHz P_{OUT} = 150mW; R_L = 8Ω	0.5		%
		R_{OUT} and L_{OUT} f = 20Hz to 20kHz P_{OUT} = 10mW; R_L = 32Ω	0.5		%
N_{OUT}	Output Noise	A-weighted(6)	26		µV
PSRR	Power Supply Rejection Ratio $SPKR_{OUT}$	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 1.0µF All audio inputs terminated into 50Ω; Output referred Gain (BTL) = 6dB			
		Output Mode 1, 7	64	57	dB (min)
		Output Mode 3	58		dB
		Output Mode 5	55		dB
	Power Supply Rejection Ratio $R_{OUT}$and L_{OUT}	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 1.0µF All audio inputs terminated into 50Ω; Output referred Maximum gain setting			
		Output Mode 2	68	60	dB (min)
		Output Mode 4	60	55	dB (min)
		Output Mode 6, 7	56	52	dB (min)
V_{IH}	Logic High Input Voltage			0.7 x V_{DD} V_{DD}	V (min) V (max)
V_{IL}	Logic Low Input Voltage			0.4 GND	V (max) V (min)

(1) Absolute Maximum Rating indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are ensured to Texas Instruments AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specifications are ensured by design, test, or statistical analysis.
(6) Please refer to the Output Noise vs Output Mode table in the Typical Performance Characteristics section for more details.

Electrical Characteristics 3.0V(1)(2) (continued)

The following specifications apply for V_{DD}= 3.0V, T_A= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4852		Units (Limits)
			Typical (3)	Limits (4) (5)	
	Digital Volume Range (R_{IN} and L_{IN})	Input referred minimum gain	-40.5	-41.1 -39.9	dB (min) dB (max)
		Input referred maximum gain	6.0	5.4 6.6	dB (min) dB (max)
	Digital Volume Stepsize		1.5		dB
	Digital Volume Stepsize Error		±0.1	±0.6	dB (max)
	Phone In Volume	BTL gain from Phone In to $SPKR_{OUT}$	6	5.4 6.6	dB (min) dB (max)
	Mute Attenuation	Output Mode 1, 3, 5	100		dB
	Phone In Input Impedance		20	15 25	kΩ (min) kΩ (max)
	R_{IN} and L_{IN} Input Impedance	Maximum gain setting	30	22.5 37.5	kΩ (min) kΩ (max)
		Mininum gain setting	100	75 125	kΩ (min) kΩ (max)
T_{SD}	Thermal Shutdown Temperature		170	150	°C (min)
t_1	SCL (Clock) Period			2.5	µs (min)
t_2	SDA to SCL Set-up Time			100	ns (min)
t_3	Data Out Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)

External Components Description

Components		Functional Description
1.	C_{IN}	This is the input coupling capacitor. It blocks the DC voltage and couples the input signal to the amplifier's input terminals. C_{IN} also creates a highpass filter with the internal resistor R_i (Input Impedance) at $f_c = 1/(2\pi R_i C_{IN})$.
2.	C_S	This is the supply bypass capacitor. It filters the supply voltage applied to the V_{DD} pin and helps maintain the LM4852's PSRR.
3.	C_B	This is the BYPASS pin capacitor. It filters the V_{DD} / 2 voltage and helps maintain the LM4852's PSRR.

Typical Performance Characteristics

THD+N vs Frequency LM4852LQ

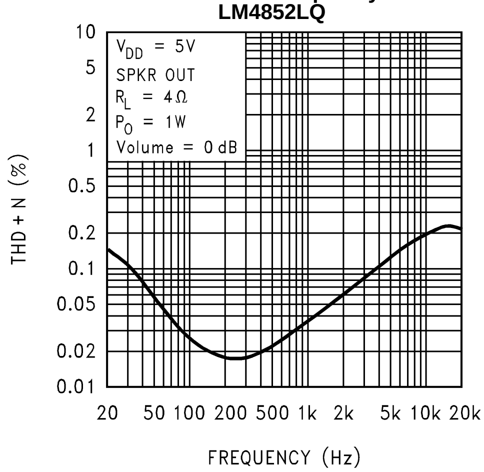

Figure 4.

THD+N vs Frequency LM4852LQ

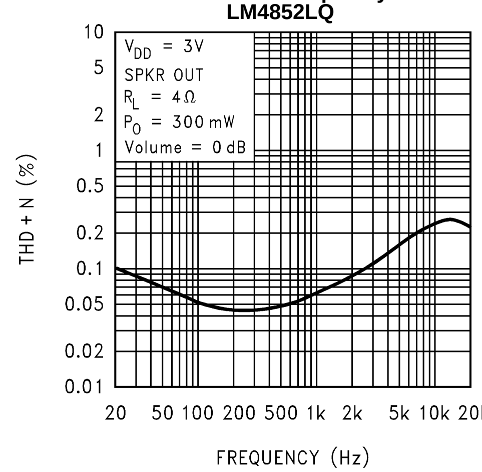

Figure 5.

THD+N vs Frequency

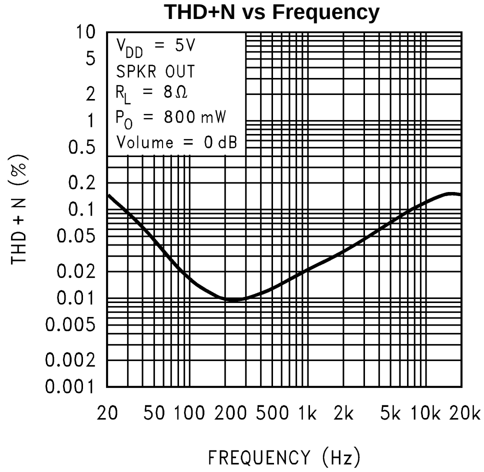

Figure 6.

THD+N vs Frequency

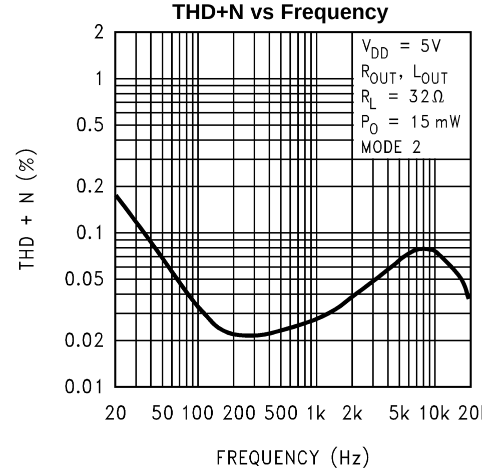

Figure 7.

THD+N vs Frequency

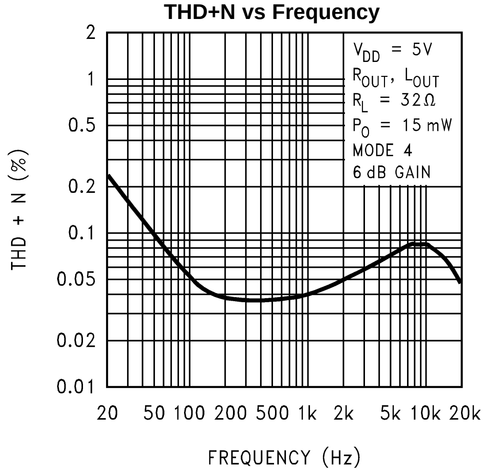

Figure 8.

THD+N vs Frequency

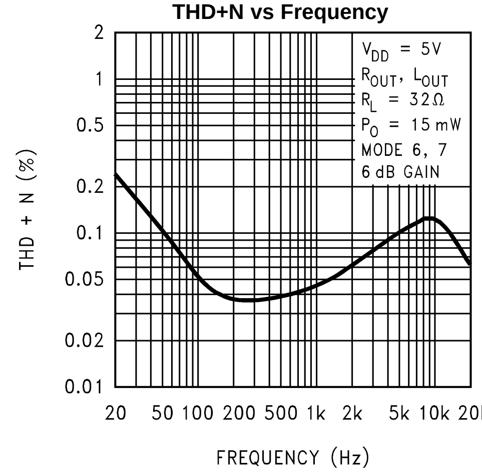

Figure 9.

Typical Performance Characteristics (continued)

THD+N vs Frequency

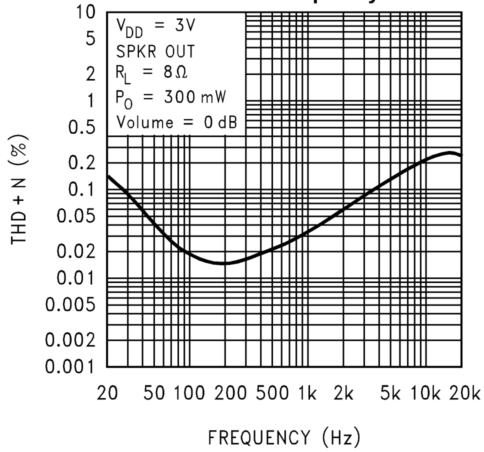

Figure 10.

THD+N vs Frequency

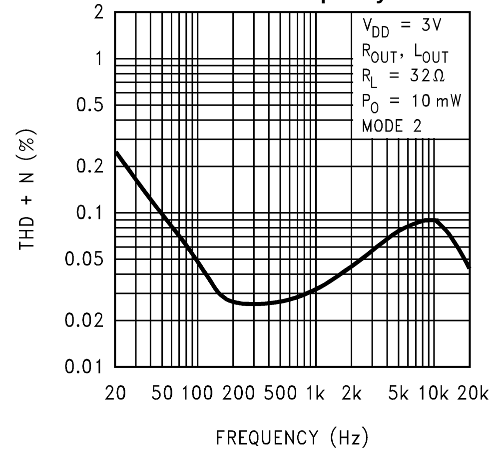

Figure 11.

THD+N vs Frequency

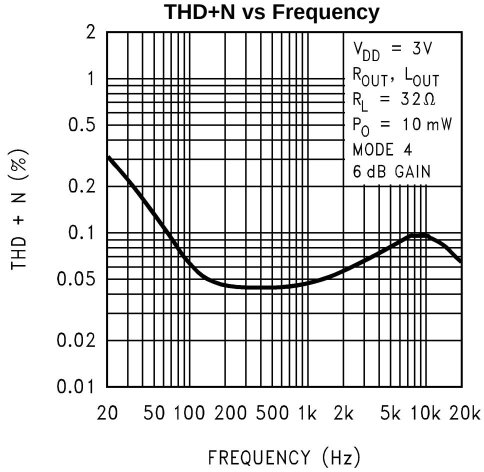

Figure 12.

THD+N vs Frequency

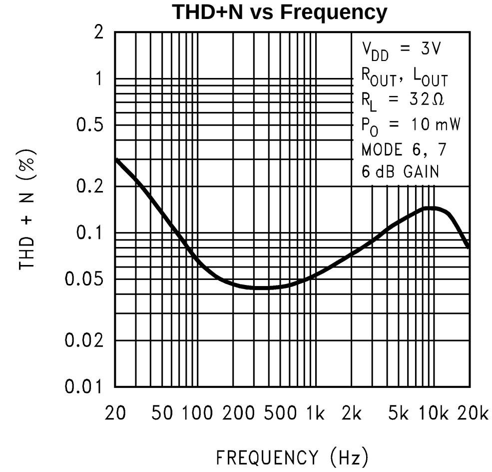

Figure 13.

THD+N vs Output Power LM4852LQ

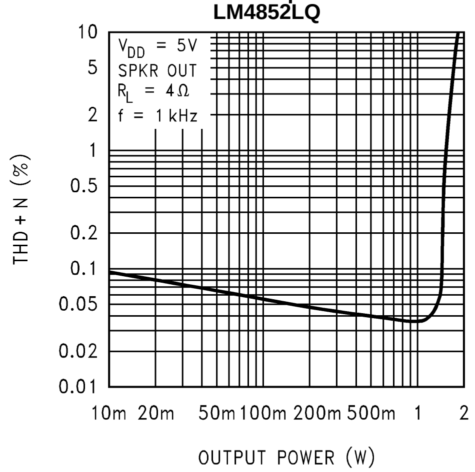

Figure 14.

THD+N vs Output Power LM4852LQ

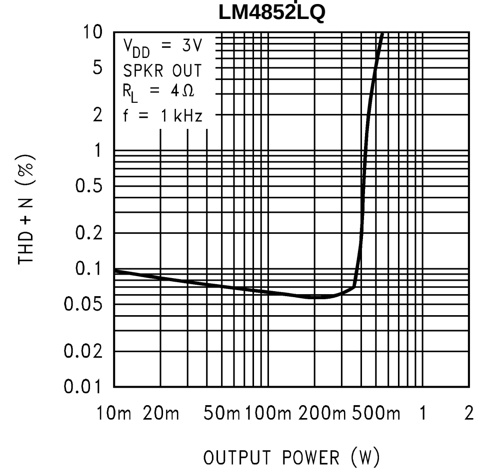

Figure 15.

Typical Performance Characteristics (continued)

THD+N vs Output Power

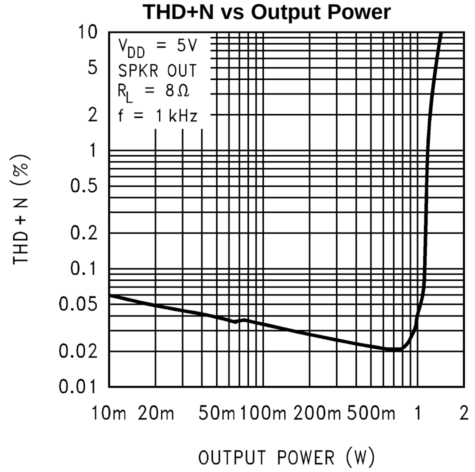

Figure 16.

THD+N vs Output Power

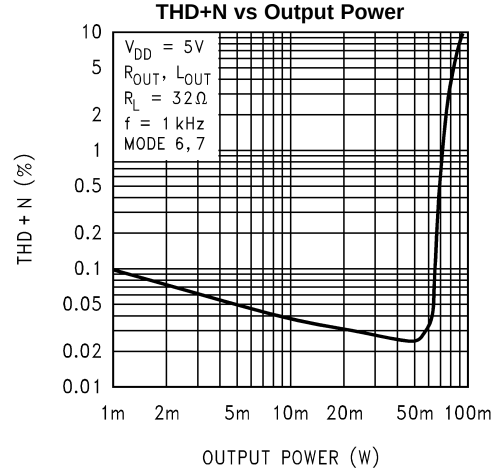

Figure 17.

THD+N vs Output Power

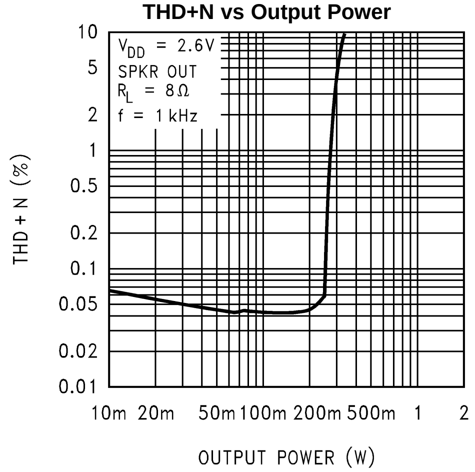

Figure 18.

THD+N vs Output Power

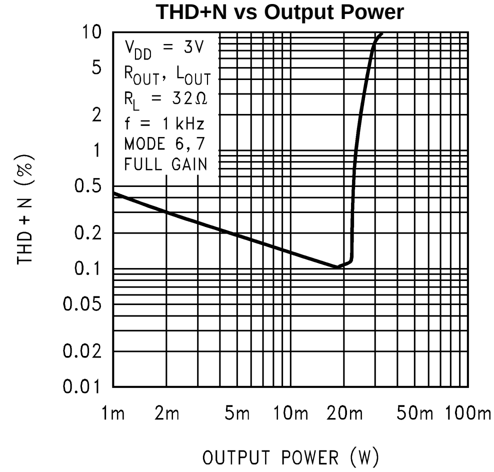

Figure 19.

Power Supply Rejection Ratio

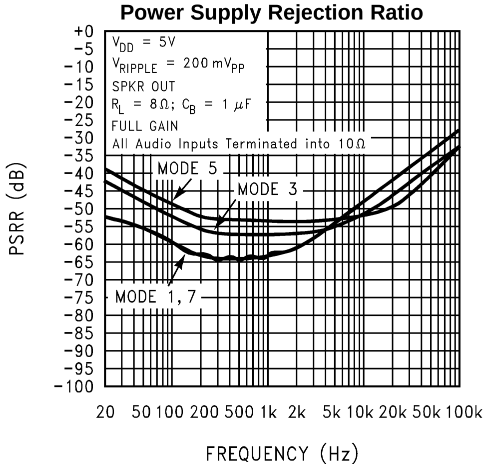

Figure 20.

Power Supply Rejection Ratio

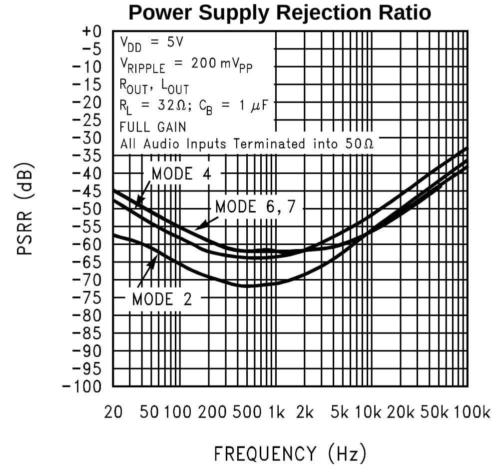

Figure 21.

Typical Performance Characteristics (continued)

Power Supply Rejection Ratio

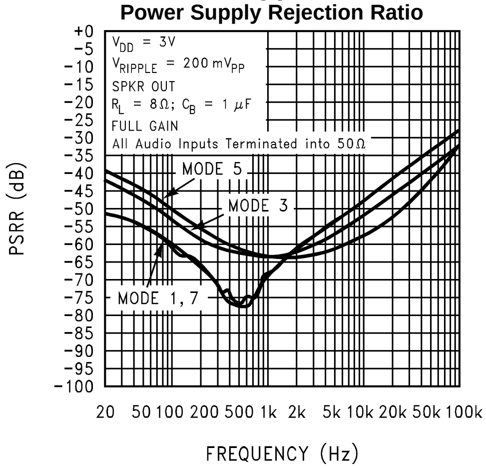

Figure 22.

Power Supply Rejection Ratio

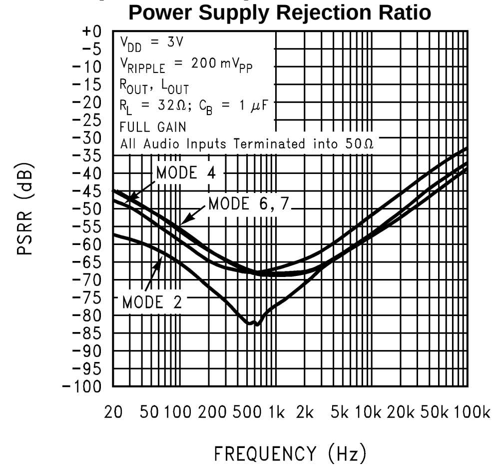

Figure 23.

Power Supply Rejection Ratio

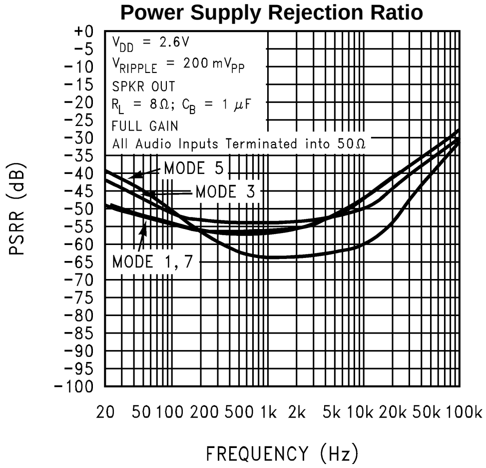

Figure 24.

Power Supply Rejection Ratio

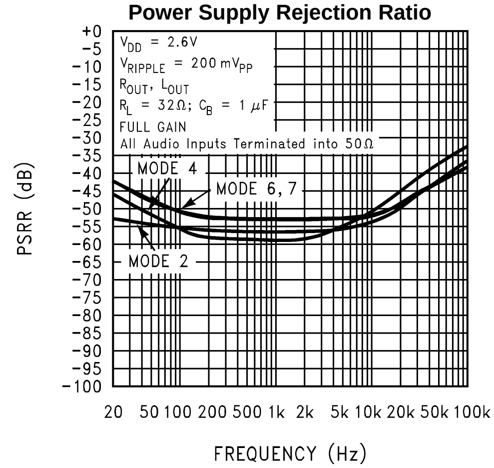

Figure 25.

Output Power vs Supply Voltage

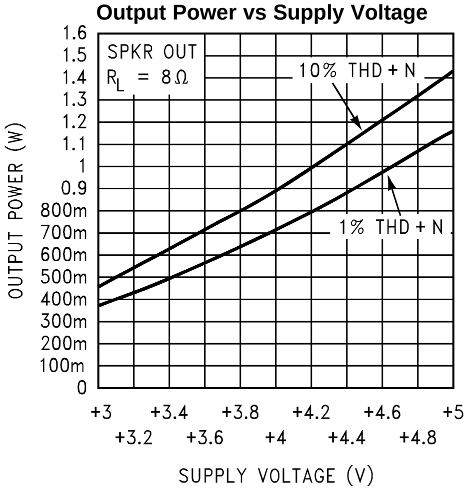

Figure 26.

Output Power vs Supply Voltage

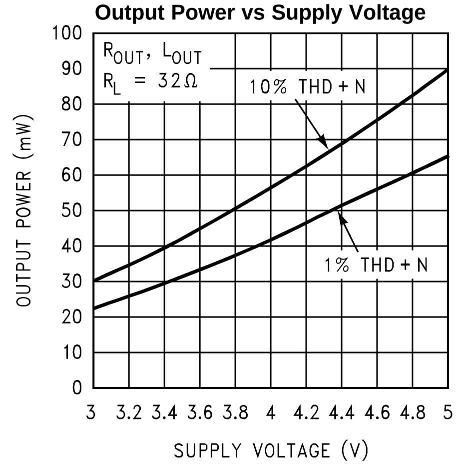

Figure 27.

Typical Performance Characteristics (continued)

Output Power vs Load Resistance

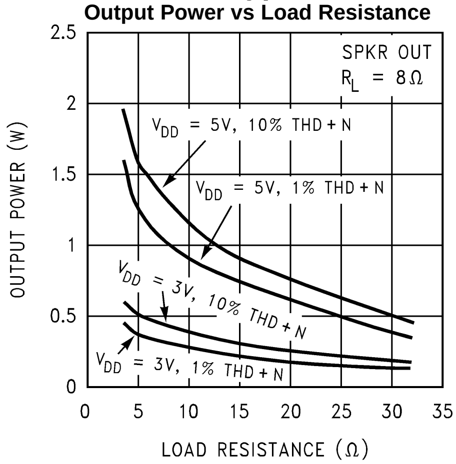

Figure 28.

Output Power vs Load Resistance

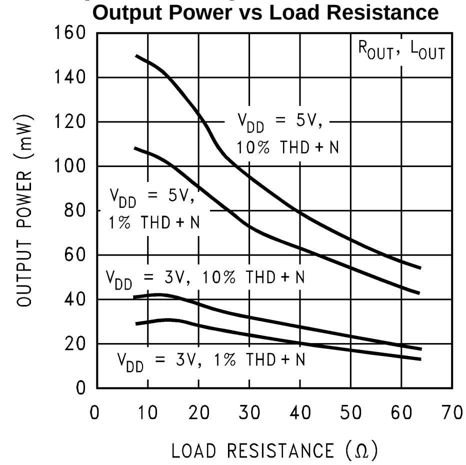

Figure 29.

Power Dissipation vs Output Power

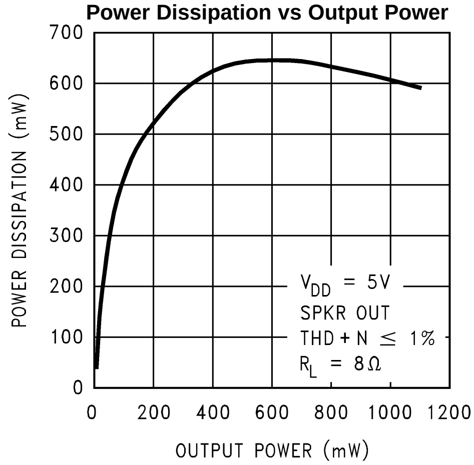

Figure 30.

Power Dissipation vs Output Power

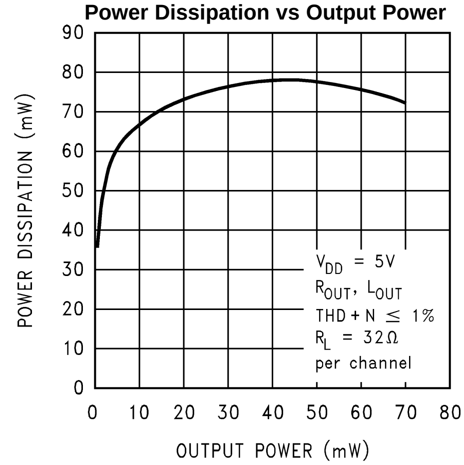

Figure 31.

Supply Current vs Supply Voltage

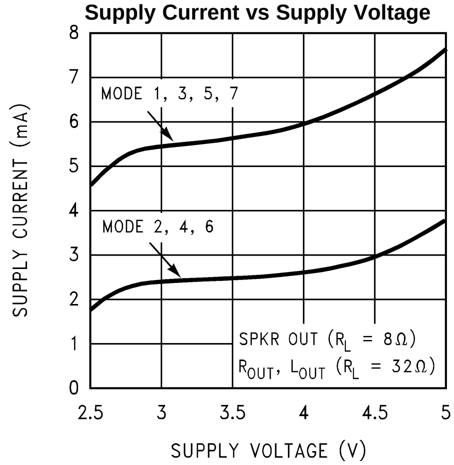

Figure 32.

Channel Separation

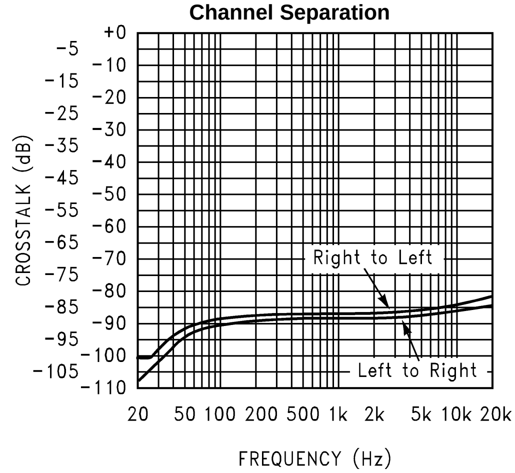

Figure 33.

Typical Performance Characteristics (continued)

Frequency Response

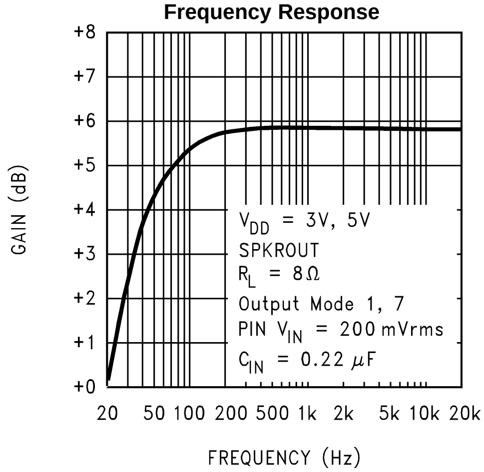

Figure 34.

Frequency Response

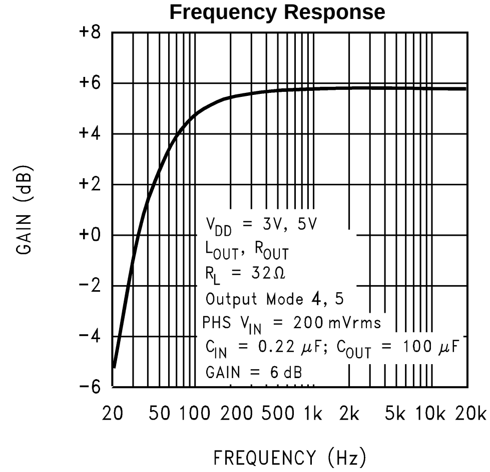

Figure 35.

Table 1. Output Noise vs Output Mode (V_{DD} = 3V, 5V)(1)

Output Mode	SPKROUT Output Noise (μV)	LOUT/ROUT Output Noise (μV)
1	26	X
2	X	15 (G = 6dB)
3	30	15 (G = 6dB)
4	X	20 (G = 6dB)
5	40	20 (G = 6dB)
6	X	25 (G = 6dB)
7	26	25 (G = 6dB)

(1) G = LIN / RIN gain setting
A - weighted filter used

APPLICATION INFORMATION

I²C PIN DESCRIPTION

SDA: This is the serial data input pin.

SCL: This is the clock input pin.

ADR: This is the address select input pin.

I²C INTERFACE

The LM4852 uses a serial bus, which conforms to the I²C protocol, to control the chip's functions with two wires: clock and data. The clock line is uni-directional. The data line is bi-directional (open-collector) with a pullup resistor (typically 10kΩ).The maximum clock frequency specified by the I²C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4852.

The I²C address for the LM4852 is determined using the ADR pin. The LM4852's two possible I²C chip addresses are of the form 110110$X_1$0 (binary), where the X_1 = 0, if ADR is logic low; and X_1 = 1, if ADR is logic high. If the I²C interface is used to address a number of chips in a system and the LM4852's chip address can be changed to avoid address conflicts.

The timing diagram for the I²C is shown in Figure 36. The data is latched in on the stable high level of the clock and the data line should be held high when not in use. The timing diagram is broken up into six major sections:

The “start” signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the clock level is high.

After the last bit of the address is sent, the master checks for the LM4852's acknowledge. The master releases the data line high (through a pullup resistor). Then the master sends a clock pulse. If the LM4852 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not low, then the master should send a “stop” signal (discussed later) and abort the transfer.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must generate another acknowledge to see if the LM4852 received the data.

If the master has more data bytes to send to the LM4852, then the master can repeat the previous two steps until all data bytes have been sent.

The “stop” signal ends the transfer. To signal “stop”, the data signal goes high while the clock signal is high.

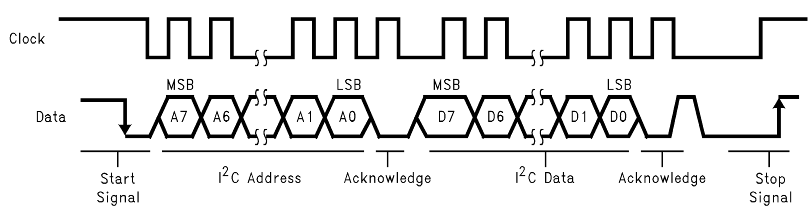

Figure 36. I²C Bus Format

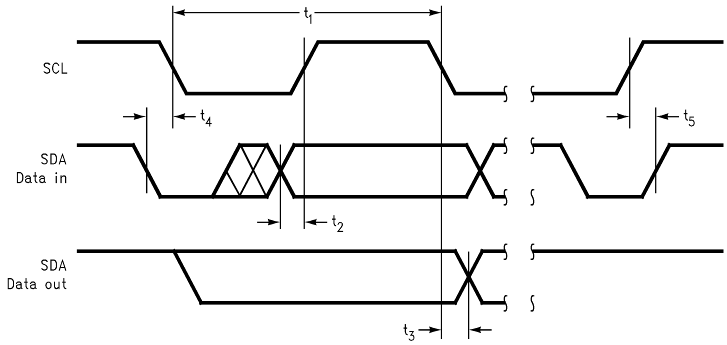

Figure 37. I²C Timing Diagram

Table 2. Data Register

	DATA							
BIT	D7	D6	D5	D4	D3	D2	D1	D0
Function	Volume Control					Output Mode Control		
Name	V4	V3	V2	V1	V0	M2	M1	M0
Default	0	0	0	0	0	0	0	0

Table 3. Output Mode Selection(1)

M2	M1	M0	Handsfree Speaker Output	Right Headphone Output	Left Headphone Output	Output Mode Number
0	0	0	SD	SD	SD	0
0	0	1	6dB x P	MUTE	MUTE	1
0	1	0	SD	P	P	2
0	1	1	G (R+L)	MUTE	MUTE	3
1	0	0	SD	G x R	Gx L	4
1	0	1	G (R+L) + 6dB x P	MUTE	MUTE	5
1	1	0	SD	(GxR) + P	(G x L) + P	6
1	1	1	6dB x P	(GxR) + P	(G x L) + P	7

(1) P = Phone In
R = R_{IN}
L = L_{IN}
SD = Shutdown
MUTE = Mute Mode
G = L_{IN} and R_{IN} gain setting

Table 4. Volume Control

V4	V3	V2	V1	V0	Gain (dB)
					G
0	0	0	0	0	-40.5
0	0	0	0	1	-39.0
0	0	0	1	0	-37.5
0	0	0	1	1	-36.0
0	0	1	0	0	-34.5
0	0	1	0	1	-33.0
0	0	1	1	0	-31.5
0	0	1	1	1	-30.0
0	1	0	0	0	-28.5
0	1	0	0	1	-27.0
0	1	0	1	0	-25.5
0	1	0	1	1	-24.0
0	1	1	0	0	-22.5
0	1	1	0	1	-21.0
0	1	1	1	0	-19.5
0	1	1	1	1	-18.0
1	0	0	0	0	-16.5
1	0	0	0	1	-15.0
1	0	0	1	0	-13.5
1	0	0	1	1	-12.0
1	0	1	0	0	-10.5
1	0	1	0	1	-9.0
1	0	1	1	0	-7.5
1	0	1	1	1	-6.0
1	1	0	0	0	-4.5
1	1	0	0	1	-3.0
1	1	0	1	0	-1.5
1	1	0	1	1	0.0
1	1	1	0	0	1.5
1	1	1	0	1	3.0
1	1	1	1	0	4.5
1	1	1	1	1	6.0

EXPOSED-DAP MOUNTING CONSIDERATIONS

The LM4852's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper area heatsink, copper traces, ground plane, and finally, surrounding air. The result is a low voltage audio power amplifier that produces 1.1W dissipation in a 8Ω load at ≤ 1% THD+N. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4852's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The LD package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is then, ideally, connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided or multi-layer PCB. (The heat sink area can also be placed on an inner layer of a multi-layer board. The thermal resistance, however, will be higher.) Connect the DAP copper pad to the inner layer or backside copper heat sink area with 6 (3 X 2) (LD) vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plugging and tenting the vias with plating and solder mask, respectively.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4852 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. In all circumstances and under all conditions, the junction temperature must be held below 150°C to prevent activating the LM4852's thermal shutdown protection. Further detailed and specific information concerning PCB layout and fabrication and mounting an LD (WQFN) is found in Texas Instruments AN1187 (SNOA401).

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 1.7W to 1.6W. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4852 consists of three pairs of output amplifier blocks (A4-A6). Amplifier block A6 consists of a bridged-tied amplifier pair that drives SPKROUT. The LM4852 drives a load, such as a speaker, connected between outputs, SPKROUT+ and SPKROUT-. In the amplifier block A6, the output of the amplifier that drives SPKROUT- serves as the input to the unity gain inverting amplifier that drives SPKROUT+.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between SPKROUT- and SPKROUT+ and driven differentially (commonly referred to as 'bridge mode'). This results in a differential or BTL gain of:

$$A_{VD} = 2(R_f / R_i) = 2 \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing SPKROUT- and SPKROUT+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM4852 has a pair of bridged-tied amplifiers driving a handsfree speaker, SPKROUT. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation 2, assuming a 5V power supply and an 8Ω load, the maximum SPKROUT power dissipation is 634mW.

$$P_{DMAX\text{-}SPKROUT} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridge Mode} \quad (2)$$

The LM4852 also has a pair of single-ended amplifiers driving stereo headphones, ROUT and LOUT. The maximum internal power dissipation for ROUT and LOUT is given by Equation 3 and Equation 4. From Equation 3 and Equation 4, assuming a 5V power supply and a 32Ω load, the maximum power dissipation for LOUT and ROUT is 40mW, or 80mW total.

$$P_{DMAX\text{-}LOUT} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (3)$$

$$P_{DMAX\text{-}ROUT} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (4)$$

The maximum internal power dissipation of the LM4852 occurs when all 3 amplifiers pairs are simultaneously on; and is given by Equation 5.

$$P_{DMAX\text{-}TOTAL} = P_{DMAX\text{-}SPKROUT} + P_{DMAX\text{-}LOUT} + P_{DMAX\text{-}ROUT} \quad (5)$$

The maximum power dissipation point given by Equation 5 must not exceed the power dissipation given by Equation 6:

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \quad (6)$$

The LM4852's T_{JMAX} = 150°C. In the ITL package, the LM4852's θ_{JA} is 48°C/W. In the LD package soldered to a DAP pad that expands to a copper area of 2.5in^2 on a PCB, the LM4852's θ_{JA} is 42°C/W. At any given ambient temperature T_A, use Equation 6 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 6 and substituting $P_{DMAX\text{-}TOTAL}$ for P_{DMAX}' results in Equation 7. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4852's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX\text{-}TOTAL}\, \theta_{JA} \quad (7)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 104°C for the IBL package.

$$T_{JMAX} = P_{DMAX\text{-}TOTAL}\, \theta_{JA} + T_A \quad (8)$$

Equation 8 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4852's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation 5 is greater than that of Equation 6, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4852's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4852's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, Proper Selection of External Components), system cost, and size constraints.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 37). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor (R_i) and the input capacitor (C_i) produce a high pass filter cutoff frequency that is found using Equation 9.

$$f_c = 1 / (2\pi R_i C_i) \quad (9)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation 9 is 0.063µF. The 0.22µF C_i shown in Figure 1 allows the LM4852 to drive high efficiency, full range speaker whose response extends below 40Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4852 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4852's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. C_B's value should be in the range of 5 times to 7 times the value of C_i. This ensures that output transients are eliminated when power is first applied or the LM4852 resumes operation after shutdown.

Demonstration ITL Board Layout

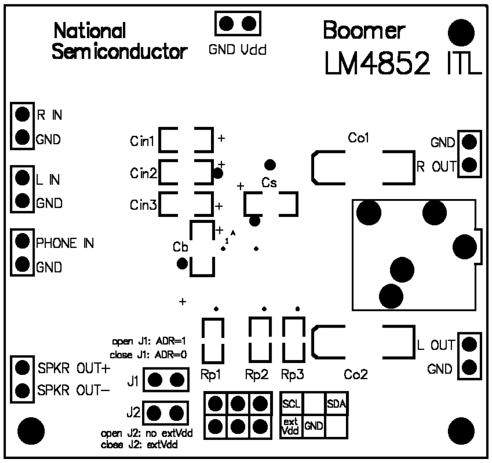

Figure 38. Recommended ITL PC Board Layout: Top Overlay Layer

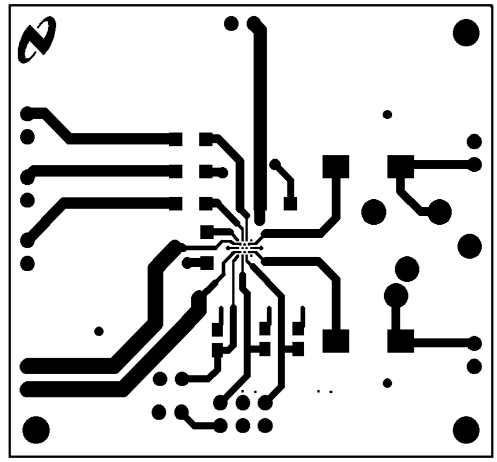

Figure 39. Recommended ITL PC Board Layout: Top Layer

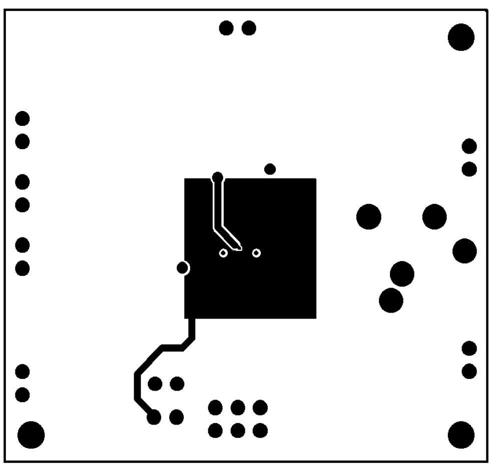

Figure 40. Recommended ITL PC Board Layout: Middle 1 Layer

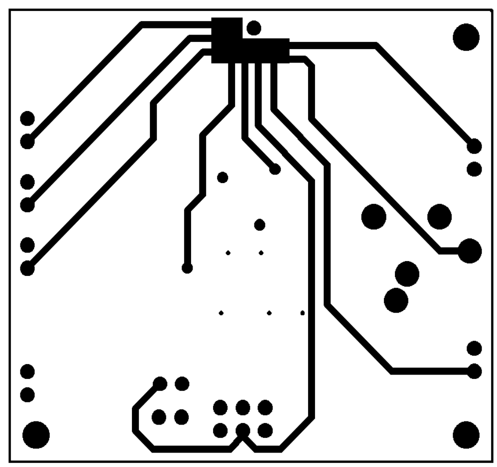

Figure 41. Recommended ITL PC Board Layout: Middle 2 Layer

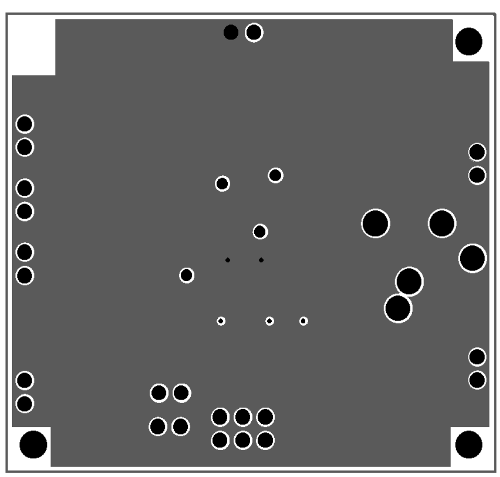

Figure 42. Recommended ITL PC Board Layout: Bottom Layer

Demonstration LQ Board Layout

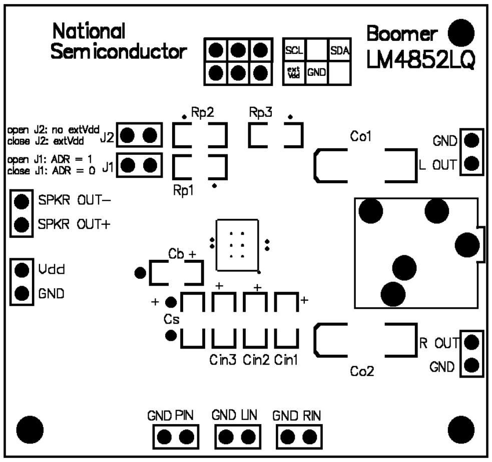

Figure 43. Recommended LQ PC Board Layout: Top Overlay Layer

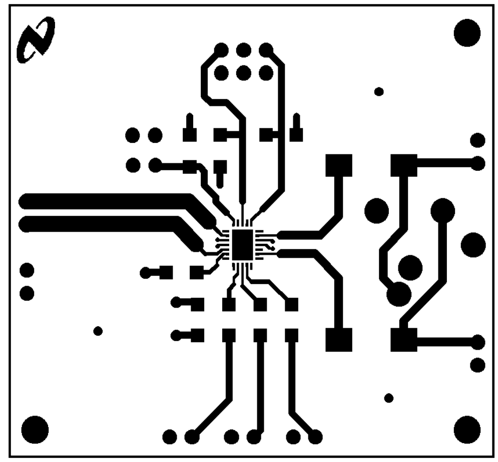

Figure 44. Recommended LQ PC Board Layout: Top Layer

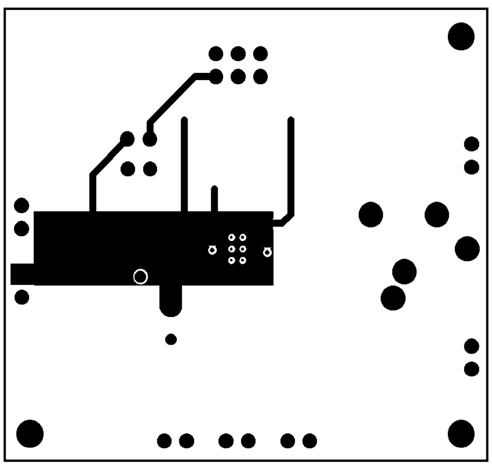

Figure 45. Recommended LQ PC Board Layout: Middle 1 Layer

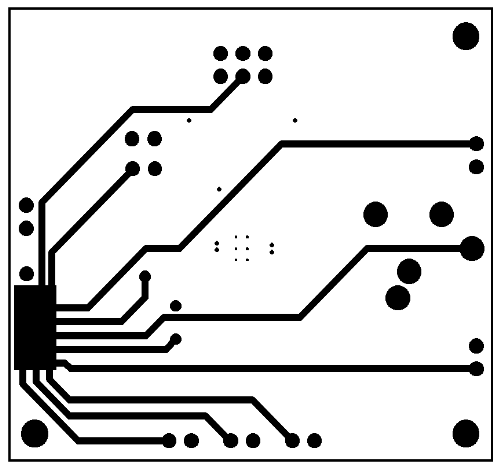

Figure 46. Recommended LQ PC Board Layout: Middle 2 Layer

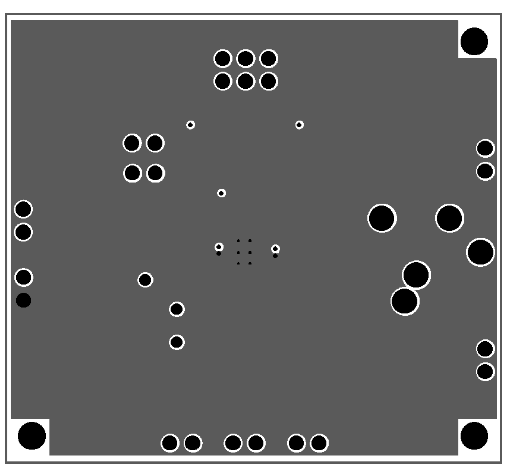

Figure 47. Recommended LQ PC Board Layout: Bottom Layer

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