

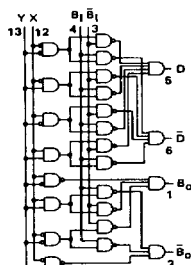
FULL SUBTRACTORS

MECL II MC1000/1200 series

MC1021 MC1221

Provides the DIFFERENCE, DIFFERENCE, BORROW OUT, and BORROW OUT functions while requiring only MINUEND (X) and SUBTRAHEND (Y) inputs with BORROW IN and BORROW IN.

POSITIVE LOGIC



$$\begin{aligned} D &= YXB_1 + Y\bar{X}\bar{B}_1 + \bar{Y}X\bar{B}_1 + \bar{Y}\bar{X}B_1 \\ \bar{D} &= \bar{Y}\bar{X}B_1 + YX\bar{B}_1 + YX\bar{B}_1 + \bar{Y}\bar{X}B_1 \\ B_0 &= \bar{Y}\bar{X}B_1 + Y\bar{X}\bar{B}_1 + YX\bar{B}_1 + YX\bar{B}_1 \\ \bar{B}_0 &= \bar{Y}\bar{X}\bar{B}_1 + \bar{Y}X\bar{B}_1 + \bar{Y}X\bar{B}_1 + YX\bar{B}_1 \end{aligned}$$

DC Input Loading Factor: X, Y = 1 B₁, B₁ = 2

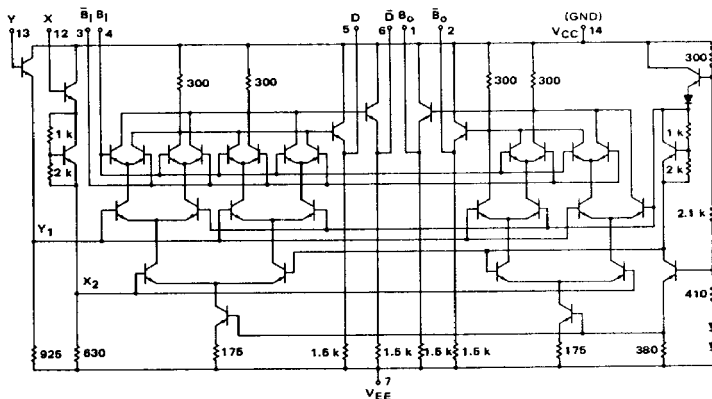
DC Output Loading Factor = 25

Power Dissipation = 145 mW typical

TRUTH TABLE

INPUT LOGIC LEVEL				OUTPUT LOGIC LEVEL			
X	Y	B ₁	B ₁	D	D	B ₀	B ₀
0	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	1	0	1	0	1	0	1
1	1	1	0	1	0	1	0

CIRCUIT SCHEMATIC



MC1021, MC1221 (continued)

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1221 Test Limits								MC1021 Test Limits							
			-55°C		+25°C		+125°C		Unit		0°C		+25°C		+75°C		Unit	
			Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	7	-	-	-	35	-	-	mAdc		-	-	-	35	-	-	mAdc	
Input Current	$2 I_{in}$	3	-	-	-	200	-	-	μ Adc		-	-	-	200	-	-	μ Adc	
	$2 I_{in}$	4	-	-	-	200	-	-			-	-	-	200	-	-		
	$1.5 I_{in}$	12	-	-	-	150	-	-			-	-	-	150	-	-		
	$1.5 I_{in}$	13	-	-	-	150	-	-			-	-	-	150	-	-		
Input Leakage Current	I_R	12	-	-	-	0.2	-	1.0	μ Adc		-	-	-	0.2	-	1.0	μ Adc	
		13	-	-	-	0.2	-	1.0			-	-	-	0.2	-	1.0		
		3	-	-	-	1.0	-	5.0			-	-	-	1.0	-	5.0		
		4	-	-	-	1.0	-	5.0			-	-	-	1.0	-	5.0		
"DIFFERENCE" Logic "1" Output Voltage ¹	V_{OH}^1	5	-0.890	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc		-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
"DIFFERENCE" Logic "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc		-1.830	-1.525	-1.800	-1.500	-1.780	-1.435	Vdc	
"BORROW" Logic "1" Output Voltage ¹	V_{OH}^1	1	-0.890	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc		-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc	
"BORROW" Logic "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc		-1.830	-1.525	-1.800	-1.500	-1.780	-1.435	Vdc	
Switching Times	Min/and Input Propagation Delay	t_{12-5+}	Typ	Max	Typ	Max	Typ	Max	ns		Typ	Max	Typ	Max	Typ	Max	ns	
			9.0	14	8.0	13	9.0	14.5			8.0	13	8.0	13	8.0	13		
		t_{12+5-}	5	8.0	13	8.0	13.5	11			8.0	13.5	8.0	13.5	9.0	15		
		t_{12-1+}	1	14	7.0	12.5	9.0	14.5			7.0	12.5	7.0	12.5	8.0	13		
	Rise Time	t_{12+1-}	1	13.5	8.0	13.5	11	17	ns		8.0	13.5	8.0	13.5	9.0	15	ns	
		t_{5+}	5	13	9.0	14	10	14			9.0	14	9.0	14	9.0	14		
	Fall Time	t_{1-}	1	13	7.0	12	9.0	14	ns		7.0	12	7.0	12	8.0	13	ns	
		t_{5-}	5	5.0	8.0	5.0	8.5	7.0			5.0	8.5	5.0	8.5	6.0	9.5		
		t_{1-}	1	5.0	8.0	5.0	8.0	7.0	ns		5.0	8.0	5.0	8.0	6.0	9.0	ns	
	Subtrahend Input Propagation Delay	t_{13+5-}	5	5.0	8.5	5.0	8.5	7.0	ns		5.0	8.5	5.0	8.5	6.0	9.5	ns	
		t_{13-5+}		6.0	8.0	5.0	8.5	7.0			5.0	8.5	5.0	8.5	6.0	9.0		
	Rise Time	t_{5+}		5.0	8.5	6.0	9.0	8.0	ns		6.0	9.0	6.0	9.0	7.0	9.5	ns	
		t_{5-}		5.0	8.5	5.0	8.5	7.0			5.0	8.5	5.0	8.5	6.0	9.5		
	Borrow Input Propagation Delay	t_{4+5-}	5	3.0	5.5	3.0	5.0	4.0	ns		3.0	5.0	3.0	5.0	3.0	5.0	ns	
		t_{4+5-}		4.0	7.5	4.0	7.5	6.0			4.0	7.5	4.0	7.5	5.0	8.5		
	Rise Time	t_{5+}		5.0	8.0	6.0	8.5	8.0	ns		6.0	8.5	6.0	8.5	7.0	10	ns	
		t_{5-}		5.0	8.0	5.0	8.5	7.0			5.0	8.5	5.0	8.5	6.0	9.5		

¹ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

² V_{OH} and V_{OL} limits apply only if not more than one

input (pin 3, 4, 12 or 13) is at a Threshold Voltage

(V_{IL} max or V_{IH} min). Conduct tests with one input

at a Threshold Voltage and apply appropriate V_{OL} max or

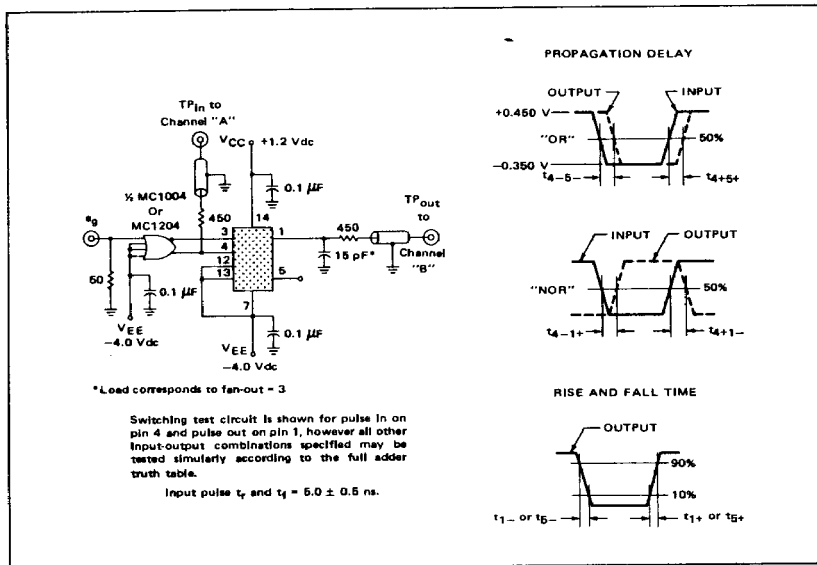
V_{OH} min voltages to all other inputs.

@Test
Temperature
MC1221 {
-55°C
+25°C
+125°C
MC1021 {
0°C
+25°C
+75°C

TEST VOLTAGE/CURRENT VALUES						
Vdc ± 1.0%						mAdc
V _{IL} min to V _{IL} max	V _{OL} max	V _{IH} min to V _{IH} max	V _{OH} min	V _{IH} max	V _{EE}	I _L
-5.2 to -1.405	-1.580	-1.165 to -0.825	-0.990	-	-5.2	-2.5
-5.2 to -1.325	-1.500	-1.025 to -0.700	-0.850	-0.700	-5.2	-2.5
-5.2 to -1.205	-1.380	-0.875 to -0.530	-0.700	-	-5.2	-2.5
-5.2 to -1.350	-1.520	-1.070 to -0.740	-0.895	-	-5.2	-2.5
-5.2 to -1.325	-1.500	-1.025 to -0.700	-0.850	-0.700	-5.2	-2.5
-5.2 to -1.260	-1.435	-0.950 to -0.615	-0.775	-	-5.2	-2.5
TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:						
V _{IL} min to V _{IL} max	V _{IH} min to V _{IH} max	V _{IH} max	V _{EE}	I _L	V _{CC} (Gnd)	
3	4	-	7, 12, 13	-	14	
4, 12, 13		3	7	-	14	
3, 12, 13		4		-	14	
3, 13	4	12		-	14	
3, 12	4	13		-	14	
4	3	-	7, 12, 13	-	14	
4	3	-	7, 12, 13	-	14	
-	3	-	3, 7, 12, 13	-	14	
			4, 7, 12, 13	-	14	
3, 12, 13*	4*	-	7	5	14	
4, 13*	3, 12*	-			14	
4, 12*	3, 13*	-			14	
3*	4, 12, 13*	-			14	
4, 12, 13*	3*	-	7	-	14	
3, 13*	3, 12*	-		-	14	
3, 12*	3, 13*	-		-	14	
4*	3, 12, 13*	-		-	14	
3, 12, 13*	4*	-	7	1	14	
3, 12*	4, 13*	-			14	
4, 12*	3, 13*	-			14	
3*	4, 12, 13*	-			14	
4, 12, 13*	3*	-	7	-	14	
4, 13*	3, 12*	-		-	14	
3, 13*	4, 12*	-		-	14	
4*	3, 12, 13*	-		-	14	
Pulse In	Pulse Out		V _{EE} = -4.0 Vdc		+1.2V	
12	5	-	7	-	14	
	5	-		-		
	1	-		-		
	1	-		-		
	5	-		-		
	1	-		-		
	5	-		-		
	1	-		-		
13	5	-	7	-	14	
		-		-		
		-		-		
		-		-		
4	5	-	7	-	14	
		-		-		
		-		-		
		-		-		

MC1021, MC1221 (continued)

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



APPLICATIONS INFORMATION

The MC1021/MC1221 full subtractor is identical to the full adder except for the interconnection metallization. It exhibits an average propagation delay time of 5.0 ns per stage in a system employing ripple borrow. This device permits building of ripple-through dividers.

The schematic of the full subtractor illustrates the techniques employed to obtain the necessary logic equations. A compensated current source drives a transistor "tree" with three levels of branching. The X input is translated negative two levels, to switch current between either the left or right branch of the tree. The Y input is translated negative one level to switch current at the second level of branching. Depending upon the eight possible combinations of inputs, one specific branch level in the Difference generating tree will be carrying current. Thus the proper output state is determined. The Borrow generating tree operates in the same manner. This series gating technique results in the best speed-power product obtainable with bipolar technology. Typical propagation delay times from the inputs to outputs are shown.

TYPICAL PROPAGATION DELAY TIMES

