Power Supply IC Series for TFT-LCD Panels for Automotive

Gamma Voltage Generated IC with Built-in DAC

BD81849MUV-C

General Description

The feature of gamma voltage generated IC with Built-in DAC BD81849MUV-C provides a single-chip solution with a high-precision 10bit DAC setting controlled by I2C BUS Control and a Buffer AMP (12ch). EEPROM Auto-read function is also incorporated.

Features

- AEC-Q100 Qualified(*Note 1*)
- Built-in 10bit DAC
- Built-in DAC Output Buffer Amplifier (12ch)
- Double Register Switching Function (SEL)
- I2C BUS Control (SDA, SCL)
  STANDARD-MODE, FAST-MODE Changeable
- EEPROM Auto-read Function
- Protection Circuits:
  Under Voltage Lock Out (UVLO)
  Over Voltage Protection (OVP)
  Thermal Shutdown Circuit (TSD)
  Power ON Reset Circuit

(*Note 1*) Grade 2

Application

TFT-LCD Panels which are used in car navigation, in-vehicle center panel, and instrument cluster

Key Specifications

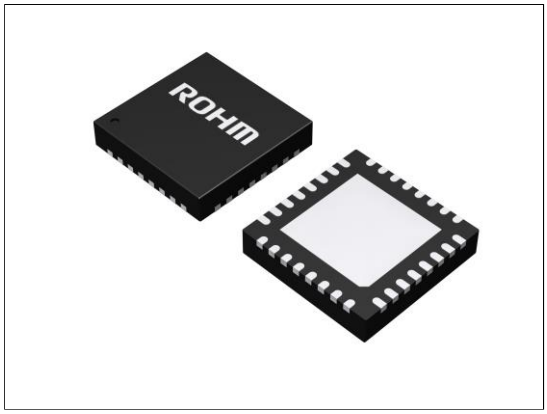
- VDD Input Voltage Range: 2.1V to 3.6V
- VCC Input Voltage Range: 10.0V to 18.0V
- Operating Temperature Range: -40°C to +105°C

Special Characteristics

- FB Regulation Voltage:
  ±2% (Ta = -25°C to +105°C)
- DAC Output Voltage Precision:
  ±200mV (Ta = -25°C to +105°C)

Package

	W(Typ) x D(Typ) x H(Max)
VQFN32SV5050	5.0mm x 5.0mm x 1.0mm



Typical Application Circuit

(TOP VIEW)

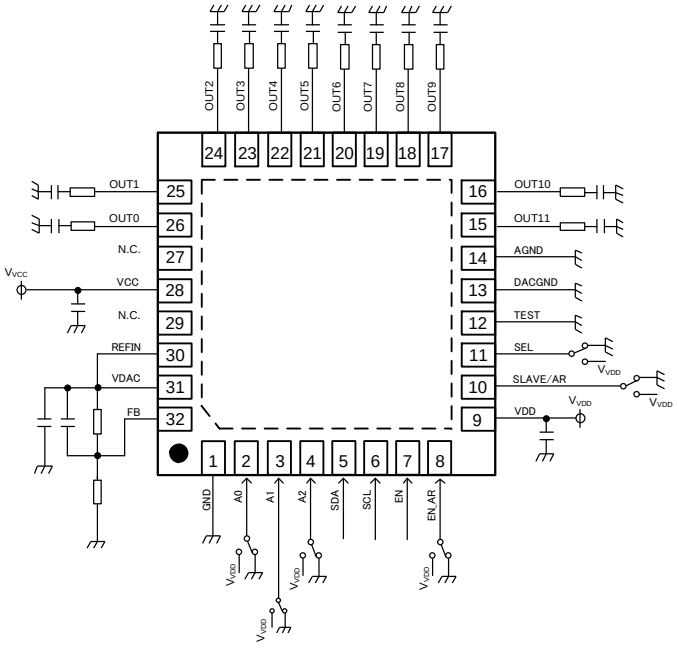


Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

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Pin Configuration

(TOP VIEW)

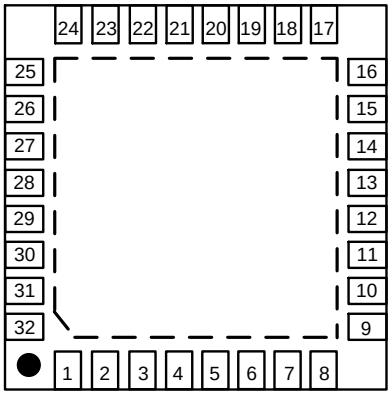


Figure 2. Pin Configuration

Pin Descriptions

No.	Pin Name	Function
1	GND	GND input
2	A0	Device address switching pin
3	A1	Word address switching pin
4	A2	Word address switching pin
5	SDA	Serial data input pin
6	SCL	Serial clock input pin
7	EN	VDAC enable pin
8	EN_AR	Auto-read enable pin
9	VDD	Logic power supply input
10	SLAVE/AR	Slave / Auto-read switching pin
11	SEL	REGISTER A/B select pin
12	TEST	Pin for test mode*(Note2)*
13	DACGND	GND input for DAC
14	AGND	Buffer AMP GND input
15	OUT11	Gamma output pin
16	OUT10	Gamma output pin
17	OUT9	Gamma output pin
18	OUT8	Gamma output pin
19	OUT7	Gamma output pin
20	OUT6	Gamma output pin
21	OUT5	Gamma output pin
22	OUT4	Gamma output pin
23	OUT3	Gamma output pin
24	OUT2	Gamma output pin
25	OUT1	Gamma output pin
26	OUT0	Gamma output pin
27	N.C.	Non Connection Pin*(Note2)*
28	VCC	Power supply input
29	N.C.	Non Connection Pin*(Note2)*
30	REFIN	DAC reference voltage input pin
31	VDAC	DAC voltage output
32	FB	Feedback pin

(Note 2) In normal use, please connect the TEST pin to OPEN or GND. Non Connection Pin to OPEN.

Block Diagram

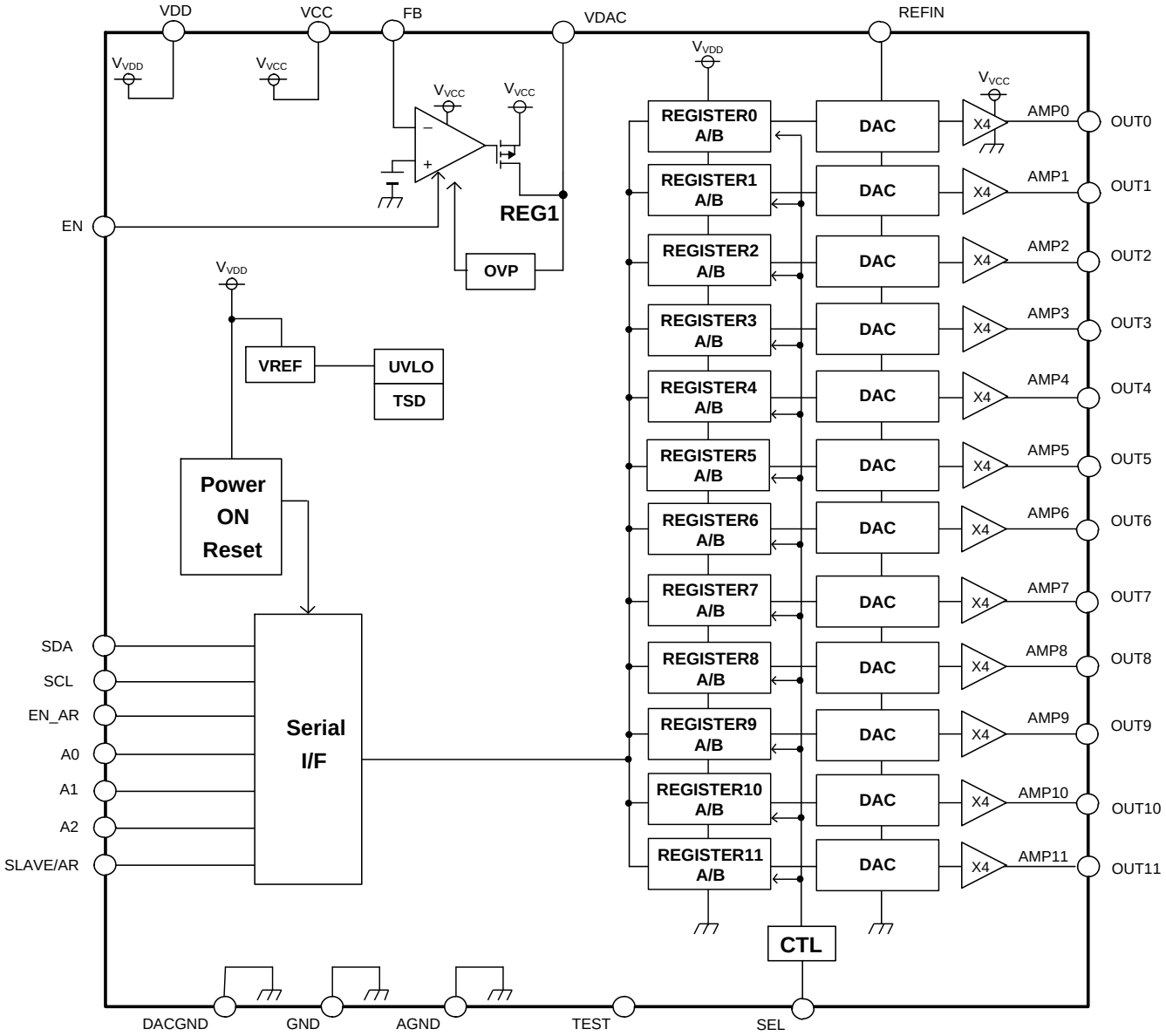


Figure 3. Block Diagram

Description of Blocks

1. REG1
   This is a regulator block for setting a reference voltage of DAC.
   VDAC has enable function so that if EN = Low, shutdown is performed, and if EN = High, settable VDAC voltage by FB voltage and external resistor. At this time, VDAC voltage < 4.5V (Max operating voltage) should be configured.
   When the VDAC pin is shorted to REFIN pin, please set VDAC voltage to meet the REFIN operating condition.

2. DAC
   Convert the 10bit digital signal read into the REGISTER to voltage.

3. AMP
   AMP amplifies the voltage output from the DAC Block by 4 times.
   While Under Voltage Lock Out (UVLO) circuit or Thermal Shutdown (TSD) circuit is operating, output goes into Hi-z.

4. Power ON Reset
   When the logic power supply VDD is activated, each IC generates a reset signal to initialize the serial I/F and each REGISTERS.

5. VREF
   This is a block to generate the inner reference voltage.

6. TSD (Thermal Shutdown)
   The TSD circuit turns output off when the chip temperature reaches or exceeds approximately 175°C (Typ) in order to prevent thermal destruction or thermal runaway. When the chip returns to a specified temperature, the circuit resets.
   The TSD circuit is designed only to protect the IC itself. The junction temperature should be designed less than 150°C (Typ).

7. REGISTER
   A serial signal (consisting of 10bit gamma correction voltage values) input by using the serial I/F is held for each register address. Data is initialized by a reset signal generated during Power ON Reset.

8. OVP (Over Voltage Protection)
   This is OVP function of VDAC voltage in order to prevent from VDAC over voltage when FB pin is short to GND.
   When VDAC voltage 5.5V (Typ) or more, BD81849MUV-C prevent overvoltage by turning off Register regulator.

9. Serial I/F
   This is a I2C BUS Control (SDA, SCL) type I/F. It can set a gamma voltage and a Register address.

10. CTL
    CTL Block selects Register by the SEL pin.
    When SEL = Low, REGISTER A is connected to DAC, and when SEL = High, REGISTER B is connected to DAC.

11. UVLO (Under Voltage Lock Out)
    It is Under Voltage Lock Out for VDD and REFIN. When VDD or REFIN voltage 1.9V (Typ) or more, IC release REG1 and AMP protection function.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{VDD}	-0.3 to +4.5	V
	V_{VCC}	-0.3 to +19.0	V
REFIN Voltage	V_{REFIN}	-0.3 to +5.0	V
DAC Reference Voltage	V_{DAC}	-0.3 to +7.0	V
Input Voltage	V_{SEL}, V_{A0}, V_{A1}, V_{A2}, V_{EN}, $V_{SLAVE/AR}$, V_{EN_AR}, V_{SDA}, V_{SCL}	-0.3 to +4.5	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 5)*	2s2p*(Note 6)*	
VQFN32SV5050				
Junction to Ambient	θ_{JA}	138.9	39.1	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	11	5	°C/W

(Note 3) Based on JESD51-2A (Still-Air).
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 5) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 6) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 7)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 7) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
VDD Supply Voltage	V_{VDD}	2.1	-	3.6	V
VCC Supply Voltage	V_{VCC}	10	-	18	V
REFIN Voltage	V_{REFIN}	2.1	-	4.5	V
DAC Reference Voltage	V_{DAC}	2.1	-	4.5	V
Input Voltage	V_{SEL},V_{EN}, V_{EN_AR}, V_{SDA}, V_{SCL}	-0.1	-	+3.6	V
	V_{A0}, V_{A1}, V_{A2}, $V_{SLAVE/AR}$	-0.1	-	V_{VDD}	V
Output Current Capability*(Note 8)* (OUT0)	I_{OA}	-40	-	-	mA
Output Current Capability*(Note 8)* (OUT1 to OUT5, OUT7 to OUT10)	I_{OB}	-20	-	+20	mA
Output Current Capability*(Note 8)* (OUT6)	I_{OC}	-40	-	+40	mA
Output Current Capability*(Note 8)* (OUT11)	I_{OD}	-	-	40	mA
I2C BUS Control Frequency	f_{CLK}	-	-	400	kHz
Operating Temperature	Topr	-40	-	+105	°C

(Note 8) Sink Current to BD81849MUV-C is a positive value. Source Current from BD81849MUV-C is a negative value.

Electrical Characteristics

(Unless otherwise specified, Ta = 25°C, V_{VDD} = 3.3V, V_{VCC} = 15.0V, V_{REFIN} = 3.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Gamma Amplifier]						
Sink Current Capability (OUT0)	I_{OOA}	-	-	10	mA	OUT0 = 14V setting Power supply inputs 15V to OUT0
Sink Current Capability (OUT1 to OUT5, OUT7 to OUT10)	I_{OOB}	-	-	30	mA	OUT1 to OUT5, OUT7 to OUT10 = 6V setting. Power supply inputs 15V to OUT1 to OUT5 and OUT7 to OUT10
Sink Current Capability (OUT6)	I_{OOC}	-	-	60	mA	OUT6 = 6V setting Power supply inputs 15V to OUT6
Sink Current Capability (OUT11)	I_{OOD}	-	-	60	mA	OUT11 = 1V setting Power supply inputs 2V to OUT11
Source Current Capability (OUT0)	I_{OIA}	-60	-	-	mA	OUT0 = 14V setting Power supply inputs 13V to OUT0
Source Current Capability (OUT1 to OUT5, OUT7 to OUT10)	I_{OIB}	-30	-	-	mA	OUT1 to OUT5, OUT7 to OUT10 = 6V setting Power supply inputs 0V to OUT1 to OUT5 and OUT7 to OUT10
Source Current Capability (OUT6)	I_{OIC}	-60	-	-	mA	OUT6 = 6V setting Power supply inputs 0V to OUT6
Source Current Capability (OUT11)	I_{OID}	-10	-	-	mA	OUT11 = 1V setting Power supply inputs 0V to OUT11
Load Stability (OUT0)	ΔV-A	-	10	70	mV	Io = -30mA to 0mA OUT0 = 6V setting
Load Stability (OUT1 to OUT5, OUT7 to OUT10)	ΔV-B	-	10	70	mV	Io = -15mA to +15mA OUTx = 6V setting
Load Stability (OUT6)	ΔV-C	-	10	70	mV	Io = -15mA to +15mA OUT6 = 6V setting
Load Stability (OUT11)	ΔV-D	-	10	70	mV	Io = 0mA to 30mA OUT11 = 6V setting
OUT Max Output Voltage (OUT0)	V_{OH-A}	V_{VCC}-0.2	V_{VCC}-0.1	-	V	Io = -30mA
OUT Max Output Voltage 1 (OUT1 to OUT5, OUT7 to OUT10)	V_{OH-B1}	V_{VCC}-1.2	V_{VCC}-0.75	-	V	Io = -15mA
OUT Max Output Voltage 2 (OUT1 to OUT5, OUT7 to OUT10)	V_{OH-B2}	V_{VCC}-0.6	V_{VCC} -0.375	-	V	Io = -7.5mA
OUT Max Output Voltage (OUT6)	V_{OH-C}	V_{VCC}-0.5	V_{VCC}-0.1	-	V	Io = -30mA
OUT Max Output Voltage (OUT11)	V_{OH-D}	V_{VCC}-1.2	V_{VCC}-0.75	-	V	Io = -15mA
OUT Min Output Voltage (OUT0)	V_{OL-A}	-	0.75	1.2	V	Io = 15mA
OUT Min Output Voltage 1 (OUT1 to OUT5, OUT7 to OUT10)	V_{OL-B1}	-	0.75	1.2	V	Io = 15mA
OUT Min Output Voltage 2 (OUT1 to OUT5, OUT7 to OUT10)	V_{OL-B2}	-	0.375	0.6	V	Io = 7.5mA
OUT Min Output Voltage (OUT6)	V_{OL-C}	-	0.1	0.5	V	Io = 30mA
OUT Min Output Voltage (OUT11)	V_{OL-D}	-	0.1	0.2	V	Io = 30mA
Slew-Rate (OUT0 to OUT11)	SRx	1	4	-	V/μs	OUT0 to OUT11 = No Load

Electrical Characteristics - continued

(Unless otherwise specified, Ta = 25°C, V_{VDD} = 3.3V, V_{VCC} = 15.0V, V_{REFIN} = 3.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[REG1]						
FB Voltage 1	V_{FB1}	1.237	1.250	1.263	V	
FB Voltage 2	V_{FB2}	1.225	1.250	1.275	V	Ta = -25°C to +105°C
Input Bias Current	I_{FB}	-1.2	+0.1	+1.2	µA	V_{FB} = 1.3V
Current Capability	I_O	10	50	-	mA	
[DAC]						
Integral Non-linearity Error (INL)	INL	-2	-	+2	LSB	00A to 3F5 is the allowance margin of error against the ideal linear.
Differential Non-linearity Error (DNL)	DNL	-2	-	+2	LSB	00A to 3F5 is the allowance margin of error against the ideal increase of 1LSB.
Output Voltage Precision Thermal Characteristics 1	V_{T1}	-200	+50	+200	mV	Ta = -25°C to +105°C
Output Voltage Precision Thermal Characteristics 2	V_{T2}	-100	+30	+100	mV	Ta = 0°C to +75°C
[Control Signal 1 SEL, EN, A0, A1, A2, SLAVE/AR, EN_AR]						
Inrush Current	I_{CTL}	7.0	16.5	33.0	µA	V_{SEL}, V_{EN}, V_{A0}, V_{A1}, V_{A2}, V_{EN_AR}, $V_{SLAVE/AR}$ = 3.3V
Input Voltage1 (High)	V_{DD1_H}	V_{VDD} x 0.65	-	V_{VDD}	V	Depend on VDD Ta = -40°C to +105°C
Input Voltage1 (Low)	V_{DD1_L}	0	-	V_{VDD} x 0.2	V	Depend on VDD Ta = -40°C to +105°C
[Control Signal 2 SDA, SCL]						
Input Voltage2 (High)	V_{DD2_H}	V_{VDD} x 0.65	-	V_{VDD}	V	Depend on VDD Ta = -40°C to +105°C
Input Voltage2 (Low)	V_{DD2_L}	0	-	V_{VDD} x 0.2	V	Depend on VDD Ta = -40°C to +105°C
Min Output Voltage	V_{CL}	-	-	0.4	V	SDA Input Current = 3mA SCL Input Current = 3mA
[Whole Device]						
VDD Power ON Reset Start-up Voltage	V_{DET1}	1.75	1.90	2.05	V	VDD UVLO Release
REFIN UVLO Voltage	V_{DET2}	1.75	1.90	2.05	V	REFIN UVLO Release
SEL Switching Time *(Note 9)*	t_{SEL}	-	0.3	1.0	µs	
VCC Circuit Current	I_{VCC}	-	6	-	mA	

(Note 9) SEL switching time timing is shown below.

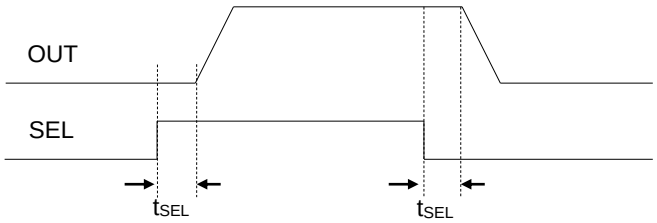


Figure 4. SEL Switching Time Timing

Typical Performance Curve (Reference Data)

(Unless otherwise specified, Ta = 25°C, V_{VDD} = 3.3V, V_{VCC} = 15.0V, V_{REFIN} = 3.5V)

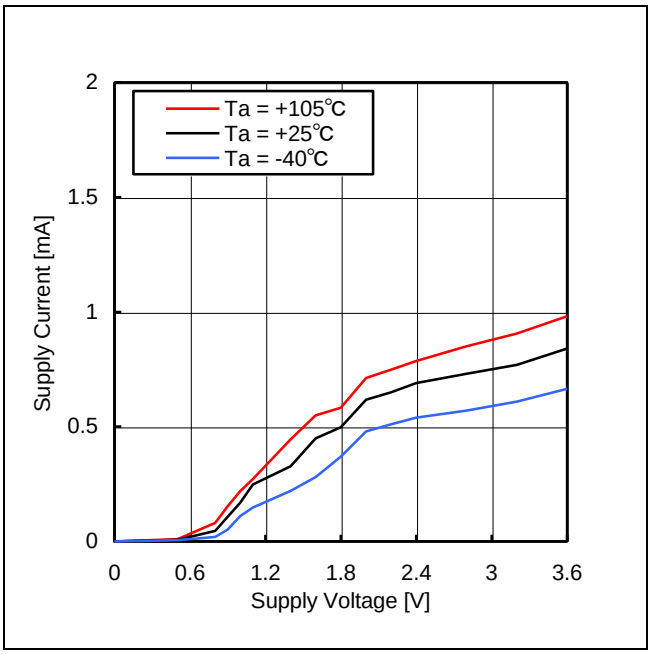


Figure 5. Supply Current vs Supply Voltage (VDD pin)

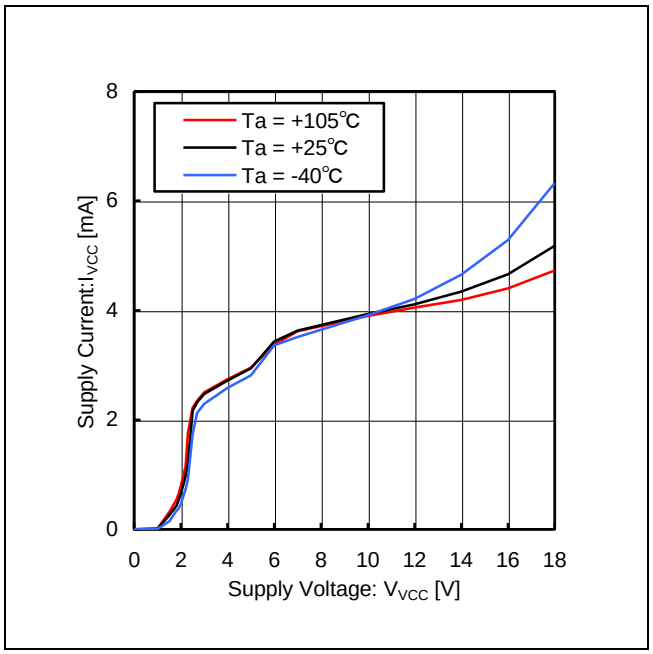


Figure 6. Supply Current: I_{VCC} vs Supply Voltage: V_{VCC}

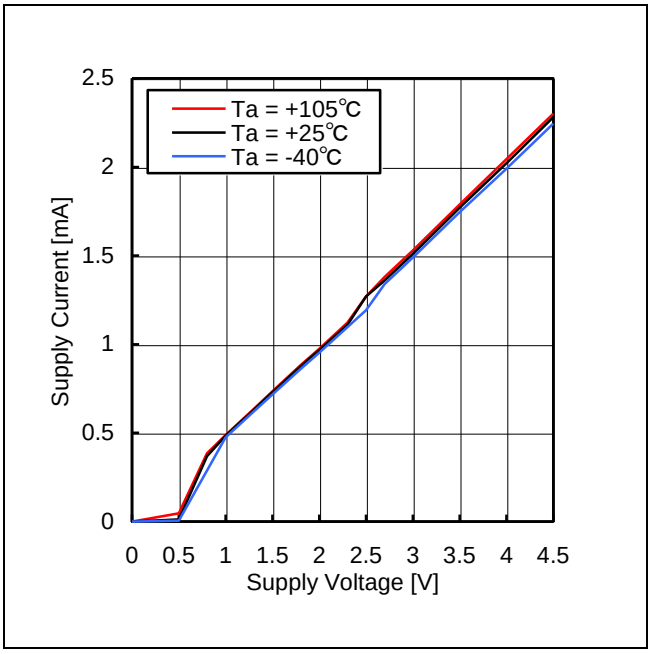


Figure 7. Supply Current vs Supply Voltage (REFIN pin)

Typical Performance Curve (Reference Data) - continued

(Unless otherwise specified, Ta = 25°C, V_{VDD} = 3.3V, V_{VCC} = 15.0V, V_{REFIN} = 3.5V)

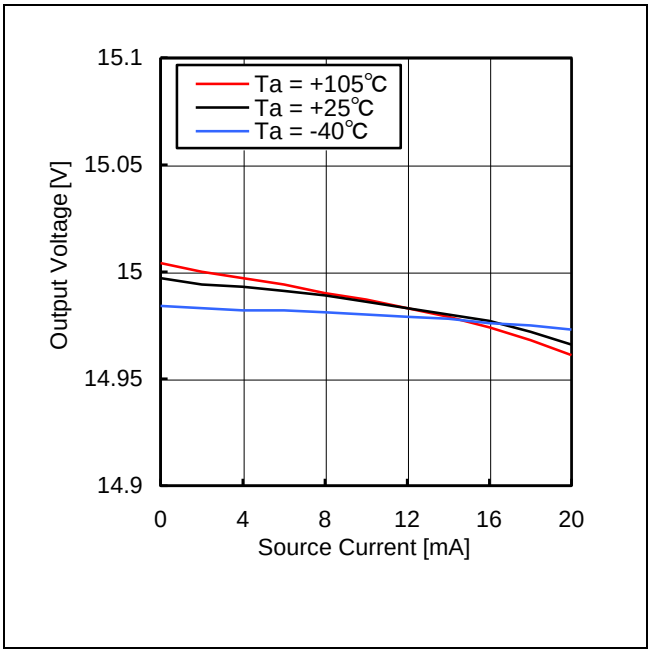


Figure 8. Output Voltage vs Source Current
(OUT0 pin, V_{REFIN} = 4.0V)

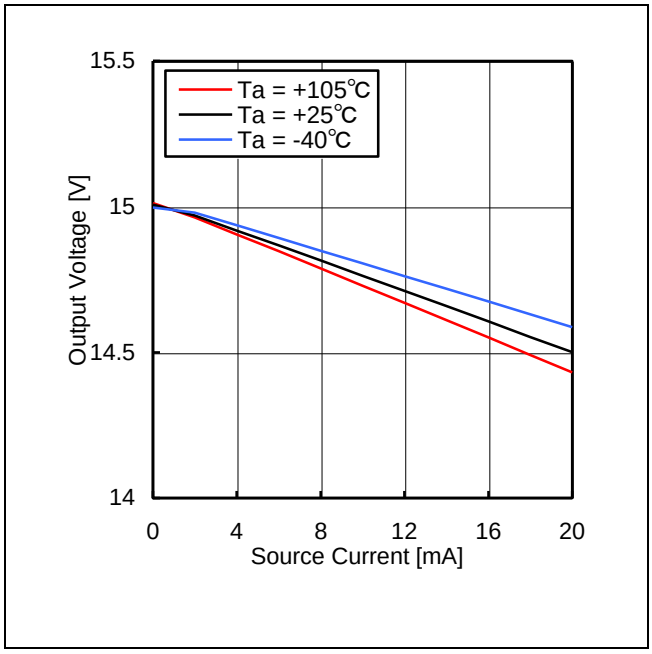


Figure 9. Output Voltage vs Source Current
(OUT1 pin to OUT5 pin, OUT7 pin to OUT10 pin,
V_{REFIN} = 4.0V)

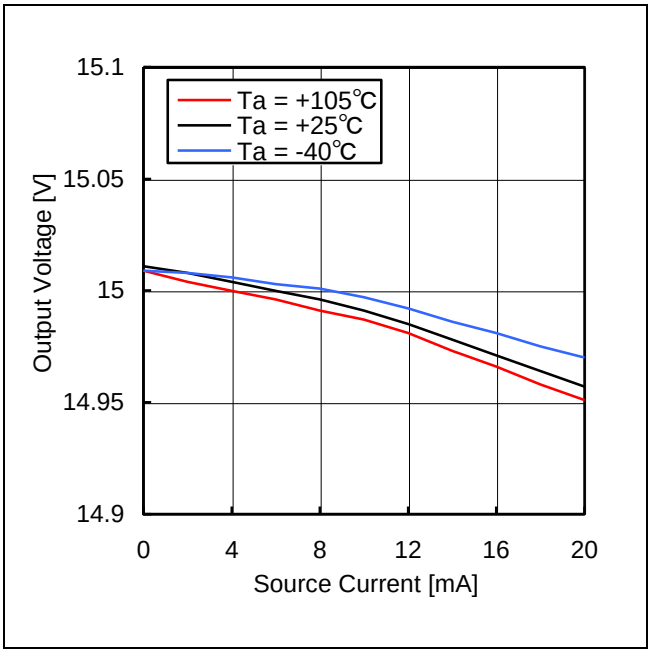


Figure 10. Output Voltage vs Source Current
(OUT6 pin, V_{REFIN} = 4.0V)

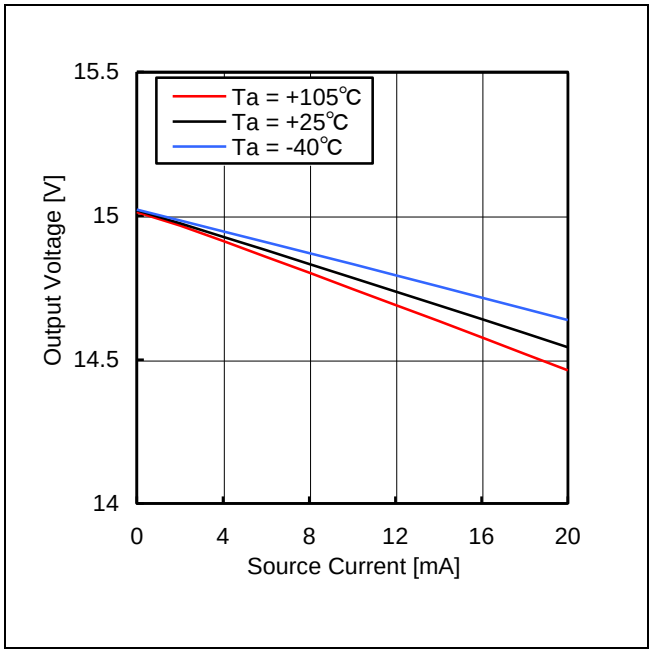


Figure 11. Output Voltage vs Source Current
(OUT11 pin, V_{REFIN} = 4.0V)

Typical Performance Curve (Reference Data) - continued
(Unless otherwise specified, Ta = 25°C, V_{VDD} = 3.3V, V_{VCC} = 15.0V, V_{REFIN} = 3.5V)

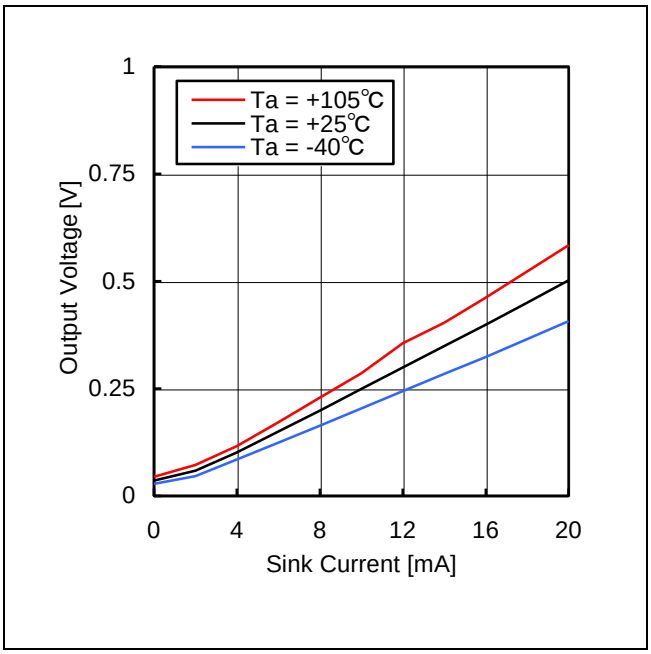


Figure 12. Output Voltage vs Sink Current
(OUT0 pin)

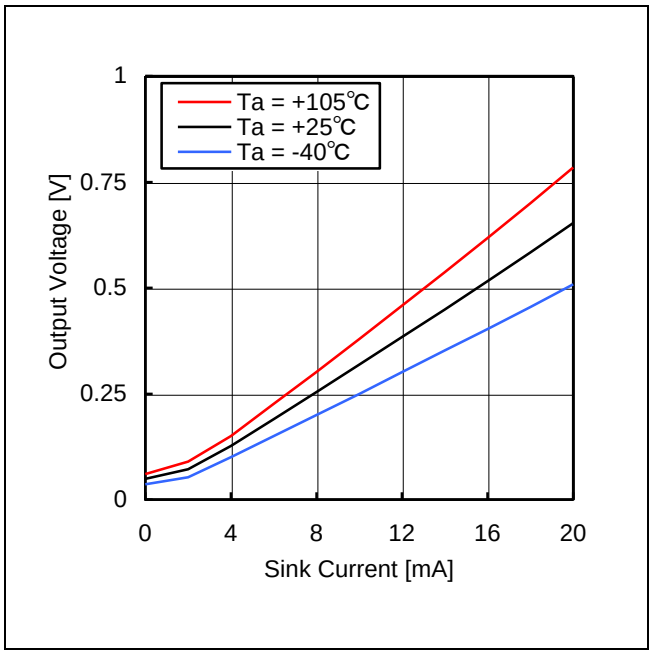


Figure 13. Output Voltage vs Sink Current
(OUT1 pin to OUT5 pin, OUT7 pin to OUT10 pin)

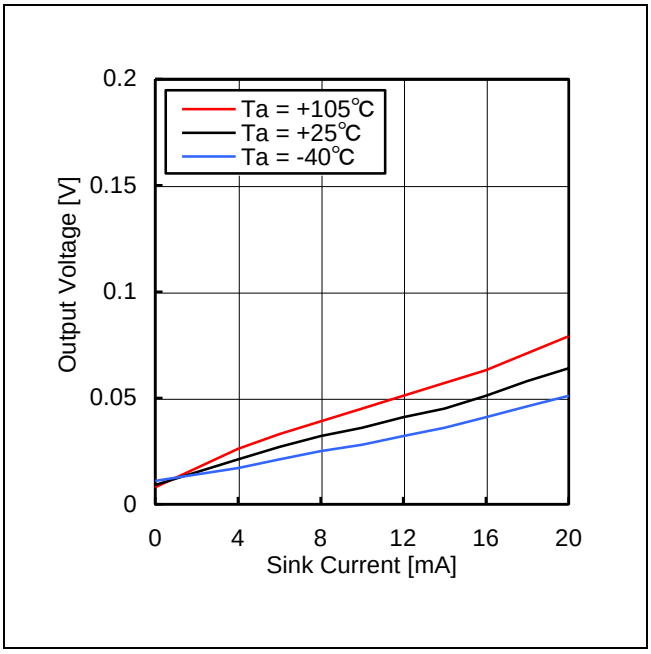


Figure 14. Output Voltage vs Sink Current
(OUT6 pin)

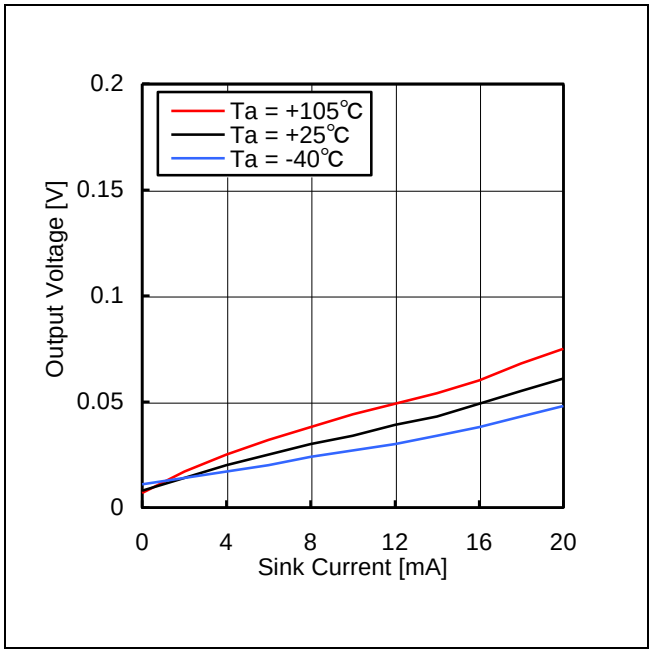


Figure 15. Output Voltage vs Sink Current
(OUT11 pin)

Typical Performance Curve (Reference Data) - continued
(Unless otherwise specified, Ta = 25°C, V_{VDD} = 3.3V, V_{VCC} = 15.0V, V_{REFIN} = 3.5V)

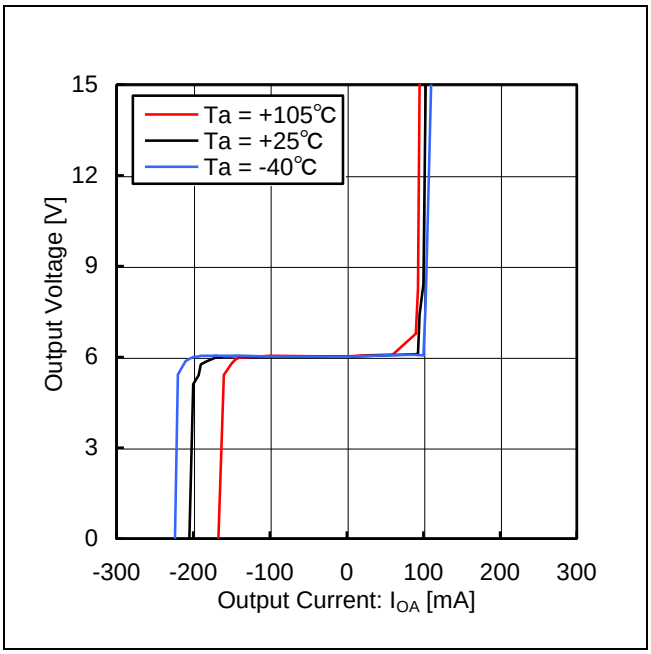


Figure 16. Output Voltage vs Output Current: I_{OA}

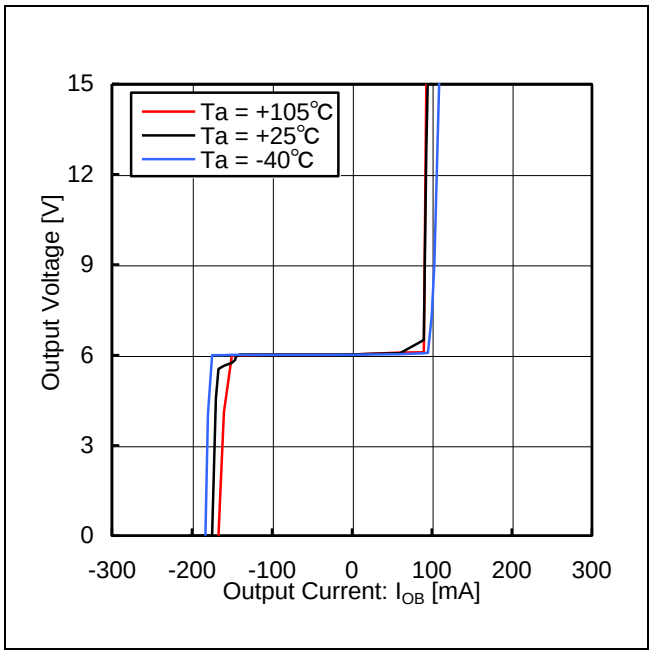


Figure 17. Output Voltage vs Output Current: I_{OB}
(OUT1 pin to OUT5 pin, OUT7 pin to OUT10 pin)

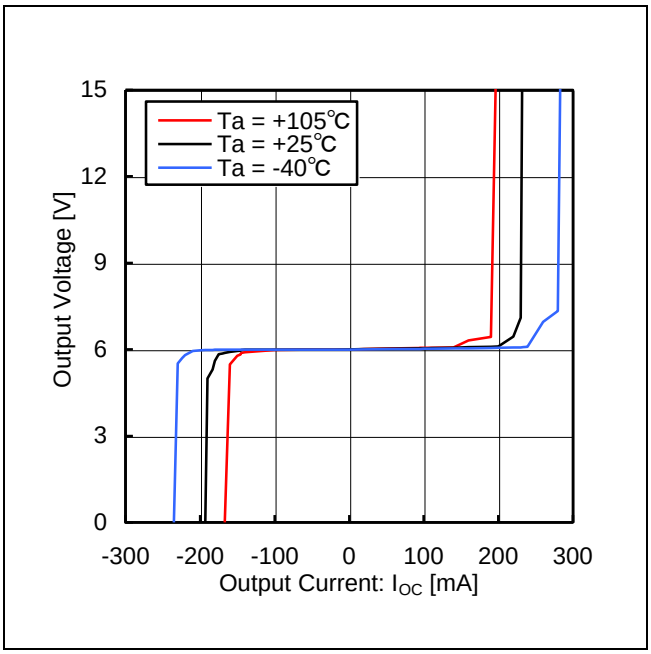


Figure 18. Output Voltage vs Output Current: I_{OC}

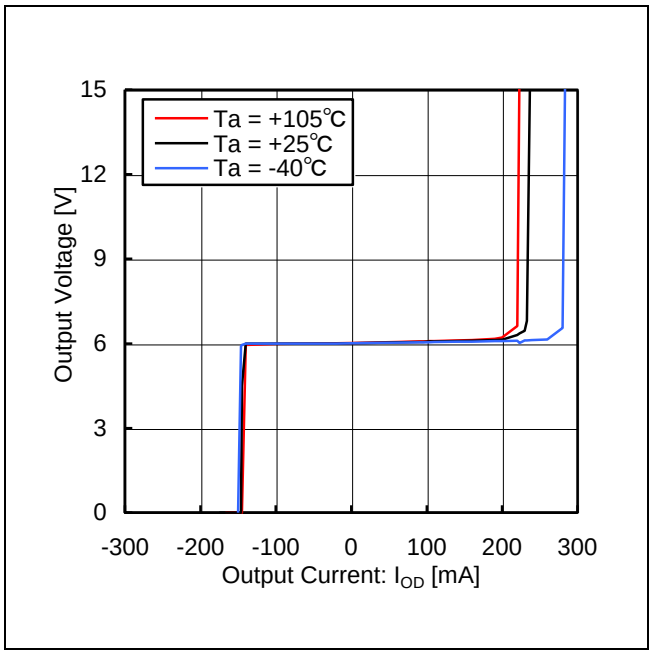


Figure 19. Output Voltage vs Output Current: I_{OD}

Typical Performance Curve (Reference Data) - continued
(Unless otherwise specified, Ta = 25°C, V_{VDD} = 3.3V, V_{VCC} = 15.0V, V_{REFIN} = 3.5V)

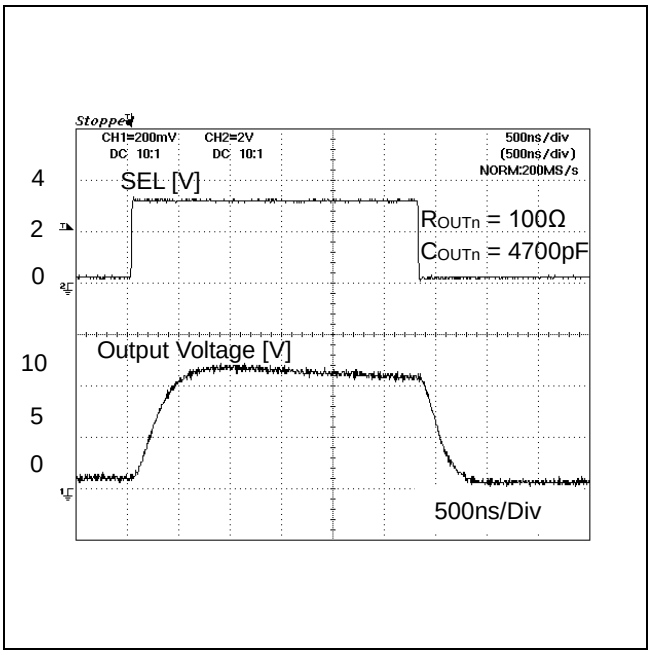


Figure 20. Slew-Rate Waveform
(High-Amplitude, OUTn pin: n = 0 to 11)

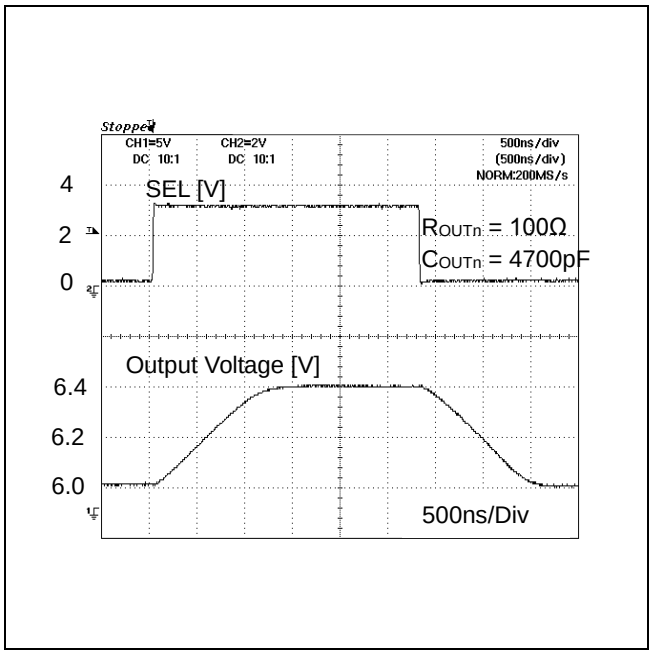


Figure 21. Slew-Rate Waveform
(Low-Amplitude, OUTn pin: n = 0 to 11)

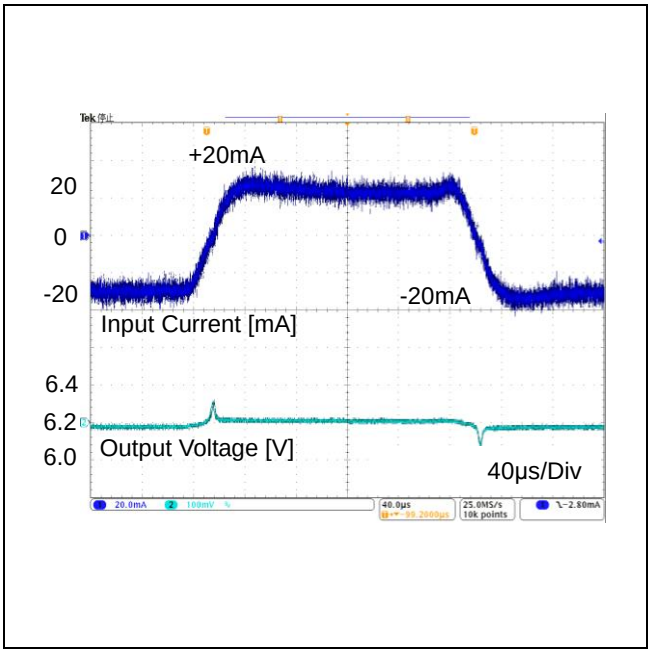


Figure 22. Load Transient

Application Example

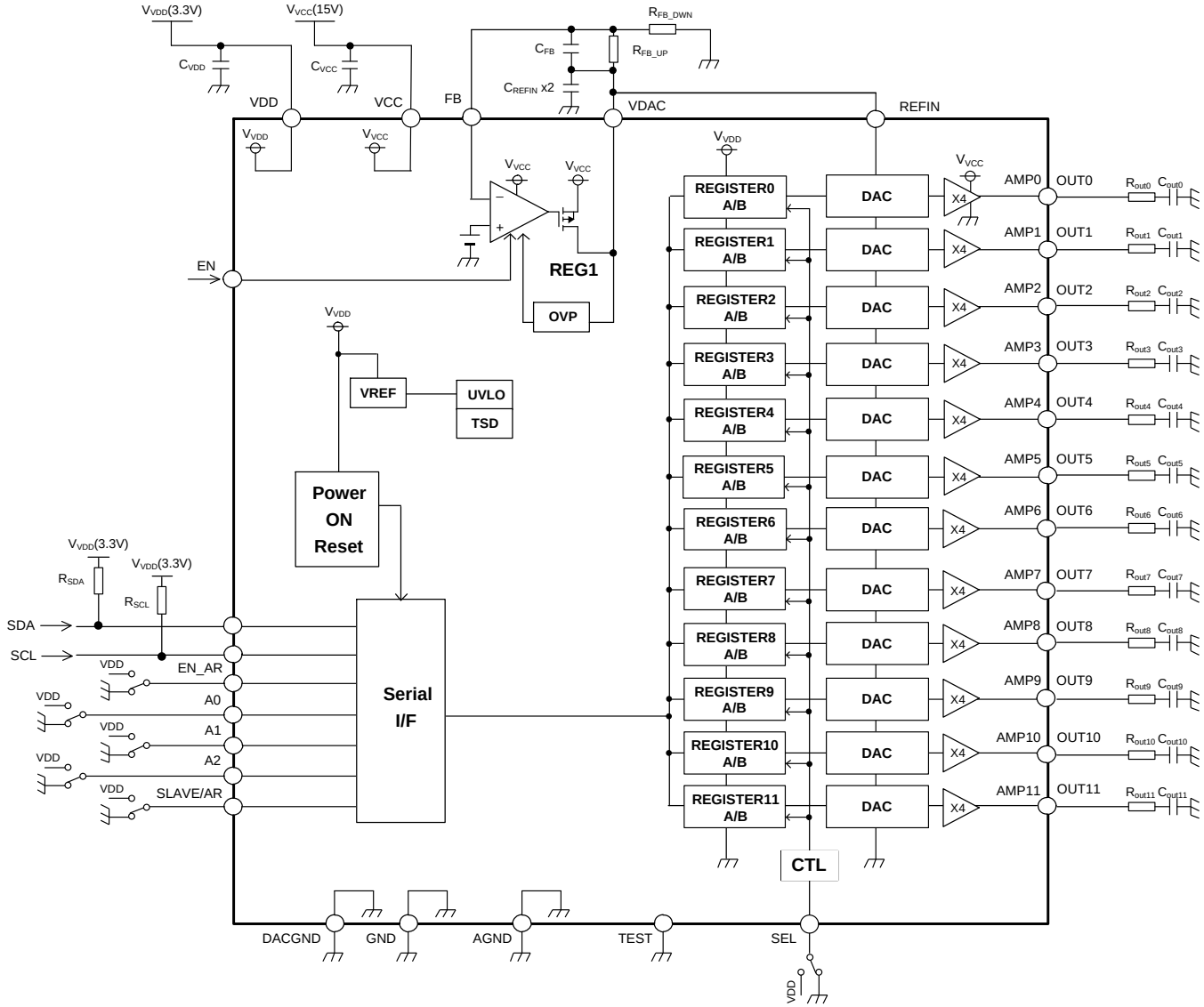


Figure 23. Application Example

Application Circuit Components List

(V_{VDD} = 3.3V, V_{VCC} = 15.0V, V_{REFIN} = 3.5V)

Parts Name	Limits			Unit	Maker	Parts Number
	Min	Typ	Max			
C_{VDD}	1	10	-	µF	Murata	GRT21BC81A106KE01
C_{VCC}	1	10	-	µF	Murata	GRT31CC81E106KE01
C_{REFIN}	-	1.0 x 2	-	µF	Murata	GRT21BC81E105KE13
C_{FB}	-	10	-	nF	Murata	GRT188R71H103KE01
R_{FB_UP}	10	36	50	kΩ	ROHM	MCR03EZPFX3602
R_{FB_DWN}	10	20	50	kΩ	ROHM	MCR03EZPFX2002
R_{OUT0} to R_{OUT11}	-	100	-	Ω	ROHM	MCR03EZPFX1000
C_{OUT0} to C_{OUT11}	-	4.7	-	nF	Murata	GRT188R71H472KE01
R_{SDA}	1	4.7	10	kΩ	ROHM	MCR03EZPFX4701
R_{SCL}	1	4.7	10	kΩ	ROHM	MCR03EZPFX4701

Please set in consideration of temperature properties and DC bias properties not to become less than the minimum.
Please consider it based on enough evaluations with the actual model.

Serial Communications

The serial data control block consists of a register that stores data from SDA and SCL, and a DAC circuit that receives the output from this register and provides adjusted voltages to other IC blocks.

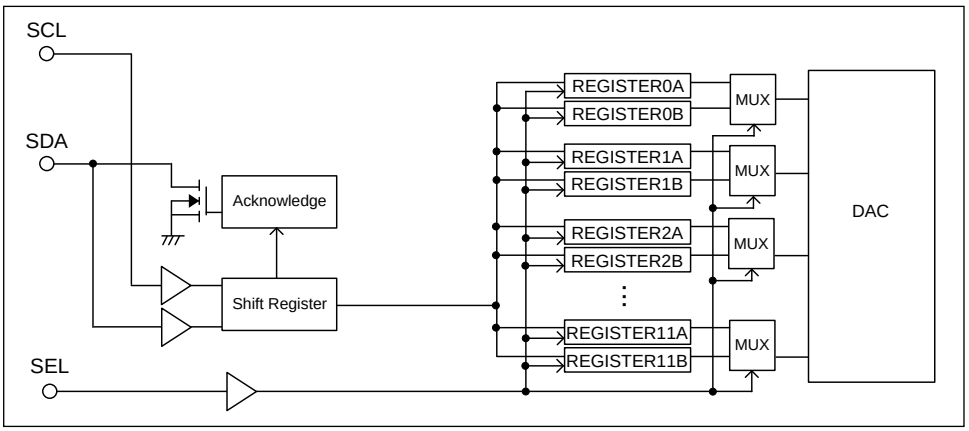


Figure 24. Serial Block Diagram

Double Register Switching Function

Switching Low/High by SEL pin enables switch to REGISTER A or REGISTER B.
At that time, 1.0µs (Max) takes from SEL pin switching to output (OUT) change start.
When SEL = Low, REGISTER A is connected to DAC.
When SEL = High, REGISTER B is connected to DAC.

Gamma Output Setting

Relation between gamma output voltage (OUT0 to OUT11) and DAC setting value is shown in formula below.

$$Gamma\ Output\ Voltage\ (OUT0\ to\ OUT11) = \{(DAC\ Setting\ Value + 1)/1024\} \times V_{REFIN} \times 4$$

Output voltage characteristics are the electrical characteristics shown in Page.8 regardless the setting voltage.

Output Voltage Setting Mode

1. Auto-read Mode

The Auto-read function enables external EEPROM to be automatically read by using the I2C BUS Control.
Automatic read from EEPROM will start when Auto-read trigger signal is inputted.
I2C BUS Control timing is FAST-MODE of Timing Specification (P.24).

Data writing to a Register is operated in order: REGISTER0A to REGISTER11A, REGISTER0B to REGISTER11B.
In addition, I2C BUS Control timing chart between the external EEPROM and BD81849MUV-C in Auto-read Mode becomes like Figure 25.

SLAVE/AR = High setting activates Auto-read Mode.
SLAVE signal is not accepted during Auto-read waiting mode after VDD input.
After data reading completion by Auto-read, it switches to SLAVE MODE.
Other command is rejected during Auto-read operation.
Auto-read Mode is corresponded to EEPROM with 1k bit, 2k bit and 4k bit.

1.1. When BD81849MUV-C is connected to EEPROM

1.1.1. When BD81849MUV-C is connected to 1k or 2k bit EEPROM

A1 serves as the EEPROM word address setting pins. Also, A2 serves as the EERPOM device address.
EEPROM device address is 1010_00(A2).

A1	REGISTER A		REGISTER B	
	READ START WORD ADDRESS	READ END WORD ADDRESS	READ START WORD ADDRESS	READ END WORD ADDRESS
L	0(000h)	23(017h)	24(018h)	47(02Fh)
H	128(080h)	151(097h)	152(098h)	175(0AFh)

1.1.2. When BD81849MUV-C is connected to 4k bit EEPROM

A1 and A2 serves as the EEPROM word address setting pins.
EEPROM device address is 1010_00(PS) (PS is a page select bit.)
When A1 and A2 are both set to Low, read access is available for word addresses 0 through 47 in EEPROM.
After data read to all Register, each output starts outputting synchronously. Until output start from VCC input, it outputs 0V.

A2	A1	REGISTER A		REGISTER B	
		READ START WORD ADDRESS	READ END WORD ADDRESS	READ START WORD ADDRESS	READ END WORD ADDRESS
L	L	0(000h)	23(017h)	24(018h)	47(02Fh)
L	H	128(080h)	151(097h)	152(098h)	175(0AFh)
H	L	256(100h)	279(117h)	280(118h)	303(12Fh)
H	H	384(180h)	407(197h)	408(198h)	431(1AFh)

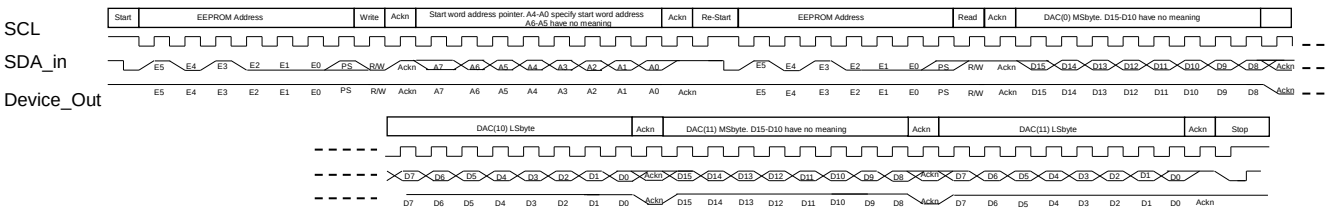


Figure 25. I2C Timing Chart (Auto-read Mode)

Output Voltage Setting Mode - continued

1.2. Explanation of Auto-read Trigger Signal

1.2.1. In case Auto-read starts by VDD power supply input

Auto-read will start after Power ON Reset release.

Gamma output voltage outputs a voltage matching the register setting synchronously after VCC voltage and REFIN voltage input.

The data reading time by Auto-read is 3ms (Max). Should maintain EN_AR = High during that time.

[Mode Setting]

- SLAVE/AR = High
- VDD input with the EN_AR pin is shorted to VDD pin

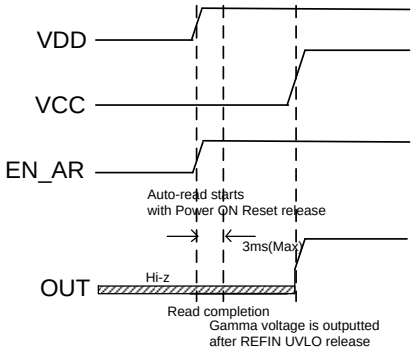


Figure 26. Auto-read Timing by VDD voltage

1.2.2. In case Auto-read starts by EN_AR

Auto-read will start with EN_AR = High.

Auto-read timing can be set optionally at the timing with EN_AR = High.

Gamma output voltage outputs a voltage matching a Register setting synchronously after VCC voltage and REFIN voltage input.

Data reading time by Auto-read is 3ms (Max). Should maintain EN_AR = High during that time.

[Mode Setting]

- SLAVE/AR = High
- EN_AR = Low => High

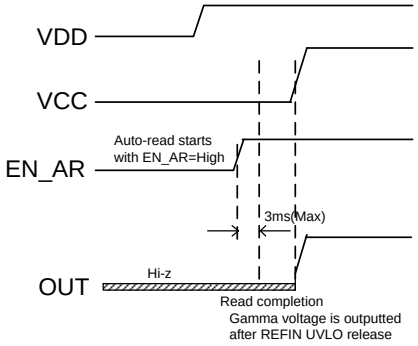


Figure 27. Auto-read Timing by EN_AR

1.2.3. In case Auto-read starts by VCC power supply input

Auto-read will start at the timing with Under Voltage Lock Out release.

Gamma output voltage outputs a voltage matching the register setting synchronously after Auto-read completion.

[Mode Setting]

- SLAVE/AR = High
- EN_AR = Low

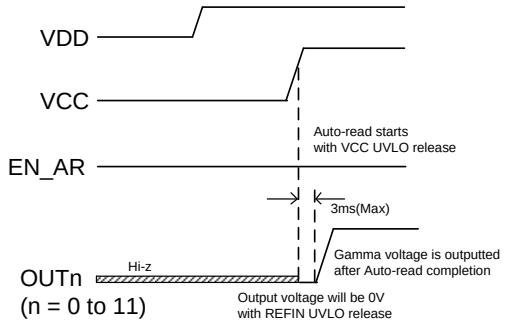


Figure 28. Auto-read Timing by VCC Voltage

*Data reading time by Auto-read is 3ms (Max).

*The Auto-read starts by the VCC voltage input becomes effective only in the case of 1st Auto-read operation after the VDD voltage input.

Output Voltage Setting Mode - continued

< About Data Refresh >

To perform reloading data “Data Refresh”, having EN_AR switches Low to High enables Auto-read operation again from EEPROM, and re-read the data. 10µs holding time is needed to determine EN_AR logic.
Data reading time by Auto-read is 3ms (Max). Should maintain EN_AR = High during that time.

< In case inputting EN_AR falls Low during Auto-read operation >

If inputting EN_AR = Low during Auto-read operation, input from D15 to D0 is completed and write the inputted data to a register taken back ACK. When EN_AR = Low is determined, the half-way and the following reading data will be invalid. 10µs holding time is needed to determine EN_AR logic.

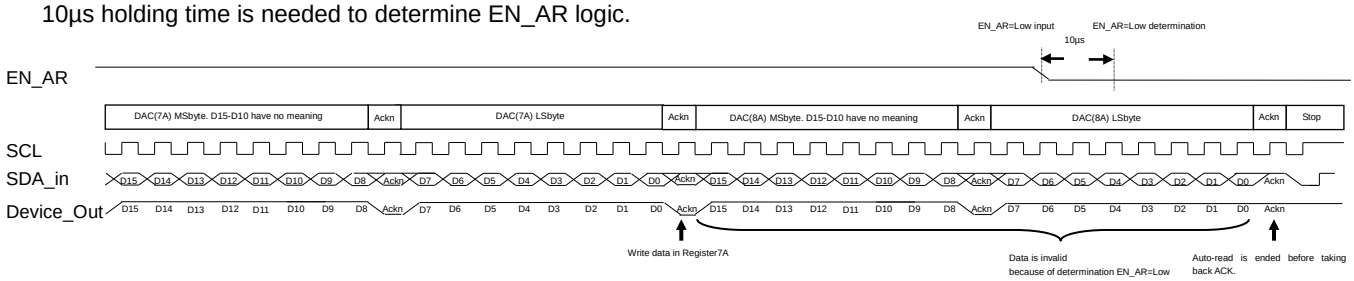


Figure 29. I2C Timing Chart (If EN_AR go to Low level in the middle of Auto-read)

Output Voltage Setting Mode - continued

2. SLAVE MODE

Set SLAVE/AR = Low in SLAVE MODE.

Write data in a specified register address through I2C BUS Control.

There are two writing modes from I2C BUS Control to REGISTER: (1) Single Mode (2) Multi-Mode.

In Single Mode, write data in one specified register.

In Multi-Mode, inputting multiple data from start address as specified register at 2nd byte enables to write data in a row.

Single Mode or Multi-Mode can be set by having or not having STOP bit.

[Mode Setting]

- SLAVE/AR = Low
- R/W = Low(1byte, 8th bit)

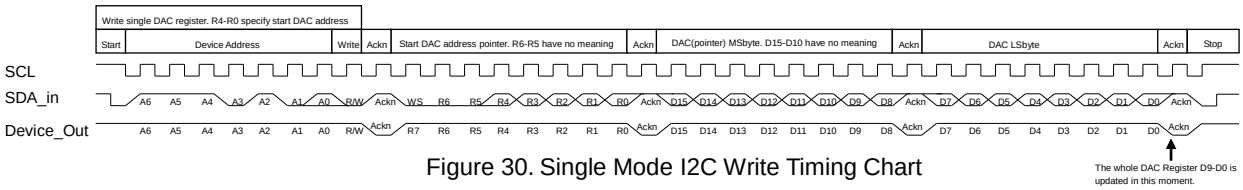


Figure 30. Single Mode I2C Write Timing Chart

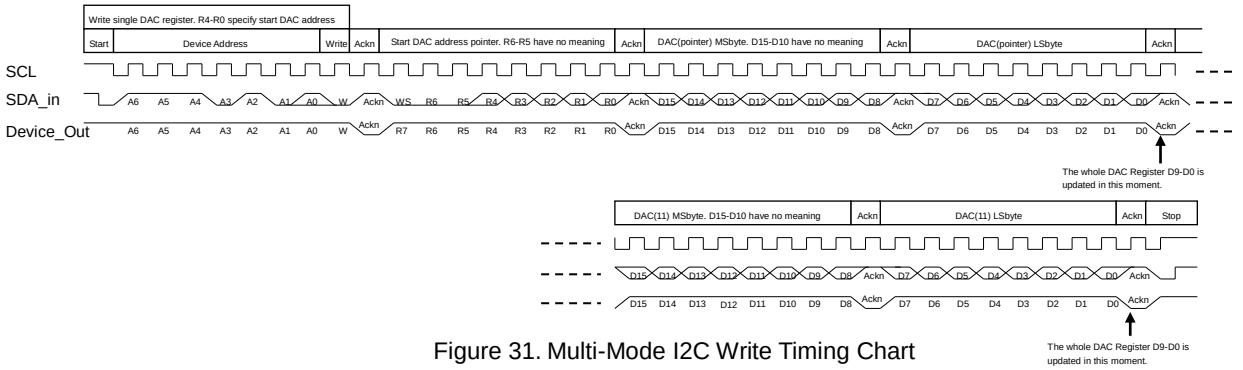


Figure 31. Multi-Mode I2C Write Timing Chart

*Writing data to a Register is operating in order: REGISTER0 A to REGISTER11 A, REGISTER0 B to REGISTER11 B.

Output Voltage Setting Mode - continued

< Reading register data >

There are two reading modes from I2C BUS Control to Register: (1) Single Mode (2) Multi-Mode.
In Single Mode, read data in one specified register.
In Multi-Mode, read out the REGISTER data in a row from the REGISTER which specified by start address.
To end the reading mode, send the NACK(ACK = H) and STOP bit.

[Mode Setting]

- SLAVE/AR = Low or High

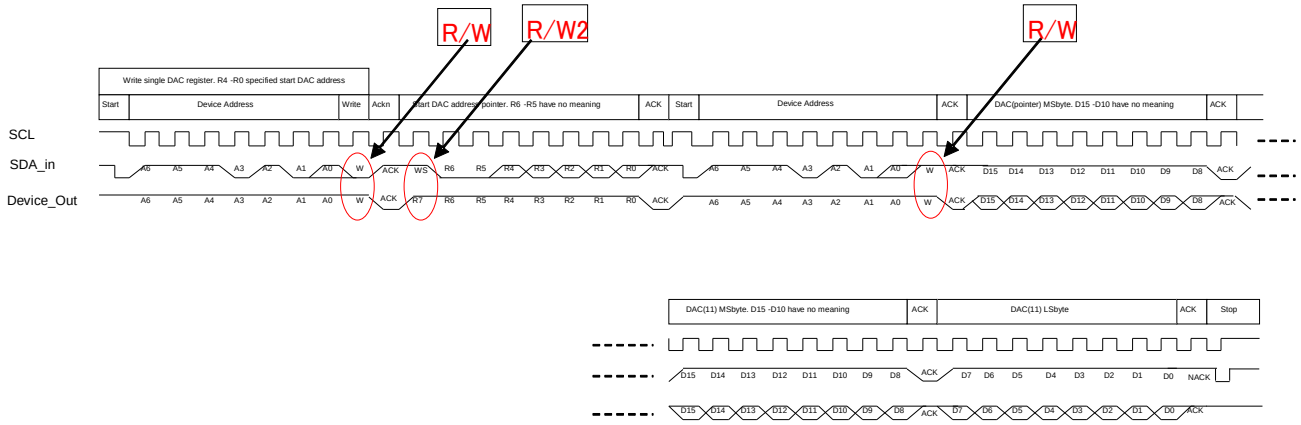


Figure 32. I2C Read Mode Timing Chart

*1st byte: Send device address and R/W bit = Low.
*2nd byte: Put R/W2 bit High and specify which REGISTER to read out with read mode.
*3rd byte: Send device address and R/W bit = High.
*After 4th byte: The REGISTER data which is read by the 4th byte and after.

REGISTER ADDRESS

Device address A6 to A1 is specific to the IC. (A6 to A0) = 111010(A0).
A0 can be set externally. It is pulled down inside so that in open state, it is“0”. If setting to “1”, please connect to VDD.

Register Name	Register Address					Initial Value	Register Name	Register Address					Initial Value
	R4	R3	R2	R1	R0			R4	R3	R2	R1	R0	
REGISTER0 A	0	0	0	0	0	000h	REGISTER0 B	1	0	0	0	0	000h
REGISTER1 A	0	0	0	0	1	000h	REGISTER1 B	1	0	0	0	1	000h
REGISTER2 A	0	0	0	1	0	000h	REGISTER2 B	1	0	0	1	0	000h
REGISTER3 A	0	0	0	1	1	000h	REGISTER3 B	1	0	0	1	1	000h
REGISTER4 A	0	0	1	0	0	000h	REGISTER4 B	1	0	1	0	0	000h
REGISTER5 A	0	0	1	0	1	000h	REGISTER5 B	1	0	1	0	1	000h
REGISTER6 A	0	0	1	1	0	000h	REGISTER6 B	1	0	1	1	0	000h
REGISTER7 A	0	0	1	1	1	000h	REGISTER7 B	1	0	1	1	1	000h
REGISTER8 A	0	1	0	0	0	000h	REGISTER8 B	1	1	0	0	0	000h
REGISTER9 A	0	1	0	0	1	000h	REGISTER9 B	1	1	0	0	1	000h
REGISTER10 A	0	1	0	1	0	000h	REGISTER10 B	1	1	0	1	0	000h
REGISTER11 A	0	1	0	1	1	000h	REGISTER11 B	1	1	0	1	1	000h

As register address, use lower 5 bit(R4 to R0) at 2nd byte. R6 to R5 should be set to “0” as usual.
When R7 = Low, Register enter writing mode and R7 = High, Register enter reading mode.

Power Supply Sequence

Activate the logic power supply VDD before the power supply VCC to prevent IC malfunctions due to undefined logic in the logic circuit. Input serial data after canceling the Power ON Reset. When turning off the IC's power supplies, turn off VCC first and then VDD.

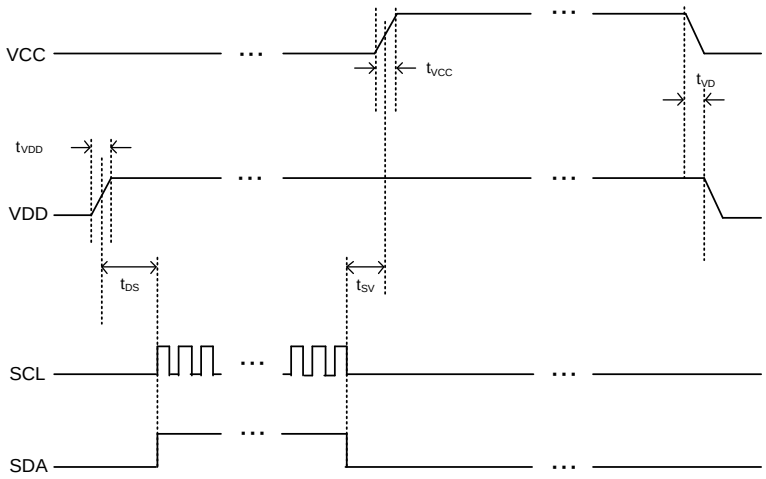


Figure 33. Power Supply Sequence Diagram

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Serial Input Timing	t_{DS}	100	-	-	µs
VCC Input Timing	t_{SV}	-	10	-	µs
Power Supply OFF Timing	t_{VD}	0	10	-	µs
VCC(REFIN) Rising Time	t_{VCC}	3	-	-	ms
VDD Rising Time	t_{VDD}	1	-	-	ms

I2C BUS Control Timing Chart

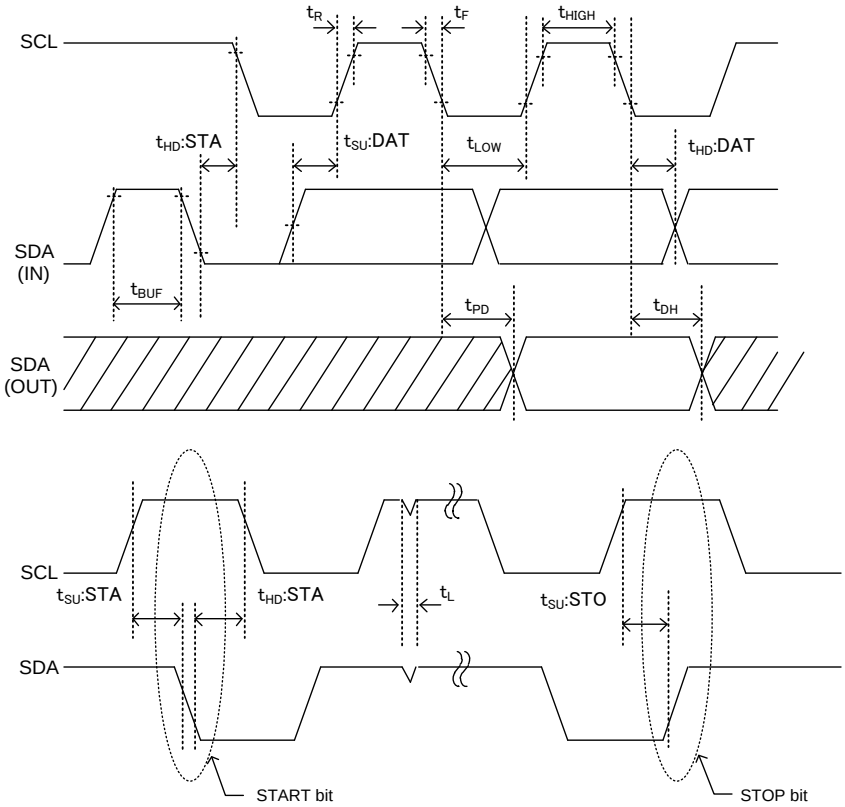


Figure 34. I2C BUS Control Timing

Timing Specification

Parameter	Symbol	STANDARD-MODE			FAST-MODE			Unit
		Min	Typ	Max	Min	Typ	Max	
Auto-read SCL Frequency	f_{ASCL}	150	275	400	150	275	400	kHz
SCL Frequency	f_{SCL}	-	-	100	-	-	400	kHz
SCL“H” Time	t_{HIGH}	4.0	-	-	0.6	-	-	µs
SCL“L” Time	t_{LOW}	4.7	-	-	1.2	-	-	µs
Rising Time	t_R	-	-	1.0	-	-	0.3	µs
Falling Time	t_F	-	-	0.3	-	-	0.3	µs
Start Condition Hold Time	t_{HD}:STA	4.0	-	-	0.6	-	-	µs
Start Condition Setup Time	t_{SU}:STA	4.7	-	-	0.6	-	-	µs
SDA Hold Time	t_{HD}:DAT	200	-	-	100	-	-	ns
SDA Setup Time	t_{SU}:DAT	200	-	-	100	-	-	ns
Acknowledge Delay Time	t_{PD}	-	-	0.9	-	-	0.9	µs
Acknowledge Hold Time	t_{DH}	-	0.1	-	-	0.1	-	µs
Stop Condition Setup Time	t_{SU}:STO	4.0	-	-	0.6	-	-	µs
BUS Discharge Time	t_{BUF}	4.7	-	-	1.2	-	-	µs
Noise Spike Width	t_L	-	0.1	-	-	0.1	-	µs

Selection of Components Externally Connected

VDAC Output Voltage Setting

Refer to the following equation to set the feedback resistor. FB voltage is 1.25V (Typ).

As the setting range, 10kΩ to 50kΩ is recommended.

If the resistor is set less than 10kΩ, it causes the reduction of power efficiency. If it is set more than 50kΩ, the offset voltage becomes larger by the input bias current 0.1μA (Typ) in the internal LDO.

$$V_{VDAC} = \frac{R_{FB\_UP} + R_{FB\_DWN}}{R_{FB\_DWN}} x V_{FB} \quad [V]$$

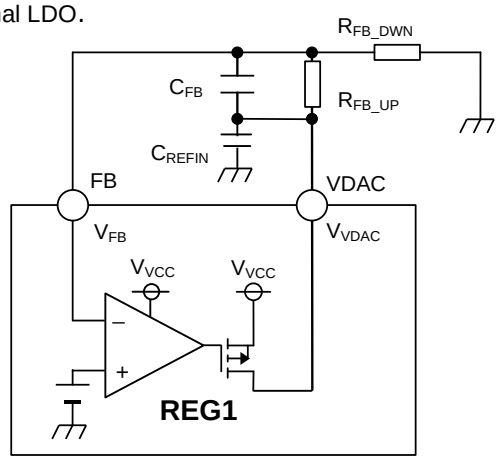


Figure 35. Application Circuit Diagram

PCB Layout Guide

GND Wiring Pattern

The high current GND (GND, AGND, DACGND) should be wired thick. To reduce line impedance, the GND lines must be as short and thick as possible and uses few via.

Power Supply Voltage Line Wiring Pattern

For power supply voltage (VDD, VCC) and internal reference voltage (REFIN), place smooth capacitor nearby IC pin. Please note that smooth capacitor does not vary PCB layer.

The figure 36 shows an application circuit on the basic PCB layout pattern guideline mentioned above.

Bold dot line (Black): High current line

One dot and dashed line (Blue): Wiring easily affected by noise

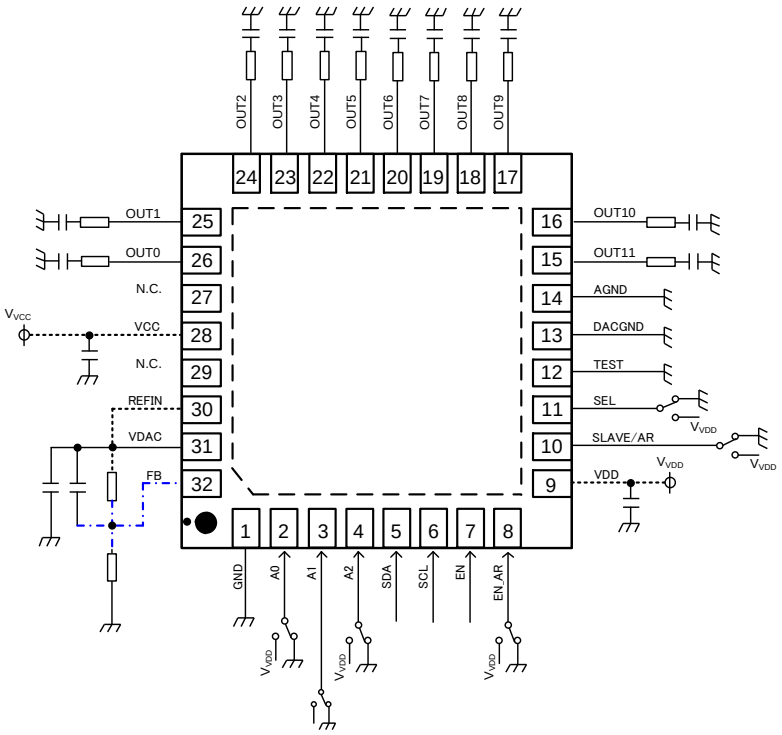
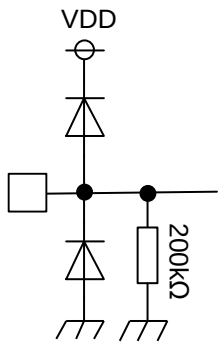
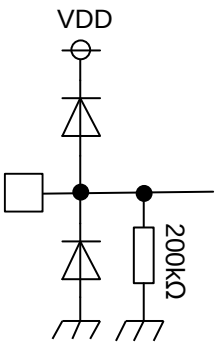
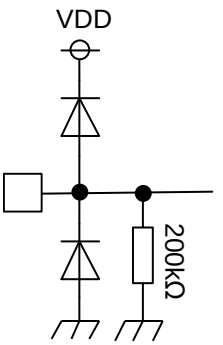
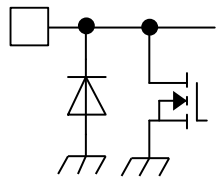
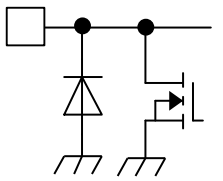
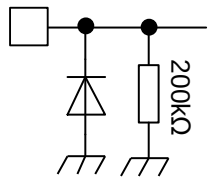
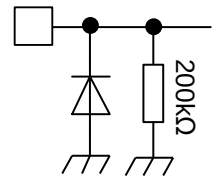
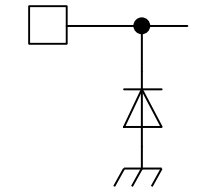
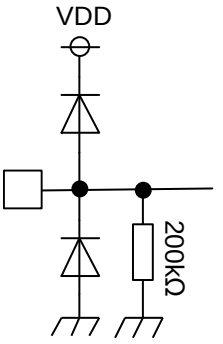
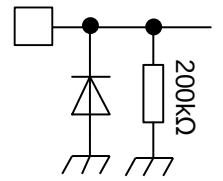
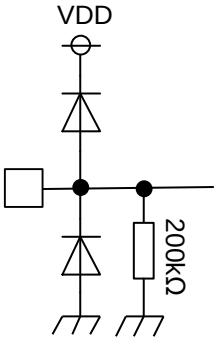
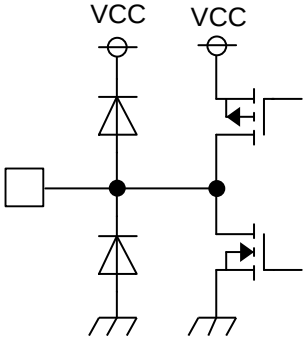
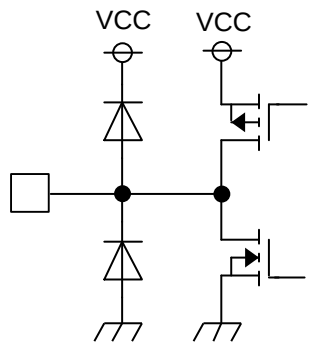
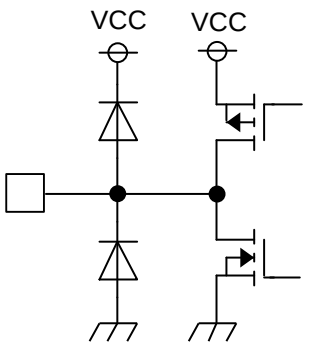
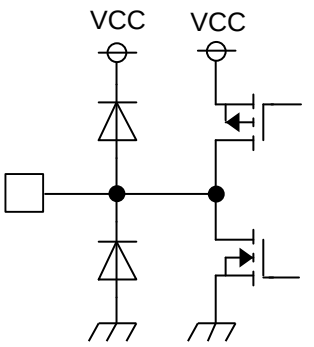


Figure 36. Application Chart (TOP VIEW)

I/O Equivalence Circuit

2. A0	3. A1	4. A2
		
5. SDA	6. SCL	7. EN
		
8. EN_AR	9. VDD	10. SLAVE/AR
		
11. SEL	12. TEST	15. OUT11
		

I/O Equivalence Circuit - continued

16. OUT10	17. OUT9	18. OUT8
		
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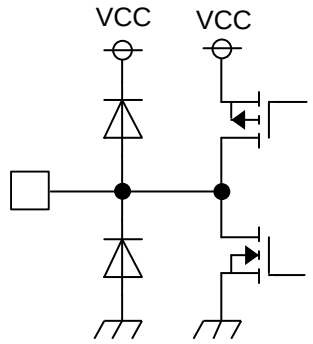
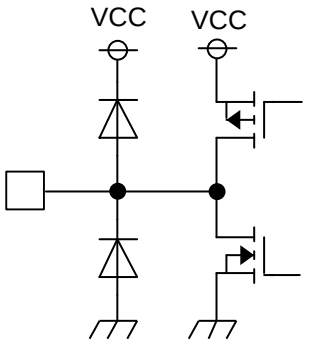
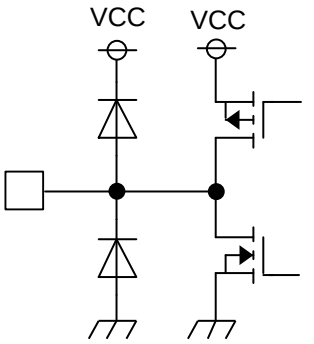
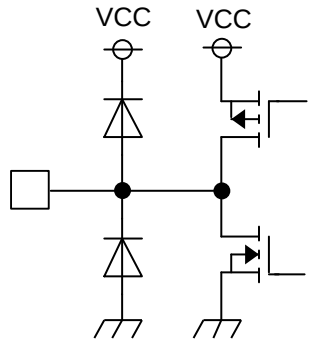
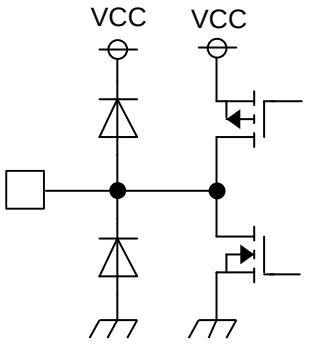
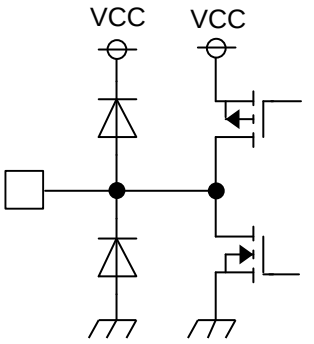
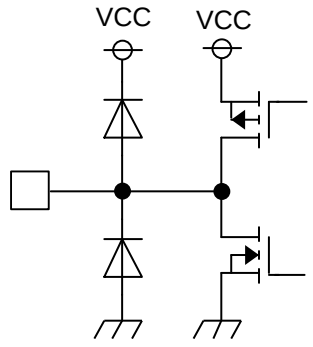
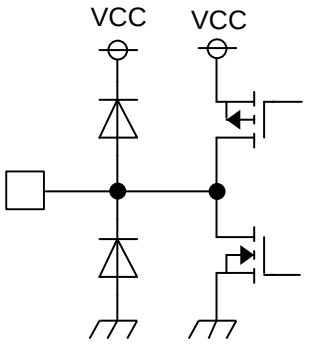
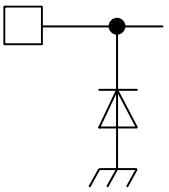
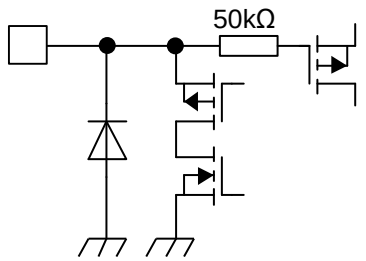
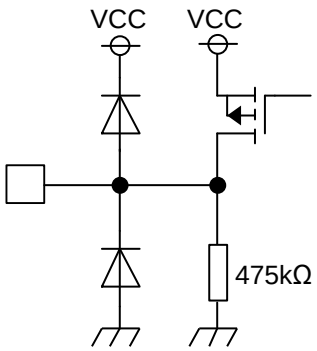
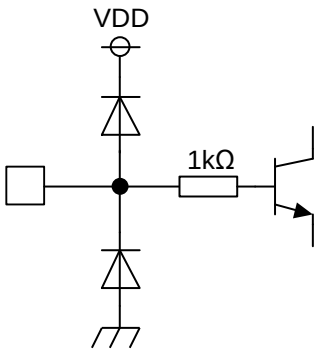
		
22. OUT4	23. OUT3	24. OUT2
		
25. OUT1	26. OUT0	28. VCC
		

I/O Equivalence Circuit - continued

30. REFIN	31. VDAC	32. FB
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

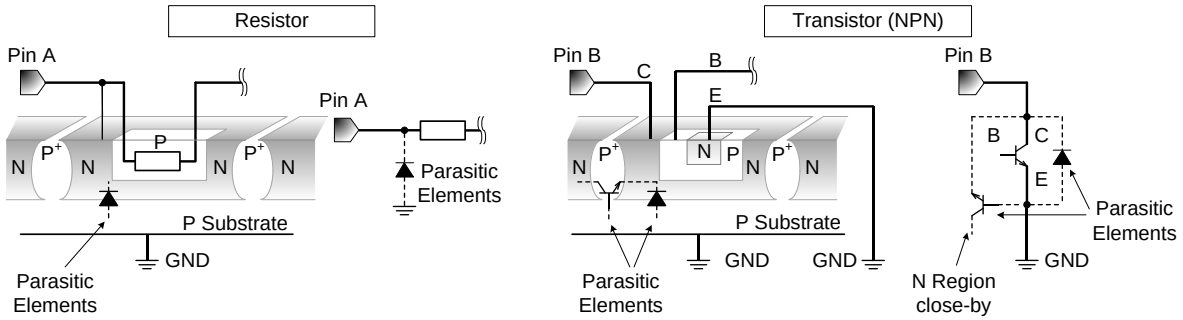


Figure 37. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

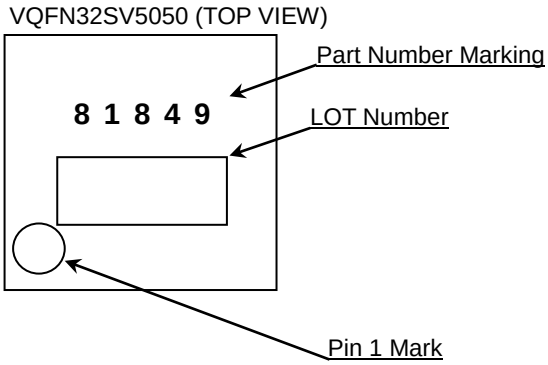
B D 8 1 8 4 9 M U V	-	CE2

Part Number

Package
MUV:VQFN32SV5050

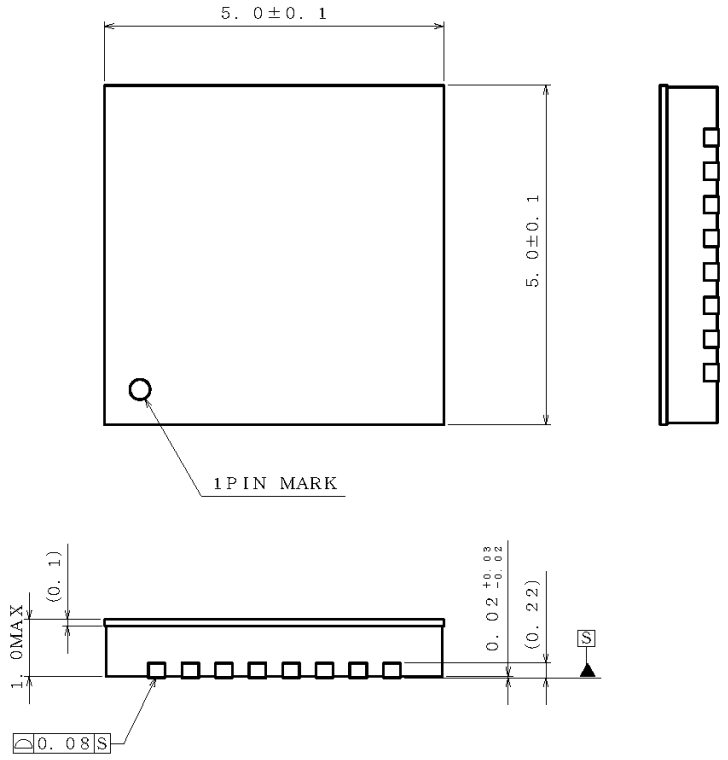
Product Rank
C: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

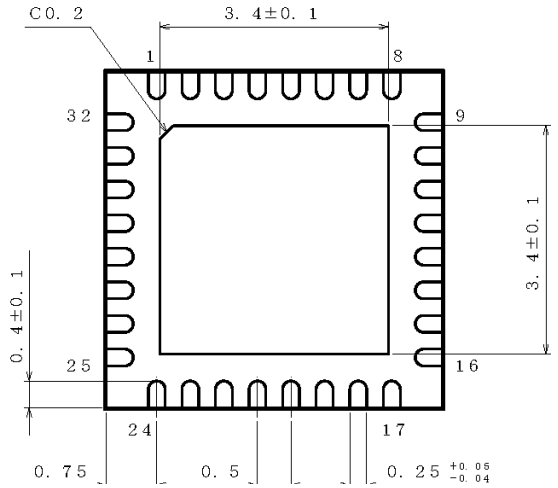
Marking Diagram



Physical Dimension and Packing Information

Package Name	VQFN32SV5050



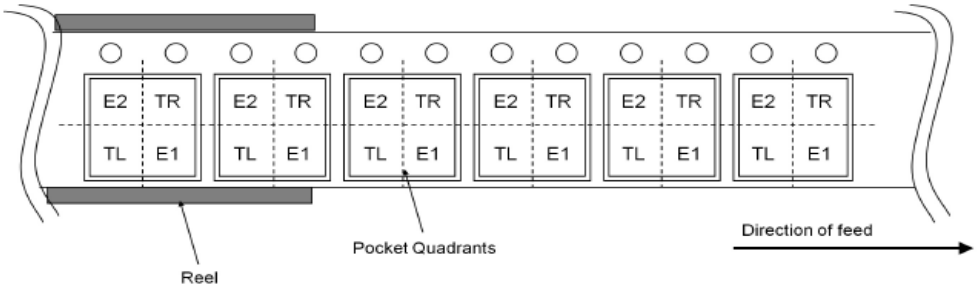


(UNIT : mm)

PKG : VQFN32SV5050
Drawing No. EX385−5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
6.Jul.2017	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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