

Product introduction

SN74LVC1G00 is a 2-input NAND integrated circuit, which can realize the mathematical logic operation of $Y = \overline{A+B}$ and $Y = \overline{A*B}$. Advanced CMOS process design is adopted, which has the working characteristics of low power consumption and high output driving capability. The chip can work normally when the power supply voltage VCC is between 1.65V and 5.5V V. And 74LVC1G00 has a variety of small package shapes, It can be widely used in high-end precision instruments, miniaturized low-power handheld devices, artificial intelligence and other fields.

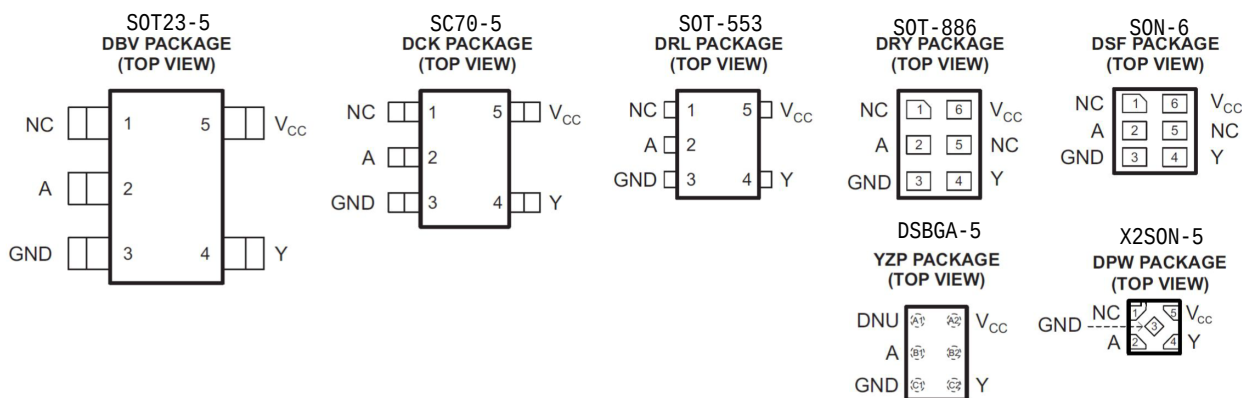
Product features

- Low input current: 0.1uA typical
- Low static power consumption: 0.1uA typical
- High output drive: VCC=4.5V, more than 32MA
- Wide working voltage range: 1.65V to 5.5V
- Package form: DBV/DCK/DRL/YZP/ DRY/DSF/ DPW

product usage

- Portable audio interface
- digital television
- Wireless headphones, smart watches, etc.
- Blu-ray player and home theater
- Solid state drive
- Smart wearable devices

Package form and pin function definition



	Pin				
Name	DBV/ DCK/ DRL	DRY/DSF	YZP	DPW	Description
NC	1	1,5	A1, B2	1	Empty foot
A	2	2	B1	2	Input
GND	3	3	C1	3	Power supply ground
Y	4	4	C2	4	Output
VCC	5	6	A2	5	Power supply positive

Note: NC null pin, no connecting wire inside.

Limit parameter

parameter	symbol	limit value	unit
operating voltage	V_{CC}	6.5	V
input	V_{IN}	-0.5~6.5	V
Output voltage (1)	V_{OUT}	-0.5~6.5	V
Single pin output current	I_{OUT}	25	mA
Or V_{CC} current.	I_{CC}	50	mA
Storage temperature	T_S	-65~150	°C
Pin welding temperature	T_W	260, 10s	°C

Note: 1. In the power-off state of $V_{CC}=0V$, the limit voltage that the output can bear,

2. Limit parameter refers to the limit value that can't be exceeded under any conditions. If it exceeds this limit value, it may cause physical damage such as product deterioration; At the same time, the chip can't work normally when it is close to the limit parameters.

Principle logic diagram



truth table

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

working conditions

project	symbol	test condition	minimum value	typical value	maximum	unit
operating voltage	VC	—	1.65	—	5.5	V
Input high level voltage	VHI	$VC = 1.65V \sim 1.95V$	$0.65 * VC$	—	—	V
		$VC = 2.3V \sim 2.7V$	1.7V	—	—	
		$VC = 3V \sim 5.5V$	$0.7 * VC$	—	—	
Input high level voltage	VHI	$VC = 1.65V \sim 1.95V$	—	—	$0.35 * VC$	V
		$VC = 2.3V \sim 2.7V$	—	—	0.7	
		$VC = 3V \sim 5.5V$	—	—	$0.3 * VC$	
input voltage	VI	—	0	—	5.5	V
Output voltage	VO	—	0	—	VC	V
High level output current	IOH	$VC = 1.65V$	—	—	-4	mA
		$VC = 2.3V$	—	—	-8	
		$VC = 3V$	—	—	-16	
		$VC = 4.5V$	—	—	-32	
Low level output current	IOL	$VC = 1.65V$	—	—	4	mA
		$VC = 2.3V$	—	—	8	
		$VC = 3V$	—	—	16	
		$VC = 4.5V$	—	—	32	

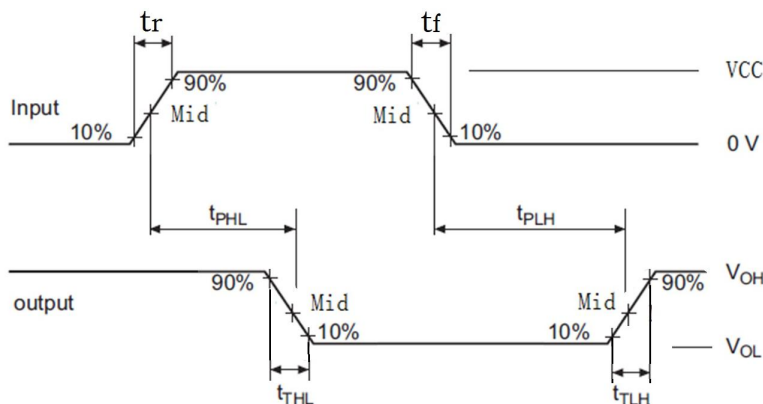
Electrical characteristics

Electrical characteristics of DC: $T_j=25^{\circ}\text{C}$

project	symbol	test condition	V	typical value	maximum	unit
High level load voltage	V_{OH}	$I_{OH} = -100\mu\text{A}$	$1.65\text{V} \sim 5.5\text{V}$	1.64	—	V
		$I_{OH} = -4\text{ mA}$	1.65V	1.47	—	
		$I_{OH} = -8\text{ mA}$	2.3V	2.15	—	
		$I_{OH} = -16\text{ mA}$	3V	2.73	—	
		$I_{OH} = -32\text{ mA}$	4.5V	4.0	—	
Low level load voltage	V_{OL}	$I_{OH} = 100\mu\text{A}$	$1.65\text{V} \sim 5.5\text{V}$	0.01	—	V
		$I_{OH} = 4\text{ mA}$	1.65V	0.11	—	
		$I_{OH} = 8\text{ mA}$	2.3V	0.11	—	
		$I_{OH} = 16\text{ mA}$	3V	0.2	—	
		$I_{OH} = 32\text{ mA}$	4.5V	0.35	—	
incoming current	I_I	$V_I = 5.5\text{V}$ 或 GND	$0 \sim 5.5\text{V}$	0.01	± 5	uA
				0.01	± 5	
Turn-off current	I_{OFF}	$V_I = 5.5\text{V}$	0	0.01	± 10	uA
		$V_O = 5.5\text{V}$	0	0.01	± 10	
operational current	I_{CC}	$V_I = 5.5\text{V}, I_O = 0$	$1.65\text{V} \sim 5.5\text{V}$	0.01	10	uA
		$V_I = \text{GND}, I_O = 0$		0.01	10	
Working current variation value	ΔI_{CC}	$A = V_{CC} - 0.6\text{V}$	$3\text{V} \sim 5.5\text{V}$	25	—	uA
		$B = V_{CC}$ 或 GND				
		$B = V_{CC} - 0.6\text{V}$		25	—	uA
		$A = V_{CC}$ 或 GND				uA

Ac electrical characteristics: $T_a=25^{\circ}\text{C}$ $V(298)=5.0\text{V}$, $t_r \leq 20\text{ns}$. See test method.

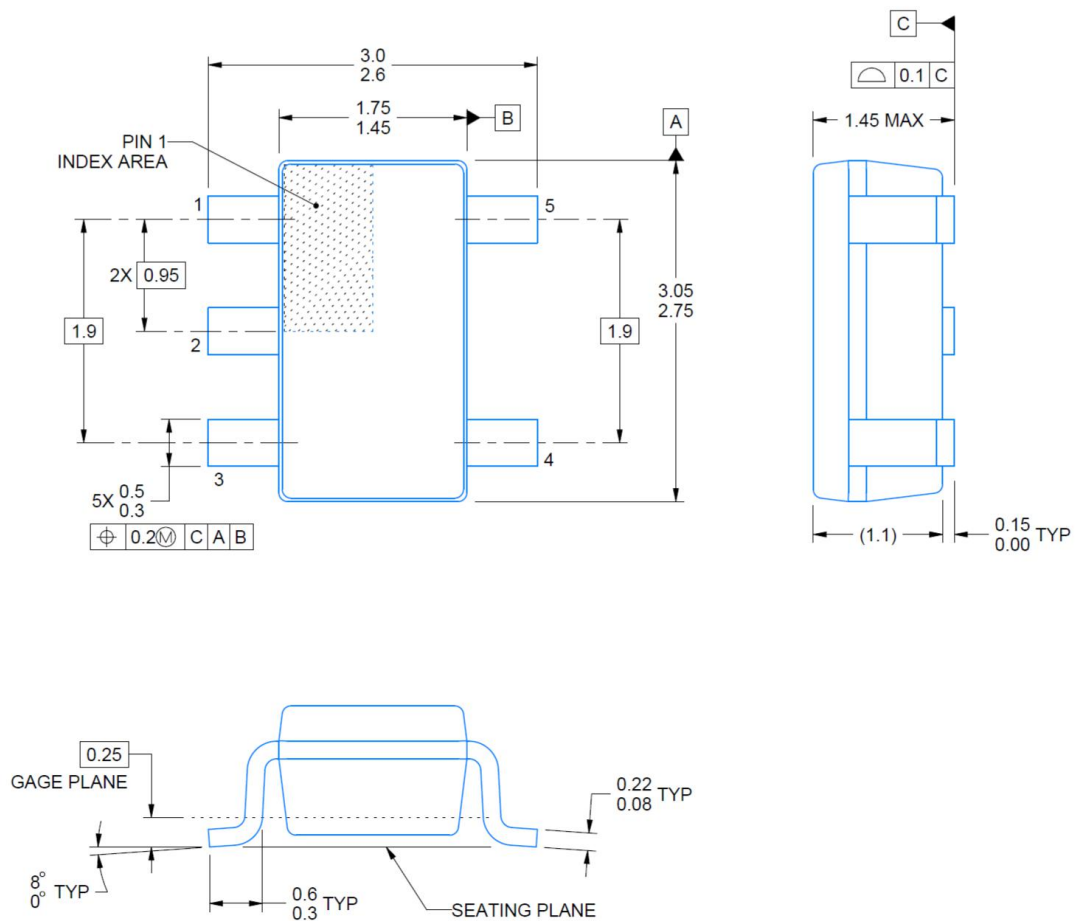
project	symbol	test condition	minimum value	typical value	maximum	unit
Maximum transmission delay time a, B to Y		$C = 15\text{pF}$	—	10	—	ns
		$C = 15\text{pF}$	—	10	—	ns



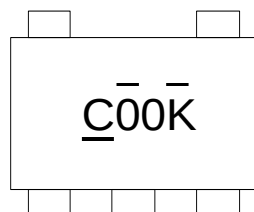
- Note: 1. CL capacitor is external chip capacitor (0603), which is connected close to the output pin, and the capacitor ground is close to the chip GND;
 2. Input: port input level, $f=500\text{kHz}$, $D=50\%$; $t_r=t_f \leq 20\text{ns}$;
 3. Output: Y-terminal output test.

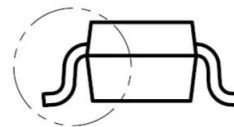
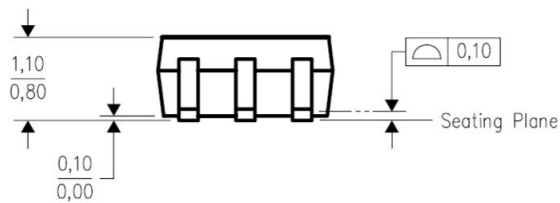
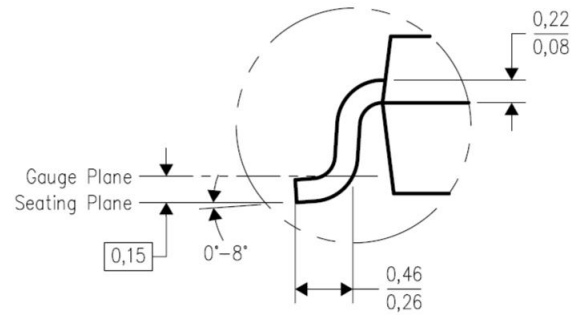
■ Encapsulated information

DBV (SOT23-5)



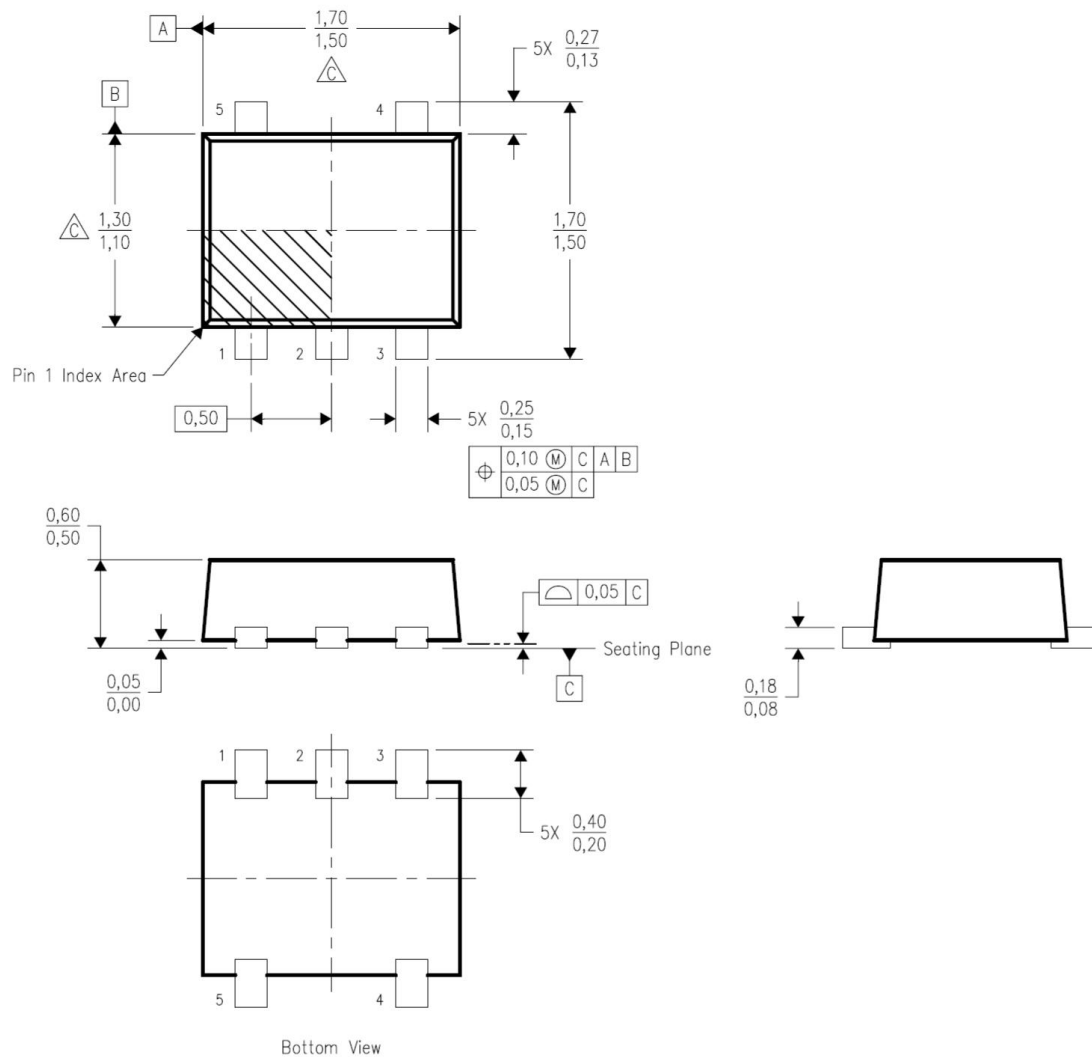
■ Marking



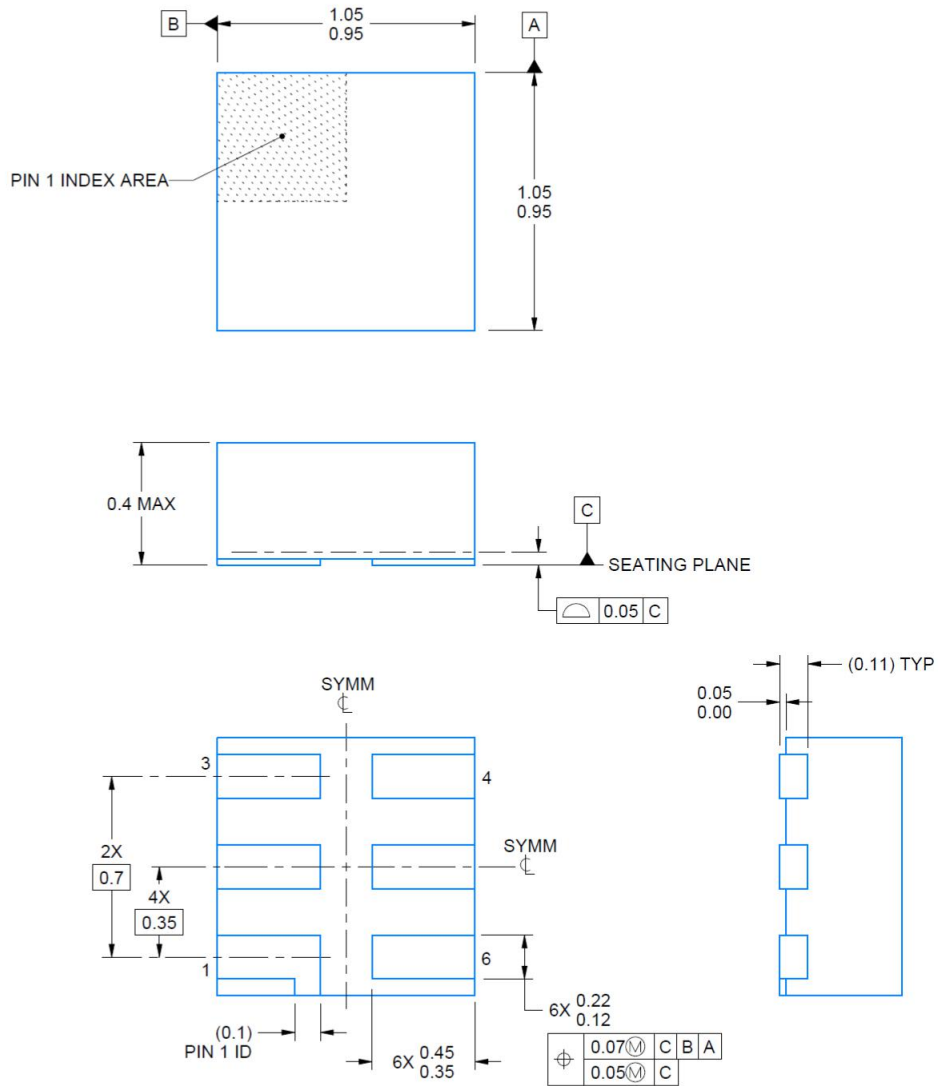
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A diagram of a 5-bit shift register. It consists of a horizontal rectangle with five input pins on the left and five output pins on the right. The inputs are labeled A, B, C, D, and E from top to bottom. The outputs are labeled F, G, H, I, and J from top to bottom. The register is shown in a state where the output J is 1 and all other outputs are 0.

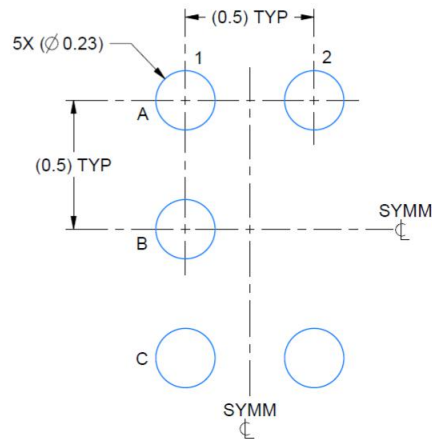
DRL (SOT-553)



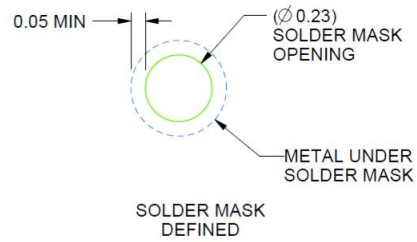
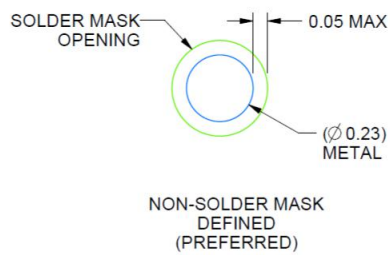
DSF (SON-6)



YZP (DSBGA-5)



LAND PATTERN EXAMPLE
SCALE:40X



DPW (X2SON-4)

