2ED020I06-FI

Dual IGBT Driver IC

April 2010

Power Managment & Drives

Never stop thinking.

2ED020I06-FI
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Previous Version:

Page	Subjects (major changes since last revision)

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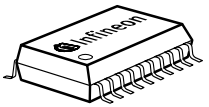
Dual IGBT Driver IC
2ED020I06-FI



PG-DSO-18-2

Product Highlights

- Fully opera tional to ±650V
- Power supply operating range from 14 to 18 V
- Gate drive currents of +1 A / –2 A
- Matched propagation delay for both channels
- High dV/dt immunity
- Low power consumption

Features

- Floating high side driver
- Undervoltage lockout for both channels
- 3.3 V and 5 V TTL compatible inputs
- CMOS Schmitt-triggered inputs with pull-down
- Non-inverting inputs
- Interlocking inputs
- Dedicated shutdown input with pull-up
- RoHS compliant

Type	Ordering Code	Package	Packaging
2ED020I06-FI		PG-DSO-18-2	Tape&Reel

1 Overview

The 2ED020I06-FI is a high voltage, high speed power MOSFET and IGBT driver with interlocking high and low side referenced outputs. The floating high side driver may be supplied directly or by means of a bootstrap diode and capacitor. In addition to the logic input of each driver the 2ED020I06-FI is equipped with a dedicated shutdown input. All logic inputs are compatible with 3.3 V and 5 V TTL. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. Both drivers are designed to drive an N-channel power MOSFET or IGBT which operate up to 650V.

2 Pin Configuration and Functionality

2.1 Pin Configuration

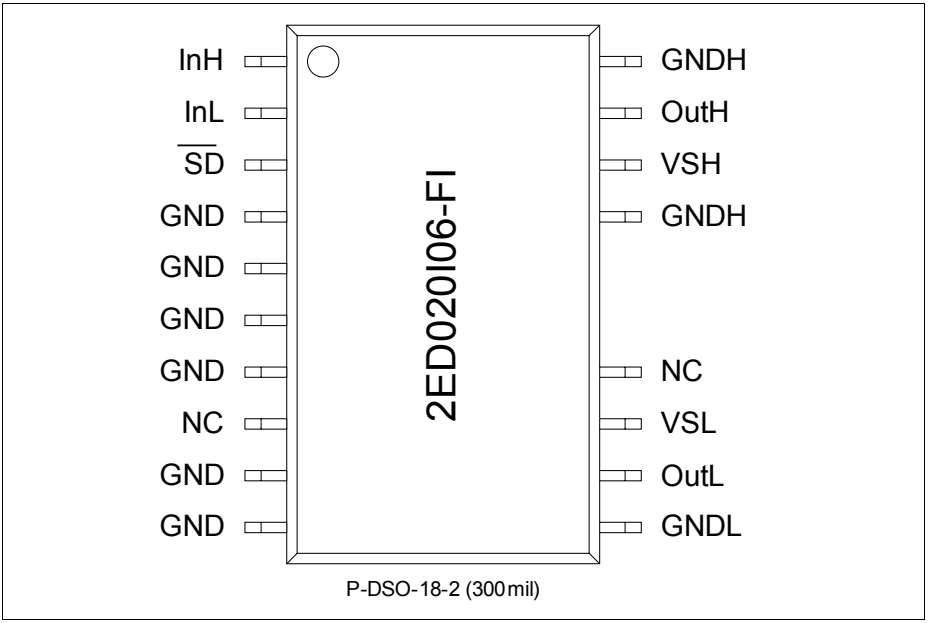


Figure 1 Pin Configuration (top view)

2.2 Pin Definitions and Functions

Pin	Symbol	Function
1	InH	Logic input for high side driver
2	InL	Logic input for low side driver
3	$\overline{SD}$	Logic input for shutdown of both drivers
4	GND	Common ground
5	GND	Connect to GND
6	GND	Connect to GND
7	GND	Connect to GND
8	n.c.	Do not connect, Pin must stay open

Table 1 Pin Description

Pin	Symbol	Function
9	GND	Connect to GND
10	GND	Connect to GND
11	GNDL	Low side power ground [1)]
12	OutL	Low side gate driver output
13	VSL	Low side supply voltage
14	n.c.	(not connected)
15	n.e.	(not existing)
16	n.e.	(not existing)
17	GNDH	High side (power) ground
18	VSH	High side supply voltage
19	OutH	High side gate driver output
20	GNDH	High side (power) ground

Table 1 Pin Description (cont'd)

1) Please note : GNDL has to be connected directly to GND

3 Block Diagram

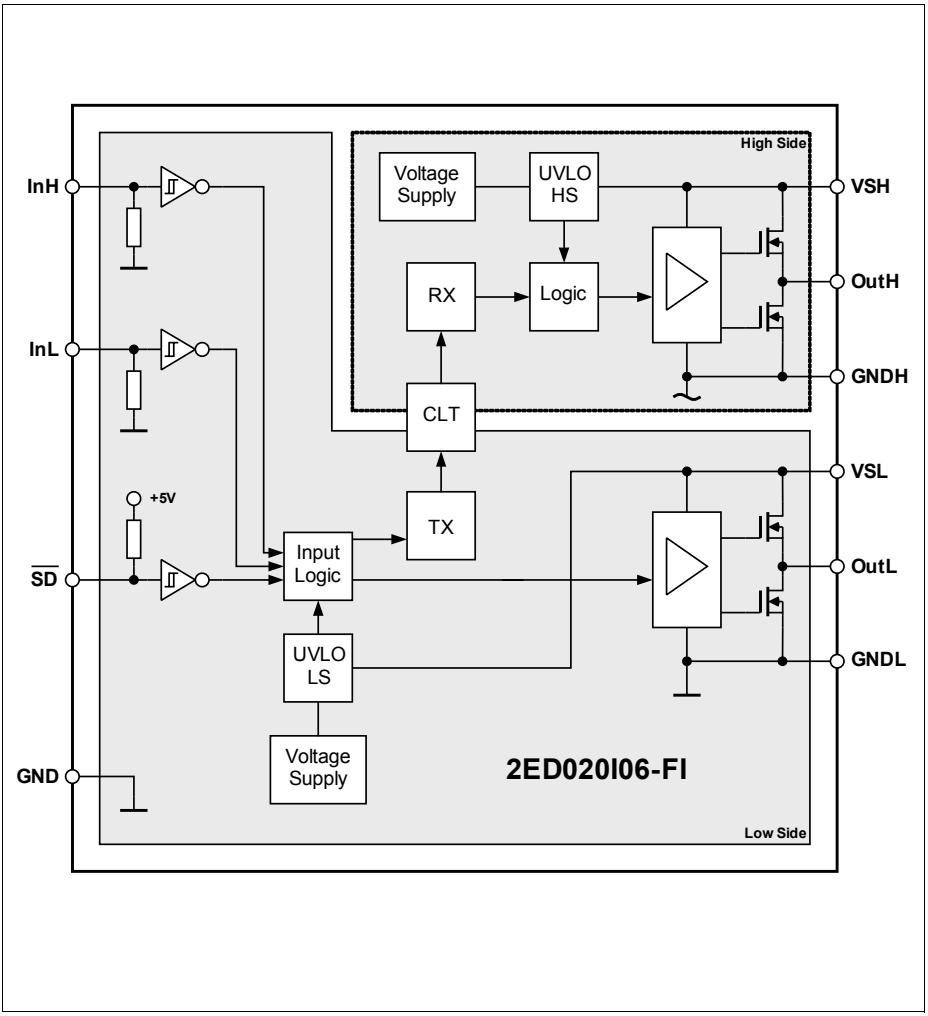


Figure 2 Block Diagram

4 Functional Description

4.1 Power Supply

The power supply of both sides, “VSL” and “VSH”, is monitored by an undervoltage lockout block (UVLO) which enables operation of the corresponding side when the supply voltage reaches the “on” threshold. Afterwards the internal voltage reference and the biasing circuit are enabled. When the supply voltage (VSL, VSH) drops below the “off” threshold, the circuit is disabled.

4.2 Logic Inputs

The logic inputs InH, InL and $\overline{SD}$ are fed into Schmitt-Triggers with thresholds compatible to 3.3V and 5V TTL. When $\overline{SD}$ is enabled (low), InH and InL are disabled. If InH is high (while InL is low), OutH is enabled and vice versa. However, if both signals are high, they are internally disabled until one of them gets low again. This is due to the interlocking logic of the device. See Figure 3 (section 4.7).

4.3 Gate Driver

2ED020I06-FI features two hard-switching gate drivers with N-channel output stages capable to source 1A and to sink 2A peak current. Both drivers are equipped with active-low-clamping capability. Furthermore, they feature a large ground bounce ruggedness in order to compensate ground bounces caused by a turn-off of the driven IGBT.

4.4 Coreless Transformer (CLT)

In order to enable signal transmission across the isolation barrier between low-side and high-side driver, a transformer based on CLT-Technology is employed. Signals, that are to be transmitted, are specially encoded by the transmitter and correspondingly restored by the receiver. In this way EMI due to variations of GNDH (dV_{GNDH}/dt) or the magnetic flux density (dH/dt) can be suppresed.To compensate the additional propagation delay of transmitter, level shifter and receiver, a dedicated propagation delay is introduced into the low-side driver.

4.5 Diagrams

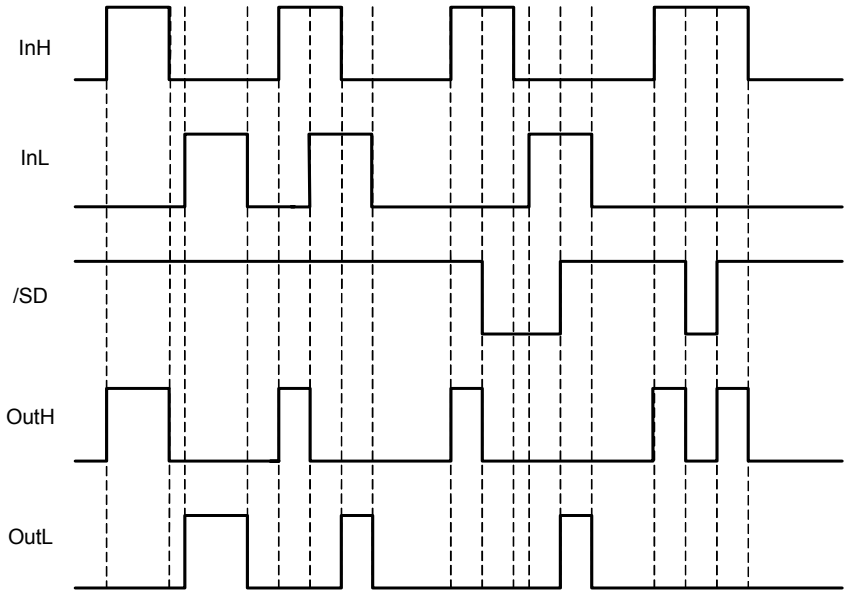


Figure 3 Input/Output Timing Diagram

5 Electrical Parameters

5.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
High side ground	GNDH	−650	650	V	
High side supply voltage	VSH	−0.3	20	V	1)
High side gate driver output	OutH	−0.3	VSH + 0.3	V	1)
Low side ground	GNDL	−0.3	5.3	V	
Low side supply voltage	VSL	−0.3	20	V	2)
Low side gate driver output	OutL	−0.3	VSL + 0.3	V	3)
Logic input voltages (InH, InL, $\overline{SD}$)	V_{IN}	−0.3	5.3	V	
High side ground, voltage transient	dV_{GNDH}/dt	−50	50	V/ns	
ESD Capability	V_{ESD}	—	2	kV	4)Human Body Model
Package power disipation @T_A = 25°C	P_D	—	1.4	W	5)
Thermal resistance (both chips active), junction to ambient	R_{THJA}	—	90	K/W	6)
Thermal resistance (high side chip), junction to ambient	$R_{THJA(HS)}$	—	110	K/W	6)
Thermal resistance (low side chip), junction to ambient	$R_{THJA(LS)}$	—	110	K/W	6)
Junction temperature	T_J	—	150	°C	
Storage temperature	T_S	−55	150	°C	

1) With reference to high side ground GNDH.

2) With respect to both GND and GNDL.

3) With respect to GNDL.

4) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor).

5) Considering Rth(both chips active)=90K/W

6) Device soldered to reference PCB without cooling area

5.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.Unless otherwise noted all parameters refer to GND.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
High side ground	GNDH	–650	650	V	
High side supply voltage	VSH	14	18	V	1)
Low side supply voltage	VSL	14	18	V	2)
Logic input voltages (InH, InL, $\overline{SD}$)	V_{IN}	0	5	V	
Junction temperature	T_J	–40	105	°C	Industrial applications, useful lifetime 87600h
Junction temperature	T_J	–40	125	°C	Other applications, useful lifetime 15000h

1) With reference to high side ground GNDH.

2) With respect to both GND and GNDL.

5.3 Electrical Characteristics

Note: The electrical characteristics involve the spread of values for the supply voltages, load and junction temperature given below. Typical values represent the median values, which are related to production processes. Unless otherwise noted all voltages are given with respect to ground (GND). VSL = VSH – GNDH = 15 V, C_L = 1 nF, T_A = 25 °C. Positive currents are assumed to be flowing into pins.

Voltage Supply

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ	max.		
High side leakage current	I_{GNDH}	—	0	—	µA	GNDH = 1.2 kV GNDL = 0 V

Voltage Supply (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ	max.		
High side quiescent supply current	I_{VSH}	—	2.4	3.2	mA	VSH = 15 V[1]
		—	2.3	3.2	mA	VSH = 15 V[1] T_J = 125 °C
High side undervoltage lockout, upper threshold	V_{VSH}[1]	10.9	12.2	13.5	V	
High side undervoltage lockout, lower threshold	V_{VSH}[1]	—	11.2	—	V	
High side undervoltage lockout hysteresis	ΔV_{VSH}	0.7	1	1.3	V	
Low side quiescent supply current	I_{VSL}	—	3.9	5.0	mA	VSL = 15 V
			3.9	5.5	mA	VSL = 15 V T_J = 125 °C
Low side undervoltage lockout, upper threshold	V_{VSL}	10.7	12	13.3	V	
Low side undervoltage lockout, lower threshold	V_{VSL}	—	11	—	V	
Low side undervoltage lockout hysteresis	ΔV_{VSL}	0.7	1	1.3	V	

[1] With reference to high side ground GNDH.

Logic Inputs

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ	max.		
Logic "1" input voltages (InH, InL, $\overline{SD}$)	V_{IN}	2	—	—	V	
Logic "0" input voltages (InH, InL, $\overline{SD}$)	V_{IN}	—	—	0.8	V	
Logic "1" input currents (InH, InL)	I_{IN}	—	40	55	µA	V_{IN} = 5 V
Logic "0" input currents (InH, InL)	I_{IN}	—	0	—	µA	V_{IN} = 0 V

Logic Inputs (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ	max.		
Logic "1" input currents ($\overline{SD}$)	I_{IN}	—	0	—	µA	V_{IN} = 5V
Logic "0" input currents ($\overline{SD}$)	I_{IN}	–60	–40	—	µA	V_{IN} = 0V

Gate Drivers

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ	max.		
High side high level output voltage	$V_{VSH} - V_{OutH}$	—	1.4	1.7	V	I_{OutH} = –1mA V_{InH} = 5V
High side low level output voltage	V_{OutH} [1)]	—	—	0.1	V	I_{OutH} = 1mA V_{InH} = 0V
Low side high level output voltage	$V_{VSL} - V_{OutL}$	—	1.4	1.7	V	I_{OutL} = –1mA V_{InL} = 5V
Low side low level output voltage	V_{OutL}	—	—	0.1	V	I_{OutL} = 1mA V_{InL} = 0V
Output high peak current (OutL, OutH)	I_{Out}	—	—	–1	A	V_{IN} = 5V V_{Out} = 0V
Output low peak current (OutL, OutH)	I_{Out}	2	—	—	A	V_{IN} = 0V V_{Out} = 15V
High side active low clamping	V_{OutH} [1)]	—	2.6	3	V	InH =0V, VSH open I_{OutH} =200mA
		—	2.7	3.2	V	InH =0V, VSH open I_{OutH} =200mA T_J = 125 °C
Low side active low clamping	V_{OutL}	—	2.6	3	V	InL =0V, VSL open I_{OutL} =200mA
		—	2.7	3.2	V	InL =0V, VSL open I_{OutL} =200mA T_J = 125 °C

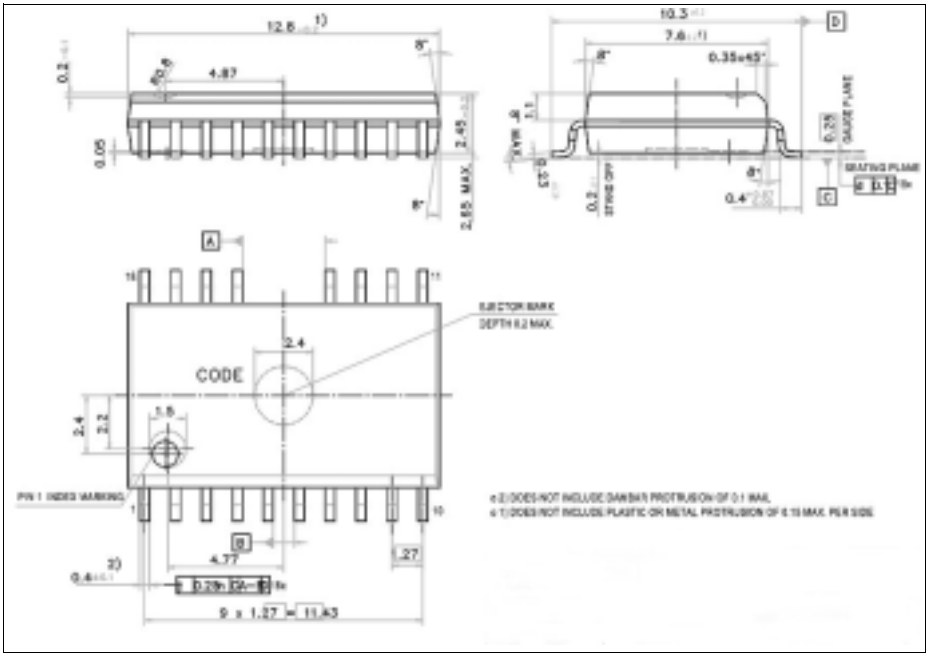
1) With reference to high side ground GNDH.

Dynamic Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ	max.		
Turn-on propagation delay	t_{ON}	—	85	105	ns	GNDH = 0 V 20% V_{out}
		—	95	120	ns	GNDH = 0 V 20% V_{out} T_J = 125 °C
Turn-off propagation delay	t_{OFF}	—	85	115	ns	80% V_{out}
		—	100	130	ns	80% V_{out} T_J = 125 °C
Shutdown propagation delay	t_{SD}	—	85	115	ns	80% V_{out}
		—	100	130	ns	80% V_{out} T_J = 125 °C
Turn-on rise time	t_r	—	20	40	ns	20% to 80% V_{out}
		—	30	50	ns	20% to 80% V_{out} T_J = 125 °C
Turn-off fall time	t_f	—	20	35	ns	80% to 20% V_{out}
		—	25	40	ns	80% to 20% V_{out} T_J = 125 °C
Delay mismatch (high & low side turn-on/off)	Δt	—	15	25	ns	T_J = 25°C see Figure 6
		—	15	30	ns	T_J = 125°C see Figure 6
Minimum turn-on input (InH, InL) pulse width	t_{pON}	—	50	75	ns	[1]
		—	55	80	ns	[1] T_J = 125°C
Minimum turn-off input (InH, InL) pulse width	t_{pOFF}	—	50	75	ns	[1]
		—	55	80	ns	[1] T_J = 125 °C

[1] InH-Pulses shorter than the “minimum turn-on(off) input pulse width” are prolonged to 50ns (See Figure 7). InL-Input doesn´t have this feature.

6 Package Outline



Note: dimensions are given in mm.

6.1 Soldering Profile

The soldering profile qualified for 2ED020I06-FI (according to the standard IPC/JEDEC J-STD-020C) is moisture sensitivity level 3. The peak reflow temperature for its package (volume < 350 mm^3) is 260 +0/-5 °C.

7 Diagrams

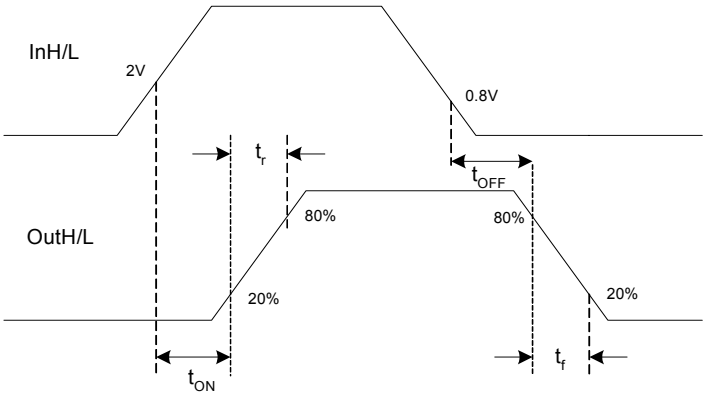


Figure 4 **Switching Time Waveform Definition**

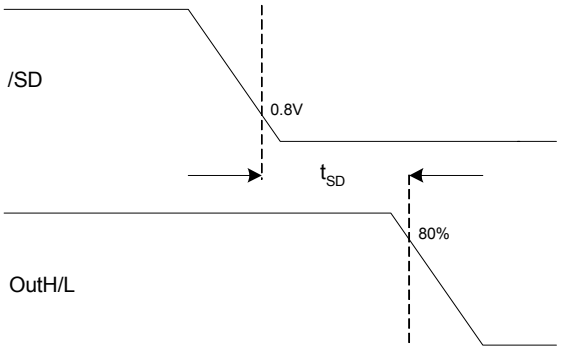
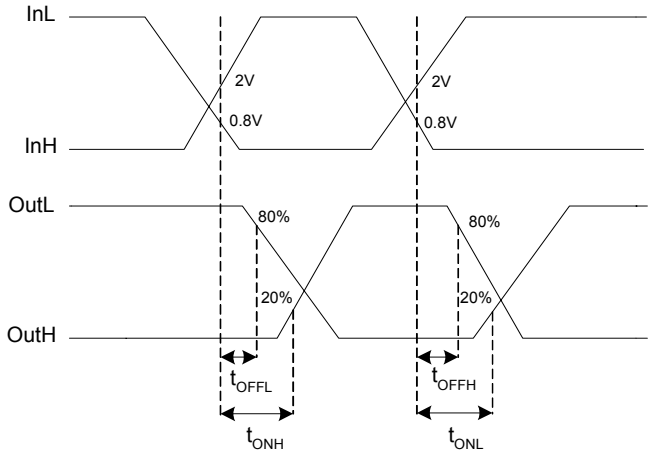


Figure 5 ***Shutdown Waveform Definition***



$\Delta t = \max (|t_{ONH} - t_{OFFL}| , |t_{OFFH} - t_{ONL}|)$

Figure 6 Delay Matching Waveform Definitions

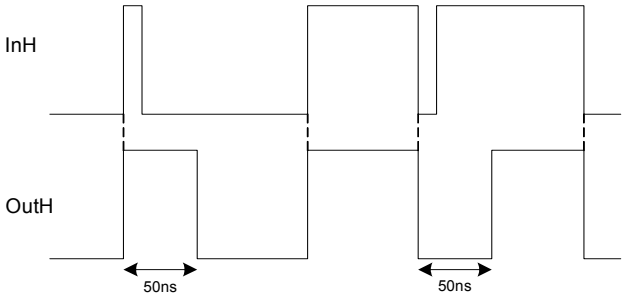


Figure 7 Short InH-Pulses Prolongation

8 Application Advices

8.1 Power Supply

a) The connection of a capacitor (>10nF) as close as possible to the supply pins VSH, VSL is recommended for avoiding that possible oscillations in the supply voltage can cause erroneous operation of the output driver stage. Total value of capacitance connected to the supply terminals has to be determined by taking into account gatecharge, peak current, supply voltage and kind of power supply.

b) If a bootstrap power supply for the high side driver is applied, a resistor of 10Ω minimum in series with the bootstrap diode is required.

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