# SNx4HC573A Octal Transparent D-Type Latches With 3-State Outputs

## 1 Features

- Wide Operating Voltage Range from 2 V to 6 V
- High-Current 3-State Outputs Drive Bus Lines Directly up to 15 LSTTL Loads
- Low Power Consumption: 80-µA Maximum $I_{CC}$
- Typical $t_{pd}$ = 21 ns
- ±6-mA Output Drive at 5 V
- Low Input Current: 1 µA (Maximum)
- Bus-Structured Pinout

## 2 Applications

- Buffer Registers
- Bidirectional Bus Drivers
- Working Registers

## 3 Description

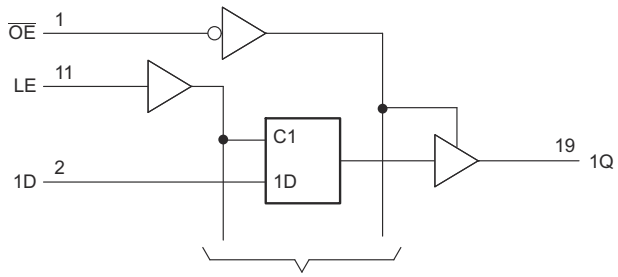
The SNx4HC573A devices are octal transparent D-type latches that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN54HC573AJ | CDIP (20) | 26.92 mm × 6.92 mm |
| SN54HC573AW | CFP (20) | 13.72 mm × 6.92 mm |
| SN54HC573AFK | LCCC (20) | 8.89 mm × 8.89 mm |
| SN74HC573AN | PDIP (20) | 25.40 mm × 6.35 mm |
| SN74HC573ADW | SOIC (20) | 12.80 mm × 7.50 mm |
| SN74HC573ADB | SSOP (20) | 7.20 mm × 5.30 mm |
| SN74HC573APW | TSSOP (20) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.






**Logic Diagram (Positive Logic)**

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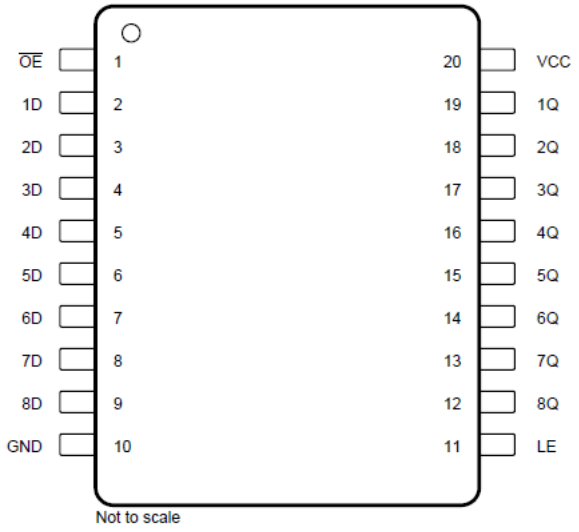
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

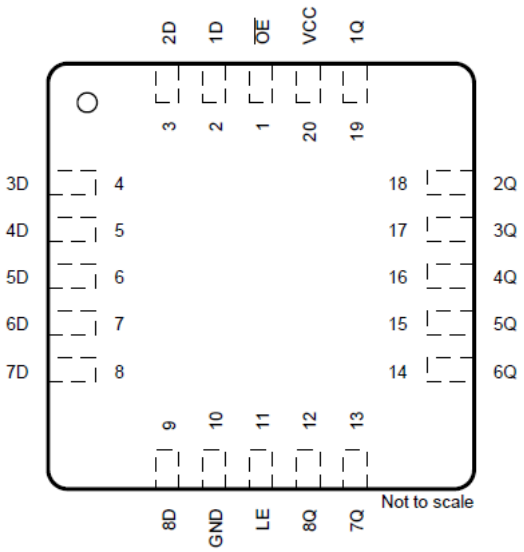
| Changes from Revision E (September 2003) to Revision F (October 2016) | Page |
|---|---|
| • Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Deleted Ordering Information table; see POA at the end of the data sheet | 1 |
| • Changed Package thermal impedance, $R_{\theta JA}$, values from 70 to 92.5 (DB), from 58 to 78.3 (DW), from 69 to 49.1 (N), and from 83 to 101.1 (PW) | 5 |

| Changes from Revision F (October 2016) to Revision G (April 2022) | Page |
|---|---|
| • Updated ESD ratings table to modern TI standards | 4 |
| • Changed Package thermal impedance, $R_{\theta JA}$, values from 92.5 to 122.7 (DB), from 78.3 to 109.1 (DW), from 49.1 to 84.6 (N), and from 101.1 to 131.8 (PW) | 5 |

## 5 Pin Configuration and Functions




**DB, DW, J, N, PW, or W Packages**
**20-Pin SSOP, SOIC, CDIP, PDIP, TSSOP, or CFP**
**Top View**




**FK Package**
**20-Pin LCCC**
**Top View**

### Pin Functions

| PIN | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | $\overline{OE}$ | I | Output enable |
| 2 | 1D | I | 1D input |
| 3 | 2D | I | 2D input |
| 4 | 3D | I | 3D input |
| 5 | 4D | I | 4D input |
| 6 | 5D | I | 5D input |
| 7 | 6D | I | 6D input |
| 8 | 7D | I | 7D input |
| 9 | 8D | I | 8D input |
| 10 | GND | — | Ground |
| 11 | LE | I | Latch enable input |
| 12 | 8Q | O | 8Q output |
| 13 | 7Q | O | 7Q output |
| 14 | 6Q | O | 6Q output |
| 15 | 5Q | O | 5Q output |
| 16 | 4Q | O | 4Q output |
| 17 | 3Q | O | 3Q output |
| 18 | 2Q | O | 2Q output |
| 19 | 1Q | O | 1Q output |
| 20 | $V_{CC}$ | — | Power pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±3500 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | |
| | | $V_{CC}$ = 6 V | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | |
| | | $V_{CC}$ = 6 V | | | 1.8 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $t_t$ | Input transition (rise and fall) time | $V_{CC}$ = 2 V | | | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | | | 500 | |
| | | $V_{CC}$ = 6 V | | | 400 | |
| $T_A$ | Operating free-air temperature | SN54HC573A | –55 | | 125 | °C |
| | | SN74HC573A | –40 | | 85 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report (SCBA004).

## 6.4 Thermal Information

| THERMAL METRIC | | SN74HC573A | | | | UNIT |
|---|---|---|---|---|---|---|
| | | DW (SOIC) | DB (SSOP) | N (PDIP) | PW (TSSOP) | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance[1] | 109.1 | 122.7 | 84.6 | 131.8 | °C/W |
| $R_{\theta JC\ (top)}$ | Junction-to-case (top) thermal resistance | 76 | 81.6 | 72.5 | 72.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 77.6 | 77.5 | 65.3 | 82.8 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 51.5 | 46.1 | 55.3 | 21.5 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 77.1 | 77.1 | 65.2 | 82.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 µA | $V_{CC}$ = 2 V | 1.9 | 1.998 | | V |
| | | | $V_{CC}$ = 4.5 V | 4.4 | 4.499 | | |
| | | | $V_{CC}$ = 6 V | 5.9 | 5.999 | | |
| | | $I_{OH}$ = –6 mA, $V_{CC}$ = 4.5 V | $T_A$ = 25°C | 3.98 | 4.3 | | |
| | | | SN54HC573A | 3.7 | | | |
| | | | SN74HC573A | 3.84 | | | |
| | | $I_{OH}$ = –7.8 mA, $V_{CC}$ = 6 V | $T_A$ = 25°C | 5.48 | 5.8 | | |
| | | | SN54HC573A | 5.2 | | | |
| | | | SN74HC573A | 5.34 | | | |
| $V_{OL}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | $V_{CC}$ = 2 V | | 0.002 | 0.1 | V |
| | | | $V_{CC}$ = 4.5 V | | 0.001 | 0.1 | |
| | | | $V_{CC}$ = 6 V | | 0.001 | 0.1 | |
| | | $I_{OL}$ = 6 mA, $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 0.17 | 0.26 | |
| | | | SN54HC573A | | | 0.4 | |
| | | | SN74HC573A | | | 0.33 | |
| | | $I_{OL}$ = 7.8 mA, $V_{CC}$ = 6 V | $T_A$ = 25°C | | 0.15 | 0.26 | |
| | | | SN54HC573A | | | 0.4 | |
| | | | SN74HC573A | | | 0.33 | |
| $I_I$ | $V_I = V_{CC}$ or 0, $V_{CC}$ = 6 V | | $T_A$ = 25°C | | ±0.1 | ±100 | nA |
| | | | SNx4HC573A | | | ±1000 | |
| $I_{OZ}$ | $V_O = V_{CC}$ or 0, $V_{CC}$ = 6 V | | $T_A$ = 25°C | | ±0.01 | ±0.5 | µA |
| | | | SN54HC573A | | | ±10 | |
| | | | SN74HC573A | | | ±5 | |
| $I_{CC}$ | $V_I = V_{CC}$ or 0, $I_O$ = 0, $V_{CC}$ = 6 V | | $T_A$ = 25°C | | | 8 | µA |
| | | | SN54HC573A | | | 160 | |
| | | | SN74HC573A | | | 80 | |
| $C_i$ | $V_{CC}$ = 2 V to 6 V | | | | 3 | 10 | pF |

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per latch | $T_A$ = 25°C, no load | | 50 | | pF |

## 6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_w$ | Pulse duration, LE high | $V_{CC}$ = 2 V | $T_A$ = 25°C | 80 | | | ns |
| | | | SN54HC573A | 120 | | | |
| | | | SN74HC573A | 100 | | | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | 16 | | | |
| | | | SN54HC573A | 24 | | | |
| | | | SN74HC573A | 20 | | | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | 14 | | | |
| | | | SN54HC573A | 20 | | | |
| | | | SN74HC573A | 17 | | | |
| $t_{su}$ | Setup time, data before LE↓ | $V_{CC}$ = 2 V | $T_A$ = 25°C | 50 | | | ns |
| | | | SN54HC573A | 75 | | | |
| | | | SN74HC573A | 63 | | | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | 10 | | | |
| | | | SN54HC573A | 15 | | | |
| | | | SN74HC573A | 13 | | | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | 9 | | | |
| | | | SN54HC573A | 13 | | | |
| | | | SN74HC573A | 11 | | | |
| $t_h$ | Hold time, data after LE↓ | $V_{CC}$ = 2 V | $T_A$ = 25°C | 20 | | | ns |
| | | | SNx4HC573A | 24 | | | |
| | | $V_{CC}$ = 4.5 V | | 5 | | | |
| | | $V_{CC}$ = 6 V | | 5 | | | |

## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted; see Figure 7-1)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ | $C_L$ = 50 pF, from D (input) to Q (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 77 | 175 | ns |
| | | | SN54HC573A | | | 265 | |
| | | | SN74HC573A | | | 220 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 26 | 35 | |
| | | | SN54HC573A | | | 53 | |
| | | | SN74HC573A | | | 44 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 23 | 30 | |
| | | | SN54HC573A | | | 45 | |
| | | | SN74HC573A | | | 38 | |
| | $C_L$ = 50 pF, from LE (input) to any Q (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 87 | 175 | |
| | | | SN54HC573A | | | 265 | |
| | | | SN74HC573A | | | 220 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 27 | 35 | |
| | | | SN54HC573A | | | 53 | |
| | | | SN74HC573A | | | 44 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 23 | 30 | |
| | | | SN54HC573A | | | 45 | |
| | | | SN74HC573A | | | 38 | |
| $t_{en}$ | $C_L$ = 50 pF, from $\overline{OE}$ (input) to any Q (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 68 | 150 | ns |
| | | | SN54HC573A | | | 225 | |
| | | | SN74HC573A | | | 190 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 24 | 30 | |
| | | | SN54HC573A | | | 45 | |
| | | | SN74HC573A | | | 38 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 21 | 26 | |
| | | | SN54HC573A | | | 38 | |
| | | | SN74HC573A | | | 32 | |
| $t_{dis}$ | $C_L$ = 50 pF, from $\overline{OE}$ (input) to any Q (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 47 | 150 | ns |
| | | | SN54HC573A | | | 225 | |
| | | | SN74HC573A | | | 190 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 23 | 30 | |
| | | | SN54HC573A | | | 45 | |
| | | | SN74HC573A | | | 38 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 21 | 26 | |
| | | | SN54HC573A | | | 38 | |
| | | | SN74HC573A | | | 32 | |

over operating free-air temperature range (unless otherwise noted; see Figure 7-1)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_t$ | $C_L$ = 50 pF to any Q (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 28 | 60 | ns |
| | | | SN54HC573A | | | 90 | |
| | | | SN74HC573A | | | 75 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 8 | 12 | |
| | | | SN54HC573A | | | 18 | |
| | | | SN74HC573A | | | 15 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 6 | 10 | |
| | | | SN54HC573A | | | 15 | |
| | | | SN74HC573A | | | 13 | |
| $t_{pd}$ | $C_L$ = 150 pF, from D (input) to Q (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 95 | 200 | ns |
| | | | SN54HC573A | | | 300 | |
| | | | SN74HC573A | | | 250 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 33 | 40 | |
| | | | SN54HC573A | | | 60 | |
| | | | SN74HC573A | | | 50 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 21 | 34 | |
| | | | SN54HC573A | | | 51 | |
| | | | SN74HC573A | | | 43 | |
| | $C_L$ = 150 pF, from LE (input) to any Q (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 103 | 225 | |
| | | | SN54HC573A | | | 335 | |
| | | | SN74HC573A | | | 285 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 33 | 45 | |
| | | | SN54HC573A | | | 67 | |
| | | | SN74HC573A | | | 57 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 29 | 40 | |
| | | | SN54HC573A | | | 60 | |
| | | | SN74HC573A | | | 50 | |
| $t_{en}$ | $C_L$ = 150 pF, from $\overline{OE}$ (input) to any Q (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 85 | 200 | ns |
| | | | SN54HC573A | | | 300 | |
| | | | SN74HC573A | | | 250 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 29 | 40 | |
| | | | SN54HC573A | | | 60 | |
| | | | SN74HC573A | | | 50 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 26 | 34 | |
| | | | SN54HC573A | | | 51 | |
| | | | SN74HC573A | | | 43 | |
| $t_t$ | $C_L$ = 150 pF to any Q (output) | $V_{CC}$ = 2 V | $T_A$ = 25°C | | 60 | 210 | ns |
| | | | SN54HC573A | | | 315 | |
| | | | SN74HC573A | | | 265 | |
| | | $V_{CC}$ = 4.5 V | $T_A$ = 25°C | | 17 | 42 | |
| | | | SN54HC573A | | | 63 | |
| | | | SN74HC573A | | | 53 | |
| | | $V_{CC}$ = 6 V | $T_A$ = 25°C | | 14 | 36 | |
| | | | SN54HC573A | | | 53 | |
| | | | SN74HC573A | | | 45 | |

## 6.8 Typical Characteristics

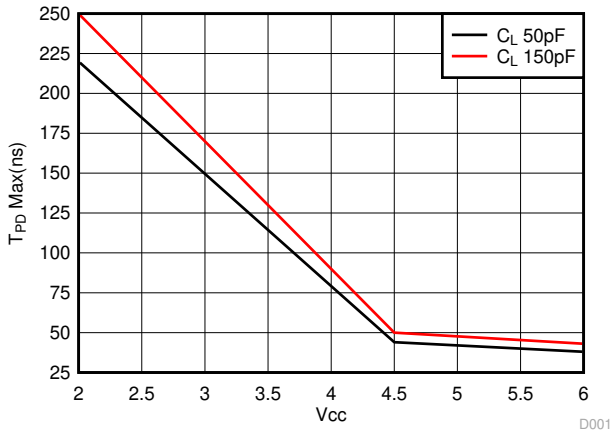
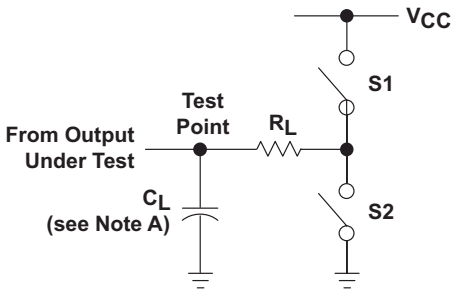


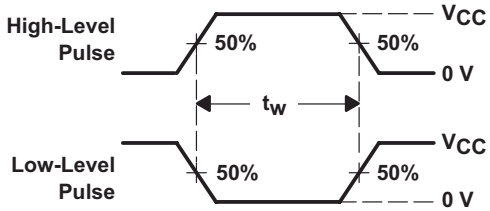

**Figure 6-1. Maximum Propagation Delay Curves**

## 7 Parameter Measurement Information

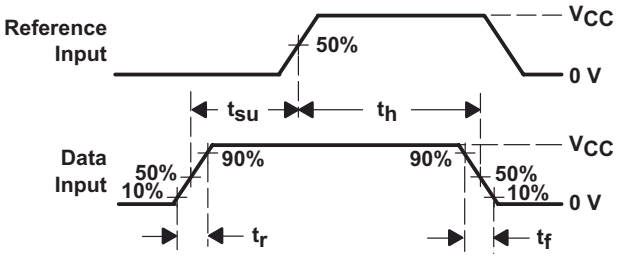



LOAD CIRCUIT

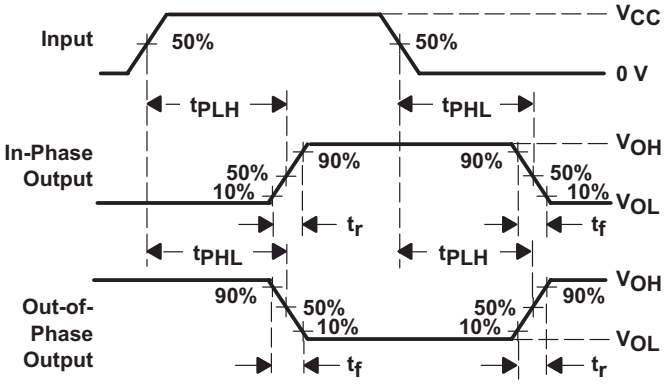
| PARAMETER | | $R_L$ | $C_L$ | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 1 kΩ | 50 pF or 150 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 1 kΩ | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | -- | 50 pF or 150 pF | Open | Open |



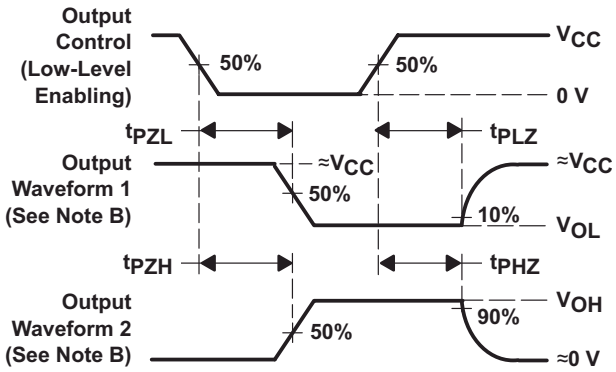

VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 7-1. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The SNx4HC573A devices are octal transparent D-type latches that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. A buffered output-enable ( $\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

## 8.2 Functional Block Diagram

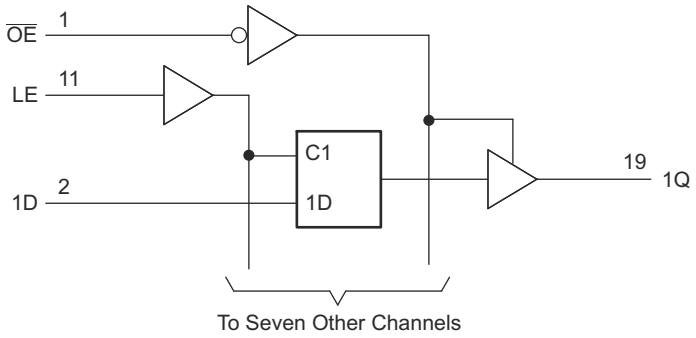





**Figure 8-1. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

The SNx4HC573A is a high current 3-state output device which can drive bus lines directly or up to 15 LSTTL loads. It has low power consumption up to 80-µA maximum $I_{CC}$. The high speed CMOS family has typical propagation delay of 21 ns with ±6-mA output drive at 5 V. The input leakage current is a very low 1-µA (maximum).

## 8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SNx4HC573A.

**Table 8-1. Function Table (Each Latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Hi-Z |

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. $\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state. The SNx4HC573A latches can be used to store 8 bits of data. Figure 9-1 shows a typical application. A low trigger event latches the output to preserve the event for processing later. With latch input high, this acts as a buffer which follows the live data at the D input when output enable pin held is low.

## 9.2 Typical Application

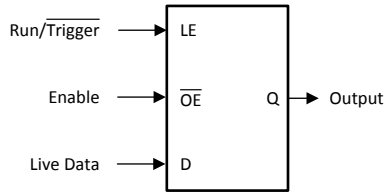





**Figure 9-1. Typical Application Schematic**

### 9.2.1 Design Requirements

The SNx4HC573A device uses CMOS technology and has balanced output drive (±7.8-mA). Take care to avoid bus contention, because it can drive currents that would exceed maximum limits.

### 9.2.2 Detailed Design Procedure

Design requirements must adhere to the *Section 6.3* and must never exceed the *Section 6.1*.

The inputs must have a ramp time less than input transition time mentioned in the *Section 6.3*. Slow inputs can cause oscillations at the output, false triggering, and increased current consumption. TI recommends a Schmitt trigger device like SN74HC14 which can tolerate slower signals.

The inputs and outputs must never exceed $V_{CC}$ to not forward bias the internal ESD diodes. The maximum frequency supported by this device is 28 MHz.

### 9.2.3 Application Curve

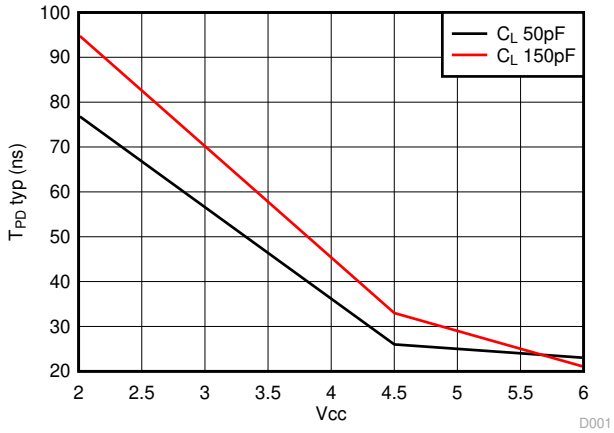



**Figure 9-2. Typical Propagation Delay Curves**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Section 6.3* table. The total current through Ground or $V_{CC}$ must not exceed ±70 mA as per *Section 6.1* table.

Each $V_{CC}$ pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1-µF capacitor; if there are multiple $V_{CC}$ pins, then TI recommends 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and 1-µF capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and the gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 11-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

## 11.2 Layout Example

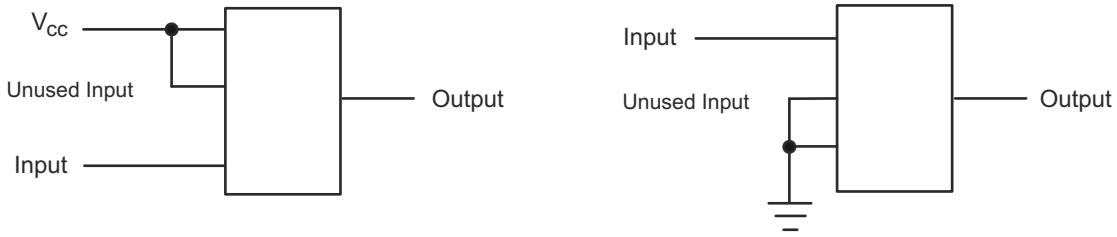



**Figure 11-1. Layout Diagram**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs* (SCBA004)

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 12-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54HC573A | Click here | Click here | Click here | Click here | Click here |
| SN74HC573A | Click here | Click here | Click here | Click here | Click here |

## 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8512801VRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8512801VR A SNV54HC573AJ | Samples |
| 85128012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 85128012A SNJ54HC 573AFK | Samples |
| 8512801RA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8512801RA SNJ54HC573AJ | Samples |
| 8512801SA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8512801SA SNJ54HC573AW | Samples |
| JM38510/65406BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65406BRA | Samples |
| M38510/65406BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65406BRA | Samples |
| SN54HC573AJ | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54HC573AJ | Samples |
| SN74HC573ADBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC573A | Samples |
| SN74HC573ADWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC573A | Samples |
| SN74HC573ADWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC573A | Samples |
| SN74HC573AN | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC573AN | Samples |
| SN74HC573ANE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC573AN | Samples |
| SN74HC573APWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC573A | Samples |
| SN74HC573APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC573A | Samples |
| SNJ54HC573AFK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 85128012A SNJ54HC 573AFK | Samples |
| SNJ54HC573AJ | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8512801RA SNJ54HC573AJ | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54HC573AW | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8512801SA SNJ54HC573AW | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN54HC573A, SN54HC573A-SP, SN74HC573A :**

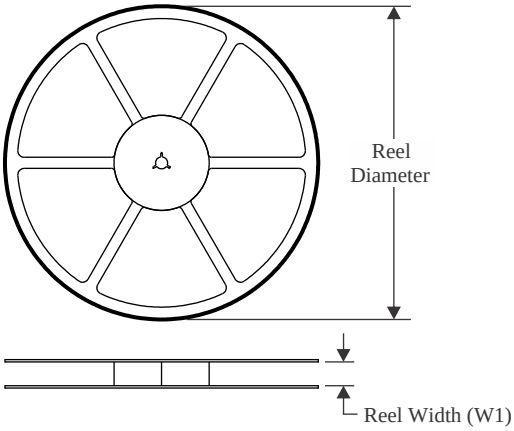
- Catalog : SN74HC573A, SN54HC573A
- Automotive : SN74HC573A-Q1, SN74HC573A-Q1
- Military : SN54HC573A
- Space : SN54HC573A-SP

NOTE: Qualified Version Definitions:

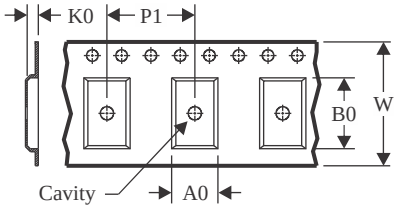
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

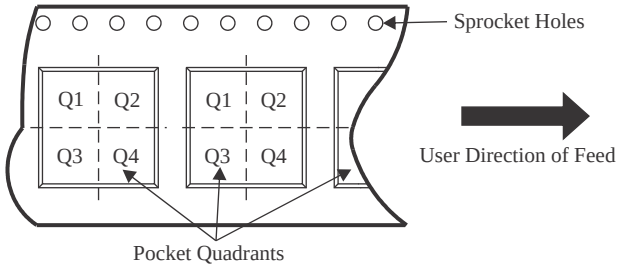



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

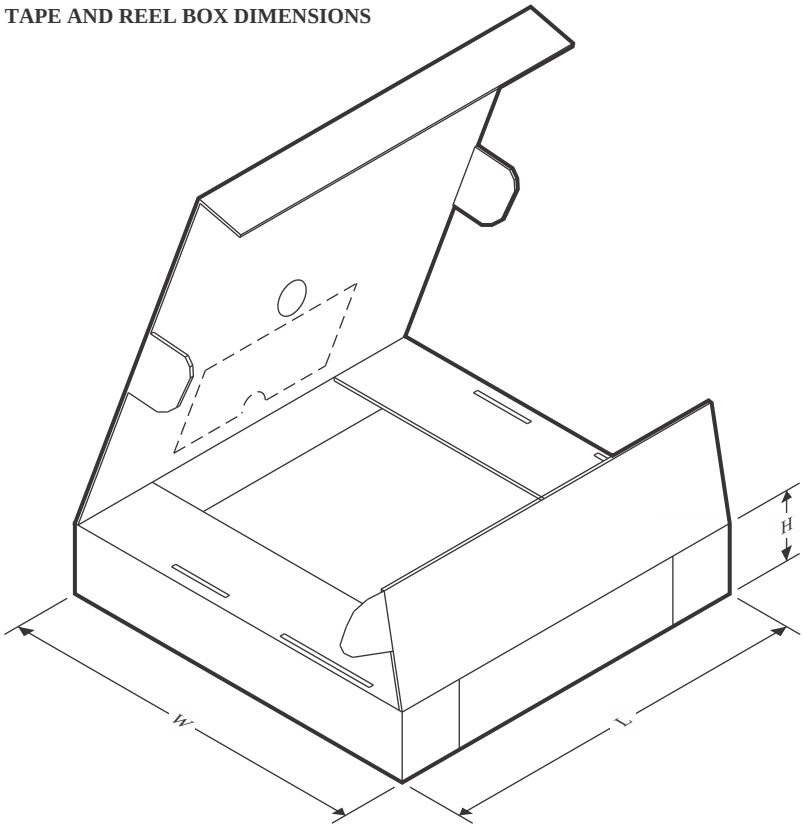
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC573ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC573ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HC573ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HC573APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74HC573APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

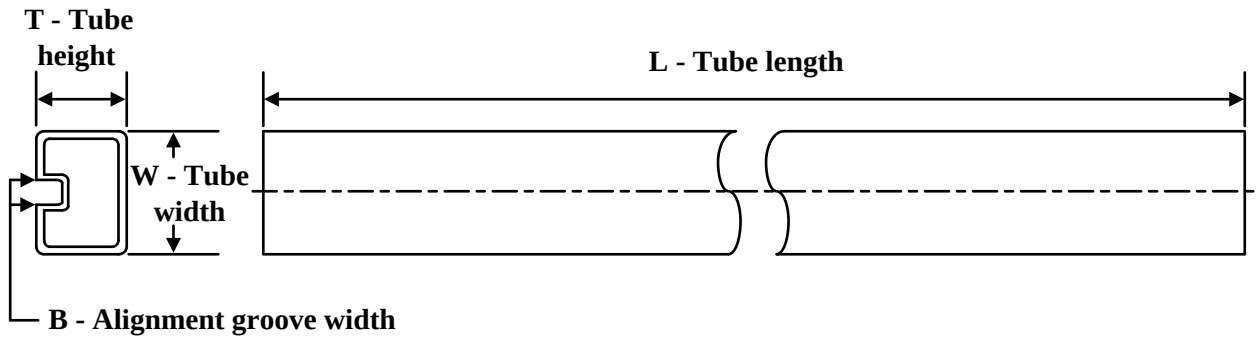
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HC573ADBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC573ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HC573ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HC573APWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC573APWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

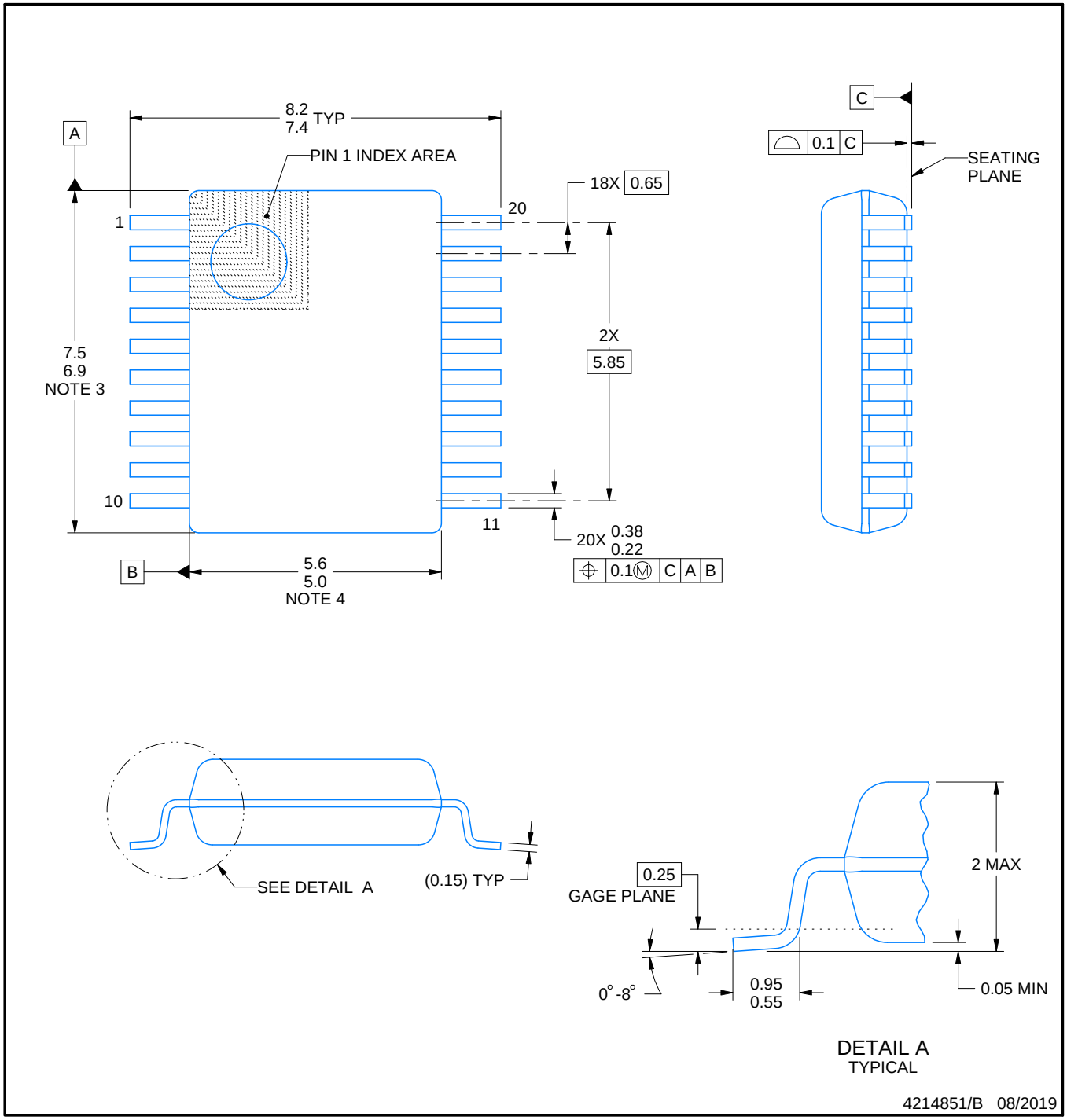
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 85128012A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 8512801SA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74HC573AN | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC573ANE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC573AFK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC573AW | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |

# PACKAGE OUTLINE

## DB0020A

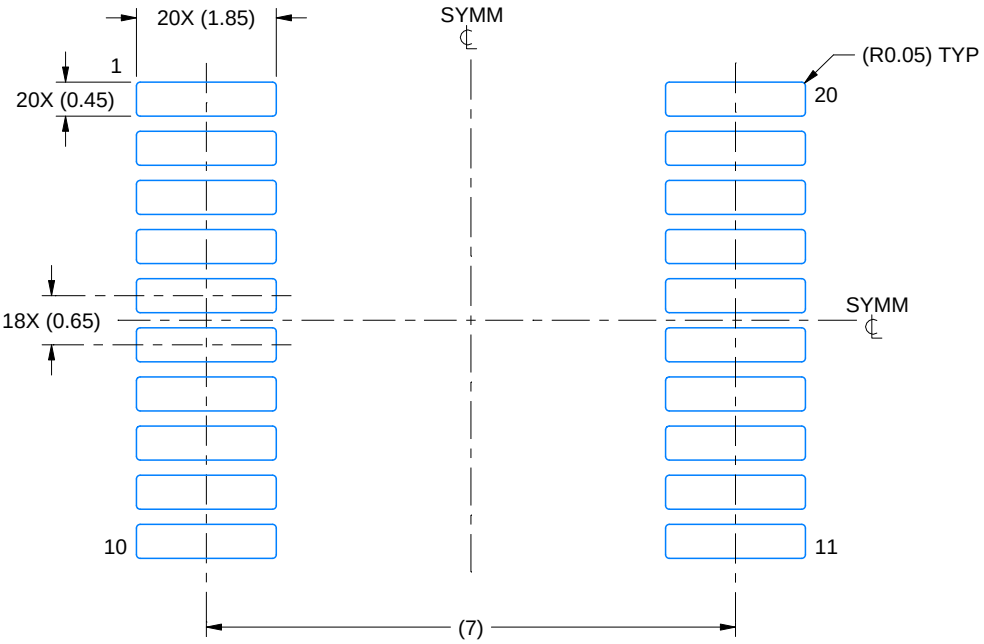
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

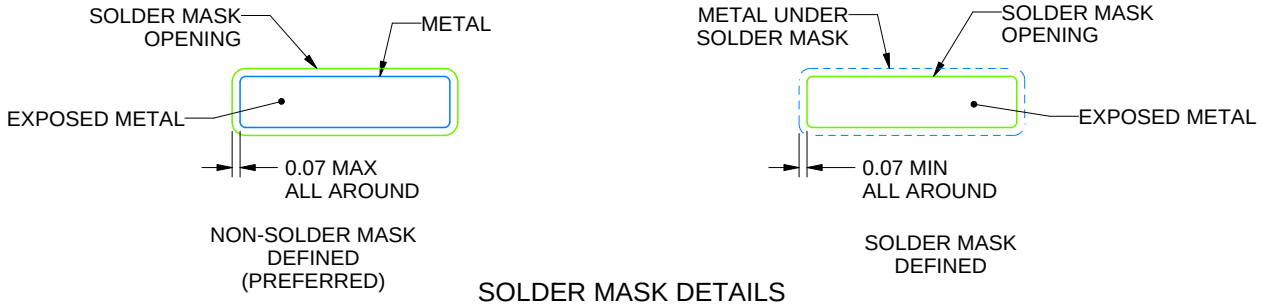



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

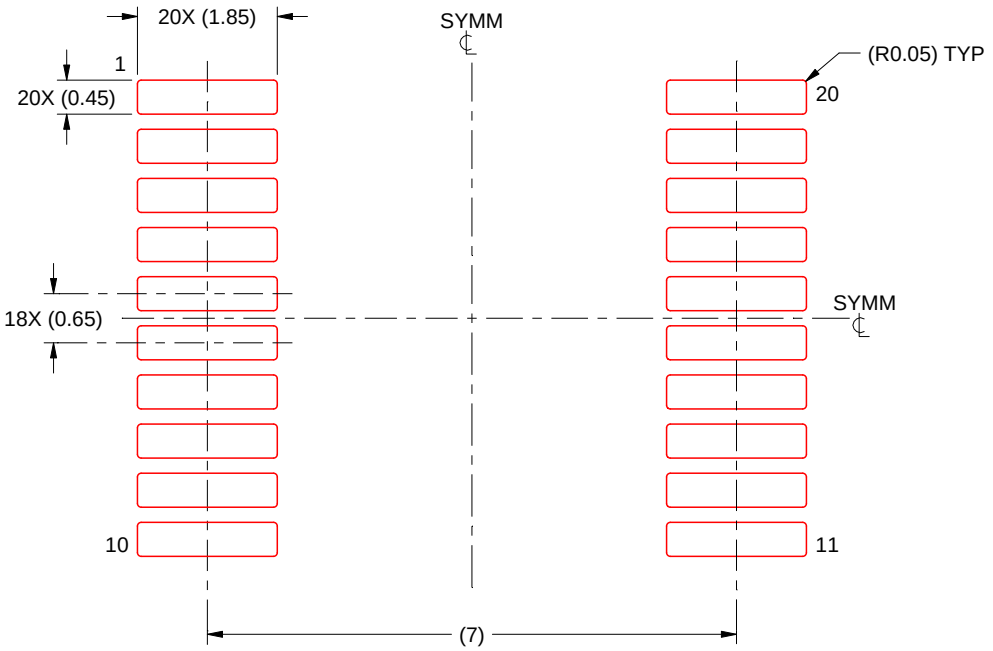
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

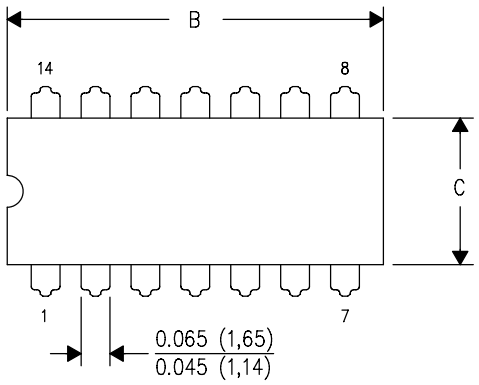
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

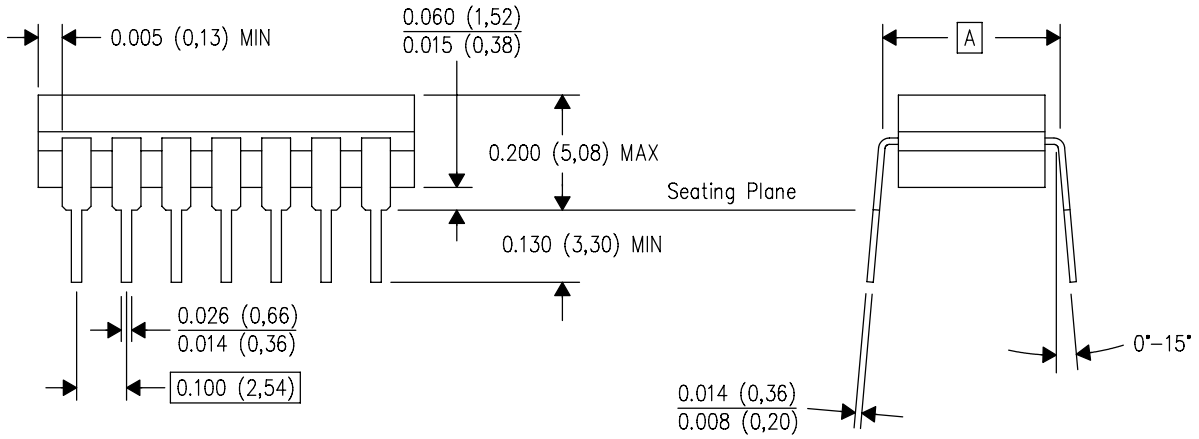
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# GENERIC PACKAGE VIEW

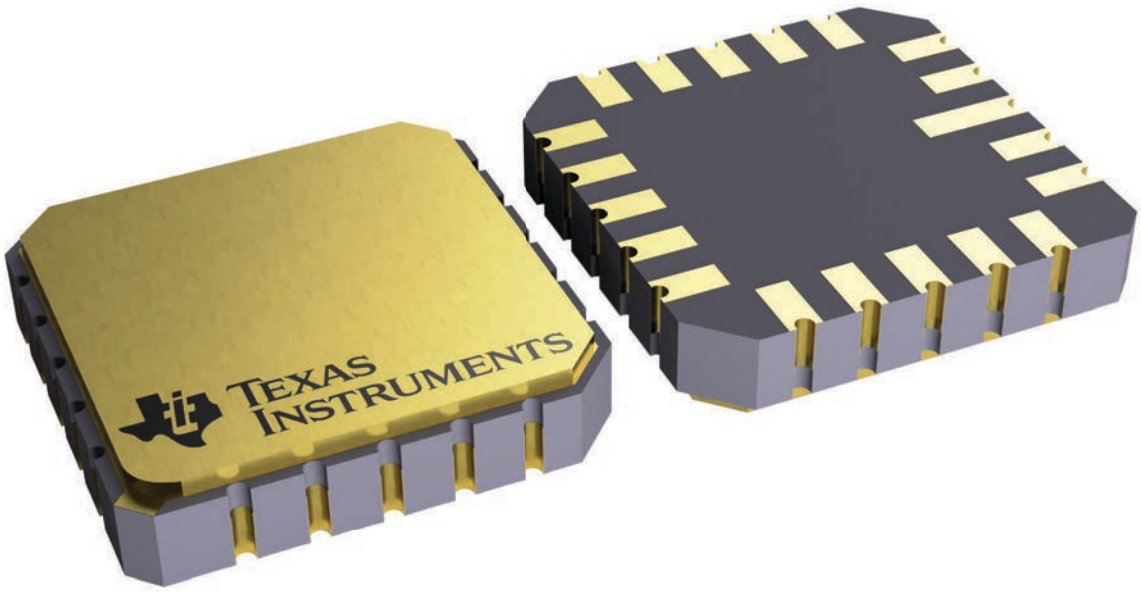
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

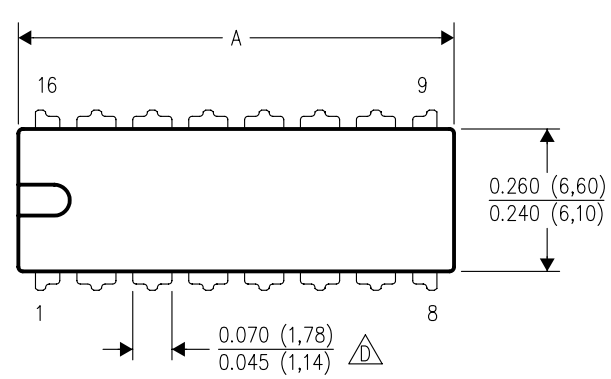



4229370VA\

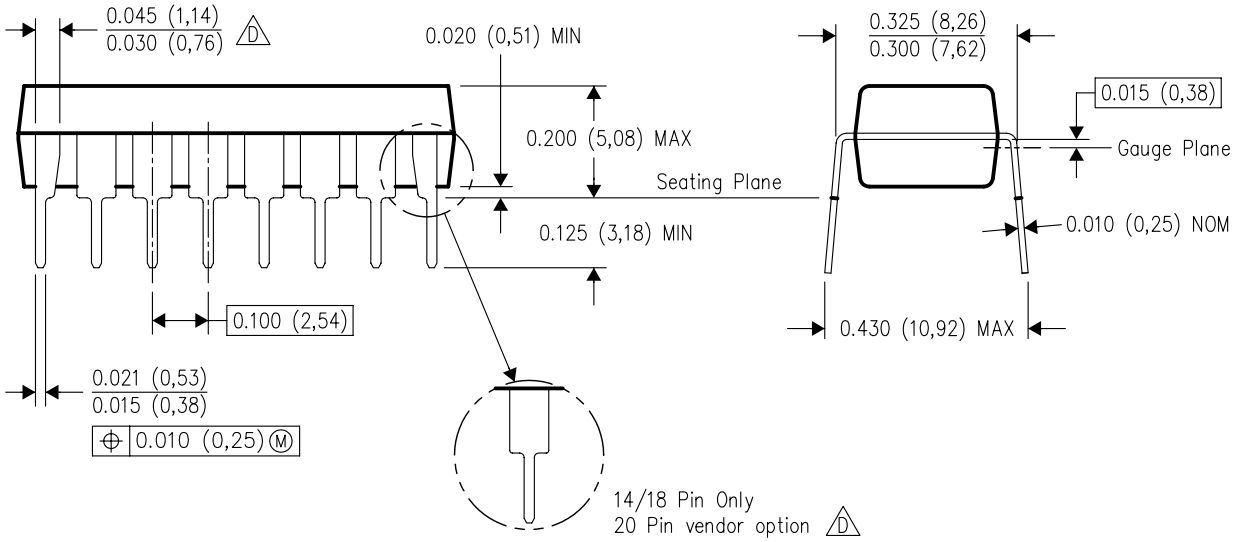
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

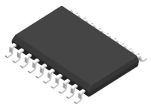



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

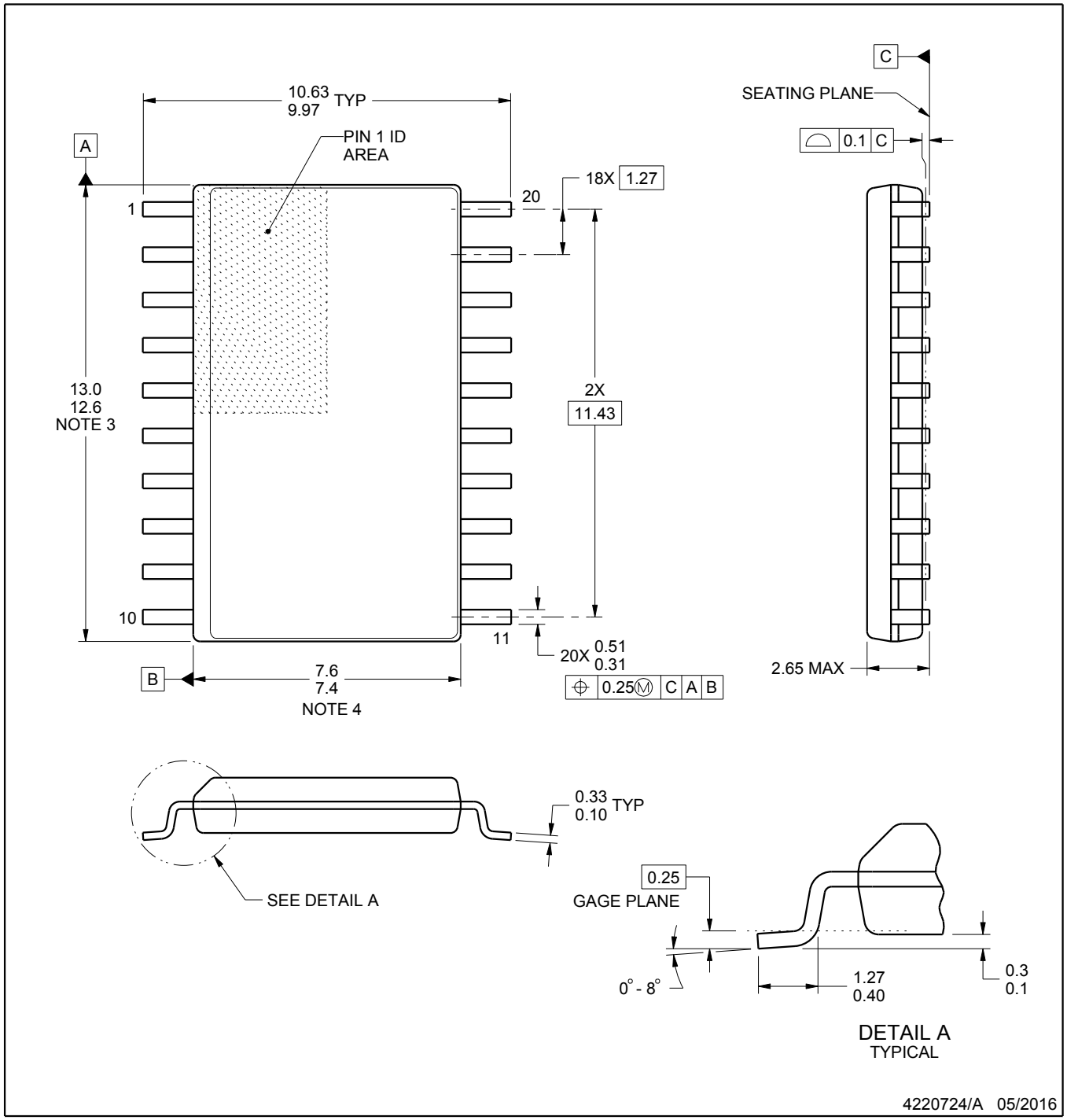


# PACKAGE OUTLINE

## DW0020A

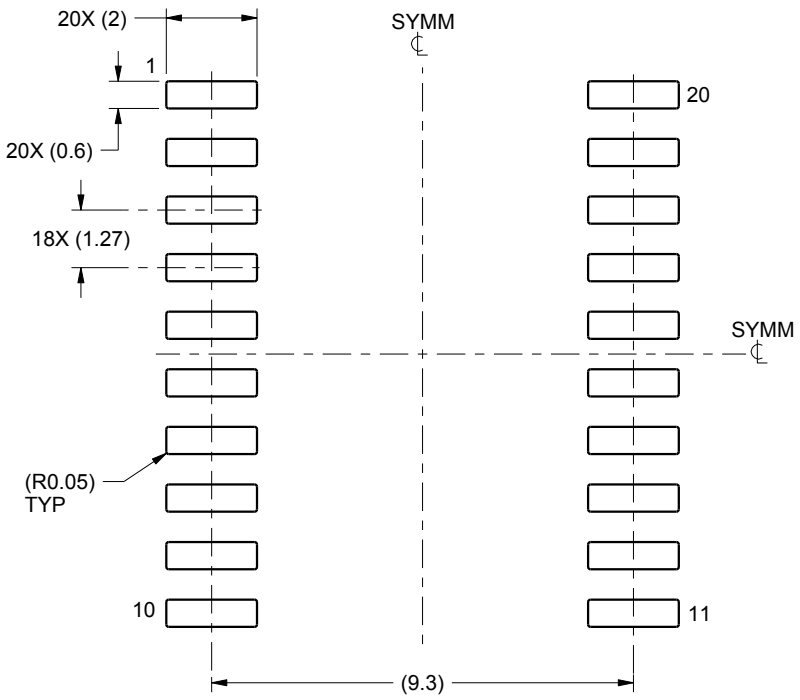
## SOIC - 2.65 mm max height

SOIC

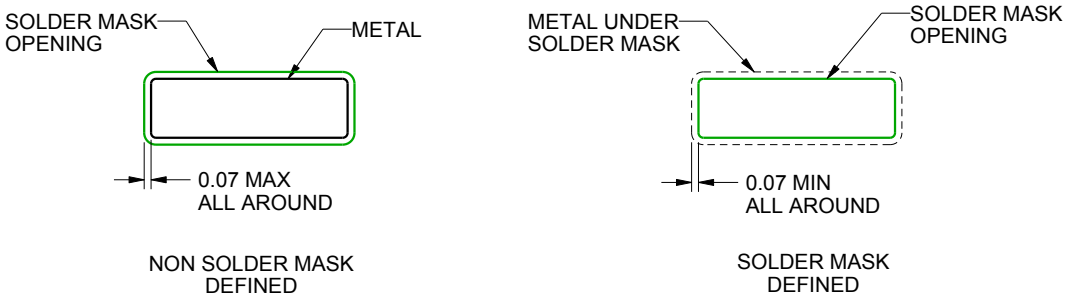



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

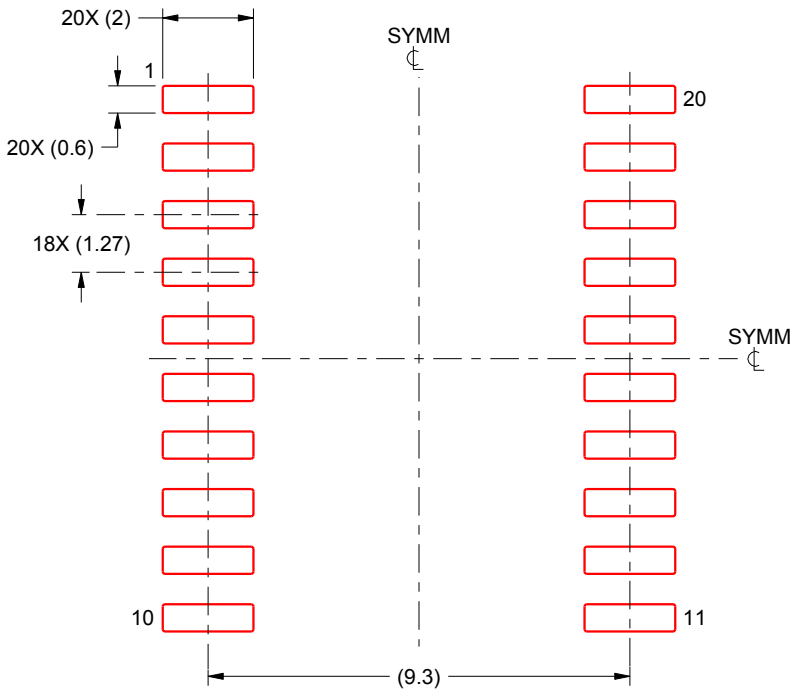



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



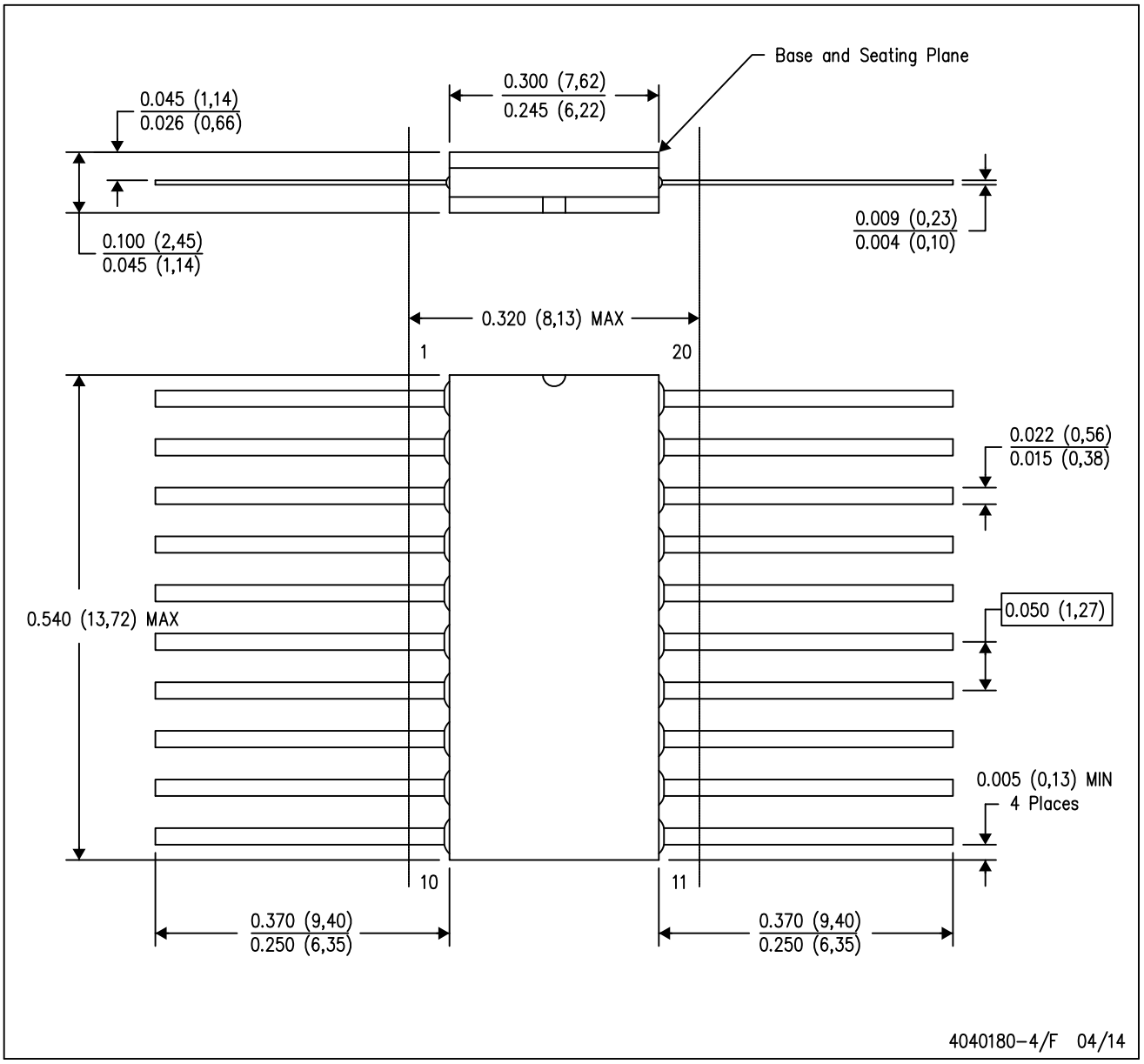

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



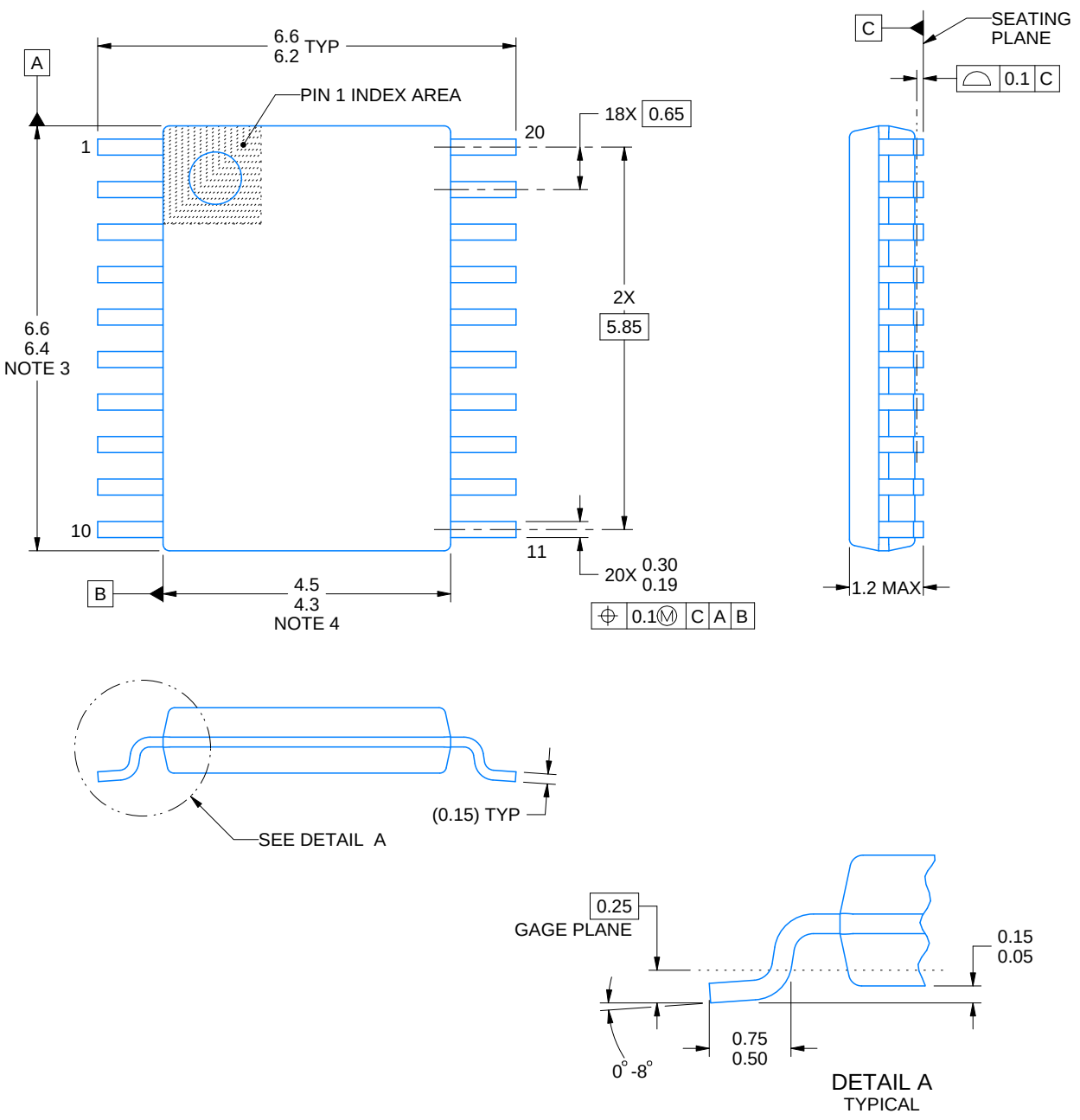

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## PW0020A

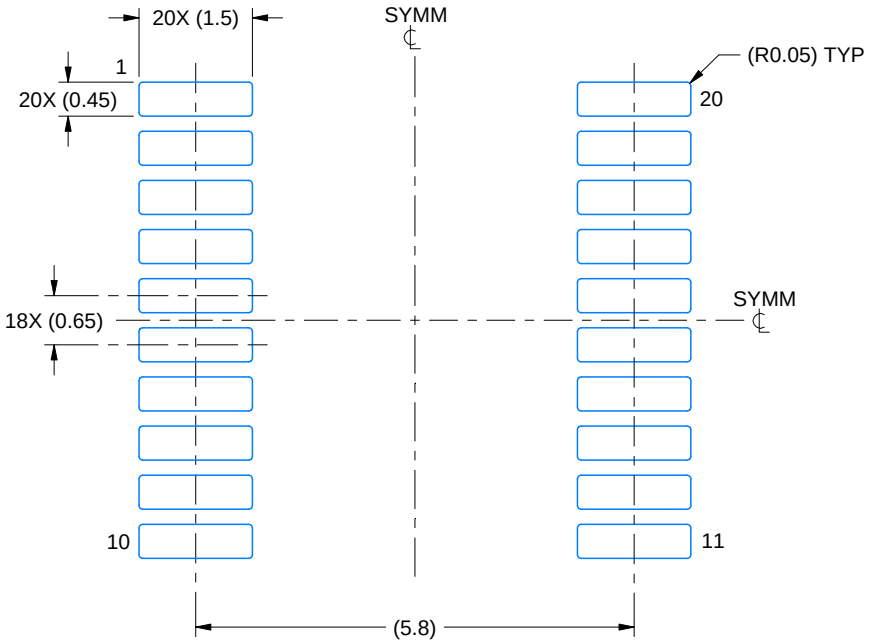
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



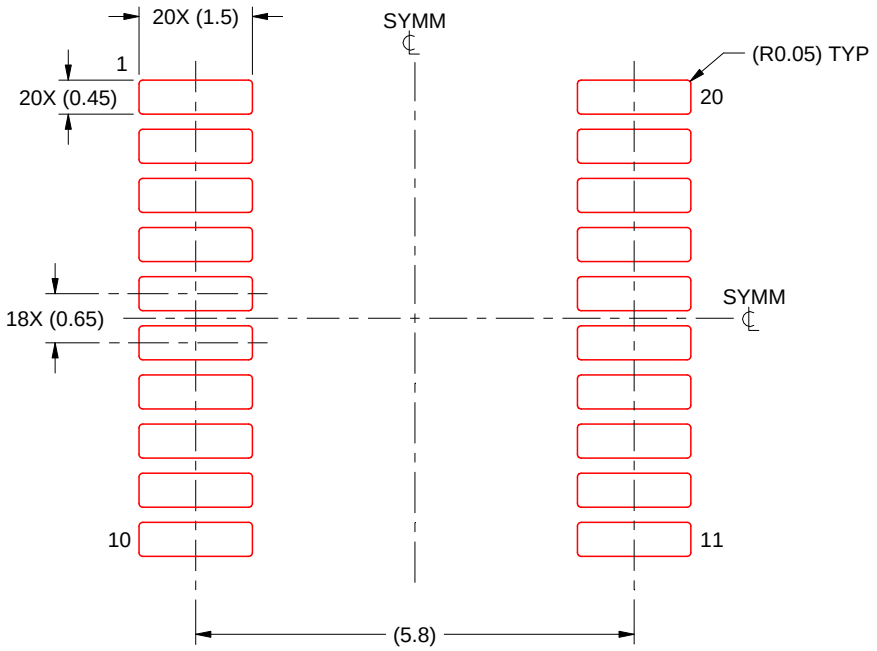

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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