# NCP5393

# 2/3/4-Phase Controller for CPU Applications

The NCP5393 controls up to four $V_{DD}$ phases and one $V_{DDNB}$ phase to provide a buck regulator solution for current and next-generation AMD processors. The NCP5393 incorporates differential voltage sensing, differential phase current sensing, optional load-line voltage positioning, and programmable $V_{DD}$ and $V_{DDNB}$ offsets to provide accurately regulated power parallel- and serial-VID AMD processors. Dual-edge multiphase modulation provides the fastest initial response to dynamic load events. This reduces system cost by requiring less bulk and ceramic output capacitance to meet transient regulation specifications.

High performance operational error amplifiers are provided to simplify compensation of the $V_{DD}$ and $V_{DDNB}$ regulators. Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between response to load transients and response to VID code changes.

### Features

- Meets AMD's Parallel, Serial (SVI) and Hybrid VR Specifications
- Up to Four $V_{DD}$ Phases
- Single-Phase $V_{DDNB}$ Controller
- Dual-Edge PWM for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifiers
- Internal Soft Start and Slew Rate Limiting
- Dynamic Reference Injection (Patent #US07057381)
- DAC Range from 12.5 mV to 1.55 V
- $\pm 0.5\%$ DAC Accuracy fro 0.8 V to 1.55 V
- $V_{DD}$ and $V_{DD}$ Offset Ranges 0 mV - 800 mV
- True Differential Remote Voltage Sense Amplifiers
- Phase-to-Phase $I_{DD}$ Current Balancing
- Differential Current Sense Amplifiers for Each Phase of Each Output
- "Lossless" Inductor Current Sensing for $V_{DD}$ and $V_{DDNB}$ Outputs
- Supports Load Lines (Droop) for $V_{DD}$ and $V_{DDNB}$ Outputs
- Oscillator Range of 100 kHz - 1 MHz
- Tracking Over Voltage Protection
- Output Inductor DCR-Based Over Current Protection for $V_{DD}$ and $V_{DDNB}$ Outputs
- Guaranteed Startup into Precharged Loads
- Temperature Range: 0°C to 70°C
- This is a Pb-Free Device*

### Applications

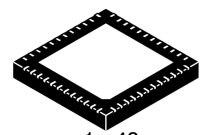
- Desktop Processors
- Server Processors
- High-End Notebook PCs

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**ON Semiconductor®**

**http://onsemi.com**

**MARKING DIAGRAM**




**QFN48, 7x7**
**CASE 485AJ**

1 ○
NCP5393
AWLYYWWG

| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb-Free Package |

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCP5393MNR2G | QFN48 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

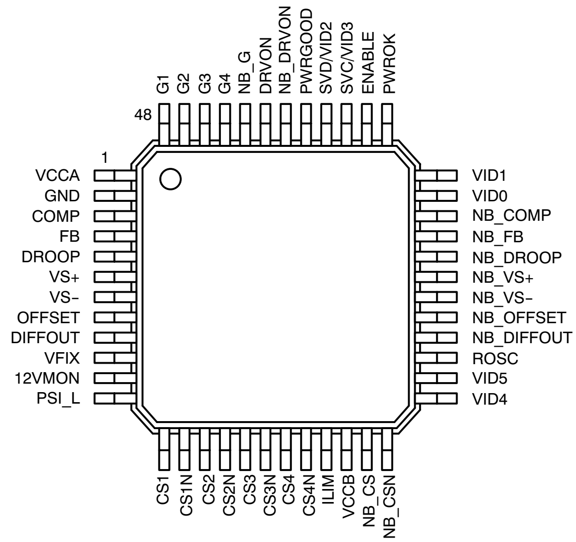



**Figure 1. Pinout**

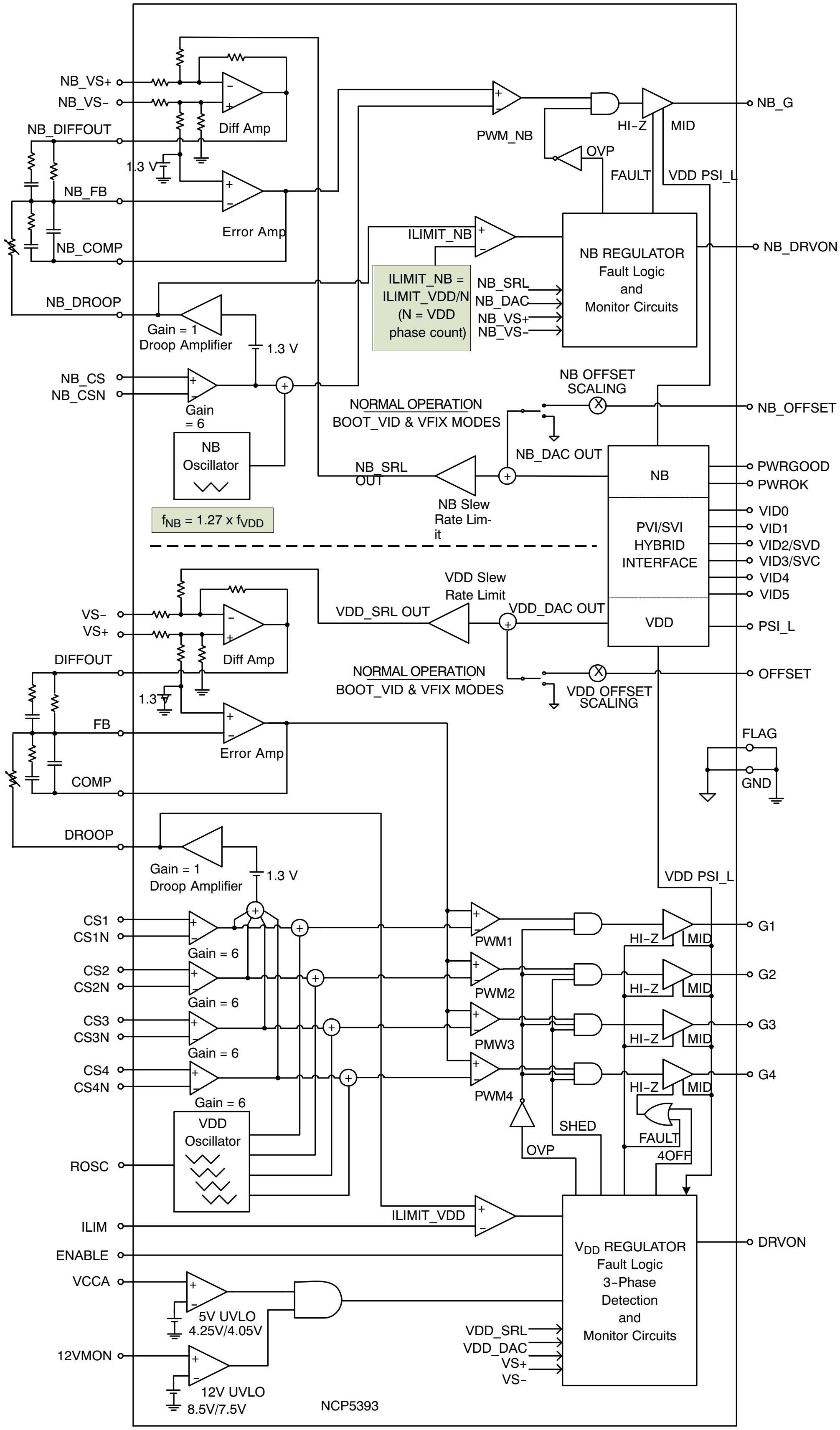



**Figure 2. NCP5393 Block Diagram**

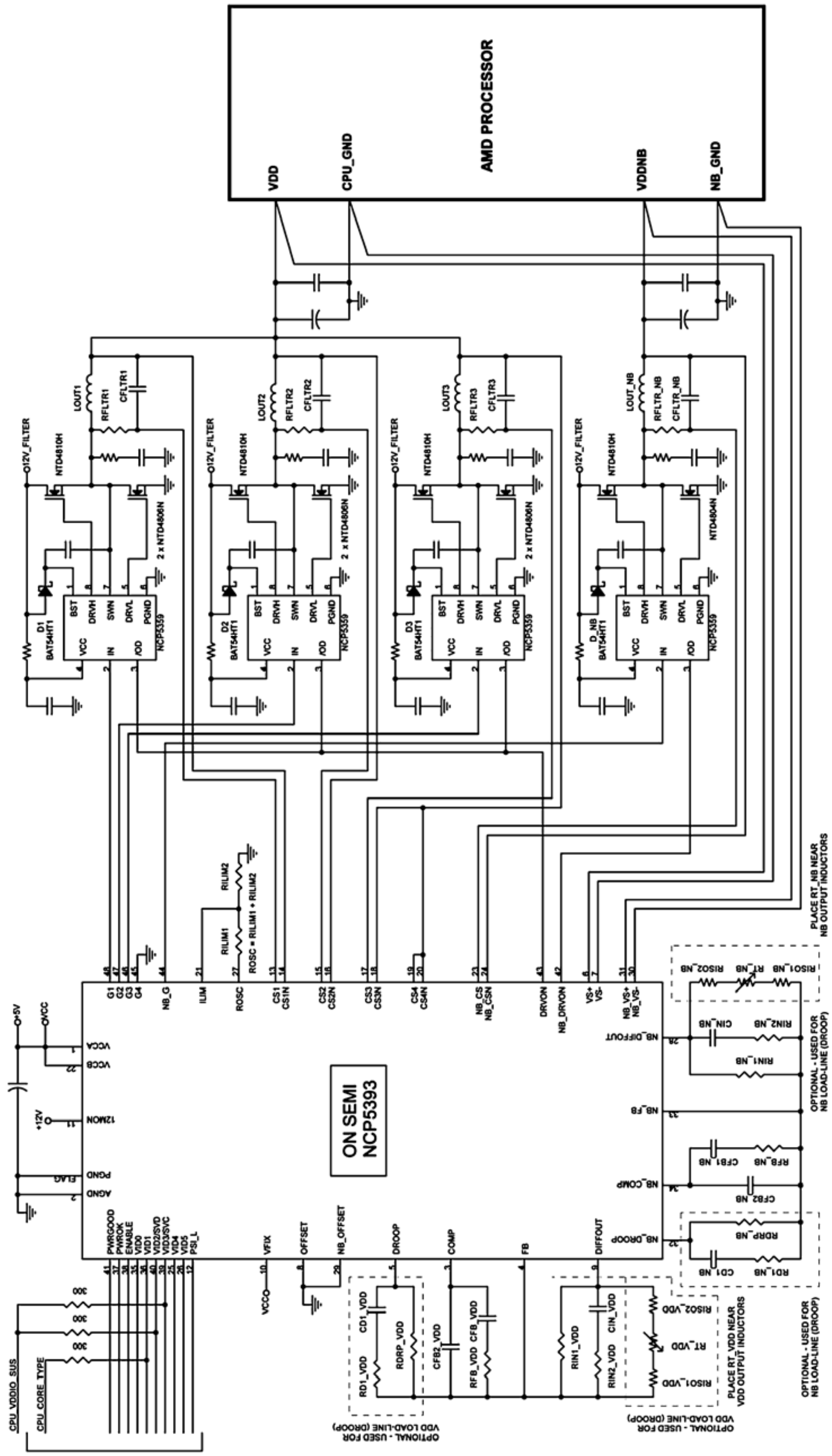



**Figure 3. NCP5393 Configured for 3 + 1 Phases, with Optional Droop**

## NCP5393 PIN DESCRIPTIONS

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VCCA | 5 V supply pin for the NCP5393. The $V_{CC}$ bypassing capacitance must be connected between this pin and GND (preferably returned to the package flag). |
| 2 | GND | Small−signal power supply return. This pin should be tied directly to the package flag (exposed pad). |
| 3 | COMP | Output of the voltage error amplifier for the $V_{DD}$ regulator. |
| 4 | FB | Voltage error amplifier inverting input for the $V_{DD}$ regulator. |
| 5 | DROOP | Voltage output signal proportional to total current drawn from the $V_{DD}$ regulator. Used when load line operation (“droop”) is desired. |
| 6 | VS+ | Non−inverting input to the differential remote sense amplifier for the $V_{DD}$ regulator. |
| 7 | VS− | Inverting input to the differential remote sense amplifier for the $V_{DD}$ regulator. |
| 8 | OFFSET | Input for offset voltage to be added to the $V_{DD}$ DAC’s output voltage. Ground this pin for zero $V_{DD}$ offset. |
| 9 | DIFFOUT | Output of the differential remote sense amplifier for the $V_{DD}$ regulator. |
| 10 | VFIX | When pulled low, this pin causes the levels on the SVC (VID3) and SVD (VID2) pins to be decoded as a two−bit DAC code, which controls the $V_{DD}$ and VDDNB outputs. |
| 11 | 12VMON | UVLO monitor input for the 12 V power rail. |
| 12 | PSI_L | Power Saving Control. Low = single phase operation, High = normal operation. This pin is not used in SVI mode. |
| 13 | CS1 | Non−inverting input to current sense amplifier #1 for the $V_{DD}$ regulator. See Table: “Pin Connections vs. Phase Count” |
| 14 | CS1N | Inverting input to current sense amplifier #1 for the $V_{DD}$ regulator. See Table: “Pin Connections vs. Phase Count” |
| 15 | CS2 | Non−inverting input to current sense amplifier #2 for the $V_{DD}$ regulator. See Table: “Pin Connections vs. Phase Count” |
| 16 | CS2N | Inverting input to current sense amplifier #2 for the $V_{DD}$ regulator. See Table: “Pin Connections vs. Phase Count” |
| 17 | CS3 | Non−inverting input to current sense amplifier #3 for the $V_{DD}$ regulator. See Table: “Pin Connections vs. Phase Count” |
| 18 | CS3N | Inverting input to current sense amplifier #3 for the $V_{DD}$ regulator. See Table: “Pin Connections vs. Phase Count” |
| 19 | CS4 | Non−inverting input to current sense amplifier #4 for the $V_{DD}$ regulator. See Table: “Pin Connections vs. Phase Count” |
| 20 | CS4N | Inverting input to current sense amplifier #4 for the $V_{DD}$ regulator. See Table: “Pin Connections vs. Phase Count” |
| 21 | ILIM | Overcurrent shutdown threshold for $V_{DD}$ and VDDNB. A resistor divider from ROSC to GND is typically used to develop an appropriate voltage on ILIM. |
| 22 | VCCB | 5 V supply pin. Tie this pin to VCCA (Pin 1). |
| 23 | NB_CS | Non−inverting input to the current sense amplifier for the VDDNB regulator |
| 24 | NB_CSN | Inverting input to the current sense amplifier for the VDDNB regulator |
| 25 | VID4 | Parallel Voltage ID DAC Input 4. Not used in SVI mode. |
| 26 | VID5 | Parallel Voltage ID DAC Input 5. Not used in SVI mode. |
| 27 | ROSC | A resistance from this pin to ground programs the $V_{DD}$ and VDDNB oscillator frequencies. This pin supplies a trimmed output voltage of 2 V. |
| 28 | NB_DIFFOUT | Output of the differential remote sense amplifier for the VDDNB regulator. |
| 29 | NB_OFFSET | Input for offset voltage to be added to the VDDNB DAC’s output voltage. Ground this pin for zero VDDNB offset. |
| 30 | NB_VS− | Inverting input to the differential remote sense amplifier for the VDDNB regulator. |
| 31 | NB_VS+ | Non−inverting input to the differential remote sense amplifier for the VDDNB regulator. |

### NCP5393 PIN DESCRIPTIONS

| Pin No. | Symbol | Description |
|---|---|---|
| 32 | NB_DROOP | Voltage output signal proportional to total current drawn from the VDDNB regulator. Used when load line operation (“droop”) is desired. |
| 33 | NB_FB | Voltage error amplifier inverting input for the $V_{DDNB}$ regulator. |
| 34 | NB_COMP | Output of the voltage error amplifier for the $V_{DDNB}$ regulator. |
| 35 | VID0 | Parallel Voltage ID DAC Input 0. Not used in SVI mode. |
| 36 | VID1 | Parallel Voltage ID DAC Input 1. Also used for PVI or SVI mode selection. |
| 37 | PWROK | System power supplies status input. Used in SVI mode only. |
| 38 | ENABLE | High = Run, Low = Standby/Reset. |
| 39 | VID3/SVC | Parallel Voltage ID DAC Input 1. Also used in SVI mode. |
| 40 | VID2/SVD | Parallel Voltage ID DAC Input 1. Also used in SVI mode. |
| 41 | PWRGOOD | Open drain output. High indicates that the active output(s) are within specification. |
| 42 | NB_DRVON | Bidirectional Gate Drive Enable to the gate driver for the $V_{DDNB}$ regulator. |
| 43 | DRVON | Bidirectional Gate Drive Enable to gate drivers for the $V_{DD}$ regulator. |
| 44 | NB_G | PWM output to the $V_{DDNB}$ gate driver. |
| 45 | G4 | PWM output #4. See Table: “Pin Connections vs. Phase Count” |
| 46 | G3 | PWM output #3. See Table: “Pin Connections vs. Phase Count” |
| 47 | G2 | PWM output #2. See Table: “Pin Connections vs. Phase Count” |
| 48 | G1 | PWM output #1. See Table: “Pin Connections vs. Phase Count” |
| FLAG | PGND | High-current power supply return via metal pad (flag) underneath package. The package flag should be tied directly to Pin 2. |

### PIN CONNECTIONS VS. PHASE COUNT

| Number of Phases | G4 | G3 | G2 | G1 | CS4 & CS4N | CS3 & CS3N | CS2 & CS2N | CS1 & CS1N |
|---|---|---|---|---|---|---|---|---|
| 4 | Phase 4 Out | Phase 3 Out | Phase 2 Out | Phase 1 Out | Phase 4 CS Input | Phase 3 CS Input | Phase 2 CS Input | Phase 1 CS Input |
| 3 | Tie to GND | Phase 3 Out | Phase 2 Out | Phase 1 Out | Tie to GND | Phase 3 CS Input | Phase 2 CS Input | Phase 1 CS Input |
| 2 | Tie to GND | Phase 2 Out | Tie to GND | Phase 1 Out | Tie to GND | Phase 2 CS input | Tie to GND | Phase 1 CS Input |

## ABSOLUTE MAXIMUM RATINGS
## ELECTRICAL INFORMATION

| Pin Symbol | $V_{MAX}$ | $V_{MIN}$ | $I_{SOURCE}$ | $I_{SINK}$ |
|---|---|---|---|---|
| 12VMON | 13.2 V | −0.3 V | N/A | 50 μA |
| VCC | 7.0 V | −0.3 V | N/A | 10 mA |
| COMP, NB_COMP | 5.5 V | −0.3 V | 10 mA | 10 mA |
| DROOP, NB_DROOP | 5.5 V | −0.3 V | 5 mA | 5 mA |
| DIFFOUT, NB_DIFFOUT | 5.5 V | −0.3 V | 20 mA | 20 mA |
| DRVON, NB_DRVON | 5.5 V | −0.3 V | 5 mA | 10 mA |
| PWRGOOD | 5.5 V | −0.3 V | N/A | 20 mA |
| VS+, NB_VS+ | 3 V | −0.3 V | 1 mA | 1 mA |
| VS−, NB_VS− | 0.3 V | −0.3 V | 1 mA | 1 mA |
| ROSC | 5.5 V | −0.3 V | 1 mA | N/A |
| All Other Pins | 5.5 V | −0.3 V | N/A | N/A |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
NOTE: All signals are referenced to GND unless noted otherwise.

## THERMAL INFORMATION

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristic, QFN Package (Note 1) | $R_{\theta JA}$ | 30.5 | °C/W |
| Operating Junction Temperature Range (Note 2) | $T_J$ | 0 to 125 | °C |
| Operating Ambient Temperature Range | $T_A$ | 0 to 70 | °C |
| Maximum Storage Temperature Range | $T_{STG}$ | −55 to +150 | °C |
| Moisture Sensitivity Level, QFN Package | MSL | 1 | |

* The maximum package power dissipation must be observed.
1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM.
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise stated: 0°C ≤ $T_A$ ≤ 70°C; 4.75 V ≤ $V_{CC}$ ≤ 5.25 V; All DAC Codes; $C_{VCC}$ = 0.1 μF)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ERROR AMPLIFIERS** ($V_{DD}$ & $V_{DDNB}$) | | | | | |
| Input Bias Current | | −200 | – | 200 | nA |
| Input Offset Voltage (Note 3) | V+ = V− = 1.3V | −1.0 | – | 1.0 | mV |
| Open Loop DC Gain | $C_L$ = 60 pF to GND, $R_L$ = 10 kΩ to GND | – | 80 | – | dB |
| Open Loop Unity Gain Bandwidth | $C_L$ = 60 pF to GND, $R_L$ = 10 kΩ to GND | – | 15 | – | MHz |
| Open Loop Phase Margin | $C_L$ = 60 pF to GND, $R_L$ = 10 kΩ to GND | – | 70 | – | deg |
| Slew Rate | $\Delta V_{IN}$ = 100 mV, AV = −10 V/V,<br>1.5 V < $V_{COMP}$ < 2.5 V,<br>$C_L$ = 60 pF, DC Loading = ±125 μA | – | 5 | – | V/μs |
| Maximum Output Voltage | 10 mV of Overdrive, $I_{SOURCE}$ = 2.0 mA | 3.5 | – | – | V |
| Minimum Output Voltage | 10 mV of Overdrive, $I_{SINK}$ = 2.0 mA | – | – | 1.0 | V |
| Output Source Current (Note 3) | 10 mV of Overdrive, $V_{OUT}$ = 3.5 V | – | 2 | – | mA |
| Output Sink Current (Note 3) | 10 mV of Overdrive, $V_{OUT}$ = 1.0 V | – | 2 | – | mA |
| **DIFFERENTIAL SUMMING AMPLIFIERS** ($V_{DD}$ & $V_{DDNB}$) | | | | | |
| VS− Input Bias Current | VS− Voltage at 0 V | | 33 | | μA |
| VS+ Input Resistance | DRVON = Low | | 1.0 | | kΩ |
| | DRVON = High | | 7 | | |
| VS+ Input Bias Voltage | DRVON = Low | | 0.37 | | V |
| | DRVON = High | | 0.05 | | |
| VS+ Input Voltage Range (Note 3) | | −0.3 | – | 3.0 | V |
| VS− Input Voltage Range (Note 3) | | −0.3 | – | 0.3 | V |
| −3dB Bandwidth (Note 3) | $C_L$ = 80 pF to GND, $R_L$ = 10 kΩ to GND | | 15 | | MHz |
| DC gain, VS+ to DIFFOUT | VS+ to VS− = 0.5 V to 2.35 V | 0.982 | 1.0 | 1.022 | V/V |
| DAC Accuracy (Measured at VS+) | Closed Loop Measurement, Error Amplifier Inside the Loop.<br>1.0125 V ≤ VDAC ≤ 1.5500 V<br>0.8000 V ≤ VDAC ≤ 1.0000 V<br>12.5 mV ≤ VDAC ≤ 0.8000 V | <br><br>−0.5<br>−5<br>−8 | <br><br>–<br>–<br>– | <br><br>0.5<br>5<br>8 | <br><br>%<br>mV<br>mV |
| Slew Rate | $\Delta V_{IN}$ = 100 mV, $\Delta V_{OUT}$ = 1.3 V−1.2 V | | 10 | | V/μs |
| Maximum Output Voltage | $I_{SOURCE}$ = 2 mA | 2.0 | | | V |
| Minimum Output Voltage | $I_{SINK}$ = 2 mA | | | 0.5 | V |
| Output source current (Note 3) | $V_{OUT}$ = 3 V | | 2.0 | | mA |
| Output sink current (Note 3) | $V_{OUT}$ = 0.5 V | | 2.0 | | mA |
| **DROOP AMPLIFIERS** ($V_{DD}$ & $V_{DDNB}$) | | | | | |
| Gain from Current Sense Input to Droop Amplifier Output | 0 mV < (CSx − CSxN) < 60 mV | 5.7 | 6.0 | 6.3 | V/V |
| Droop Amplifier DC Output Voltage | CSx = CSxN = 1.3 V | | 1.3 | | V |
| Slew Rate | $C_L$ = 20 pF to GND, $R_L$ = 1 kΩ to GND | – | 5.0 | – | V/μs |
| Maximum Output Voltage | $I_{SOURCE}$ = 4.0 mA | 3.0 | – | – | V |
| Minimum Output Voltage | $I_{SINK}$ = 1.0 mA | – | – | 1.0 | V |
| Output Source Current (Note 3) | $V_{OUT}$ = 3.0 V | – | 4.0 | – | mA |
| Output Sink Current (Note 3) | $V_{OUT}$ = 1.0 V | | 1.0 | – | mA |

3. Guaranteed by design. Not production tested.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise stated: 0°C ≤ $T_A$ ≤ 70°C; 4.75 V ≤ $V_{CC}$ ≤ 5.25 V; All DAC Codes; $C_{VCC}$ = 0.1 μF)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CURRENT SENSE AMPLIFIERS** ($V_{DD}$ & $V_{DDNB}$) | | | | | |
| Input Bias Current | CSx = CSxN = 1.4 V | −50 | – | 50 | nA |
| Common Mode Input Voltage Range | | −0.3 | – | 2.6 | V |
| Differential Mode Input Voltage Range (Note 3) | | −120 | – | 120 | mV |
| Input Offset Voltage (Note 3) | CSx = CSxN = 1.00 V | −1.0 | – | 1.0 | mV |
| Gain from Current Sense Input to PWM Comparator | 0 mV < (CSx − CSxN) < 60 mV | 5.0 | 6.0 | 7.0 | V/V |
| **INTERNAL OFFSET VOLTAGE** | | | | | |
| Voltage at Error Amplifier Non−Inverting Inputs | | – | 1.3 | – | V |
| **DRVON & NB_DRVON** | | | | | |
| Output Voltage (High) | Sourcing 500 μA | 3.0 | – | – | V |
| Output Voltage (Low) | Sinking 500 μA | – | – | 0.7 | V |
| Delay Time | Propagation Delays | – | 10 | – | ns |
| Active Internal Pull−up Resistance | Sourcing 500 μA | – | 2.0 | – | kΩ |
| Active Internal Pull−down Resistance | Sinking 500 μA | – | 150 | – | Ω |
| Rise Time | $C_L$ (PCB) = 20 pF, $\Delta V_{OUT}$ = 10% to 90% | – | 130 | – | ns |
| Fall Time | $C_L$ (PCB) = 20 pF, $\Delta V_{OUT}$ = 10% to 90% | – | 15 | – | ns |
| **$V_{DD}$ PWM OSCILLATOR** | | | | | |
| Switching Frequency Range | | 100 | – | 900 | kHz |
| Switching Frequency Accuracy 2− or 4−phase | ROSC = 49.9 kΩ<br>ROSC = 24.9 kΩ<br>ROSC = 10 kΩ | 196<br>380<br>803 | –<br>–<br>– | 226<br>420<br>981 | kHz |
| Switching Frequency Accuracy 3−phase | ROSC = 49.9 kΩ<br>ROSC = 24.9 kΩ<br>ROSC = 10 kΩ | 196<br>380<br>803 | –<br>–<br>– | 226<br>420<br>981 | kHz |
| ROSC Output Voltage | 10 μA ≤ IROSC ≤ 200 μA | 1.94 | 2.0 | 2.06 | V |
| **$V_{DDNB}$ PWM OSCILLATOR** | | | | | |
| Switching Frequency | | – | 1.25 | – | x $f_{VDD}$ |
| **PWM COMPARATORS** ($V_{DD}$ & $V_{DDNB}$) | | | | | |
| Minimum Pulse Width (Note 3) | $F_{SW}$ = 800 kHz | – | 30 | – | ns |
| Propagation Delay (Note 3) | ± 20 mV of Overdrive | – | 10 | – | ns |
| Magnitude of the PWM Ramp | | – | 1.0 | – | V |
| 0% Duty Cycle | COMP Voltage at which the PWM Outputs Remain LOW | – | 0.2 | – | V |
| 100% Duty Cycle | COMP Voltage at which the PWM Outputs Remain HIGH | – | 1.2 | – | V |
| PWM Phase Angle Error | Between Adjacent Phases | −15 | | +15 | ° |
| **PWRGOOD OUTPUT** | | | | | |
| PWRGOOD Output Voltage (Low) | $I_{PGD}$ = 5 mA | – | – | 0.4 | V |
| PWRGOOD Rise Time | External Pullup of 1 kΩ to 5 V $C_{TOTAL}$ = 45 pF, $\Delta V_{OUT}$ = 10% to 90% | – | 125 | – | ns |
| PWRGOOD High−State Leakage | $V_{PWRGOOD}$ = 5.25 V | – | – | 1 | μA |

3. Guaranteed by design. Not production tested.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise stated: $0°C \le T_A \le 70°C$; $4.75\ V \le V_{CC} \le 5.25\ V$; All DAC Codes; $C_{VCC}$ = 0.1 μF)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **PWRGOOD OUTPUT** | | | | | |
| PWRGOOD Upper Threshold | $V_{OUT}$ Increasing, DAC = 1.3 V (Wrt DAC) | – | 300 | – | mV |
| PWRGOOD Lower Threshold | $V_{OUT}$ Decreasing, DAC = 1.3 V | – | 350 | – | mV |
| **PWM OUTPUTS** ($V_{DD}$ & $V_{DDNB}$) | | | | | |
| Output Voltage (High) | Sourcing 500 μA | 3.0 | – | $V_{CC}$ | V |
| Output Voltage (Mid) | $R_L$ = 4 kΩ to GND | 1.3 | 1.5 | 1.7 | V |
| Output Voltage (Low) | Sinking 500 μA | – | – | 0.15 | V |
| Rise and Fall Times | $C_L$ = 50 pF, 0.7 V to 3.0 V or 3.0 V to 0.7 V | – | 15 | – | ns |
| Tri-State Output Leakage | Gx = 2.5 V (x = 1-4 or NB) | -1.5 | – | 1.5 | μA |
| Output Impedance - HIGH or LOW State | Resistance to $V_{CC}$ or GND | – | 50 | – | Ω |
| **VDD REGULATOR 2/3/4 PHASE DETECTION** | | | | | |
| Gate Pin Source Current | | – | 80 | – | μA |
| Gate Pin Threshold Voltage | | – | 250 | – | mV |
| Phase Detect Timer | | – | 20 | – | μs |
| **SLEW RATE LIMITERS** | | | | | |
| Soft Start Ramp Time | DAC = 0 to DAC = BOOT_VID | – | 2 | – | ms |
| Slew Rate Limit | In Any Mode after Soft-Start Completes | – | 3.25 | – | mV/μs |
| **VID INPUTS** (Note: In SVI Mode, VID[2] = Bidirectional “SVD’ Line and VID[3] = “SVC” Clock Input) | | | | | |
| VID Input Voltage (High) | $V_{HIGH}$ | 0.9 | – | – | V |
| VID Input Voltage (Low) | $V_{LOW}$ | – | – | 0.6 | V |
| VID Hysteresis | $V_{HIGH} - V_{LOW}$ or $V_{LOW} - V_{HIGH}$ | – | 100 | – | mV |
| Input Pulldown Current | $V_{IN}$ = 0.6 V - 1.9 V | – | 15 | – | μA |
| SVD Output Voltage (Low) | In SVI Mode, $I_{SINK}$ = 5 mA | 0 | – | 0.25 | V |
| **ENABLE INPUT** | | | | | |
| ENABLE Input Voltage (High) | $V_{HIGH}$ | 2.0 | – | – | V |
| ENABLE Input Voltage (Low) | $V_{LOW}$ | – | – | 0.8 | V |
| Enable Hysteresis | Low - High or High - Low | – | 200 | – | mV |
| Enable Input Pull-Up Current | Internal Pullup to $V_{CC}$ | – | 15 | – | μA |
| **VFIXEN INPUT** (Active-Low Input) | | | | | |
| VFIXEN Input Voltage (High) | $V_{HIGH}$ | 0.9 | – | – | V |
| VFIXEN Input Voltage (Low) | $V_{LOW}$ | – | – | 0.6 | V |
| VFIXEN Hysteresis | Low - High or High - Low | | 100 | | mV |
| VFIXEN Input Pull-Up Current | Internal Pullup to $V_{CC}$ | – | 15 | – | μA |

3. Guaranteed by design. Not production tested.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise stated: 0°C ≤ $T_A$ ≤ 70°C; 4.75 V ≤ $V_{CC}$ ≤ 5.25 V; All DAC Codes; $C_{VCC}$ = 0.1 μF)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **PSI_L (Power Saving Control, Active Low)** (This pin is used in PVI mode only) | | | | | |
| PSI_L Input Voltage (High) | $V_{HIGH}$ | 0.9 | – | – | V |
| PSI_L Input Voltage (Low) | $V_{LOW}$ | – | – | 0.6 | V |
| PSI_L Hysteresis | $V_{HIGH}$ – $V_{LOW}$ or $V_{LOW}$ – $V_{HIGH}$ | | 100 | | mV |
| **CURRENT LIMIT** | | | | | |
| Current Sense Amp to ILIM Gain | 20 mV < (CSx – CSxN) < 60 mV (CS inputs tied) | 5.7 | 6.0 | 6.3 | V/V |
| ILIM Pin Input Bias Current | | – | – | 0.5 | μA |
| ILIM Pin Working Voltage Range (Note 3) | | 0.2 | – | 2.0 | V |
| ILIM Offset Voltage | Offset extrapolated to CSx–CSxN = 0 V, and referred to the ILIM pin | – | 30 | – | mV |
| Delay | | – | 600 | – | ns |
| VDDNB Current Limit Coefficient | = N x $V_{NBILIM}$ /$V_{ILIM}$, where N = number of VDD phases, and $V_{NBILIM}$ is the equivalent voltage threshold for NB Current Limit resulting from $V_{ILIM}$. | | 1.0 | | V |
| **OFFSET INPUTS** ($V_{DD}$ & $V_{DDNB}$) | | | | | |
| Output Offset Voltage Above VDAC | | 0 | – | 800 | mV |
| **OUTPUT OVERVOLTAGE PROTECTION** ($V_{DD}$ & $V_{DDNB}$) | | | | | |
| Over Voltage Threshold | In normal operation, with no VID changes | | | $V_{DAC}$ + 250 | mV |
| **VCCA UNDERVOLTAGE PROTECTION** | | | | | |
| VCCA UVLO Start Threshold | | 4.0 | 4.25 | 4.5 | V |
| VCCA UVLO Stop Threshold | | 3.8 | 4.05 | 4.3 | V |
| VCCA UVLO Hysteresis | | | 200 | | mV |
| **INPUT SUPPLY CURRENT** | | | | | |
| VCC Operating Current | ENABLE held Low, No PWM operation | – | 25 | 35 | mA |
| **12VMON** | | | | | |
| 12VMON (High Threshold) | | 8 | 8.5 | 9 | V |
| 12VMON (Low Threshold) | | 7 | 7.5 | 8 | V |
| 12VMON Hysteresis | Low – High or High – Low | | 1.0 | | V |

3. Guaranteed by design. Not production tested.

## TYPICAL CHARACTERISTICS

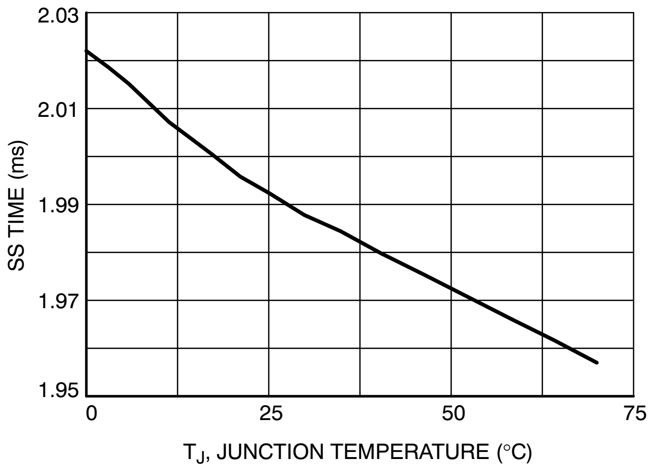



**Figure 1. SS Time vs. Temperature**

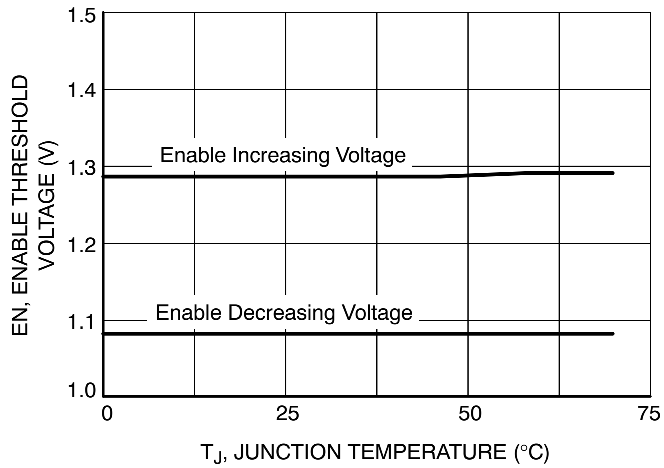



**Figure 2. Enable Threshold Voltage vs. Temperature**

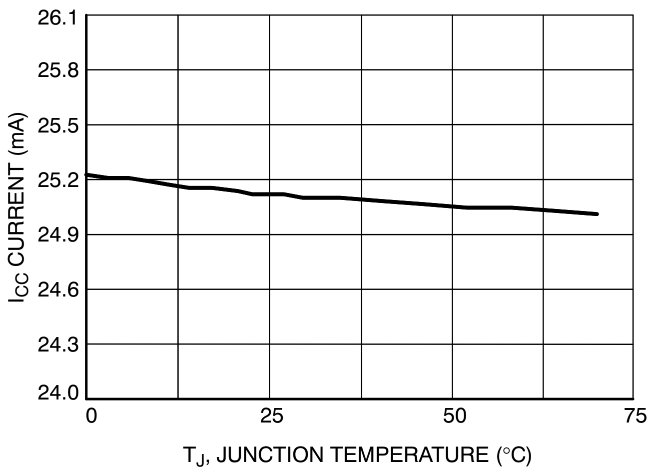



**Figure 3. $I_{CC}$ Current vs. Temperature**

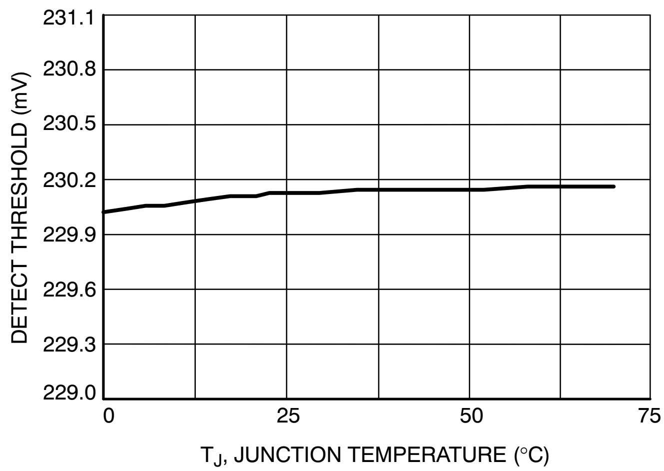



**Figure 4. 2/3/4 Phase Detection Threshold vs. Temperature**

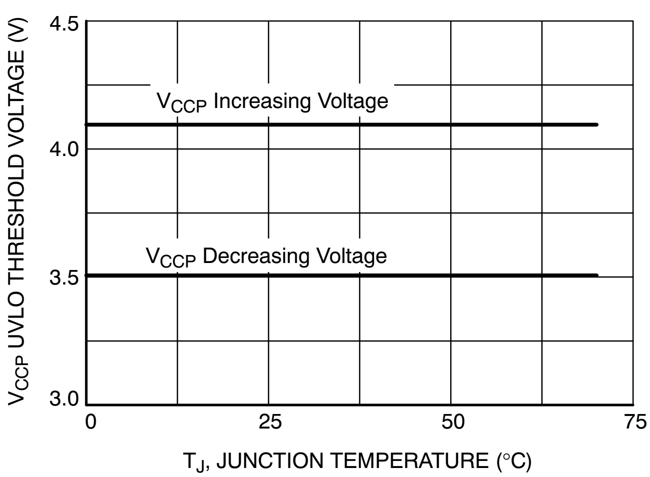



**Figure 5. $V_{CCP}$ Undervoltage Lockout Threshold Voltage vs. Temperature**

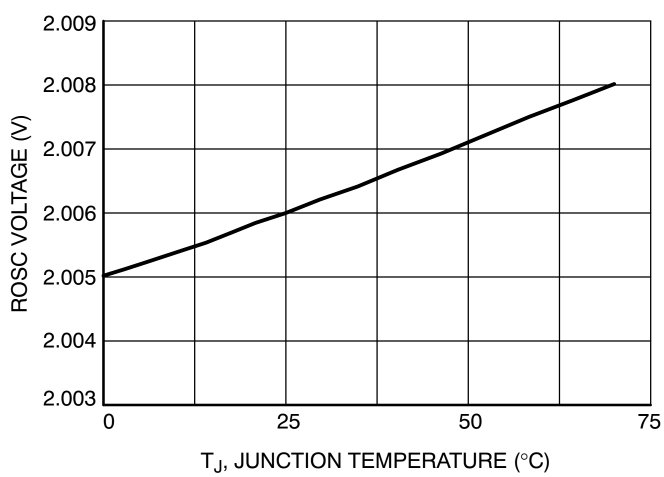



**Figure 6. ROSC Voltage vs. Temperature**

## TYPICAL CHARACTERISTICS

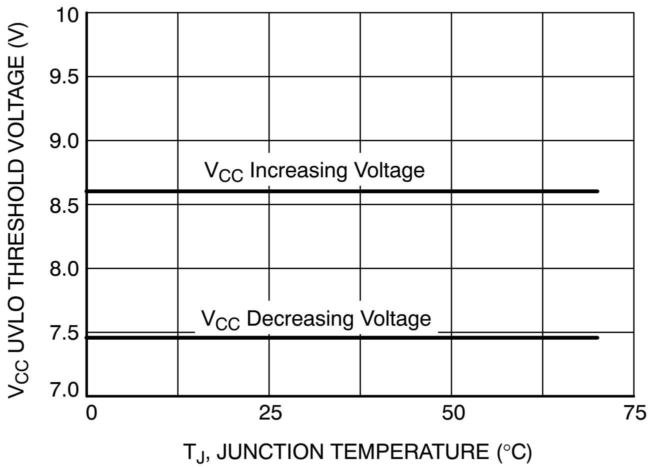



**Figure 7. 12VMON Undervoltage Lockout Threshold Voltage vs. Temperature**

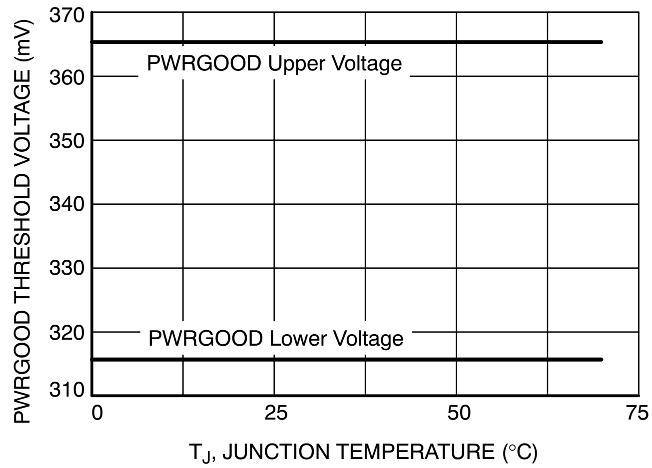



**Figure 8. PWRGOOD Voltage vs. Temperature**

## Functional Description

### General

NCP5393 is an universal CPU Power Supply Controller compatible with both Parallel (PVI) and Serial (SVI) protocols for AMD Processors. The device provides complete control logic and protections for a high-performance step-down DC-DC voltage regulator, optimized for advanced microprocessor power supply supporting both PVI and SVI communication. It embeds two independent controllers for CPU CORE and the integrated NB, each one with its set of protections. The Controller performs a single-phase control for the NB Section and a programmable 2- to-4 phase control for the CORE Section featuring Dual-Edge multiphase architecture.

NCP5393 also supports V_FIX mode for board debug: in this particular configuration the SVI bus is used as a static bus configuring 4 operative voltages for both the sections and ignoring any serial-VID command. It can be used for the board debug before plugging-in the CPU.

The NCP5393 incorporates differential voltage sensing, differential phase current sensing, optional load-line voltage positioning, and programmable $V_{DD}$ and $V_{DDNB}$ offsets to provide accurately regulated power parallel- and serial-VID AMD processors. Dual-edge multiphase modulation provides the fastest initial response to dynamic load events.

NCP5393 is able to detect which kind of CPU is connected in order to configure itself to work as a Single-Plane PVI controller or Dual-Plane SVI controller. The NCP5393 manages On the Fly VID transitions and maintains the slew rates as defined when the transitions take place. NCP5393 is available in TQFN48 Package.

### Remote Output Sensing Amplifier (RSA)

A true differential amplifier allows the NCP5393 to measure $V_{core}$ voltage feedback with respect to the $V_{core}$ ground reference point by connecting the $V_{core}$ reference point to VSP, and the $V_{core}$ ground reference point to VSN. This configuration keeps ground potential differences between the local controller ground and the $V_{core}$ ground reference point from affecting regulation of $V_{core}$ between $V_{core}$ and $V_{core}$ ground reference points. The RSA also subtracts the DAC (minus VID offset) voltage, thereby producing an unamplified output error voltage at the DIFFOUT pin. This output also has a 1.3 V bias voltage as the floating ground to allow both positive and negative error voltages.

### Precision Programmable DAC

A precision programmable DAC is provided and system trimmed. This DAC has 0.5% accuracy over the entire operating temperature range of the part. The DAC can be programmed to support both PVI and SVI VID code specifications.

### High Performance Voltage Error Amplifier

The error amplifier is designed to provide high slew rate and bandwidth. Although not required when operating as the controller of a voltage regulator, a capacitor from COMP to VFB is required for stable unity gain test configurations.

### Gate Driver Outputs and 2/3/4 Phase Operation

The part can be configured to run in 2-, 3-, or 4-phase mode. In 2-phase mode, phases 1 and 3 should be used to drive the external gate drivers, G2 and G4 must be grounded. In 3-phase mode, gate output G4 must be grounded. In 4-phase mode all 4 gate outputs are used as shown in the 4-phase Applications Schematic. The Current Sense inputs of unused channels should be connected to GND. Please refer to table “PIN CONNECTIONS vs. PHASE COUNTS” for details.

### Differential Current Sense Amplifiers and Summing Amplifier

Four differential amplifiers are provided to sense the output current of each phase. The inputs of each current sense amplifier must be connected across the current sensing element of the phase controlled by the corresponding gate output (G1, G2, G3, or G4). If a phase is unused, the differential inputs to that phase's current sense amplifier must be shorted together and connected to the GND.

The current signals sensed from inductor DCR are fed into a summing amplifier to have a summed-up output. The outputs of current sense amplifiers control three functions. First, the summing current signal of all phases will go through DROOP amplifier and join the voltage feedback loop for output voltage positioning. Second, the output signal from DROOP amplifier also goes to ILIM amplifier to monitor the output current limit. Finally, the individual phase current contributes to the current balance of all phases by offsetting their ramp signals of PWM comparators.

### Oscillator and Triangle Wave Generator

The controller embeds a programmable precision dual-Oscillator: one section is used for the CORE and it is a multiphase programmable oscillator managing equal phase-shift among all phases and the other section is used for the NB section. The oscillator's frequency is programmed by the resistance connected from the ROSC pin to ground. The user will usually form this resistance from two resistors in order to create a voltage divider that uses the ROSC output voltage as the reference for creating the current limit setpoint voltage. The oscillator frequency range is 100_kHz per phase to 1.0_MHz per phase. The oscillator generates up to 4 symmetrical triangle waveforms with amplitude between 1.3_V and 2.3_V. The triangle waves have a phase delay between them such that for 2-, 3- and 4-phase operation the PWM outputs are separated by 180, 120, and 90 angular degrees, respectively.

When the NB phase is enabled, in order to ensure that the VDDNB oscillator does not accidentally lock to the VDD oscillator, the VDDNB oscillator will free-run at a frequency which is nominally 1.25 ratio of $f_{VDD}$.

### CPU Support

NCP5393 is able to detect the CPU it is going to supply and configure itself accordingly. At system Start-up, on the rising-edge of the EN signal, the device monitors the status of VID1 and switches in PVI mode (VID1 = 1) or SVI mode (VID1 = 0). When in PVI mode, NCP5393 uses the information available on the VID[0:5] bus to address the CORE Section output voltage. NB Section is kept in HiZ mode. When in SVI mode, NCP5393 discards the information available on VID0, VID4 and VID5 and uses VID2 and VID3 for SVC and SVD respectively.

### PVI - Parallel Interface

PVI is a 6-bit-wide parallel interface used to address the CORE Section reference. According to the selected code, the device sets the CORE Section reference and regulates its output voltage. NB Section is kept in HiZ; no activity is performed on this section. furthermore, PWROK information is ignored as well since the signal is propietary of the SVI protocol. Start-up sequences before soft start and after soft start are given in Figure 9. Voltage identifications for the 6Bit AMD mode is given in Table 1.

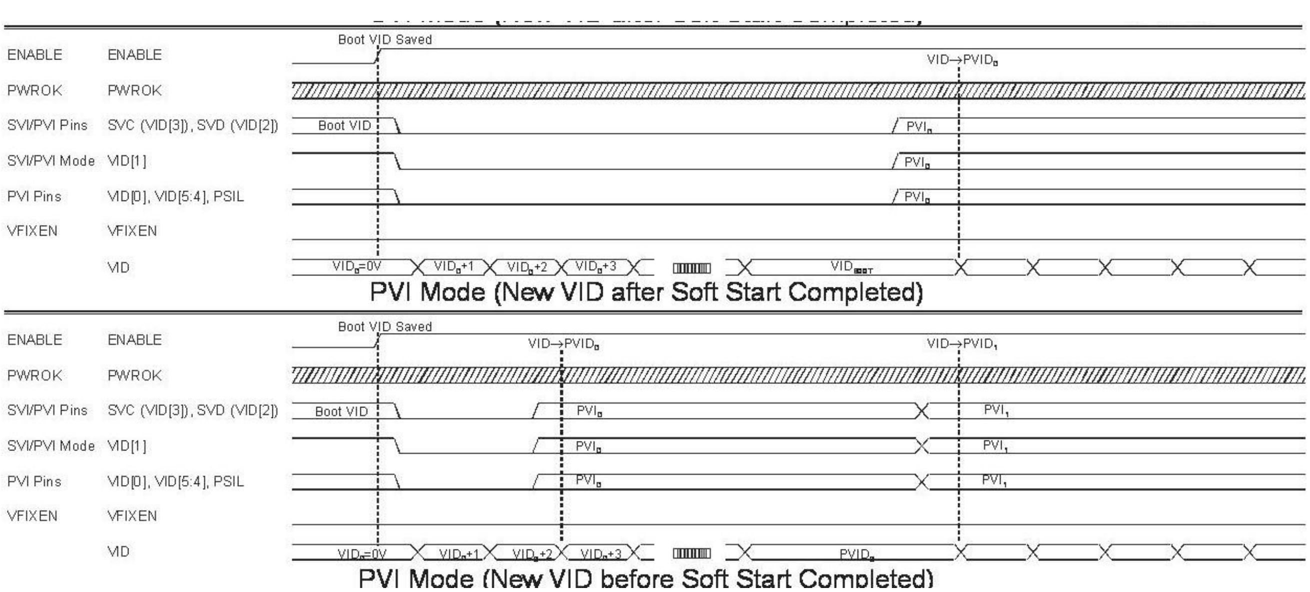



**Figure 9. Power Up Sequences Before and After Soft Start in PVI Mode**

**Table 1. SIX−BIT PARALLEL VID CODES in PVI Modes**

| SVID[5:0] | $V_{OUT}$ (V) | SVID[5:0] | $V_{OUT}$ (V) | SVID[5:0] | $V_{OUT}$ (V) | SVID[5:0] | $V_{OUT}$ (V) |
|---|---|---|---|---|---|---|---|
| 00_0000 | 1.5500 | 01_0000 | 1.1500 | 10_0000 | 0.7625 | 11_0000 | 0.5625 |
| 00_0001 | 1.5250 | 01_0001 | 1.1250 | 10_0001 | 0.7500 | 11_0001 | 0.5500 |
| 00_0010 | 1.5000 | 01_0010 | 1.1000 | 10_0010 | 0.7375 | 11_0010 | 0.5375 |
| 00_0011 | 1.4750 | 01_0011 | 1.0750 | 10_0011 | 0.7250 | 11_0011 | 0.5250 |
| 00_0100 | 1.4500 | 01_0100 | 1.0500 | 10_0100 | 0.7125 | 11_0100 | 0.5125 |
| 00_0101 | 1.4250 | 01_0101 | 1.0250 | 10_0101 | 0.7000 | 11_0101 | 0.5000 |
| 00_0110 | 1.4000 | 01_0110 | 1.0000 | 10_0110 | 0.6875 | 11_0110 | 0.4875 |
| 10_0111 | 1.3750 | 01_0111 | 0.9750 | 10_0111 | 0.6750 | 11_0111 | 0.4750 |
| 00_1000 | 1.3500 | 01_1000 | 0.9500 | 10_1000 | 0.6625 | 11_1000 | 0.4625 |
| 00_1001 | 1.3250 | 01_1001 | 0.9250 | 10_1001 | 0.6500 | 11_1001 | 0.4500 |
| 00_1010 | 1.3000 | 01_1010 | 0.9000 | 10_1010 | 0.6325 | 11_1010 | 0.4375 |
| 00_1011 | 1.2750 | 01_1011 | 0.8750 | 10_1011 | 0.6250 | 11_1011 | 0.4250 |
| 00_1100 | 1.2500 | 01_1100 | 0.8500 | 10_1100 | 0.6125 | 11_1100 | 0.4125 |
| 00_1101 | 1.2250 | 10_1101 | 0.8250 | 10_1101 | 0.6000 | 11_1101 | 0.4000 |
| 00_1110 | 1.2000 | 01_1110 | 0.8000 | 10_1110 | 0.5875 | 11_1110 | 0.3875 |
| 00_1111 | 1.1750 | 01_1111 | 0.7750 | 10_1111 | 0.5750 | 11_1111 | 0.3750 |

## SVI − Serial Interface

SVI is a two wire, Clock and Data, bus that connects a single master (AMD processor) to one NCP5393. The master initiates and terminates SVI transactions and drives the clock, SVC, and the data SVD, during a transaction. The slave receives the SVI transactions and acts accordingly. SVI wire protocol is based on fast−mode I2C. The SVI communications are given in Figure 10.

SVI interface also considers EN and PWROK signals for start−up. The device returns a PWRGOOD signal if the output voltages are in regulation. The VID codes for SVI are given in Table 2.

The start−up sequences before and after soft start are given in Figure 11.

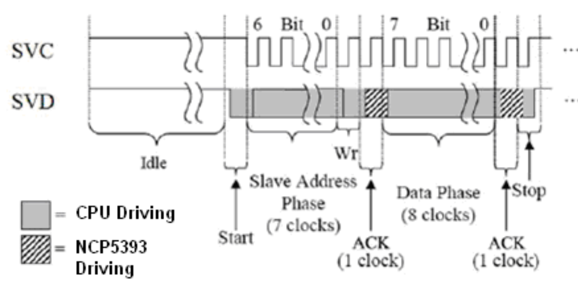



**Figure 10. SVI Communication − Send Byte**

**Table 2. SEVEN−BIT SERIAL VID CODES for SVI Mode**

| SVID[6:0] | $V_{OUT}$ (V) | SVID[6:0] | $V_{OUT}$ (V) | SVID[6:0] | $V_{OUT}$ (V) | SVID[6:0] | $V_{OUT}$ (V) |
|---|---|---|---|---|---|---|---|
| 000_0000 | 1.5500 | 010_0000 | 1.1500 | 100_0000 | 0.7500 | 110_0000 | 0.3500 |
| 000_0001 | 1.5375 | 010_0001 | 1.1375 | 100_0001 | 0.7375 | 110_0001 | 0.3375 |
| 000_0010 | 1.5250 | 010_0010 | 1.1250 | 100_0010 | 0.7250 | 110_0010 | 0.3250 |
| 000_0011 | 1.5125 | 010_0011 | 1.1125 | 100_0011 | 0.7125 | 110_0011 | 0.3125 |
| 000_0100 | 1.5000 | 010_0100 | 1.1000 | 100_0100 | 0.7000 | 110_0100 | 0.3000 |
| 000_0101 | 1.4875 | 010_0101 | 1.0875 | 100_0101 | 0.6875 | 110_0101 | 0.2875 |
| 000_0110 | 1.4750 | 010_0110 | 1.0750 | 100_0110 | 0.6750 | 110_0110 | 0.2750 |
| 000_0111 | 1.4625 | 010_0111 | 1.0625 | 100_0111 | 0.6625 | 110_0111 | 0.2625 |
| 000_1000 | 1.4500 | 010_1000 | 1.0500 | 100_1000 | 0.6500 | 110_1000 | 0.2500 |
| 000_1001 | 1.4375 | 010_1001 | 1.0375 | 100_1001 | 0.6325 | 110_1001 | 0.2375 |
| 000_1010 | 1.4250 | 010_1010 | 1.0250 | 100_1010 | 0.6250 | 110_1010 | 0.2250 |
| 000_1011 | 1.4125 | 010_1011 | 1.0125 | 100_1011 | 0.6125 | 110_1011 | 0.2125 |
| 000_1100 | 1.4000 | 010_1100 | 1.0000 | 100_1100 | 0.6000 | 110_1100 | 0.2000 |
| 000_1101 | 1.3875 | 010_1101 | 0.9875 | 100_1101 | 0.5875 | 110_1101 | 0.1875 |
| 000_1110 | 1.3750 | 010_1110 | 0.9750 | 100_1110 | 0.5750 | 110_1110 | 0.1750 |
| 000_1111 | 1.3625 | 010_1111 | 0.9625 | 100_1111 | 0.5625 | 110_1111 | 0.1625 |
| 001_0000 | 1.3500 | 011_0000 | 0.9500 | 101_0000 | 0.5500 | 111_0000 | 0.1500 |
| 001_0001 | 1.3375 | 011_0001 | 0.9375 | 101_0001 | 0.5375 | 111_0001 | 0.1375 |
| 001_0010 | 1.3250 | 011_0010 | 0.9250 | 101_0010 | 0.5250 | 111_0010 | 0.1250 |
| 001_0011 | 1.3125 | 011_0011 | 0.9125 | 101_0011 | 0.5125 | 111_0011 | 0.1125 |
| 001_0100 | 1.3000 | 011_0100 | 0.9000 | 101_0100 | 0.5000 | 111_0100 | 0.1000 |
| 001_0101 | 1.2875 | 011_0101 | 0.8875 | 101_0101 | 0.4875 | 111_0101 | 0.0875 |
| 001_0110 | 1.2750 | 011_0110 | 0.8750 | 101_0110 | 0.4750 | 111_0110 | 0.0750 |
| 001_0111 | 1.2625 | 011_0111 | 0.8625 | 101_0111 | 0.4625 | 111_0111 | 0.0625 |
| 001_1000 | 1.2500 | 011_1000 | 0.8500 | 101_1000 | 0.4500 | 111_1000 | 0.0500 |
| 001_1001 | 1.2375 | 011_1001 | 0.8375 | 101_1001 | 0.4375 | 111_1001 | 0.0375 |
| 001_1010 | 1.2250 | 011_1010 | 0.8250 | 101_1010 | 0.4250 | 111_1010 | 0.0250 |
| 001_1011 | 1.2125 | 011_1011 | 0.8125 | 101_1011 | 0.4125 | 111_1011 | 0.0125 |
| 001_1100 | 1.2000 | 011_1100 | 0.8000 | 101_1100 | 0.4000 | 111_1100 | OFF |
| 001_1101 | 1.1875 | 011_1101 | 0.7875 | 110_1101 | 0.3875 | 111_1101 | OFF |
| 001_1110 | 1.1750 | 011_1110 | 0.7750 | 101_1110 | 0.3750 | 111_1110 | OFF |
| 001_1111 | 1.1625 | 011_1111 | 0.7625 | 101_1111 | 0.3625 | 111_1111 | OFF |

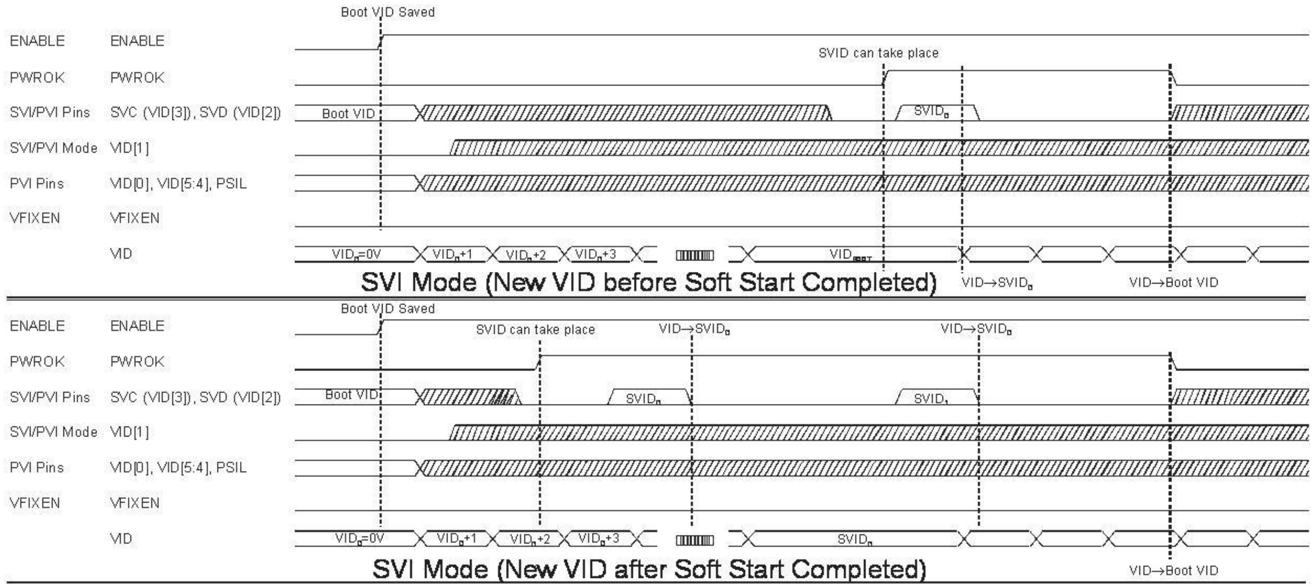


**Figure 11. Power Up Sequences Before and After Soft Start in SVI Mode**

### Hardware Jumper Override – V_FIX

VFIX is an active low pin and when it is pulled low, the controller enters V_FIX mode.The voltage regulator can be powered when an external SVI bus master is not present. When in VFIX mode, all of the voltage regulator's output voltages will be governed by the information shown in Table 3, regardless of the state of PWROK. VFIX mode is for debug and bring-up only. If VFIX mode is necessary for processor bring-up, VFIXEN, SVC, and SVD should be connected with jumpers to either ground or VDDIO through suitable pull-up resistors. SVC and SVD are considered as static VID and the output voltage will change according to their status.

**Table 3. SVI VFIX VID CODES (TWO-BIT PARALLEL)**

| SVC | SVD | $V_{OUT}$ (V) |
|---|---|---|
| 0 | 0 | 1.4 |
| 0 | 1 | 1.2 |
| 1 | 0 | 1.0 |
| 1 | 1 | 0.8 |

Start-up sequences are presented below:

- Boot VID is captured from SVC and SVD pins on rising edge of ENABLE.
- This capture is *INDEPENDENT* of any other signal. SVI/PVI is determined by sampling VID[1] during rising edge of ENABLE (SVI: VID[1]=0, PVI: VID[1]=1). Once SVI/PVI is determined, the VID controller is enabled and increments to the Boot VID at the Soft Start rate. VFIXEN mode is entered once VFIXEN is asserted.
- If VFIXEN is asserted prior to the VID controller reaching the Boot VID, the VID controller will move to the VFIXEN VID. Once the first VID value is reached (either BOOT VID or VFIXEN VID), the VID will now increment at the Normal rate. Once the VID controller is enabled, the VID controller can receive VFIXEN VIDs, independent of PWROK which is ignored in VFIXEN mode.
- If VFIXEN is de-asserted, the device PORs. This occurs independent of ENABLE

### PWROK De-assertion

Anytime PWROK de-asserts while EN is asserted, the controller uses the previously stored *BOOT VID* and regulates all planes to that level performing an on-the-Fly transition to that level. PWRGOOD remains asserted in this process.

## Protection Features:

### Undervoltage Lockout

An undervoltage lockout (UVLO) senses the VCC and VCCP input. During powerup, the input voltage to the controller is monitored, and the PWM outputs and the soft-start circuit are disabled until the input voltage exceeds the threshold voltage of the UVLO comparator. The UVLO comparator incorporates hysteresis to avoid chattering, since VCC is likely to decrease as soon as the converter initiates soft-start.

### Overcurrent Shutdown

A programmable overcurrent function is incorporated within the IC. A comparator and latch make up this function. The inverting input of the comparator is connected to the ILIM pin. The voltage at this pin sets the maximum output current the converter can produce. The ROSC pin provides a convenient and accurate reference voltage from which a resistor divider can create the overcurrent setpoint voltage. Although not actually disabled, tying the ILIM pin directly to the ROSC pin sets the limit above useful levels - effectively disabling overcurrent shutdown. The comparator noninverting input is the summed current information from the VDRP minus offset voltage. The overcurrent latch is set when the current information exceeds the voltage at the ILIM pin. The outputs are pulled low, and the soft-start is pulled low. The outputs will remain disabled until the VCC voltage is removed and re-applied, or the ENABLE input is brought low and then high.

### Output Overvoltage and Undervoltage Protection and Power Good Monitor

An output voltage monitor is incorporated. During normal operation, if the output voltage is 250 mV over the DAC voltage, the PWRGOOD goes low, the DRVON signal remains high, the PWM outputs are set low. The outputs will remain disabled until the VCC voltage is removed and reapplied. Every time the OV is triggered it will increment the OV counter. If the counter reaches a count of 16 then the OV condition will latch into a permanent OV state. It will require POR or disable/enable to restart. Prior to latching if the OV condition goes away then normal operation will resume. An OV decrement counter is also incorporated. It consists of a free-running clock which runs at 8x the PWM frequency. So essentially every 4096 PWM cycles the OV counter will decrement. For example, for a max PWM frequency of 1 MHz, the counter decrements roughly every 4 ms and for a PWM frequency of 400 kHz, it would be about every 10 ms. During normal operation, if the output voltage falls more than 350_mV below the DAC setting, the PWRGOOD pin will be set low until the output voltage rises.

### Soft-Start

The NCP5393 simply ramps $V_{core}$ to boot voltage at a fixed rate of 2 ms (0.8 mV/uS), and then reads the VID pins to determine the DAC setting. Then ramps $V_{core}$ to the final DAC setting at the Dynamic VID slew rate of up to 3.25 mV/μS. In SVI mode, SoftStart Time is intended as the time required by the device to set the output voltages to the *Pre-PWROK Metal VID. In PVI mode,* VID[0:5] or V_FIX VID in V_FIX mode are the set output voltages. Typical soft start sequence timing in SVI mode is given in Figure 12.

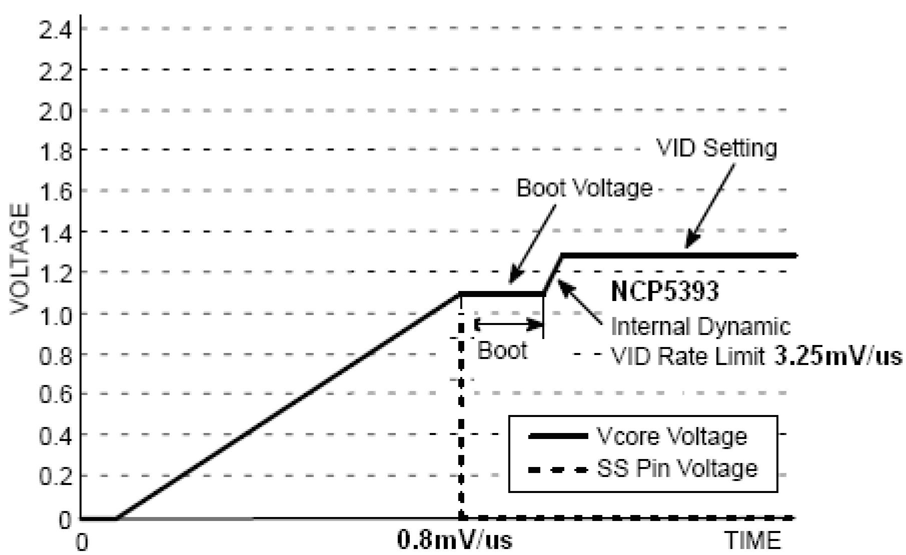



**Figure 12. Soft-Start Sequence to Vcore = 1.3 V**

### Programming the Current Limit and the Oscillator Frequency

The demo board is set for an operating frequency of approximately 330 kHz. The ROSC pin provides a 2.0 V reference voltage which is divided down with a resistor divider and fed into the current limit pin ILIM. Calculate the total series resistance to set the frequency and then calculate the individual RLIM1 and RLIM2 values for the divider.

The series resistors RLIM1 and RLIM2 sink current from the ILIM pin to ground. This current is internally mirrored into a capacitor to create an oscillator. The period is proportional to the resistance and frequency is inversely proportional to the total resistance. The total resistance may be estimated by Equation 2. This equation is valid for the individual phase frequency in both three and four phase mode.

$$R_{TOTAL} \cong 24686 \times Fsw^{-1.1549}$$
$$30.5 \cdot k\Omega \cong 24686 \times 330^{-1.1549} \quad \text{(eq. 1)}$$

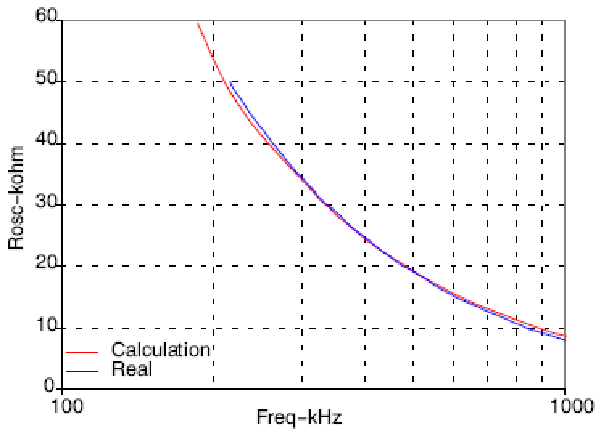



**Figure 13. ROSC vs. Frequency**

The current limit function is based on the total sensed current of all phases multiplied by a gain of 6. DCR sensed inductor current is function of the winding temperature. The best approach is to set the maximum current limit based on the expected average maximum temperature of the inductor windings.

$$DCR_{Tmax} = DCR_{25C} \cdot (1 + 0.00393\,(T_{max} - 25)) \quad \text{(eq. 2)}$$

Calculate the current limit voltage:

$$V_{ILIMIT} \cong 6 \cdot \left( I_{MIN\_OCP} \cdot DCR_{Tmax} + \frac{DCR_{Tmax} \cdot Vout}{2 \cdot Vin \cdot F_{SW}} \cdot \left( \frac{Vin - Vout}{L} - (N-1) \cdot \frac{Vout}{L} \right) \right) \quad \text{(eq. 3)}$$

Solve for the individual resistors:

$$RLIM2 = \frac{V_{ILIMIT} \cdot R_{TOTAL}}{2 \cdot V} \quad \text{(eq. 4)}$$

$$RLIM1 = R_{TOTAL} - R_{LIM2} \quad \text{(eq. 5)}$$

#### Final Equation for the Current Limit Threshold

$$I_{LIMIT}(T_{inductor}) \cong \frac{\left(\frac{2 \cdot V \cdot RLIM2}{RLIM1 + RLIM2}\right)}{6 \cdot (DCR_{25C} \cdot (1 + 0.00393(T_{Inductor} - 25)))} - \frac{Vout}{2 \cdot Vin \cdot F_{SW}} \cdot \left( \frac{Vin - Vout}{L} - (N-1) \cdot \frac{Vout}{L} \right) \quad \text{(eq. 6)}$$

The inductors on the demo board have a DCR at 25°C of 0.75 mΩ. Selecting the closest available values of 16.9 kΩ for RLIM1 and 13.7 kΩ for RLIM2 yield a nominal operating frequency of 330 kHz and an approximate current limit of 152 A at 100°C. The total sensed current can be observed as a scaled voltage at the VDRP pin added to a positive, no-load offset of approximately 1.3 V.

**OUTPUT OFFSET VOLTAGES**

External offset voltages from 0 mv to 800 mV ‘above the DAC’ can be added for the $V_{DD}$ and $V_{DD\_NB}$ independently. Offset is set by a resistor divider from $V_{CC}$ to GND. Output offsets are ratiometric to $V_{CC}$. As $V_{CC}$ changes, the on−chip scaling factors change by the same amount:

$$\text{Offset} = 0.8\text{ V x } V_{OFFSET}/V_{CC}$$

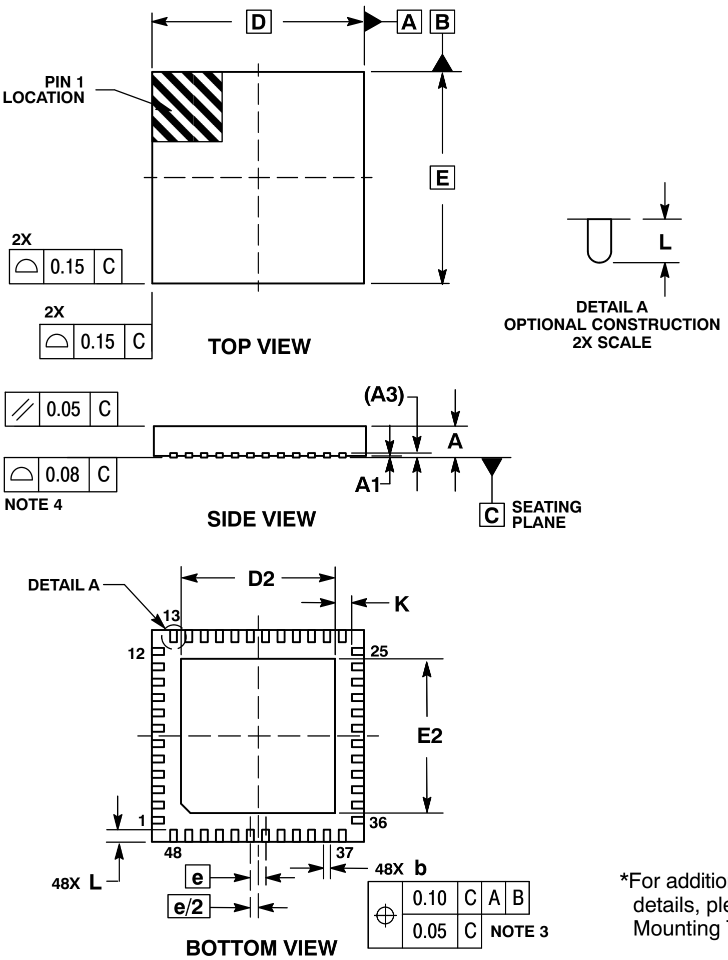
For example: For 0 V offset: pin voltage = GND; For 800 mV offset: pin voltage = $V_{CC}$

| Minimum Voffset_IN (as Vin/Vcc) | Typical Voffset_IN (as Vin/Vcc) | Maximum Voffset_IN (as Vin/Vcc) | Resulting Output Offset | Units |
|---|---|---|---|---|
| 0 | 0 | 0.046875 | 0 | mV |
| 0.046875 | 0.06250 | 0.078125 | 25 | mV |
| 0.078125 | 0.09375 | 0.109375 | 50 | mV |
| 0.109375 | 0.12500 | 0.140625 | 75 | mV |
| 0.140625 | 0.15625 | 0.171875 | 100 | mV |
| 0.171875 | 0.18750 | 0.203125 | 125 | mV |
| 0.203125 | 0.21875 | 0.234375 | 150 | mV |
| 0.234375 | 0.25000 | 0.265625 | 175 | mV |
| 0.265625 | 0.28125 | 0.296875 | 200 | mV |
| 0.296875 | 0.31250 | 0.328125 | 225 | mV |
| 0.328125 | 0.34375 | 0.359375 | 250 | mV |
| 0.359375 | 0.37500 | 0.390625 | 275 | mV |
| 0.390625 | 0.40625 | 0.421875 | 300 | mV |
| 0.421875 | 0.43750 | 0.453125 | 325 | mV |
| 0.453125 | 0.46875 | 0.484375 | 350 | mV |
| 0.484375 | 0.50000 | 0.515625 | 375 | mV |
| 0.515625 | 0.53125 | 0.546875 | 400 | mV |
| 0.546875 | 0.56250 | 0.578125 | 425 | mV |
| 0.578125 | 0.59375 | 0.609375 | 450 | mV |
| 0.609375 | 0.62500 | 0.640625 | 475 | mV |
| 0.640625 | 0.65625 | 0.671875 | 500 | mV |
| 0.671875 | 0.68750 | 0.703125 | 525 | mV |
| 0.703125 | 0.71875 | 0.734375 | 550 | mV |
| 0.734375 | 0.75000 | 0.765625 | 575 | mV |
| 0.765625 | 0.78125 | 0.796875 | 600 | mV |
| 0.796875 | 0.81250 | 0.828125 | 625 | mV |
| 0.828125 | 0.84375 | 0.859375 | 650 | mV |
| 0.859375 | 0.87500 | 0.890625 | 675 | mV |
| 0.890625 | 0.90625 | 0.921875 | 700 | mV |
| 0.921875 | 0.93750 | 0.953125 | 725 | mV |
| 0.953125 | 0.96875 | 0.984375 | 750 | mV |
| 0.984375 | 1.00000 | Vcc+0.3V | 800 | mV |

The input to the OFFSET pin for the VDD output is encoded by an internal ADC.
The input to the NB_OFFSET pin for the VDDNB output is encoded by the same ADC.
The reference for this ADC is VCC. The ADC’s output is ratiometric to VCC.
Voffset IN represents the voltage applied to the OFFSET or NB_OFFSET pin.
It is intended that these voltages be derived by a resistive divider from Vcc.
The recommended total driving impedance is <10 kilohms.

## PACKAGE DIMENSIONS

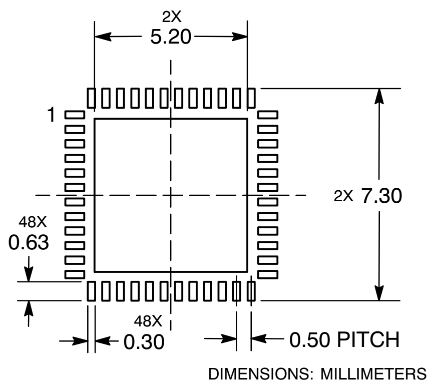
**QFN48 7x7, 0.5P**
CASE 485AJ−01
ISSUE O




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 7.00 BSC | |
| D2 | 5.00 | 5.20 |
| E | 7.00 BSC | |
| E2 | 5.00 | 5.20 |
| e | 0.50 BSC | |
| K | 0.20 | −−− |
| L | 0.30 | 0.50 |

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NCP5393), may be covered by one or more of the following U.S. patents, #US07057381. There may be other patents pending.



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