

July 1994

High Speed Precision Sample and Hold Amplifier

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Gain, DC 2×10^6 V/V (Typ)
- Acquisition Time $1.0 \mu\text{s}$ (0.01%) (Typ)
- Droop Rate $0.08 \mu\text{V}/\mu\text{s}$ (+25°C) (Typ)
 $17 \mu\text{V}/\mu\text{s}$ (Full Temperature) (Typ)
- Aperture Time 25ns (Typ)
- Hold Step Error 1.0mV (Typ)
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Applications

- High Bandwidth Precision Data Acquisition Systems
- Inertial Navigation and Guidance Systems
- Ultrasonics
- SONAR / RADAR
- Digital to Analog Converter Deglitcher

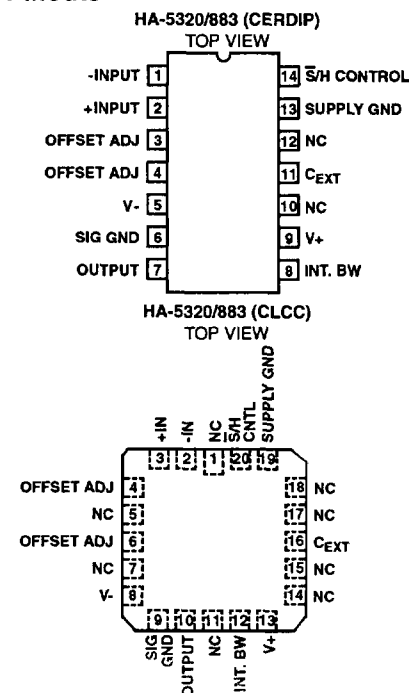
Description

The HA-5320/883 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. For further information, please see Application Note AN538.

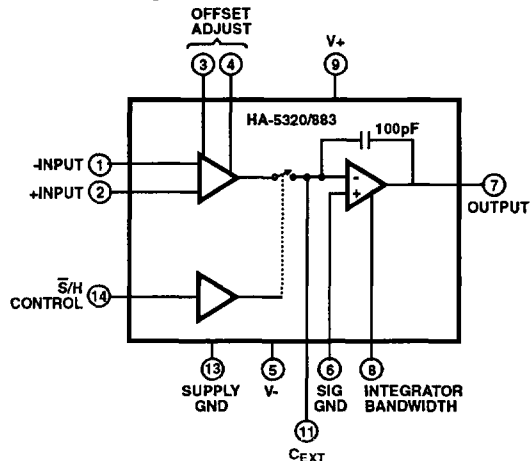
Pinouts



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-5320/883	-55°C to +125°C	14 Lead CerDIP
HA4-5320/883	-55°C to +125°C	20 Lead Ceramic LCC

Functional Diagram



Specifications HA-5320/883

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals	40V
Differential Input Voltage	24V
Digital Input Voltage (S/H Pin)	+8V, -15V
Output Current, Continuous (Note 1)	±20mA
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+175°C
Lead Temperature (Soldering 10s)	+300°C
ESD Classification	<2000V

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	66°C/W	16°C/W
Ceramic LCC Package	57°C/W	9°C/W
Package Power Dissipation at +75°C		
CerDip Package	1.5W	
Ceramic LCC Package	1.75W	
Package Power Dissipation Derating Factor Above +75°C		
CerDip Package	15mW/°C	
Ceramic LCC Package	17mW/°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range	-55°C ≤ T _A ≤ +125°C	Logic Level Low (V _{IL})	0.0V to 0.8V
Operating Supply Voltage (±V _S)	±15V	Logic Level High (V _{IH})	2.0V to 5.0V
Analog Input Voltage	±10V		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = +15V; V- = -15V; V_{IL} = 0.8V (Sample); V_{IH} = 2.0V (Hold); C_H = Internal = 100pF; Signal GND = Supply GND, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Offset Voltage	V _{IO}		1	+25°C	-1	+1	mV
			2, 3	+125°C, -55°C	-2	+2	mV
Input Bias Current	+I _B		1	+25°C	-200	+200	nA
			2, 3	+125°C, -55°C	-200	+200	nA
	-I _B		1	+25°C	-200	+200	nA
			2, 3	+125°C, -55°C	-200	+200	nA
Input Offset Current	I _{IO}		1	+25°C	-100	+100	nA
			2, 3	+125°C, -55°C	-100	+100	nA
Open Loop Voltage Gain	+A _{VS}	R _L = 1kΩ, V _{OUT} = +10V	1	+25°C	120	-	dB
			2, 3	+125°C, -55°C	110	-	dB
	-A _{VS}	R _L = 1kΩ, V _{OUT} = -10V	1	+25°C	120	-	dB
			2, 3	+125°C, -55°C	110	-	dB
Common Mode Rejection Ratio	+CMRR	V+ = 10V, V- = -20V, V _{OUT} = -5V, V _{SH} = -4.2V, V _{GND} = -5V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	V+ = 20V, V- = -10V, V _{OUT} = +5V, V _{SH} = 5.8V, V _{GND} = +5V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Output Current	+I _O	V _{OUT} = +10V	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	-I _O	V _{OUT} = -10V	1	+25°C	-10	-	mA
			2, 3	+125°C, -55°C	-10	-	mA

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Spec Number **511096-883**

Specifications HA-5320/883

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $V_+ = +15V$; $V_- = -15V$; $V_{IL} = 0.8V$ (Sample); $V_{IH} = 2.0V$ (Hold); $C_H = \text{Internal} \approx 100pF$; Signal GND = Supply GND, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	$+V_{OP}$	$R_L = 1k\Omega$	1	$+25^\circ C$	10	-	V
			2, 3	$+125^\circ C, -55^\circ C$	10	-	V
	$-V_{OP}$	$R_L = 1k\Omega$	1	$+25^\circ C$	-	-10	V
			2, 3	$+125^\circ C, -55^\circ C$	-	-10	V
Power Supply Current	$+I_{CC}$	$V_{OUT} = 0V, I_{OUT} = 0mA$	1	$+25^\circ C$	-	13	mA
			2, 3	$+125^\circ C, -55^\circ C$	-	13	mA
	$-I_{CC}$	$V_{OUT} = 0V, I_{OUT} = 0mA$	1	$+25^\circ C$	-13	-	mA
			2, 3	$+125^\circ C, -55^\circ C$	-13	-	mA
Power Supply Rejection Ratio	+PSRR	$V_+ = 14.5V, 15.5V$ $V_- = -15V, -15V$	1	$+25^\circ C$	80	-	dB
			2, 3	$+125^\circ C, -55^\circ C$	80	-	dB
	-PSRR	$V_+ = +15V, +15V$ $V_- = -14.5V, -15.5V$	1	$+25^\circ C$	65	-	dB
			2, 3	$+125^\circ C, -55^\circ C$	65	-	dB
Digital Input Current	I_{INL}	$V_{IN} = 0V$	1	$+25^\circ C$	-	4	μA
			2, 3	$+125^\circ C, -55^\circ C$	-	10	μA
	I_{INH}	$V_{IN} = 5V$	1	$+25^\circ C$	-	0.1	μA
			2, 3	$+125^\circ C, -55^\circ C$	-	0.1	μA
Digital Input Voltage	V_{IL}		1	$+25^\circ C$	-	0.8	V
			2, 3	$+125^\circ C, -55^\circ C$	-	0.8	V
	V_{IH}		1	$+25^\circ C$	2.0	-	V
			2, 3	$+125^\circ C, -55^\circ C$	2.0	-	V
Output Voltage Droop Rate	V_D	$V_{OUT} = 0V$	2	$+125^\circ C$	-	100	$\mu V/\mu s$

NOTE:

1. Internal power dissipation may limit output current below 20mA.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See AC Specifications in Table 3.

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Hold Mode Feedthrough	V_{HMF}	$V_{IN} = 10V_{P-P}$, 100kHz	1	+25°C	-	3	mV
Hold Step Error	V_{ERROR}	$V_{IH} = 3.5V$, $V_{IL} = 0V$, $T_{RISE} (V_{IL} \text{ to } V_{IH}) = 10ns$	1	+25°C	-11	11	mV
Sample Mode Noise Voltage	$E_{N(SAMPLE)}$	DC to 10MHz, $V_{SH} = 0V$, $R_{LOAD} = 2k\Omega$	1	+25°C	-	200	μV_{RMS}
Hold Mode Noise Voltage	$E_{N(HOLD)}$	DC to 10MHz, $V_{SH} = 5V$, $R_{LOAD} = 2k\Omega$	1	+25°C	-	200	μV_{RMS}
Input Capacitance	C_{IN}	$V_{SH} = 0V$	1	+25°C	-	5	pF
Input Resistance	R_{IN}	$V_{SH} = 0V$, Delta $V_{IN} = 20V$	1	+25°C	1	-	M Ω
Slew Rate	+SR	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = -5V \text{ to } +5V \text{ Step}$ 10%, 90% pts	1	+25°C	30	-	V/ μs
	-SR	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = +5V \text{ to } -5V \text{ Step}$ 10%, 90% pts	1	+25°C	30	-	V/ μs
Rise and Fall Times	T_R	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } +200mV \text{ Step}$ 10%, 90% pts	1	+25°C	-	150	ns
	T_F	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } -200mV \text{ Step}$ 10%, 90% pts	1	+25°C	-	150	ns
Overshoot	+OS	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } +200mV \text{ Step}$	1	+25°C	-	25	%
	-OS	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } -200mV \text{ Step}$	1	+25°C	-	25	%
0.1% Acquisition Time	$T_{ACQ} 0.1\%$	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } 10V \text{ Step}$	1	+25°C	-	1.2	μs

NOTE:

- The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	-
Final Electrical Test Parameters	1(Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

NOTE:

- PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Die Characteristics**DIE DIMENSIONS:**

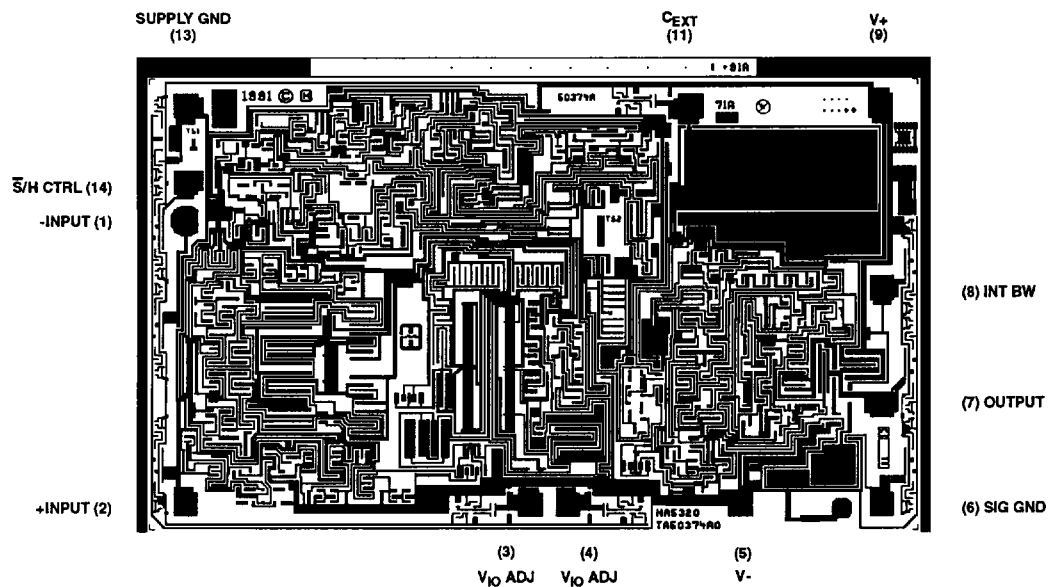
92 x 152 x 19 ± 1mils

METALLIZATION:

Type: Al, 1% Cu

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$ **GLASSIVATION:**Type: Nitride (Si_3N_4) over Silox (SiO_2 , 5% Phos)Silox Thickness: $12\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$ Nitride Thickness: $3.5\text{k}\text{\AA} \pm 1.5\text{k}\text{\AA}$ **WORST CASE CURRENT DENSITY:** $1.742 \times 10^5 \text{ A/cm}^2$ **TRANSISTOR COUNT:** 184**SUBSTRATE POTENTIAL:** V-**Metallization Mask Layout**

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