

FMS6243

Low Cost, 3-Channel, SD Video Filter Drivers with External Delay Control

Features

- Three Fourth-Order 8MHz (SD) Filters
- External Delay Control
- Transparent Input Clamping
- Dual-Video Load Drive ($2V_{PP}$, 75Ω)
- AC- or DC-Coupled Inputs
- AC- or DC-Coupled Outputs
- DC-Coupled Outputs Eliminate AC-Coupling Capacitors
- 5V Only

Applications

- Cable and Satellite Set-Top Boxes
- DVD Players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

The FMS6243 Low-Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Three fourth-order filters provide improved image quality compared to typical second- or third-order passive solutions.

The FMS6243 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required (see the *Applications Information* section for details).

Delay for each channel can be independently controlled with an external capacitor.

The outputs can drive AC- or DC-coupled single (150Ω) or dual (75Ω) loads. DC-coupling the outputs removes the need for output coupling capacitors. The input DC levels are offset approximately +280mV at the output (see the *Applications Information* section for details).

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FMS6243MTC14X	-40°C to +85°C	RoHS	14-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html

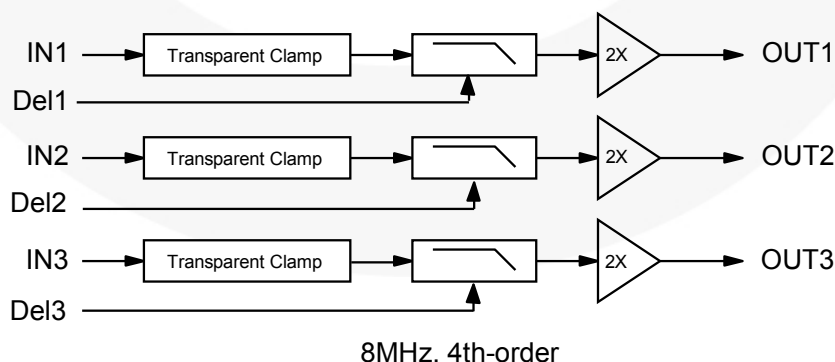


Figure 1. Block Diagram

Pin Configuration

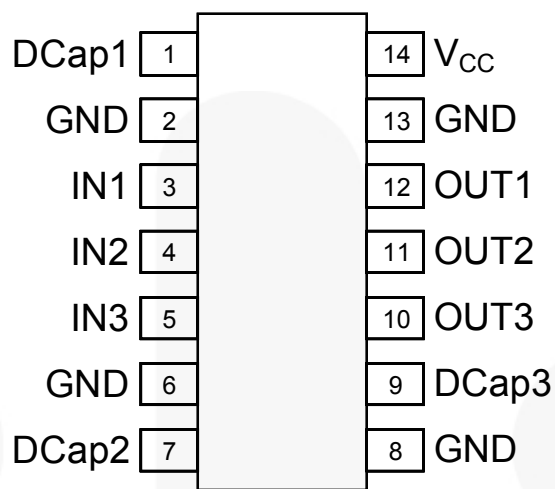


Figure 2. Pin Configuration

Pin Definitions

Pin#	Name	Type	Description
1	DCap1	Input	External group delay and Chroma / Luma delay adjustment for Channel 1
2	GND	Input	Must be tied to ground, do not float
3	IN1	Input	Video input channel 1
4	IN2	Input	Video input channel 2
5	IN3	Input	Video input channel 3
6	GND	Input	Must be tied to ground, do not float
7	DCap2	Input	External group delay and Chroma / Luma delay adjustment for Channel 2
8	GND	Input	Must be tied to ground, do not float
9	DCap3	Input	External group delay and Chroma / Luma delay adjustment for Channel 3
10	OUT3	Output	Filtered output for channel 3
11	OUT2	Output	Filtered output for channel 2
12	OUT1	Output	Filtered output for channel 1
13	GND	Input	Must be tied to ground; do not float
14	V _{CC}	Input	+5V supply; do not float

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	$V_{CC}+0.3$	V
I_{OUT}	Output Current, Any One Channel, Do Not Exceed		50	mA

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{CC}	Supply Voltage Range	4.75	5.00	5.25	V

Electrostatic Discharge Information

Symbol	Parameter	Max.	Unit
ESD	Human Body Model, JESD22-A114	8	kV
	Charged Device Model, JESD22-C101	2	

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Reflow Temperature, Soldering			+260	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard Multi-Layer Test Boards, Still Air		100		°C/W

DC Electrical Characteristics

Unless otherwise noted, $T_A=25^{\circ}\text{C}$, $V_{CC}=5.0\text{V}$, $R_{SOURCE}=37.5\Omega$, all inputs are AC coupled with $0.1\mu\text{F}$, and all outputs are AC coupled with $220\mu\text{F}$ into 150Ω loads.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current ⁽¹⁾	No Load		24	34	mA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC Coupled		1.4		V_{PP}
PSRR	Power Supply Rejection Ratio (All Channels)	DC		48		dB

Note:

1. 100% tested at 25°C .

AC Electrical Characteristics

Unless otherwise noted, $T_A=25^{\circ}\text{C}$, $V_{IN}=1V_{PP}$, $V_{CC}=5.0\text{V}$, $R_{SOURCE}=37.5\Omega$, all inputs are AC coupled with $0.1\mu\text{F}$, and all outputs are AC coupled with $220\mu\text{F}$ into 150Ω loads.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
AV	Channel Gain ⁽²⁾	All Channels	5.6	6.0	6.6	dB
f_{1dB}	-1dB Bandwidth ⁽²⁾	All Channels	5.5	6.5		MHz
f_C	-3dB Bandwidth	All Channels		8.0		MHz
f_{SB}	Attenuation (Stopband Reject)	All Channels at $f=27\text{MHz}$		44		dB
DG	Differential Gain	All Channels		0.3		%
DP	Differential Phase	All Channels		0.6		$^{\circ}$
THD	Total Harmonic Distortion, Output (All Channels)	$V_{OUT}=1.8V_{PP}$, 1MHz		0.4		%
X_{TALKSD}	Crosstalk (Channel-to-Channel)	$f=1\text{MHz}$		-70		dB
SNR	Signal-to-Noise Ratio	All Channels, Chroma Weighting; 5MHz Low Pass		75		dB

Note:

2. 100% tested at $T_A=25^{\circ}\text{C}$.

Applications Information

Functional Description

The FMS6243 Low-Cost Video Filter (LCVF) provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 3.

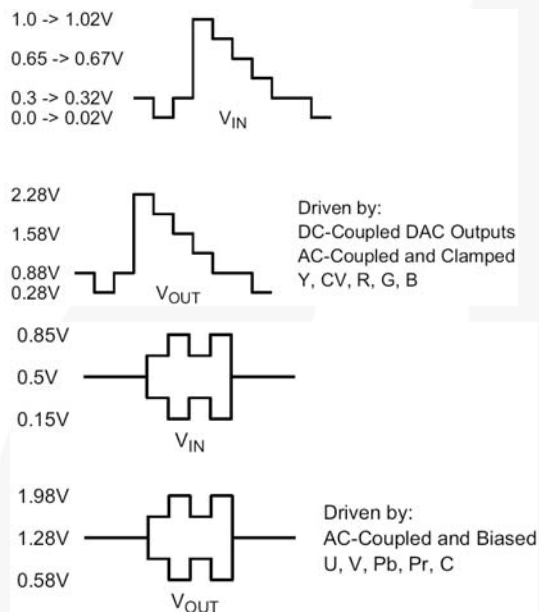


Figure 3. Typical Voltage Levels

The FMS6243 provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6243 without an AC coupling capacitor. When the input is AC coupled, the diode clamps sets the sync tip (or lowest voltage) just below ground. The worst-case sync tip compression due to the clamp does not exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within acceptable range.

For symmetric signals like Chroma, U, V, Pb, and Pr; the average DC bias is fairly constant and the inputs can be AC coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 4.

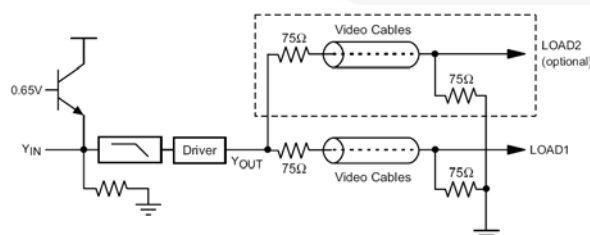


Figure 4. Input Clamp Circuit

I/O Configurations

For DC-coupled DAC drive with DC-coupled outputs, use the configuration shown in Figure 5.

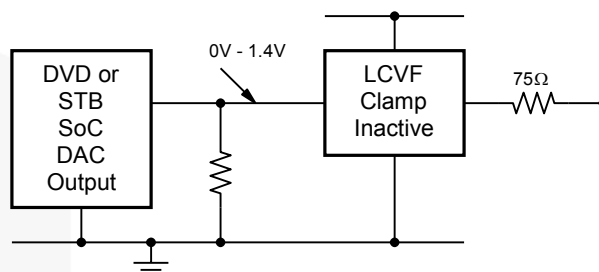


Figure 5. DC-Coupled Inputs and Outputs

If the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC-coupled as shown in Figure 6.

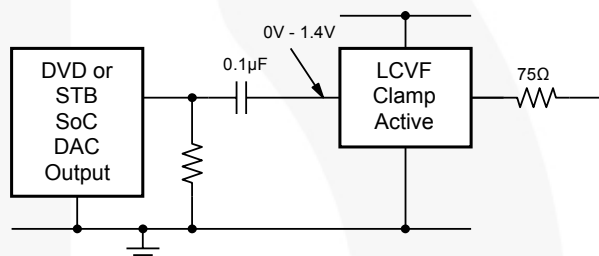


Figure 6. AC-Coupled Inputs, DC-Coupled Outputs

When driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC coupled, as shown in Figure 7.

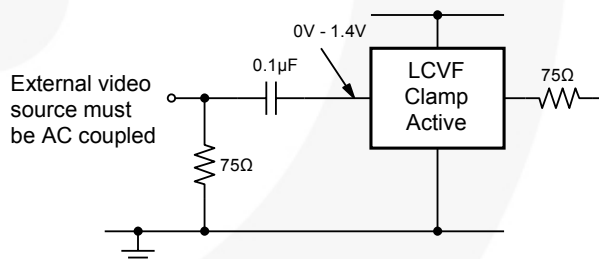


Figure 7. SCART with DC-Coupled Outputs

The same method can be used for biased signals with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is $800k\Omega \pm 20\%$, so the external resistance should be $7.5M\Omega$ to set the DC level to 500mV.

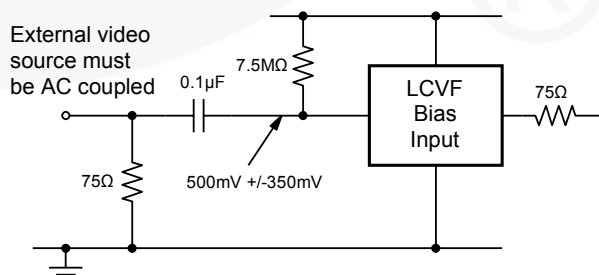


Figure 8. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired, as shown in Figure 9.

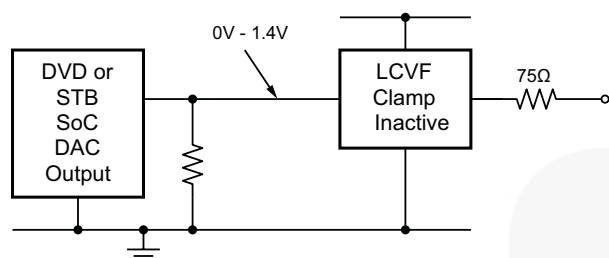


Figure 9. DC-Coupled Inputs, AC-Coupled Outputs

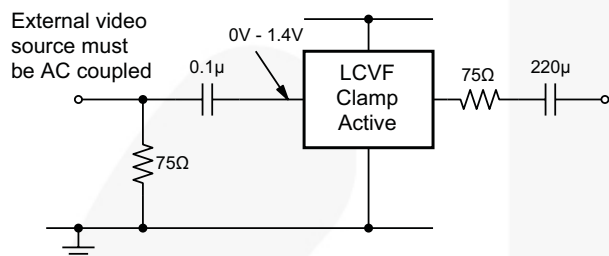


Figure 10. AC-Coupled Inputs and Outputs

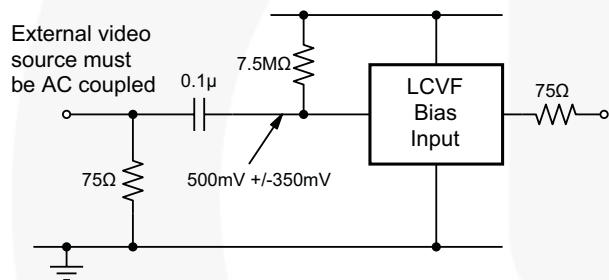


Figure 11. Biased AC-Coupled Inputs with AC-Coupled Outputs

Note:

3. The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220μF to obtain satisfactory operation in some applications.

Power Dissipation

Output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed maximum die junction temperature. The following example can be used to calculate power dissipation and internal temperature rise:

$$T_J = T_A + P_d \cdot \theta_{JA}$$

where $P_d = P_{CH1} + P_{CH2} + P_{CH3}$ and

$$P_{CHx} = V_S \cdot I_{CH} - (V_O^2 / R_L)$$

where $V_O = 2V_{IN} + 0.280V$

$$I_{CH} = (I_{CC} / 3) + (V_O / R_L)$$

V_{IN} = RMS value of input signal

$$I_{CC} = 24mA, V_S = 5V$$

R_L = channel load resistance

Board layout can affect thermal characteristics. Refer to the *Layout Considerations* section for more information.

The FMS6243 is specified to operate with output current typically less than 50mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief-duration, short-circuit conditions; however, this capability is not guaranteed.

Group Delay Adjustment

The FMS6243 has the ability to independently adjust each channel for Sin X/X group delay and Chroma/Luma delay. This is accomplished by placing a capacitor from the device delay adjust pin to ground. The group delay can be adjusted from the nominal of +10ns to -80ns. This means that, under a nominal situation, a video system may have an overall group delay measurement of +50ns. If the system specification is +40ns, the FMS6243 could be used to decrease this group delay to fall within specification with a guard band to allow for system variation.

Adding a 50pF capacitor to the desired channel DCap pin (see Figure 15) generates a -20ns delay through the FMS6243, which, when summed with the +50ns of the system, gives a new system overall group delay of +30ns. It now meets the system specification with a +10ns guard band for system group delay variation.

Figure 12 shows the effect on group delay by adding capacitance to the FMS6243 DCap pins. The correct capacitor can be chosen by determining the format of the video system (NTSC 3.58 or PAL 4.43), then choosing the desired group delay to sum with overall system delay. The desired delay and format line intersection is the delay capacitor needed for the DCap pins.

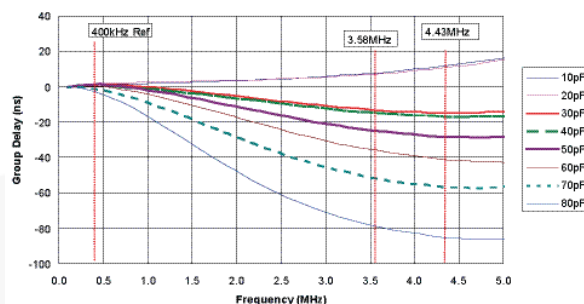


Figure 12. Group Delay vs. Delay Capacitor Value

Signal Peaking Adjustment

The peaking of a video input signal can be adjusted by placing a peaking capacitor across the series-75 Ω resistor on the output of the FMS6243. Where the input video signal to the FMS6243 has a soft roll-off, meaning the input video signal is attenuated at 4MHz by -0.5dB, the Chroma/Luma gain is approximately -5% and fails a system specification of $\pm 2.5\%$. This attenuation can be adjusted by adding a 150pF capacitor across the series-75 Ω resistor on the output (see Figure 15). This brings the attenuation at 4.0MHz to approximately 0dB, giving a Chroma/Luma gain of 0%. Figure 13 shows the peaking effect of adding a peaking capacitor across the series-75 Ω resistor. The graph shows a 10pF delay capacitor with a 10pF, 50pF, and 100pF peaking capacitor.

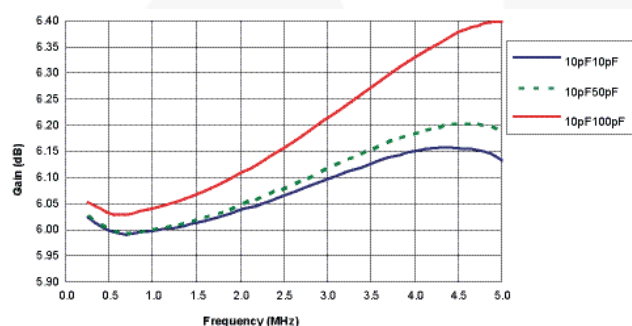


Figure 13. Frequency Response Delay Capacitor vs. Peaking Capacitor

Group Delay and Peaking Adjustment Simultaneously

If both group delay adjustment and peaking adjustment are to be incorporated in a system design, the following methodology should be followed. Address the group delay adjustment first, then the peaking adjustment, because the group delay adjustment causes video signal attenuation at 4MHz.

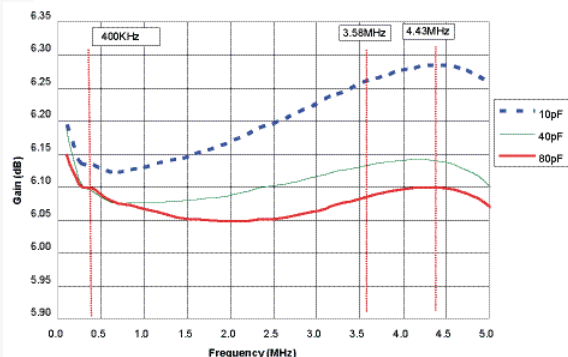


Figure 14. Frequency Response vs. Delay Capacitor Value

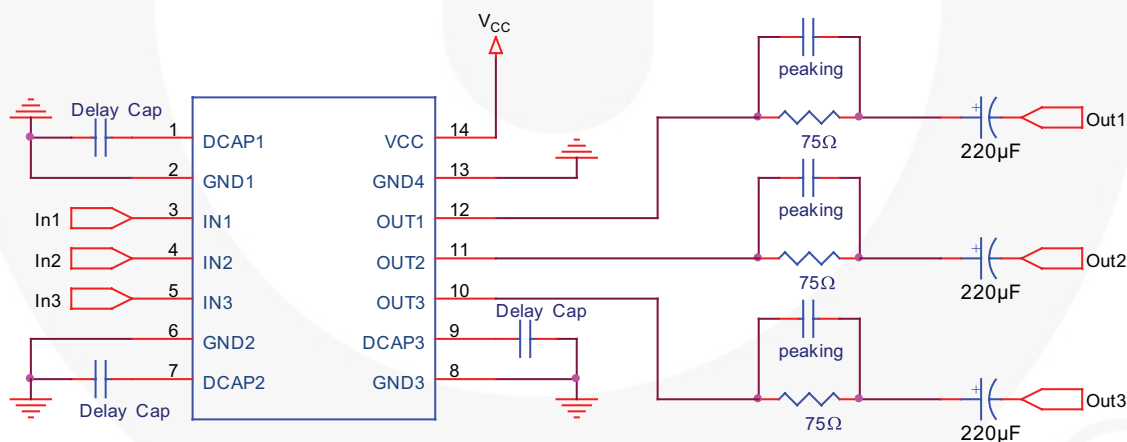


Figure 15. Schematic

Output Considerations

The FMS6243 outputs are DC offset from the input by 150mV; therefore, $V_{OUT} = 2 \cdot V_{IN} \text{ DC} + 150\text{mV}$. This offset is required to obtain optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6243 has a 2x (6dB) gain, the output is typically connected via a 75 Ω -series back-matching resistor followed by the 75 Ω video cable. Due to the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less than 1V. When AC coupling the output, ensure that the coupling capacitor of choice passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. To obtain the highest quality output video signal, the series termination resistor must be placed as close to the output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the output driver. Recommended distance from the device pin to the series termination resistor should be no greater than 0.1 inches.

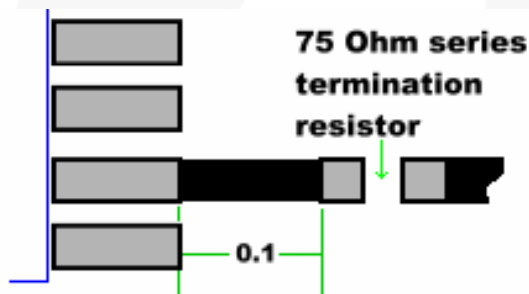


Figure 16. Distance from Device Pin to Series Termination Resistor

Layout Considerations

It is critical that the delay capacitor pins (1, 7, and 9) have the delay capacitor placed as close to the device pin as possible. The ground connection should be as short as possible, ideally a direct connection to the adjacent ground pin. These layout considerations create the best environment and reduce noise.

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board to guide layout and aid device evaluation. The evaluation board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules.

Recommended Routing / Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground / power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10 μ F and 0.1 μ F ceramic power supply bypass capacitors.
- Place the 0.1 μ F capacitor within 0.1 inches of the device power pin.
- Place the 10 μ F capacitor within 0.75 inches of the device power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body at least 0.5 inches on all sides.
- Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

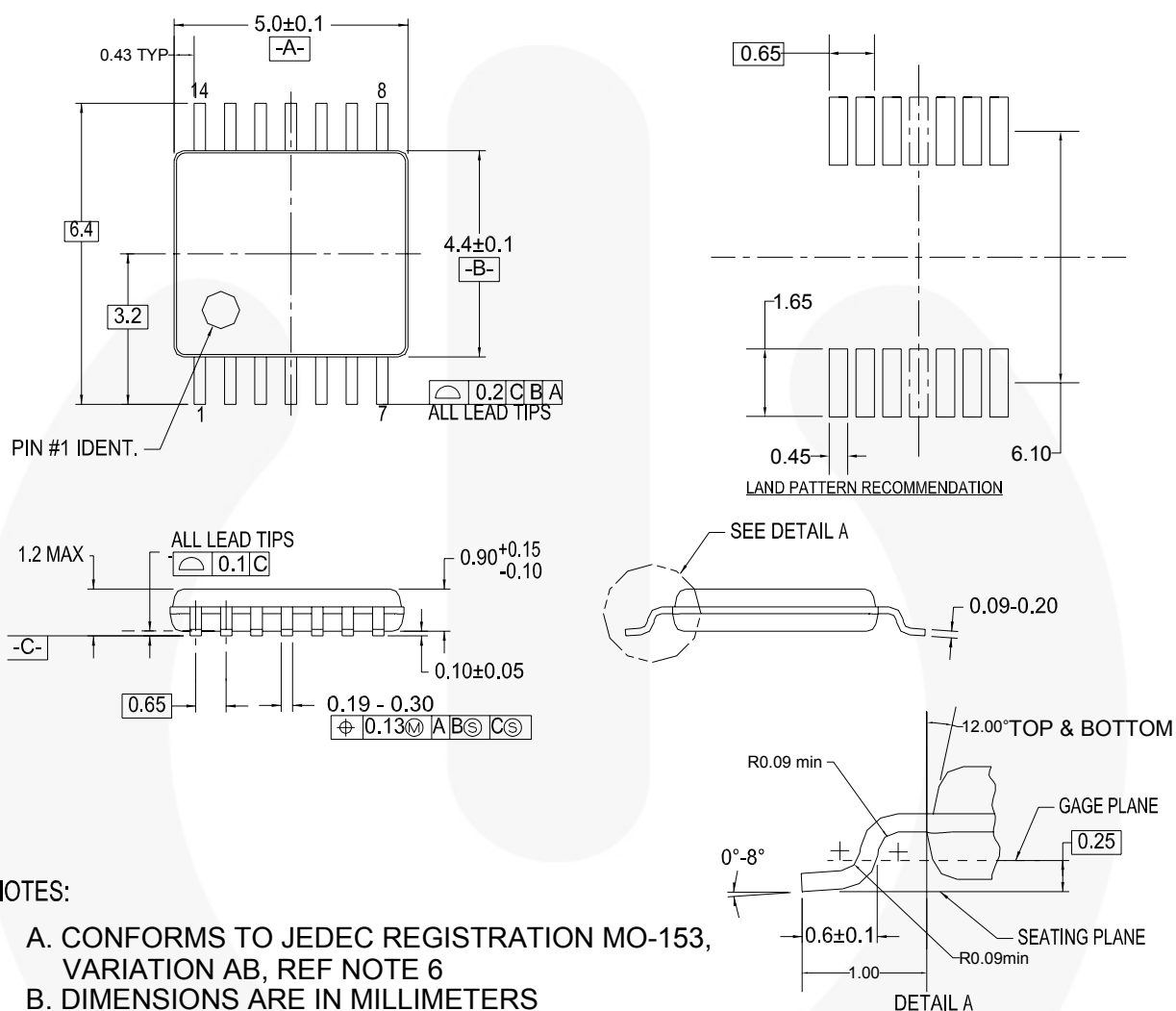
Thermal Considerations

Since the interior of most systems, such as set-top boxes, TVs, and DVD players, are at +70°C; consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane), each other on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70 μ m of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in the power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Use modeling techniques to provide first-order approximation.

Physical Dimensions



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 17. 14-Lead Thin Shrink Small Outline Package (TSSOP)

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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