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BATTERY PROTECTION IC FOR 1-CELL PACK (SECONDARY PROTECTION)

The S-8216A Series is used for secondary protection of lithium-ion / lithium polymer rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit.
The S-8216A Series has functions with an overcharge detection and a discharge overcurrent detection.

■ Features

- High-accuracy voltage detection circuit

Overcharge detection voltage	4.000 V to 5.000 V (5 mV step)	Accuracy ±15 mV
Overcharge release voltage	3.600 V to 4.950 V*1	Accuracy ±50 mV
Discharge overcurrent detection voltage	0.003 V to 0.100 V (0.5 mV step)	Accuracy ±1.5 mV

- Detection delay time is generated only by an internal circuit (external capacitors are unnecessary).
- Output logic is selectable: Active "H", active "L"
- Output form: CMOS output
- Wide operation temperature range: Ta = –40°C to +85°C
- Low current consumption
  During operation: 2.0 μA typ., 4.0 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected from a range of 0.05 V to 0.4 V in 50 mV step.)

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Package

- SNT-6A

■ Block Diagram

1. Active "H"

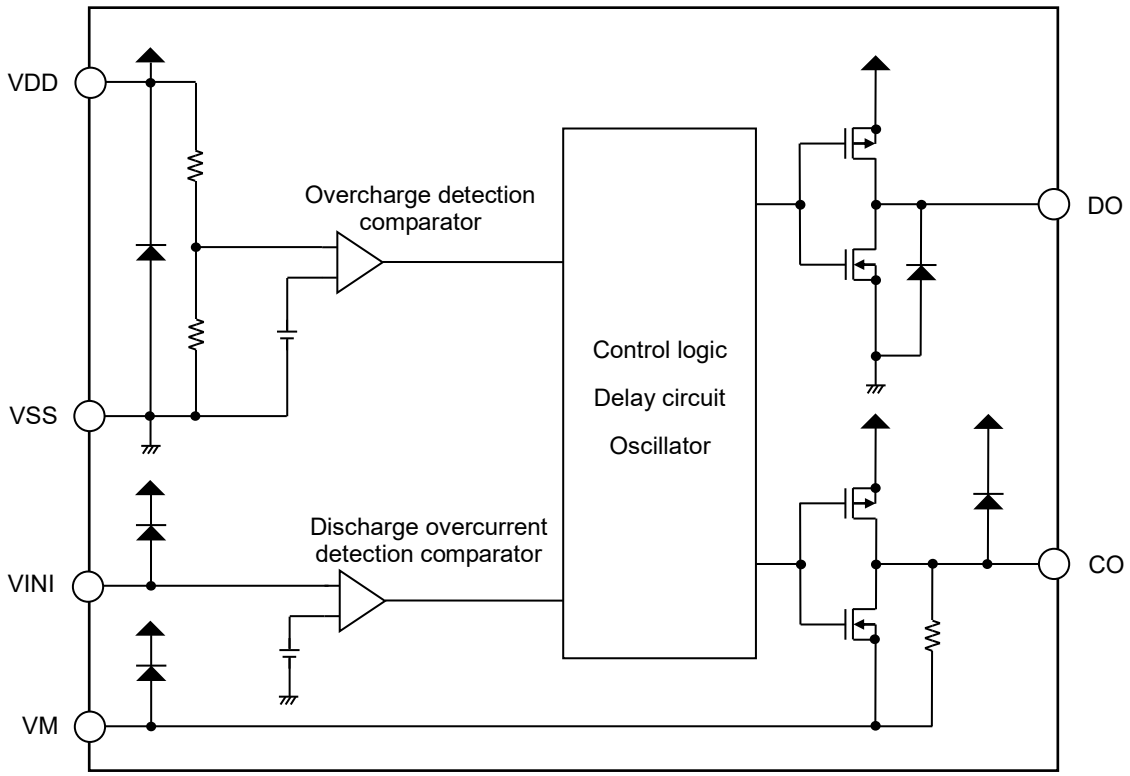


Figure 1

2. Active "L"

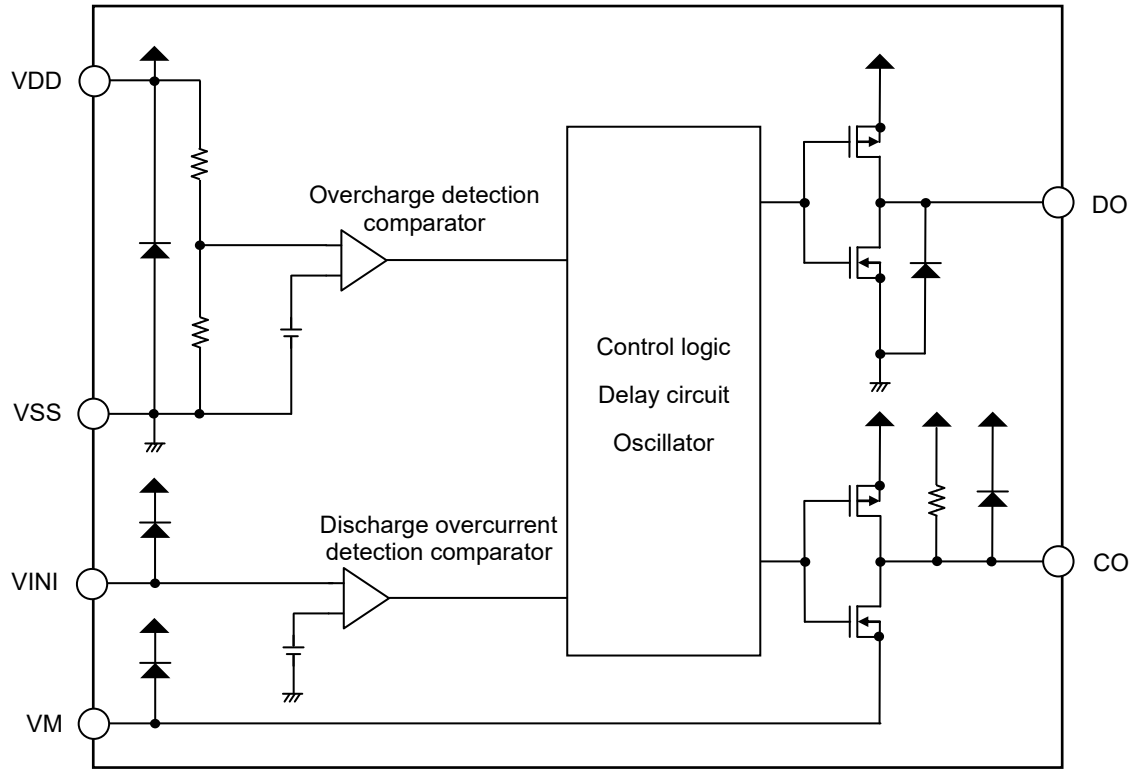


Figure 2

■ Product Name Structure

1. Product name

S-8216A xx - I6T1 U

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications*1
I6T1: SNT-6A, Tape

Serial code*2
Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product name list

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Discharge Overcurrent Detection Voltage [V_{DIOV}]	Overcharge Detection Delay Time*1 [t_{CU}]	Discharge Overcurrent Detection Delay time*2 [t_{DIOV}]	Output Logic*3
S-8216AAA-I6T1U	4.550 V	4.200 V	0.0105 V	2 s	4 s	Active "H"

***1.** Overcharge detection delay time 1 s / 2 s / 4 s is selectable.
***2.** Discharge overcurrent detection delay time 1 s / 2 s / 3.75 s / 4 s is selectable.
***3.** Output logic active "H" / active "L" is selectable.

Remark Please contact our sales office for products other than the above.

■ Pin Configurations

1. SNT-6A

Top view

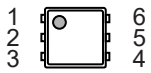


Figure 3

Table 3

Pin No.	Symbol	Description
1	VM	Negative power supply pin for CO pin
2	CO	Connection pin of charge control FET gate (CMOS output)
3	DO	Input pin for test signal
4	VSS	Input pin for negative power supply
5	VDD	Input pin for positive power supply
6	VINI	Discharge overcurrent detection pin

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 6	V
VM pin input voltage	V_{VM}	VM	V_{DD} – 28 to V_{DD} + 0.3	V
VINI pin input voltage	V_{VINI}	VINI	V_{DD} – 6 to V_{DD} + 0.3	V
DO pin input voltage	V_{DO}	DO	V_{SS} – 0.3 to V_{DD} + 0.3	V
CO pin output voltage	V_{CO}	CO	V_{DD} – 28 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SNT-6A	Board A	–	224	–	°C/W
			Board B	–	176	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Ta = +25°C

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	$V_{CU} - 0.015$	V_{CU}	$V_{CU} + 0.015$	V	1
Overcharge release voltage	V_{CL}	–	$V_{CL} - 0.050$	V_{CL}	$V_{CL} + 0.050$	V	1
Discharge overcurrent detection voltage	V_{DIOV}	–	$V_{DIOV} - 0.0015$	V_{DIOV}	$V_{DIOV} + 0.0015$	V	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	–	1.5	–	6.0	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	2.0	4.0	μA	3
Output Resistance							
CO pin resistance "H" 1	R_{COH1}	–	5	10	20	kΩ	4
CO pin resistance "L" 1	R_{COL1}	–	5	10	20	kΩ	4
DO pin resistance "H"	R_{DOH}	–	5	10	20	kΩ	4
DO pin resistance "L"	R_{DOL}	–	1	2	4	kΩ	4
CO pin resistance "H" 2	R_{COH2}	Active "L"	1	4	–	MΩ	4
CO pin resistance "L" 2	R_{COL2}	Active "H"	1	4	–	MΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.7$	t_{CU}	$t_{CU} \times 1.3$	–	5
Discharge overcurrent detection delay time	t_{DIOV}	–	$t_{DIOV} \times 0.75$	t_{DIOV}	$t_{DIOV} \times 1.25$	–	5

2. Ta = –20°C to +60°C*1

Table 7

(Ta = –20°C to +60°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	$V_{CU}-0.020$	V_{CU}	$V_{CU}+0.020$	V	1
Overcharge release voltage	V_{CL}	–	$V_{CL}-0.065$	V_{CL}	$V_{CL}+0.057$	V	1
Discharge overcurrent detection voltage	V_{DIOV}	–	$V_{DIOV}-0.002$	V_{DIOV}	$V_{DIOV}+0.002$	V	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	–	1.5	–	6.0	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	2.0	5.0	μA	3
Output Resistance							
CO pin resistance "H" 1	R_{COH1}	–	2.5	10	30	kΩ	4
CO pin resistance "L" 1	R_{COL1}	–	2.5	10	30	kΩ	4
DO pin resistance "H"	R_{DOH}	–	2.5	10	30	kΩ	4
DO pin resistance "L"	R_{DOL}	–	0.5	2	6	kΩ	4
CO pin resistance "H" 2	R_{COH2}	Active "L"	0.25	4	–	MΩ	4
CO pin resistance "L" 2	R_{COL2}	Active "H"	0.25	4	–	MΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU}\times0.6$	t_{CU}	$t_{CU}\times1.4$	–	5
Discharge overcurrent detection delay time	t_{DIOV}	–	$t_{DIOV}\times0.65$	t_{DIOV}	$t_{DIOV}\times1.35$	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM}.

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

1. 1 Active "H"

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

1. 2 Active "L"

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

2. Discharge overcurrent detection voltage (Test circuit 2)

2. 1 Active "H"

Discharge overcurrent detection voltage (V_{DIOV}) is defined as the voltage V4 whose delay time for changing V_{CO} from "L" to "H" is discharge overcurrent detection delay time (t_{DIOV}) when the voltage V4 is increased after setting V1 = 3.4 V, V4 = 0 V.
Then, when V4 drops to V_{DIOV} typ. or lower, V_{CO} goes from "H" to "L".

2. 2 Active "L"

Discharge overcurrent detection voltage (V_{DIOV}) is defined as the voltage V4 whose delay time for changing V_{CO} from "H" to "L" is discharge overcurrent detection delay time (t_{DIOV}) when the voltage V4 is increased after setting V1 = 3.4 V, V4 = 0 V.
Then, when V4 drops to V_{DIOV} typ. or lower, V_{CO} goes from "L" to "H".

3. Current consumption during operation (Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through VDD pin (I_{DD}) under the set condition of V1 = 3.4 V.

4. CO pin resistance "H" 1 (Test circuit 4)

4. 1 Active "H"

The CO pin resistance "H" 1 (R_{COH1}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 5.1 V, V2 = 4.7 V.

4. 2 Active "L"

The CO pin resistance "H" 1 (R_{COH1}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 3.0 V.

5. CO pin resistance "L" 1 (Test circuit 4)

5. 1 Active "H"

The CO pin resistance "L" 1 (RCOL1) is the resistance between VM pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 0.4 V.

5. 2 Active "L"

The CO pin resistance "L" 1 (RCOL1) is the resistance between VM pin and CO pin under the set conditions of V1 = 5.1 V, V2 = 0.4 V.

6. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V3 = 3.0 V.

7. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V3 = 0.4 V.

8. CO pin resistance "H" 2 (Active "L") (Test circuit 4)

The CO pin resistance "H" 2 (R_{COH2}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 5.1 V, V2 = 0 V.

9. CO pin resistance "L" 2 (Active "H") (Test circuit 4)

The CO pin resistance "L" 2 (R_{COL2}) is the resistance between VM pin and CO pin under the set conditions of V1 = 5.1 V, V2 = 5.1 V.

10. Overcharge detection delay time (Test circuit 5)

10. 1 Active "H"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "H" just after the voltage V1 increases and exceeds V_{CU} under the set condition of V1 = 3.4 V.

10. 2 Active "L"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "L" just after the voltage V1 increases and exceeds V_{CU} under the set condition of V1 = 3.4 V.

11. Discharge overcurrent detection delay time (Test circuit 5)

11. 1 Active "H"

The discharge overcurrent detection delay time (t_{DIOV}) is the time needed for V_{CO} to go to "H" just after the voltage V4 increases and exceeds V_{DIOV} under the set condition of V1 = 3.4 V, V4 = 0 V.

11. 2 Active "L"

The discharge overcurrent detection delay time (t_{DIOV}) is the time needed for V_{CO} to go to "L" just after the voltage V4 increases and exceeds V_{DIOV} under the set condition of V1 = 3.4 V, V4 = 0 V.

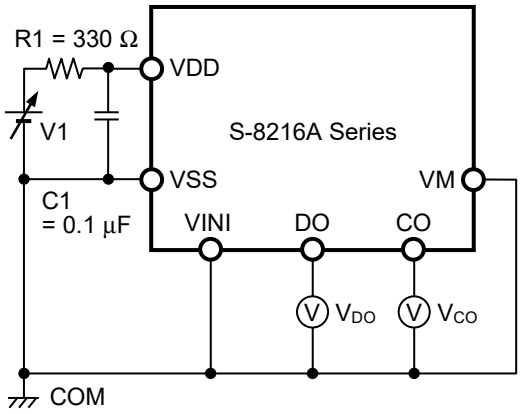


Figure 4 Test Circuit 1

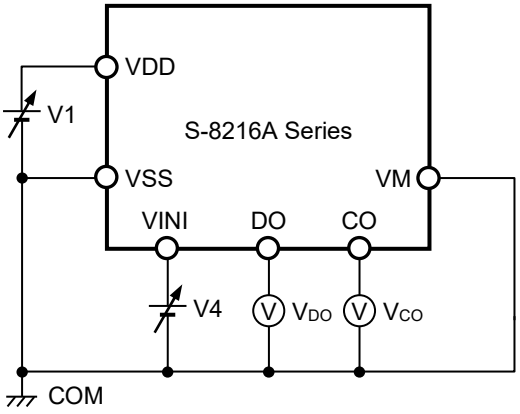


Figure 5 Test Circuit 2

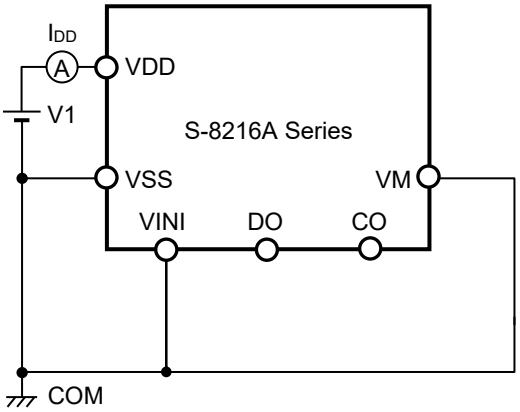


Figure 6 Test Circuit 3

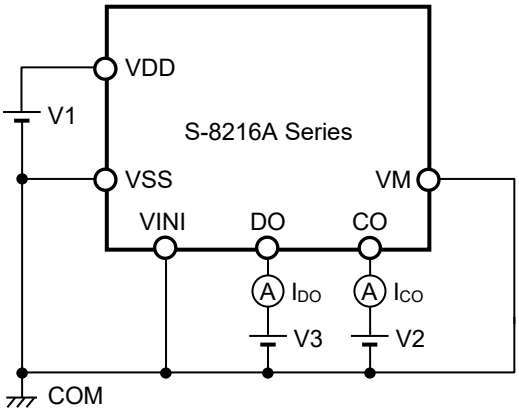


Figure 7 Test Circuit 4

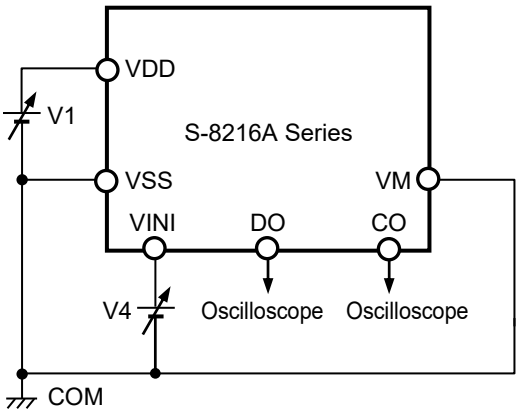


Figure 8 Test Circuit 5

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Example**".

1. Overcharge status

The S-8216A Series monitors the voltage of the battery connected between VDD pin and VSS pin to detect overcharge. When the battery voltage exceeds the overcharge detection voltage (V_{CU}) during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, the S-8216A Series outputs overcharge detection signal from the CO pin. This condition is called overcharge status. Connecting FET to the CO pin provides charge control and a second protection.

2. Discharge overcurrent status

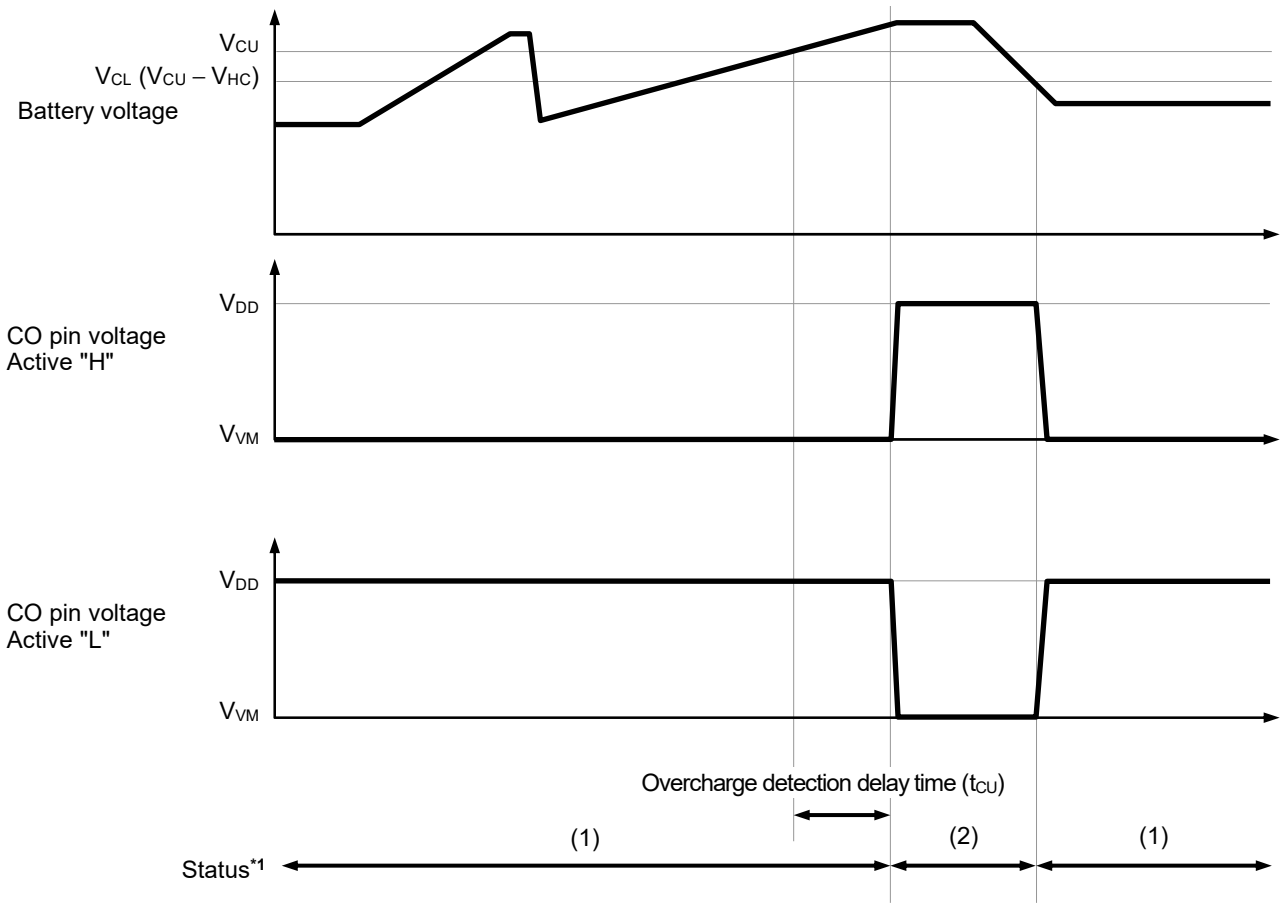
The S-8216A Series monitors the voltage of the VINI pin to detect discharge overcurrent. When the VINI pin voltage exceeds the discharge overcurrent detection voltage (V_{DIOV}) and the condition continues for the discharge overcurrent detection delay time (t_{DIOV}) or longer, the S-8216A Series outputs discharge overcurrent detection signal from the CO pin. This condition is called discharge overcurrent status. Connecting FET to the CO pin provides discharge control and a second protection.

3. Test mode

In the S-8216A Series, t_{CU} and t_{DIOV} can be shortened by forcibly setting the DO pin to V_{SS} level from external. When the DO pin is forcibly set to V_{SS} level from external, t_{CU} and t_{DIOV} will be shortened to approximately 1/64.

■ Timing Charts

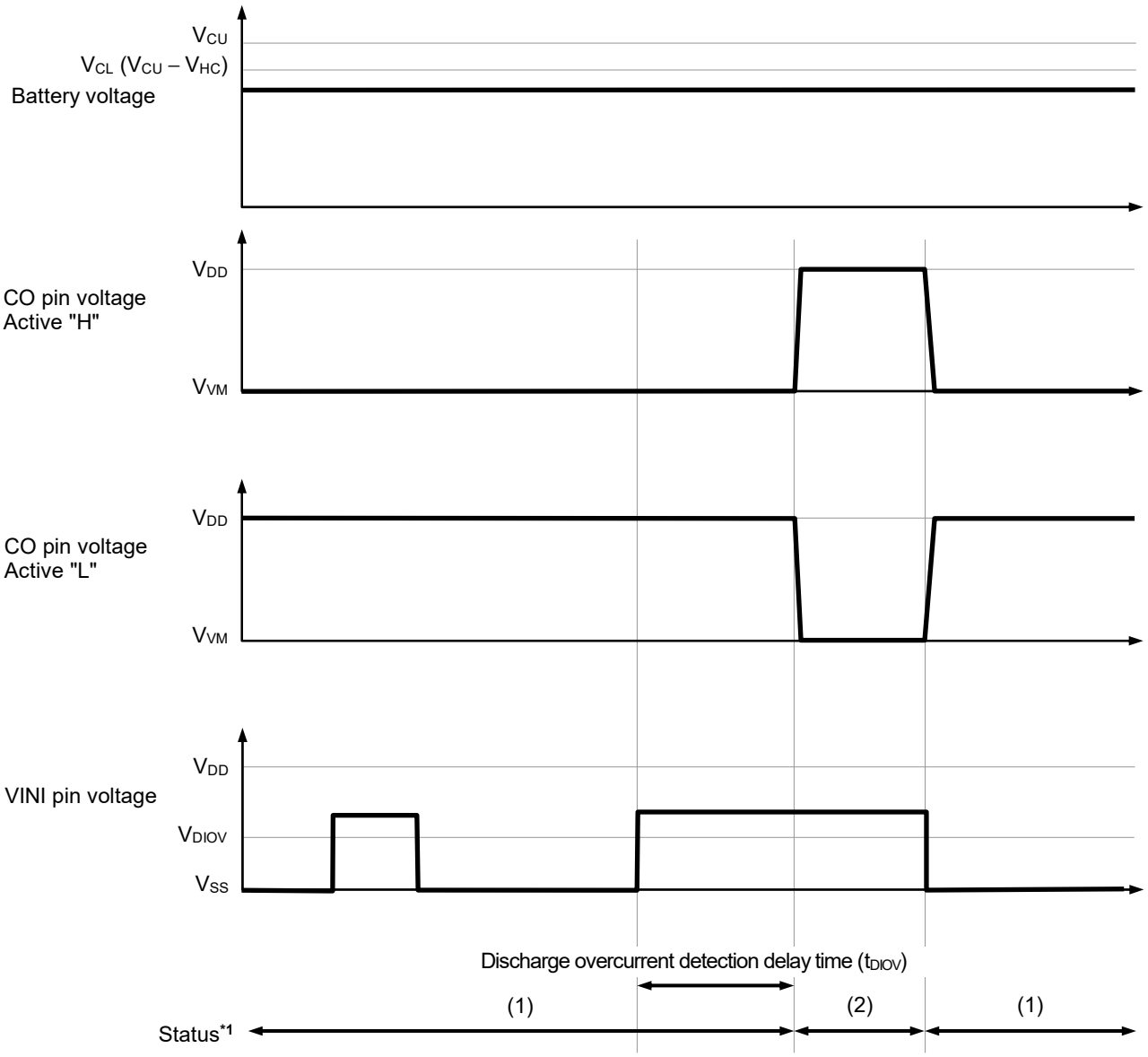
1. Overcharge detection



***1.** (1) : Normal status
(2) : Overcharge status

Figure 9

2. Discharge overcurrent detection



***1.** (1) : Normal status
(2) : Discharge overcurrent status

Figure 10

■ Battery Protection IC Connection Example

Figure 11 shows the connection example when active "H" product is used.

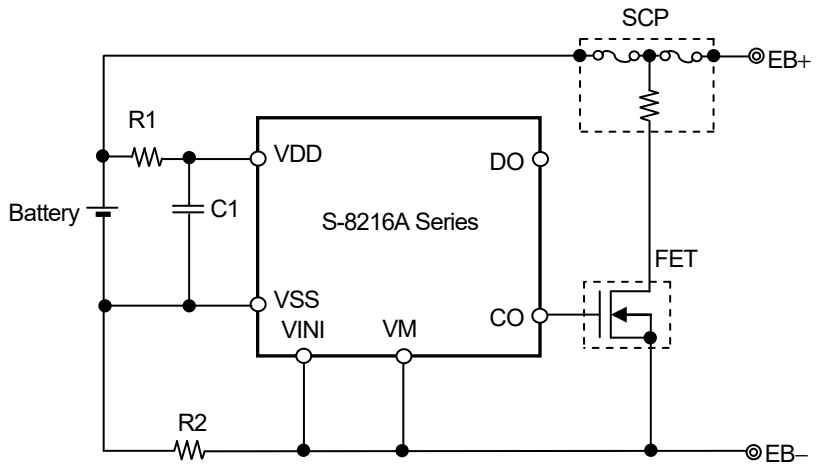


Figure 11

Table 8 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
FET	Nch MOS FET	Charge and discharge control	–	–	–	–
R1	Resistor	ESD protection, For power fluctuation	150 Ω	330 Ω	1.0 kΩ*1	–
C1	Capacitor	For power fluctuation	0.068 µF	0.1 µF	1.0 µF	–
R2	Resistor	Discharge overcurrent detection	–	3 mΩ	–	–

***1.** Accuracy of overcharge detection voltage is guaranteed by R1 = 330 Ω. Connecting resistors with other values will worsen the accuracy.

Caution 1. The above constants may be changed without notice.
2. The connection example and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

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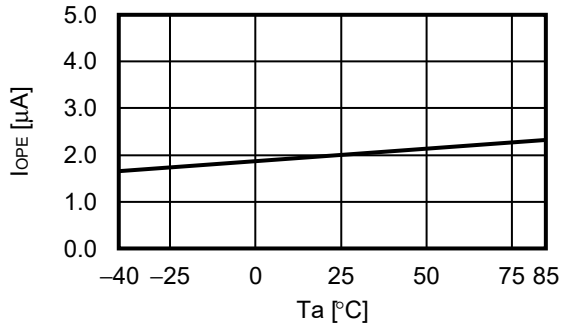
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

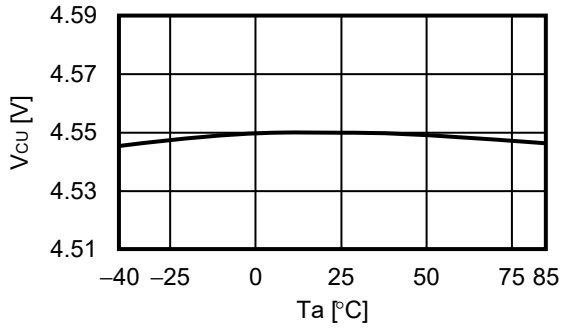
1. Current consumption

1. 1 I_{OPE} vs. Ta

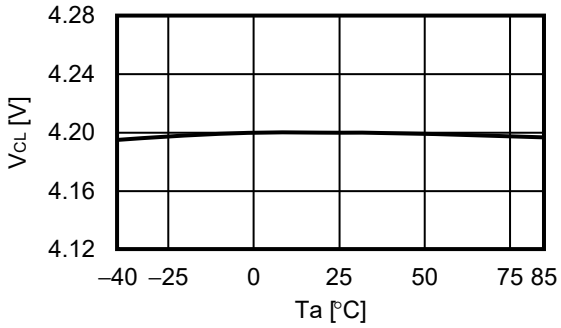


2. Detection voltage

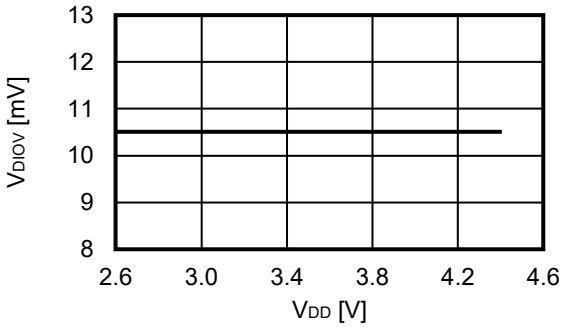
2. 1 V_{CU} vs. Ta



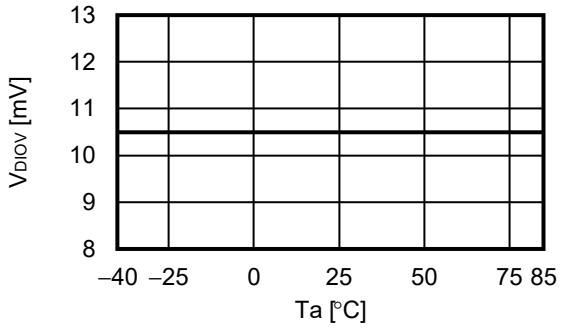
2. 2 V_{CL} vs. Ta



2. 3 V_{DIOV} vs. V_{DD}

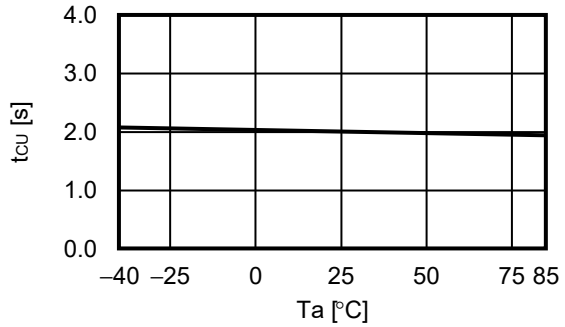


2. 4 V_{DIOV} vs. Ta

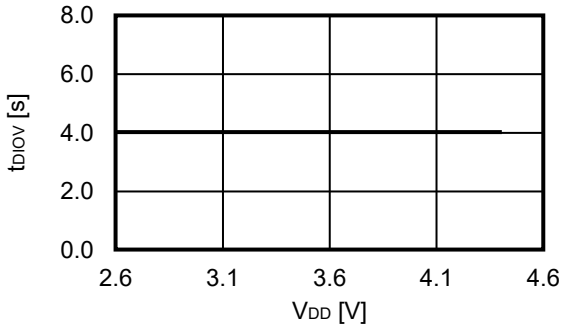


3. Delay time

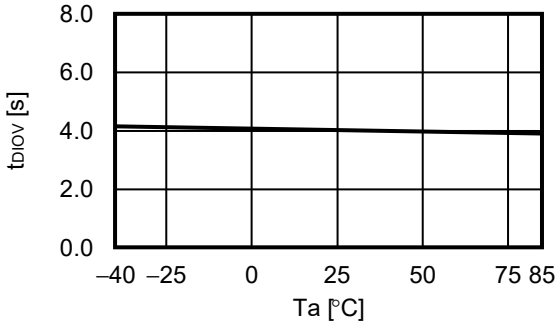
3. 1 t_{CU} vs. Ta



3. 2 t_{DIOV} vs. V_{DD}

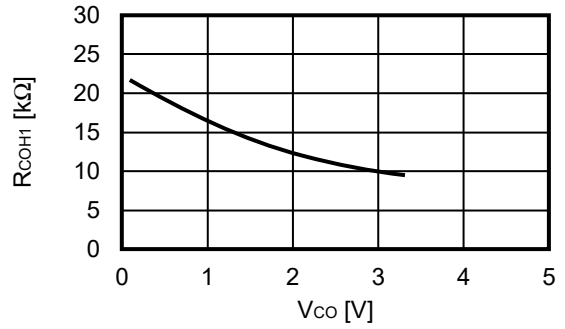


3. 3 t_{DIOV} vs. Ta

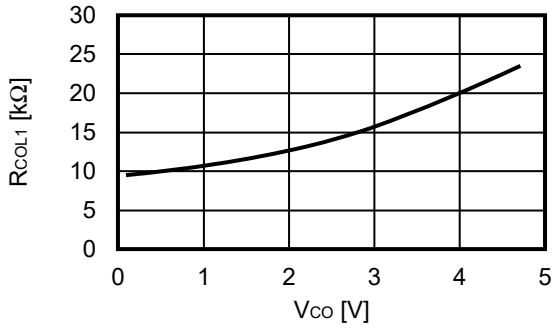


4. Output resistance

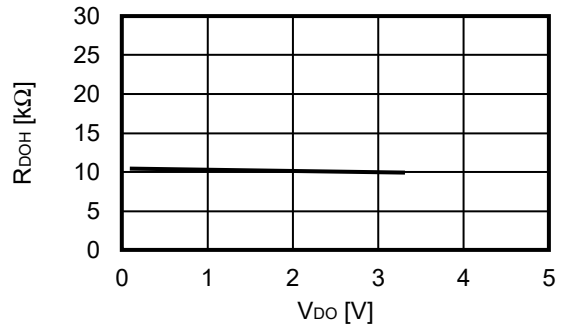
4. 1 R_{COH1} vs. V_{CO}



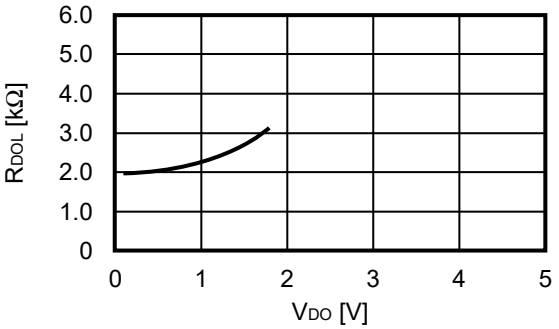
4. 2 R_{COL1} vs. V_{CO}



4. 3 R_{DOH} vs. V_{DO}



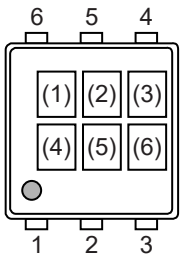
4. 4 R_{DOL} vs. V_{DO}



■ Marking Specifications

1. SNT-6A

Top view



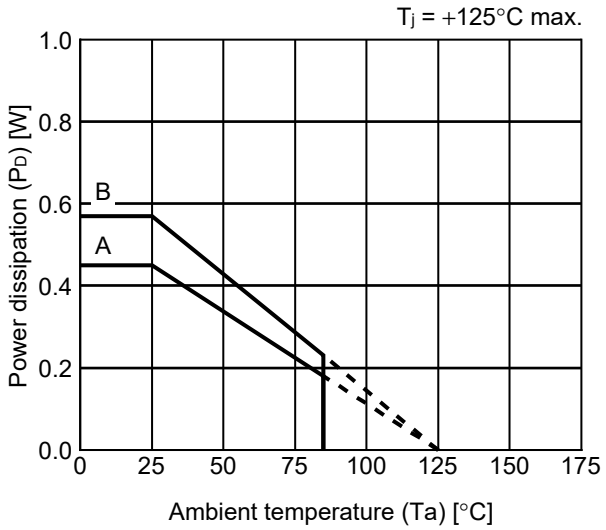
(1) to (3): Product code (refer to **Product name vs. Product code**)
(4) to (6): Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8216AAA-I6T1U	6	9	A

■ Power Dissipation

SNT-6A

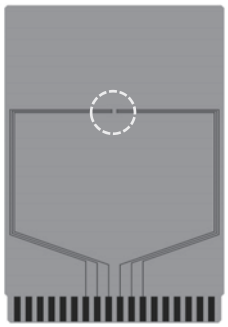


Board	Power Dissipation (P_D)
A	0.45 W
B	0.57 W
C	–
D	–
E	–

SNT-6A Test Board

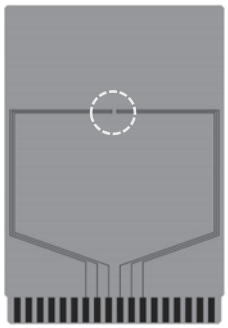
(1) Board A

IC Mount Area



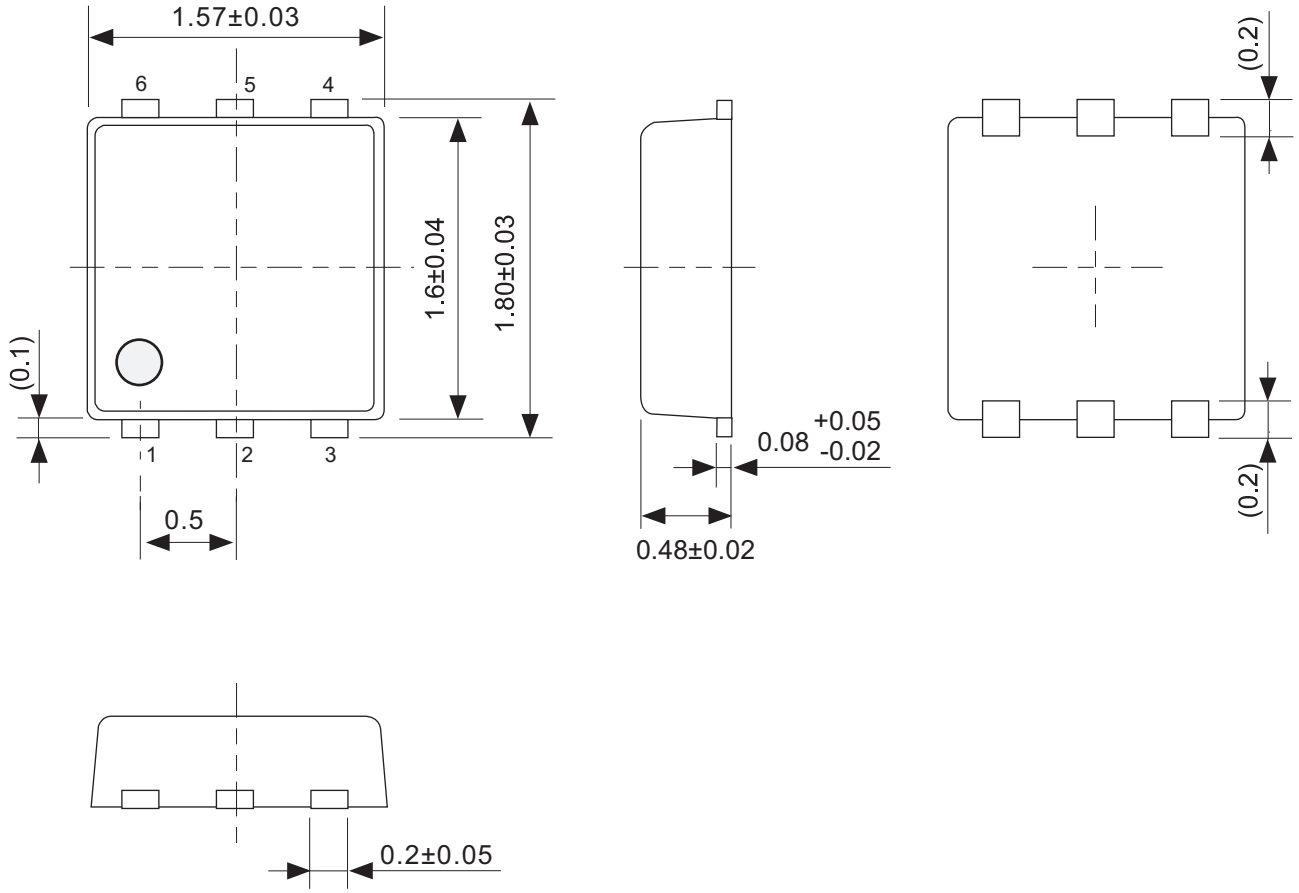
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



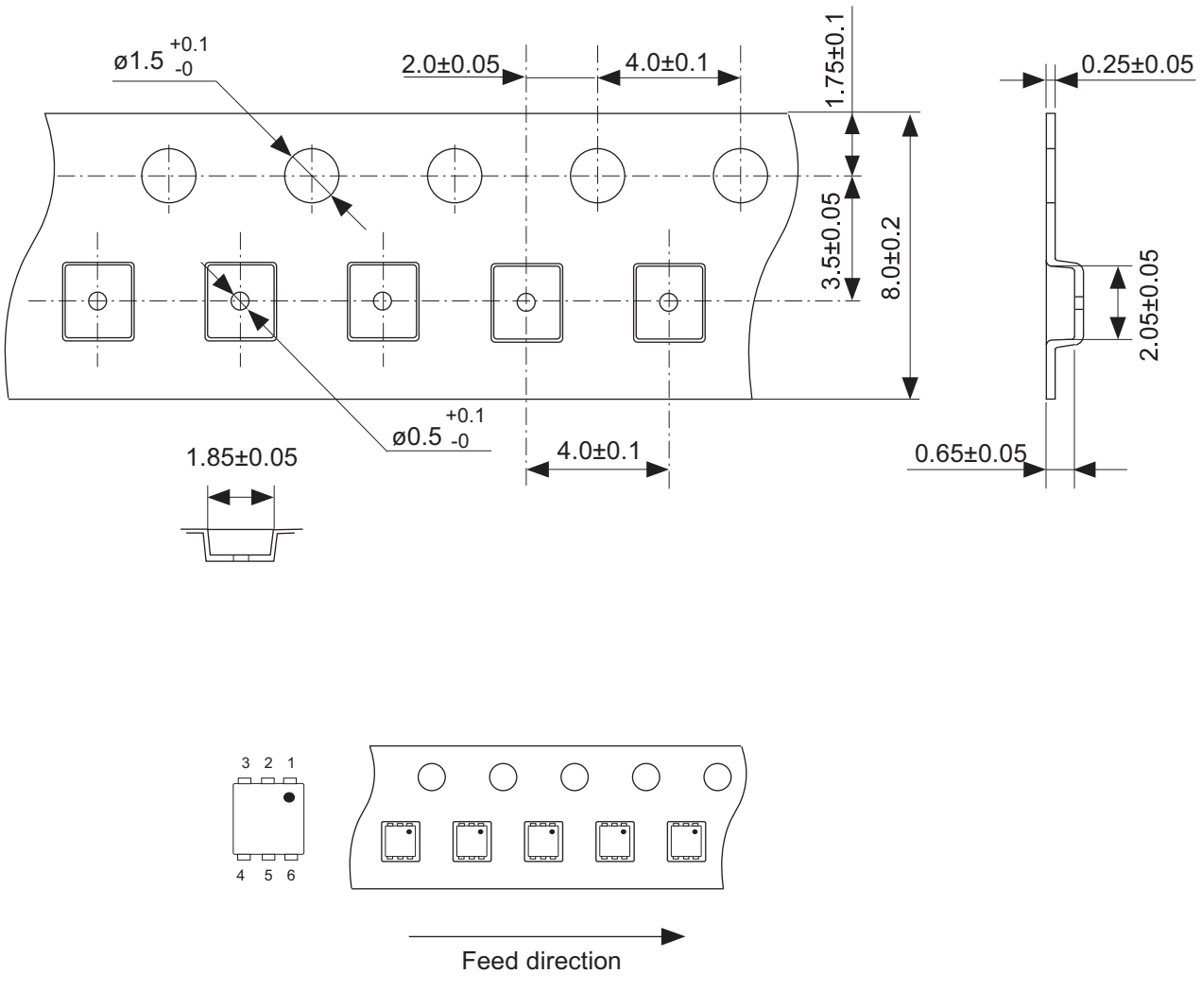
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SNT6A-A-Board-SD-1.0



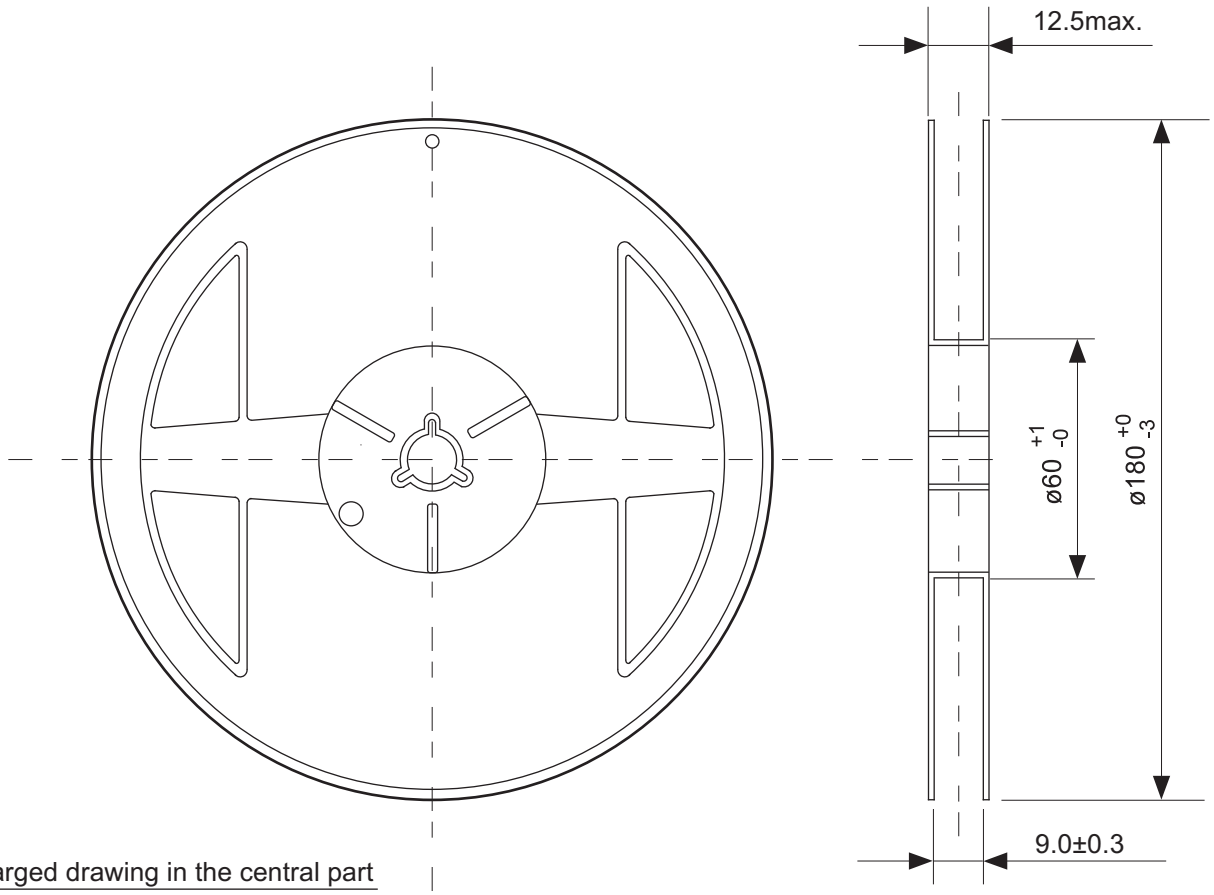
No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

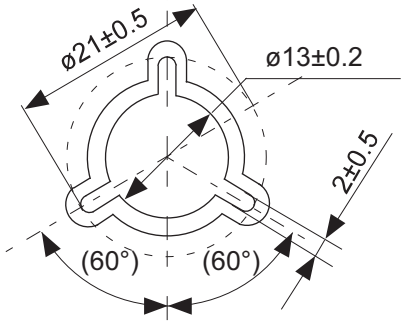


No. PG006-A-C-SD-2.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

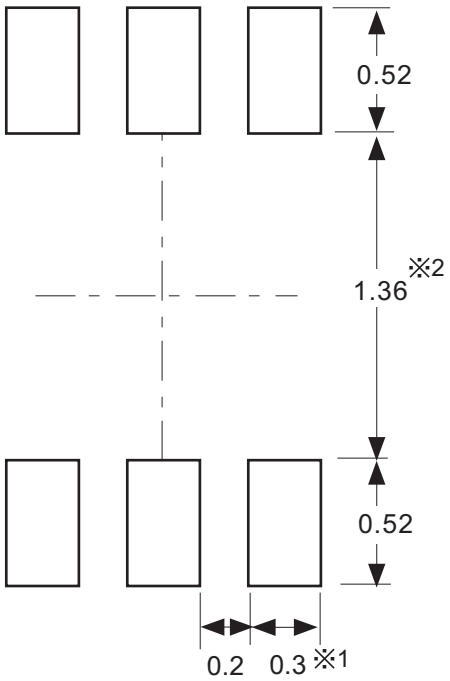


Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝**SNT**パッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.4-2019.07