August 2015

FAH4820
Direct Driver for DC Motors (ERMs)

Features

- Single-Pin Direct-Drive of ERM for Simple Vibration Control
- External Motor Enable/Disable, Vibration Control
- Register-Based I^2C Control (Optional; Device Operates in Default Condition)
- Over-Driving Motor Control, Drive ERM Voltage to V_{DD} Rail
- Programmable Motor Drive Voltage
- Low Standby Current: <1 µA
- Fast Wake-up Time
- Nearly Rail-to-Rail Output Swing
- Protections: Under-Voltage, Over-Current, Over-Temperature
- Package: 10-Lead MLP

Applications

- Mobile Phones
- Handheld Devices
- Keypad Interfaces

Description

The FAH4820 is a high-performance enhanced ERM driver for mobile phone and other hand-held devices. This device does not require a PWM signal to generate vibration of the ERM; it is controlled by the drive level on the HEN input. The ERM spins for the length of time that the HEN pin is held HIGH, then stops when the HEN pin is pulled LOW. The FAH4820's register maps are accessible via I^2C serial communication, which is useful for higher or lower drive voltage across the ERM or if disabling the device is desired.

Related Resources

- *AN-5067 — PCB Land Pattern Design and Surface-Mount Guidelines for MLP Packages*

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAH4820MPX	-40°C to +85°C	10-Lead, Dual, JEDEC MO-229, 3 mm Square, Molded Leadless Package (MLP)	3000 Units on Tape & Reel

Block Diagram

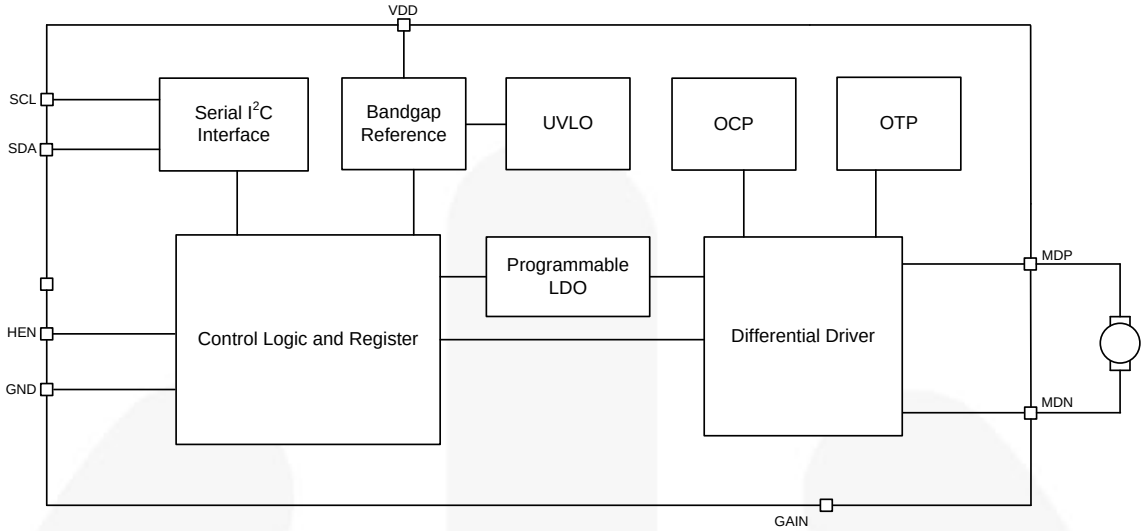


Figure 1. Block Diagram

Pin Configuration

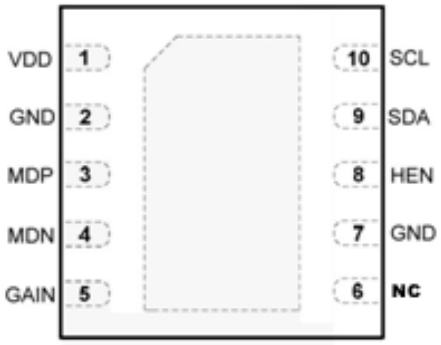


Figure 2. Pin Assignments

Pin Definitions

Name	Pin #	Type	Description
VDD	1	Power	Power
GND	2, 7	Power	Ground
MDP	3	Output	Positive motor driver output
MDN	4	Output	Negative motor driver output
GAIN	5	Input	Gain control for motor driving
NC	6	NA	No connection
HEN	8	Input	Motor enable/disable (HIGH: enable, LOW: disable)
SDA	9	Input	I^2C data input
SCL	10	Input	I^2C clock input

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O (All Input and Output Pins)	-0.3	V_{CC}+0.3	V

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multi-Layer Test Boards, Still Air		200		°C/W

Electrostatic Discharge Information

Symbol	Parameter	Max.	Unit
ESD	Human Body Model, JESD22-A114	±4	kV
	Charged Device Model, JESD22-C101	±1	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		+85	°C
V_{DD}	Supply Voltage Range	2.7	3.3	5.5	V

DC Electrical Characteristics

T_A = 25°C, V_{DD} = 3.3 V, and V_{LDO} = 3.0 V unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
IIH_{HEN}	Input Current	HEN = 3.3 V		1	2	µA
IIL_{HEN}	Input Current	HEN = 0.0 V		1	2	µA
IIH_{SCL}	Input Current	SCL = 3.3 V		0	1	µA
IIH_{SDA}	Input Current	SDA = 3.3 V		0	1	µA
IIL_{SCL}	Input Current	SCL = 0.0 V		0	1	µA
IIL_{SDA}	Input Current	SDA = 0.0 V		0	1	µA
V_{IH}	Input Logic HIGH		0.7 X V_{DD}			V
V_{IL}	Input Logic LOW				0.3 X V_{DD}	V
V_{OL}	Output Voltage	V_{DD} = 3.3 V, R_L = 10 Ω		100	200	mV
V_{OH}	Output Voltage	V_{DD} = 3.3 V, R_L = 10 Ω	V_{LDO}-0.3			V
I_{OUT}	Short-Circuit Protection	V_{DD} = 3.3 V, MDP to MDN Short to Each Other & Short to GND		500		mA
t_{WU}	Wake-up Time			50	150	µs
t_{SD}	Shutdown Time	HEN HIGH to LOW		1	150	µs
R_{IN}	Input Resistance	Gain Input – Default Register Setting		10		kΩ
C_{IN}	Input Capacitance	Gain Input		10		pF
I_{DD1}	Supply Current	R_L = No Load, HEN=LOW		10	20	µA
I_{DD2}	Supply Current	R_L = No Load, HEN=HIGH		2.5	5.0	mA
I_{DD3}	Supply Current	R_L = 10 Ω, HEN=HIGH		275		mA
I_{PD}	Power-Down Supply Current	V_{DD} = 2.7 V, V_{LDO} = 2.4 V, Reg 0x20 Bit 7=0		20	50	nA
V_{OUT}	Output Voltage Range		2.4	3.0	3.6	V
V_{REG}	Output Voltage Accuracy		-10		10	%

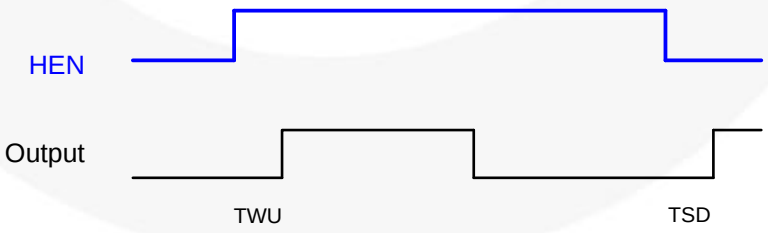


Figure 3. Enable/Disable Functional Timing

I²C DC Electrical Characteristics

T_A = 25°C, V_{DD} = 3.3 V, and V_{LDO} = 3.0 V unless otherwise noted.

Symbol	Parameter	Fast Mode (400 kHz)		
		Min.	Max.	Unit
V_{IL}	Low-Level Input Voltage	-0.3	0.6	V
V_{IH}	High-Level Input Voltage	1.3		V
V_{OL}	Low-Level Output Voltage at 3 mA Sink Current (Open-Drain or Open-Collector)	0	0.4	V
I_{IH}	High-Level Input Current of Each I/O Pin, Input Voltage = V_{DD}	-1	1	µA
I_{IL}	Low-Level Input Current of Each I/O Pin, Input Voltage = 0 V	-1	1	µA

I²C AC Electrical Characteristics

Symbol	Parameter	Fast Mode (400 kHz)		
		Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	Low Period of SCL Clock	1.3		µs
t_{HIGH}	High Period of SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time(1)	100		ns
t_r	Rise Time of SDA and SCL Signals(2)	20+0.1C_b	300	ns
t_f	Fall Time of SDA and SCL Signals(2)	20+0.1C_b	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	Bus-Free Time between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

1. A Fast-Mode I²C Bus® device can be used in a Standard-Mode I²C bus system, but the requirement $t_{SU;DAT}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the Serial Data (SDA) line t_{r_max} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C Bus specification) before the SCL line is released.
2. C_b equals the total capacitance of one bus line in pf. If mixed with High-Speed Mode devices, faster fall times are allowed according to the I²C specification.

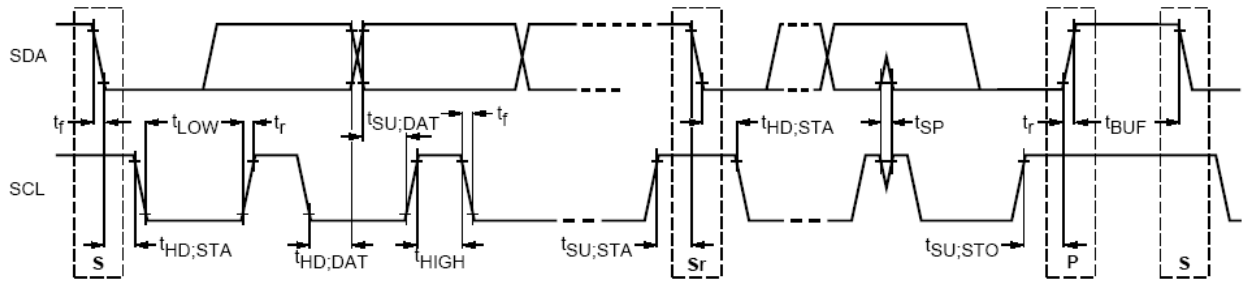


Figure 4. Definition of Timing for Full-Speed Mode Devices on the I²C Bus

Functional Description

I²C Control

Writing to and reading from registers is accomplished via the I²C interface. The I²C protocol requires that one device on the bus initiates and controls all read and write operations. This device is called the "master" device. The master device generates the SCL signal, which is the clock signal for all other devices on the bus. All other devices on the bus are called "slave" devices. The FAH4820 is a slave device. Both the master and slave devices can send and receive data on the bus.

During I²C operations, one data bit is transmitted per clock cycle. All I²C operations follow a repeating nine-clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device. Note that there are no unused clock cycles during any operation; therefore, there must be no breaks in the stream of data and ACKs/NACKs during data transfers.

For most operations, I²C protocol requires the SDA line remain stable (unmoving) whenever SCL is HIGH. For example, transitions on the SDA line can only occur when SCL is LOW. The exceptions are when the master device issues a START or STOP condition. The slave device cannot issue a START or STOP condition.

START Condition: This condition occurs when the SDA line transitions from HIGH to LOW while SCL is HIGH. The master device uses this condition to indicate that a data transfer is about to begin.

STOP Condition: This condition occurs when the SDA line transitions from LOW to HIGH while SCL is HIGH. The master device uses this condition to signal the end of a data transfer.

Acknowledge and Not Acknowledge: When data is transferred to the slave device, the slave device sends acknowledge (ACK) after receiving every byte of data. The receiving device sends an ACK by pulling SDA LOW for one clock cycle.

When the master device is reading data from the slave device, the master sends an ACK after receiving every byte of data. Following the last byte, a master device sends a "not acknowledge" (NACK) instead of an ACK, followed by a STOP condition. A NACK is indicated by leaving SDA HIGH during the clock after the last byte.

Slave Address

Each slave device on the bus must have a unique address so the master can identify which device is sending or receiving data. The FAH4820 slave address is 0000110X binary, where "X" is the read/write bit. Master write operations are indicated when X = 0. Master read operations are indicated when X = 1.

Writing to and Reading from the FAH4820

All read and write operations must begin with a START condition generated by the master. After the START condition, the master must immediately send a slave address (7 bits), followed by a read/write bit. If the slave address matches the address of the FAH4820, the FAH4820 sends an ACK after receiving the read/write bit by pulling the SDA line LOW for one clock cycle.

Setting the Pointer

For all operations, a "pointer" stored in the command register must be indicating the register to be written or read. To change the pointer value in the command register, the read/write bit following the address must be 0. This indicates that the master writes new information into the command register.

After the FAH4820 sends an ACK in response to receiving the address and read/write bit, the master must transmit an appropriate 8-bit pointer value, as explained in the I²C Registers section. The FAH4820 sends an ACK after receiving the new pointer data.

The pointer-set operation is illustrated in Figure 7 and Figure 8. Any time a pointer-set is performed, it must be immediately followed by a read or write operation. The command register retains the pointer between operations; once a register is indicated, subsequent read operations do not require a pointer set cycle. Write operations always require the pointer be reset.

Reading

If the pointer is already pointing to the desired register, the master can read from that register by setting the read/write bit (following the slave address) to 1. After sending an ACK, the FAH4820 begins transmitting data during the following clock cycle. The master should respond with a NACK, followed by a STOP condition *(see Figure 5)*.

The master can read multiple bytes by responding to the data with an ACK instead of a NACK and continuing to send SCL pulses, as shown in Figure 6. The FAH4820 increments the pointer by one and sends the data from the next register. The master indicates the last data byte by responding with a NACK, followed by a STOP.

To read from a register other than the one currently indicated by the command register, a pointer to the desired register must be set. Immediately following the pointer-set, the master must perform a REPEAT START condition *(see Figure 8)*, which indicates to the FAH4820 that a new operation is about to occur. If the REPEAT START condition does not occur, the FAH4820 assumes that a write is taking place and the selected register is overwritten by the upcoming data on the data bus. After the START condition, the master must again send the device address and read/write bit. This time, the read/write bit must be set to 1 to indicate a read. The rest of the read cycle is the same as described for reading from a preset pointer location.

Writing

All writes must be preceded by a pointer set, even if the pointer is already pointing to the desired register.

Immediately following the pointer-set, the master must begin transmitting the data to be written. After transmitting each byte of data, the master must release the Serial Data (SDA) line for one clock cycle to allow the FAH4820 to acknowledge receiving the byte. The write operation should be terminated by a STOP condition from the master *(see Figure 7)*.

As with reading, the master can write multiple bytes by continuing to send data. The FAH4820 increments the pointer by one and accepts data for the next register. The master indicates the last data byte by issuing a STOP condition.

Read / Write Diagrams

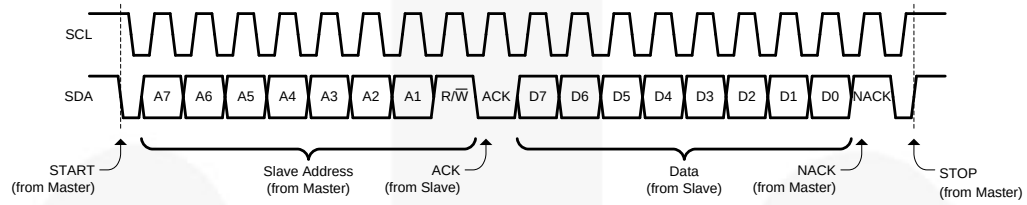


Figure 5. I²C Read

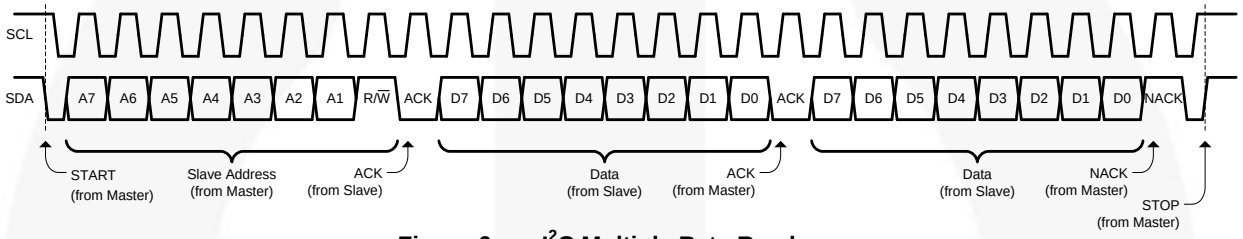


Figure 6. I²C Multiple Byte Read

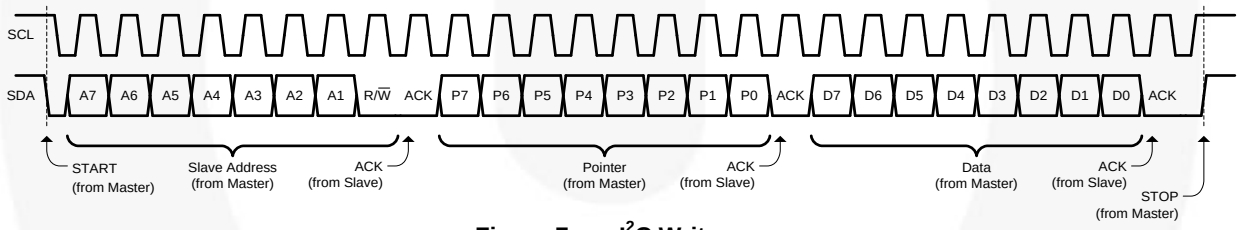


Figure 7. I²C Write

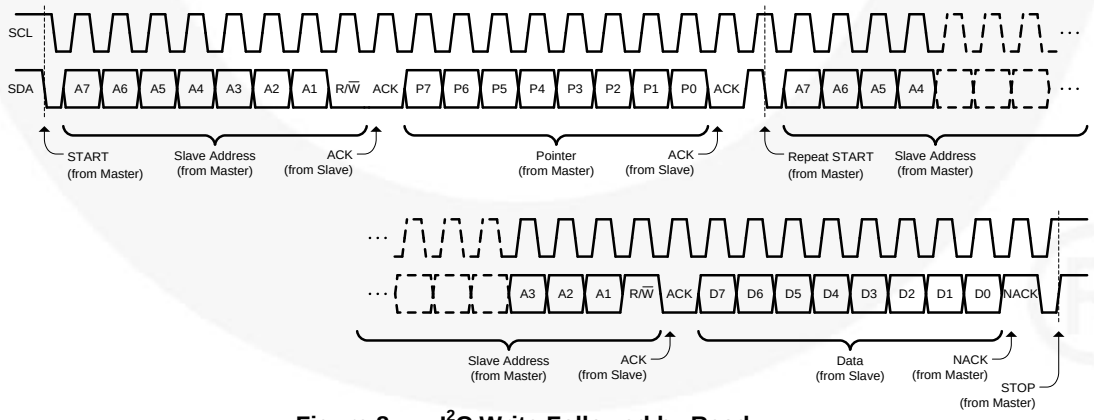


Figure 8. I²C Write Followed by Read

Digital Interface

The I²C-compatible interface is used to program the FAH4820 as listed in the below register configurations. The I²C address of the FAH4820 is 0x06.

Binary	Hex
00000110	0x06

Register Definitions

Table 1. Control Registers and Default Values

Address	Register Name	Type	Reset Value
0x20	CONTROL0	R/W	10010000
0x21	CONTROL1	R/W	00101100
0x22	STAT	R	00001110

Table 2. Control Register MAP (Control0, Control1, Status)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
En	ODRV_EN	ODRVEN_HL	Reserved				
Input Resistance[7:5]			VLDO_OUT			Reserved	
Reserved[7:4]				VDD_G	VREG_G	OT	Reserved

Notes:
3. Connect the bottom DAP to ground.

Table 3. Control 0

- Address: 20h
- Reset Value: 1001_0000
- Type: Read/Write
- **BOLD** is default state

Bit #	Name	Size (Bits)	Description
7	En	1	Drive Enable Mode 0: Power-Down Mode **1: Normal Operation Mode**
6	ODRV_EN	1	Over-Drive Enable Mode **0: Disable Over Drive** 1: Enable Over Drive
5	ODRVEN_HL	1	Selection of Over-Drive **0: Over-Drive LOW (MDN to VDD RAIL)** 1: Over-Drive HIGH (MDP TO VDD RAIL)
4	Reserved	1	Not used
3:2	Reserved	2	Not used
1:0	Reserved	2	Not used

Table 4. Control 1

- Address: 21h
- Reset Value: 0010_1100
- Type: Read/Write
- **BOLD** is default state

Bit #	Name	Size (Bits)	Description
7:5	Input Resistance	3	000: 8 kΩ **001: 10 kΩ** 010: 12 kΩ 011: 14 kΩ 100: 16 kΩ 101: 18 kΩ 110: 20 kΩ 111: 22 kΩ
4:2	VLDO_OUT	3	000: 2.4 V 001: 2.6 V 010: 2.8 V **011: 3.0 V** 100: 3.2 V 101 :3.4 V 110: 3.6 V
1:0	Reserved	2	Not used

Table 5. Status

- Address: 22h
- Reset Value: 0000_1110
- Type: Read Only

Bit #	Name	Size (Bits)	Description
7:4	Reserved	4	Not used
3	VDD_G	1	0: Input voltage is not valid (under UVLO); input voltage is less than 2.3 V (rising) / 2.1 V (falling) **1: Input voltage is valid (over UVLO)**
2	VLDO_OUT_G	1	0: Regulator output is not valid (V_{LDO_OUT} is less than 70% of V_{LDO_OUT} programmed) **1: Regulator output is valid**
1	OT	1	0: Over-temperature protection is tripped **1: Over-temperature protection is not tripped**
0	Reserved	1	Not used, default is 0

Table 6. V_{DD} vs. V_{LDO_OUT}

V_{LDO_OUT} (Programmed Voltage)	V_{DD} (V)					
	2.7	3.0	3.3	4.5	5.0	5.5
	2.4	2.4	2.4	2.4	2.4	2.4
	2.6	2.6	2.6	2.6	2.6	2.6
		2.8	2.8	2.8	2.8	2.8
			3.0	3.0	3.0	3.0
			3.2	3.2	3.2	3.2
				3.4	3.4	3.4
				3.6	3.6	3.6

Applications Information

Many of the FAH4820 functions can be controlled through the I^2C interface, but this application demonstrates the device in default state when powered up. In the default state; the device is enabled, overdrive is disabled, input resistance is 10 kΩ, and the differential drive voltage is set to 3.0 V. The device design allows the user to leave the SCL and SDA line floating. The differential outputs are held at ground until the HEN pin is pulled HIGH, which causes the ERM to rotate until the HEN signal is pulled LOW or a timer circuit pulls the HEN signal LOW. Figure 9 shows an example using a 555 timer to control a single vibration from an ERM. The length of time the ERM is rotating is determined by the RC time constant of R3 and C3. In this case, the motor rotate for 1.1 second every time the button is pressed. Electromagnetic Interference (EMI) is the radiation of electromagnetic noise. This noise can affect control signals and other electronics, which can produce errors and reduce performance. The DC motors used in ERMs are a common source of EMI due to commutator arcing. It is recommended that a 100 pF capacitor be placed across the MDP and MPN pins. In this case, this is C2, which greatly reduces EMI produced by the ERM.

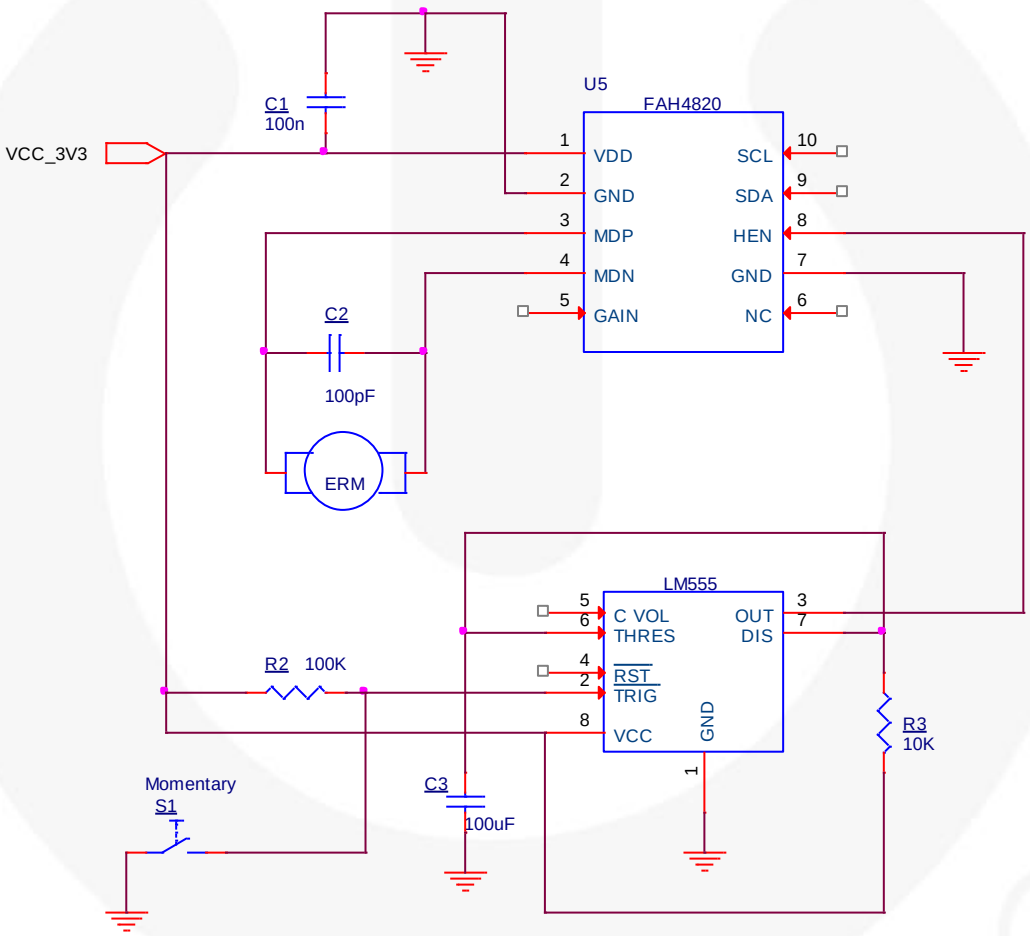


Figure 9. 555 Timer Control of Single Vibration from ERM

Figure 10 is an example of using Arduino Uno to control the HEN pin based on which of the three switches is pressed. In the example program below; when SW1 is pressed (which is connected to Arduino input pin 10), the ERM spins once for the length of time the program holds pin 12 HIGH. The other switches produce a double pulse (SW2) and a triple pulse (SW3) output. Due to EMI noise, it is recommended that a 100 pF capacitor be placed across the MDP and MPN pins. In this case, this is C3, which greatly reduces EMI produced by the ERM.

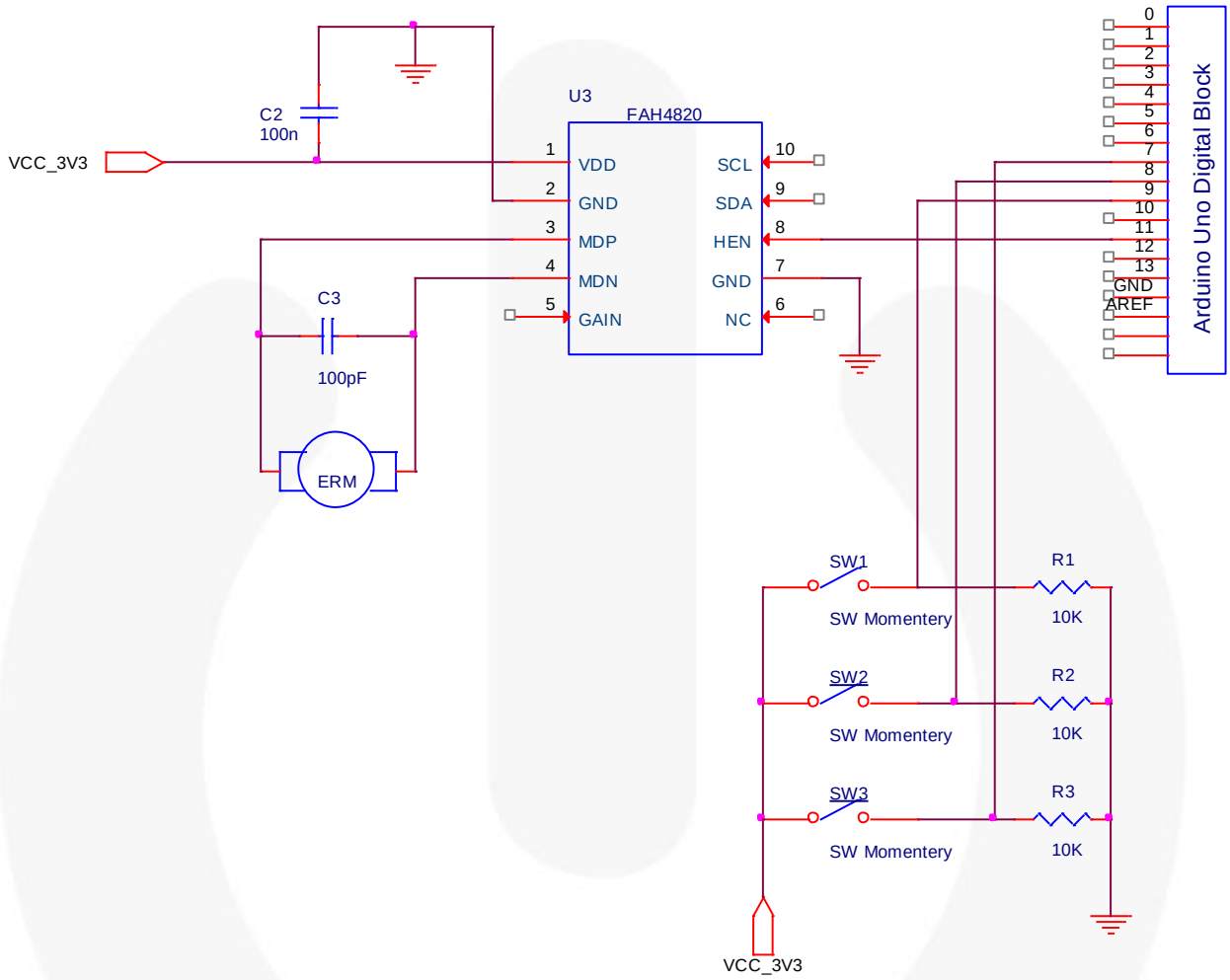


Figure 10. Arduino Uno Control HEN Pin

Vibration Alert Arduino Example Program

```
/* FAH4820 vibration alert Arduino program*/
int VIBpin = 12;
int switchPin = 8;
int switchPin1 = 9;
int switchPin2 = 10;

void setup()
{
  pinMode(VIBpin, OUTPUT);
  pinMode(switchPin, INPUT);
  pinMode(switchPin1, INPUT);
  pinMode(switchPin2, INPUT);
}

void loop()
{
```

```
  if (digitalRead(switchPin) == HIGH) /* run this sequence if pin 8 is high - triple
pulse*/
  {
  digitalWrite(VIBpin,HIGH);
  delay(600);
  digitalWrite(VIBpin,LOW);
  delay(300);
  digitalWrite(VIBpin,HIGH);
  delay(300);
  digitalWrite(VIBpin,LOW);
  delay(300);
  digitalWrite(VIBpin,HIGH);
  delay(150);
  digitalWrite(VIBpin,LOW);
  delay(300);
  }
  else
  {
   digitalWrite(VIBpin,LOW);
  }
  if (digitalRead(switchPin1) == HIGH) /* run this sequence if pin 9 is high - double
pulse*/
  {
  digitalWrite(VIBpin,HIGH);
  delay(600);
  digitalWrite(VIBpin,LOW);
  delay(300);
  digitalWrite(VIBpin,HIGH);
  delay(150);
  digitalWrite(VIBpin,LOW);
  delay(300);
  }
  else
  {
   digitalWrite(VIBpin,LOW);
  }
   if (digitalRead(switchPin2) == HIGH) /* run this sequence if pin 10 is high -
single pulse*/
  {
  digitalWrite(VIBpin,HIGH);
  delay(600);
  digitalWrite(VIBpin,LOW);
  delay(300);
  }
  else
  {
   digitalWrite(VIBpin,LOW);
  }
}
```

Internal LDO

The internal LDO is designed for an I^2C seven-step adjustable output voltage. This provides flexibility for various motor voltages and configurations for low-power consumption. The LDO includes an internal circuit for short-circuit current protection.

Serial Interface

On power-up, the device default values are invoked. The FAH4820 allows programming through the registers: the VLDO out, over drive, power down, and others functions. The device functions without any I^2C input signals connected.

Thermal Shutdown

If the junction temperature is above 150°C, the temperature control block shuts down and stays off until the temperature is below 134°C. The register values are kept as written so that it's not required to initialize again.

Over-Current Limitation

The driver includes a current-limitation block to protect against an over-current condition, mainly caused by a stuck-rotor condition. Over-current protection limitation is 500 mA, typical.

Over-Drive Motor Control

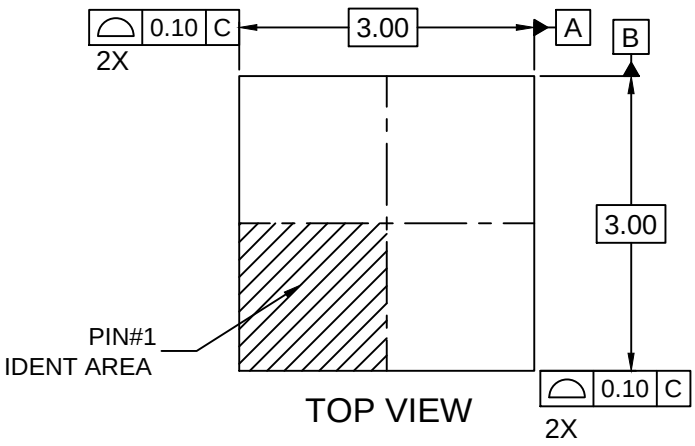
A common approach to driving DC motors is to over-drive a voltage that overcomes the inertia of the motor's mass. The motor is often overdriven for a short time before returning to the rated voltage to sustain rotation. The FAN4820 block can over-drive a motor up to the V_{DD} voltage.

Over-Drive Duration

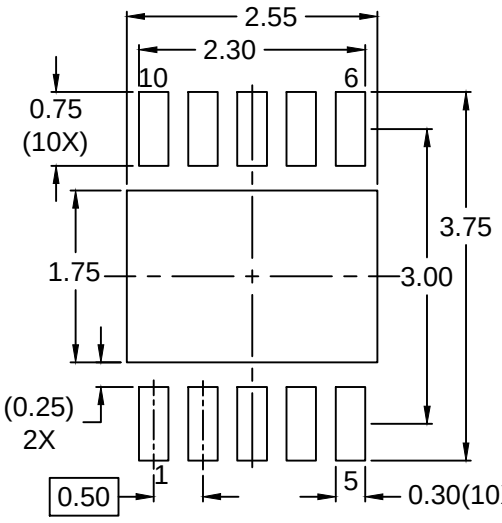
It is important that over-drive time not damage the motor. The over-drive duration must be dependent on the motor datasheet and care must be taken not to assert an over-voltage condition over the rated time limit of the motor.

Status Registers

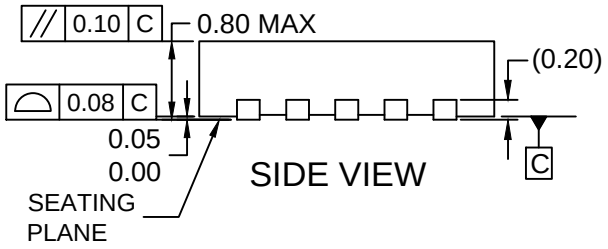
The FAH4820 has a status register set that monitors LDO input voltage, regulator output voltage, and over-temperature status.



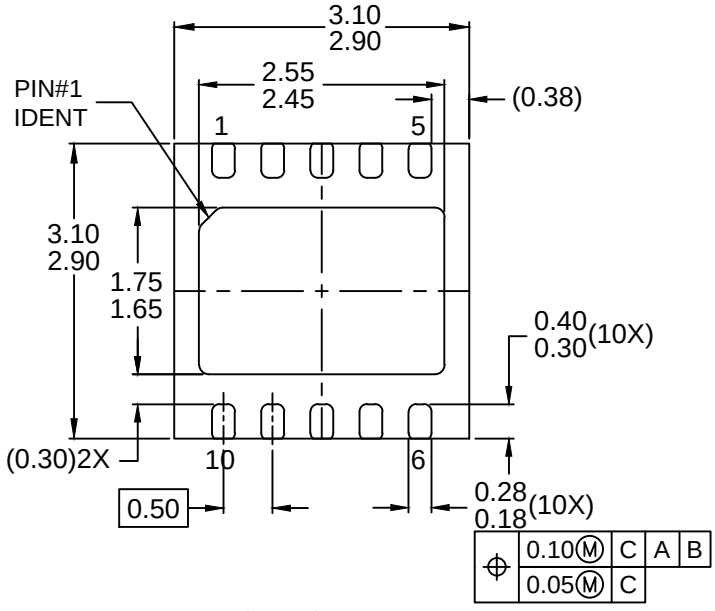
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION W3030D-5.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN IPC REFERENCE : SON50P300X300X100-11N.

E. DRAWING FILENAME: MKT-UMLP10Jrev1.

F. FAIRCHILD SEMICONDUCTOR.

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