

0.39 Ω , Low- R_{ON} , Ultra-Low Distortion, Compact DPDT Analog Switch

DESCRIPTION

The DG2751 is a compact, low resistance, ultra-low distortion double pole double throw (DPST) analog switch.

The DG2751 features a flat 0.39 Ω ON resistance over the analog signal range from (V+) - 5.5 V to V+, supporting bi-directional negative signal swing. The design brings superior signal fidelity by eliminating the distortion caused by double hump switch resistance character of conventional analog switches.

The DG2751 operates over a voltage range from 3 V to 5.5 V. Because of its low current consumption, it can be powered directly by a GPIO. When V+ power is off, all switch pins are of high impedance mode.

Shunt switches are integrated at normally close (NO_n) channels to discharge the AC-coupling capacitance at the terminals.

The part is controlled by a single bit, S, which can interface with 1.2 V low voltage I/O. Switch ON/OFF is of break-before-make (BBM).

The DG2751 is available in ultra-compact 1.2 mm x 1.2 mm, 9-bump WCSP package, and operate over the -40 °C to +85 °C extended temperature range.

FEATURES

- 2.3 V to 5.5 V single supply operation
- Low resistance: 0.39 Ω / typ. at 2.7 V
- Highly flat and matched R_{ON}
- Low parasitic capacitance, $C_{ON} = 31$ pF, $C_{OFF} = 30$ pF
- High bandwidth: 290 MHz
- Guaranteed logic high 1.2 V, logic low 0.3 V
- Break before make switching
- Signal swing over V+ capable
- Power down protection
- Latch up current: 300 mA (JESD78)
- ESD/HBM: > 8 kV
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

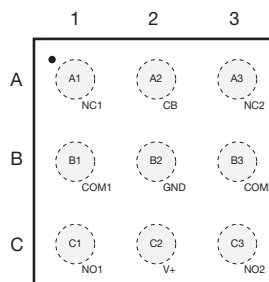
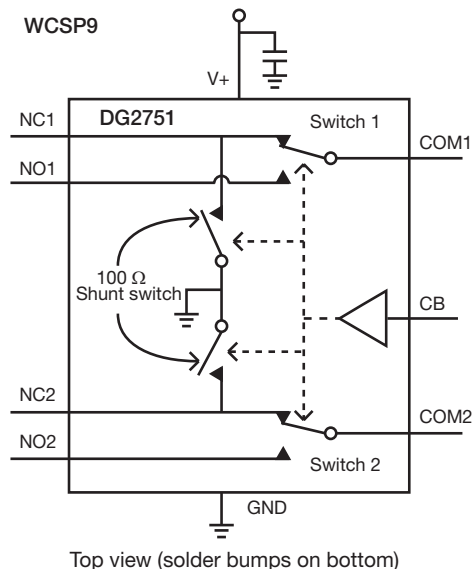
APPLICATIONS

- Applications
- Smart phones
- Tablets
- Portable media players
- Headphones
- Audio / video equipment
- Low-distortion signal switches
- Digital cameras
- Docking devices

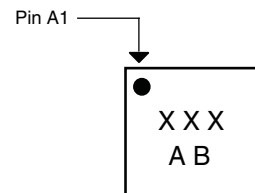
BENEFITS

- Low and flat resistance
- Excellent total harmonic distortion
- Low parasitic capacitance
- Low voltage control interface

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



WCSP9, 1.25 mm x 1.25 mm
Top view (solder bumps on bottom)



Device marking: AB for DG2751
x = date / lot traceability code

**TRUTH TABLE**

CB	FUNCTION
0	COMx is connected to NCx
1	COMx is connected to NOx, NCx is connected to shunt resistor

ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKING CODE	TEMPERATURE RANGE	STANDARD PACKAGING QUANTITY
DG2751DB-T2-GE1	WCSP9	AB	-40 °C to +85 °C lead (Pb)-free	Tape and reel 3000 units

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1	NC1	Normally close terminal for switch 1
A2	CB	Logic control input. Drive CB low to connect COMx to NCx. Drive CB high to connect COMx to NOx.
A3	NC2	Normally closed terminal for switch 2
B1	COM1	Common terminal for switch 1
B2	GND	Ground
B3	COM2	Common terminal for switch 2
C1	NO1	Normally open terminal for switch 1
C2	V+	Device power supply input. Bypass V+ to GND with a 0.1 μ capacitor as close to the pin as possible
C3	NO2	Normally open terminal for switch 2

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER		LIMIT	UNIT
Reference to GND	V+, IN	-0.3 to 6	V
	COM, NO, NC ^a	(V+) - 5.5 to (V+ + 0.3)	
Current (any terminal except COM, NO, NC, IN)		30	mA
Continuous Current (COM, NO, NC, IN)		± 250	
Peak Current (pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature (D suffix)		-65 to +150	$^{\circ}\text{C}$
Power Dissipation (packages) ^b	WCSP9-40 ^c	963	mW
Junction-to-Ambient Thermal Resistance (θ_{JA})		83	$^{\circ}\text{C}/\text{W}$
ESD (human body model) I/O to GND		8	kV
Latch-Up (per JESD78)		400	mA

Notes

- a. Signals on COM, NO, NC, exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 12 mW/ $^{\circ}\text{C}$ above 70 $^{\circ}\text{C}$.
d. Package thermal resistances were obtained using the method described in JEDEC[®] specification JESD51-7.

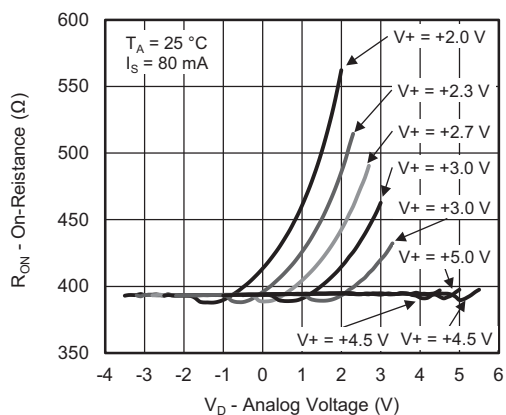
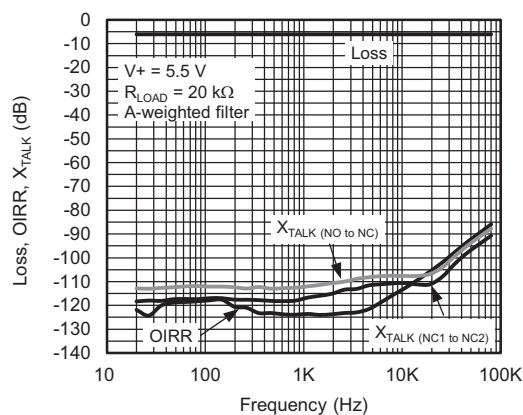
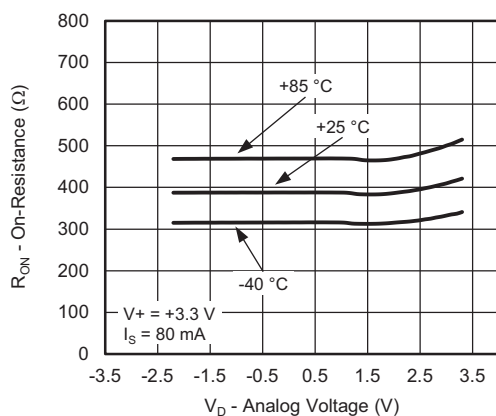
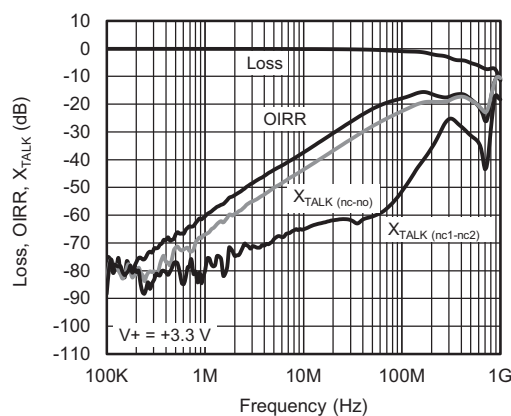
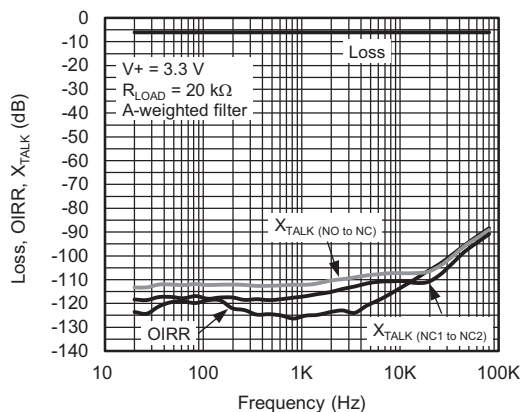
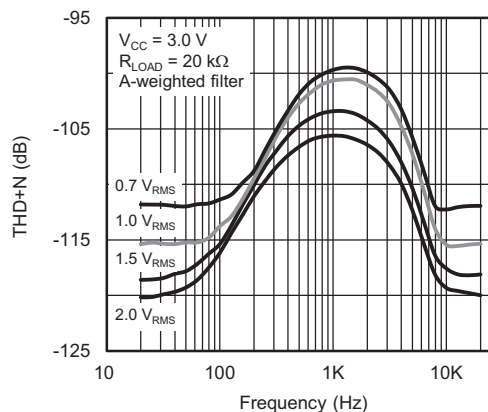
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



SPECIFICATIONS									
PARAMETER	SYMBOL	TEST CONDITIONS unless otherwise specified, V+ = 3.3 V, TA = -40 °C to +85 °C control logic are either at 0 V or V+, typical values are at 25 °C with V+	TEMP. ^a	LIMITS -40 °C to +85 °C			UNIT		
				MIN. ^b	TYP. ^c	MAX. ^b			
Analog Switch									
Analog Signal Range ^d	VANALOG		Full	(V+) - 5.5	-	V+	V		
On-Resistance	RDS(on)	V+ = 3.3 V, VS = 0 V, ± 1.8 V, IS = 80 mA	Room	-	0.390	0.600	Ω		
On-Resistance Match	ΔRON		Full	-	0.470	0.800			
On-Resistance Flatness	RON Flatness		Room	-	0.002	0.050			
			Room	-	0.020	0.050			
Pull Down Resistance	RpD	I = 80 mA, VSW = ± 1.8 V, V+ = 3 V	Room	-	118	130			
			Full	-	130	150			
Switch Off Leakage Current	INO(off)	V+ = 3.3 V, VNO = ± 2 V, VNC = ∓ 2 V	Room	-50	10	50	μA		
			Full	-50	11	50			
	ICOM(off)	V+ = 3.3 V, VCOM = ± 2 V, VNO or VNC = ∓ 2 V	Room	-100	31	100			
			Full	-100	33	100			
	INC(off) ^g	V+ = 3.3 V, VNC = ± 2 V, VNO = ∓ 2 V	Room	-30	20	30	mA		
			Full	-30	21	30			
Channel On Leakage Current	ICOM(on)	V+ = 3.3 V, VCOM = +2 V or -2 V	Room	-100	31	100	μA		
			Full	-100	33	100			
Digital Control									
Input Voltage High	VINH	V+ = 2.3 V to 5.5 V	Full	1.2	-	-	V		
Input Voltage Low	VINL		Full	-	-	0.3			
Input Capacitance	CIN		Room	-	3	-	pF		
Input Current	IINL or IINH	V+ = 5 V, VIN = 0 or V+	Full	-1	0.02	1	μA		
Dynamic Characteristics									
Break-Before-Make Time ^{e, d}	tBBM	V+ = 2.7 V, VS = 1.5 V, RL = 50 Ω, CL = 35 pF	Room	3	41	90	μs		
			Full	2	-	-			
Switch Turn-On Time ^{e, d}	tON		Room	-	44	95			
			Full	-	51	95			
Switch Turn-Off Time ^{e, d}	tOFF		Room	-	0.72	1.5			
			Full	-	0.72	1.5			
Power ON Delay	TON_DLY		Room	-	108	184			
			Full	-	134	213			
Switch On Rise Time	TR		Room	-	20	31			
			Full	-	24	35			
Charge Injection ^d	QINJ		CL = 1 nF, RGEN = 0 Ω, VGEN = 0 V	Room	-	18.9		-	pC
Total Harmonic Distortion Plus Noise	THD+N		f = 1 kHz, V+ = 3 V, A-weighted filter, RL = 20 kΩ		-	-106		-	dB
					-	-103		-	
					-	-101		-	
					-	-100		-	
					-	-111		-	
		f = 1 kHz, V+ = 3.3 V, A-weighted filter, RL = 32 Ω	-		-114	-			
			-		-113	-			
			-		-110	-			
			-		-106	-			
			-		-107	-			
Off-Isolation ^d	OIRR	V+ = 3.3 V, RL = 50 Ω, CL = 5 pF, f = 20 kHz, PSRR at 3.3 V	-		290	-	MHz		
Crosstalk ^d	XTALK		-		30	-	pF		
Bandwidth ^d	BW	V+ = 3.3 V, RL = 50 Ω, -3 dB	-		31	-			
Channel-Off Capacitance ^d	CNC/NO(off)	V+ = 3.3 V, RL = 50 Ω, CL = 5 pF							
Channel-On Capacitance ^d	CCOM/NC/NO(on)								
Power Supply									
Power Supply Range	V+			2.3	-	5.5	V		
Power Supply Current	I+	V+ = 3.3 V, VIN = 0 V, or 1.8 V	Full	-	18	29	μA		
Power Supply Rejection Ratio	PSRR	RCOM = 50 Ω, f = 1 kHz, V+ = 3.3 V	Room	-	-104	-	dB		
		RCOM = 50 Ω, f = 217 Hz, V+ = 3.3 V	Room	-	-106	-			

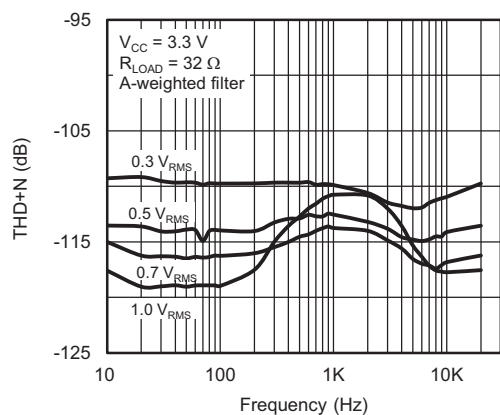
Notes

- a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Crosstalk measured between channels.
g. When NC is off, NC is connected to the 100 Ω shunt resistor.

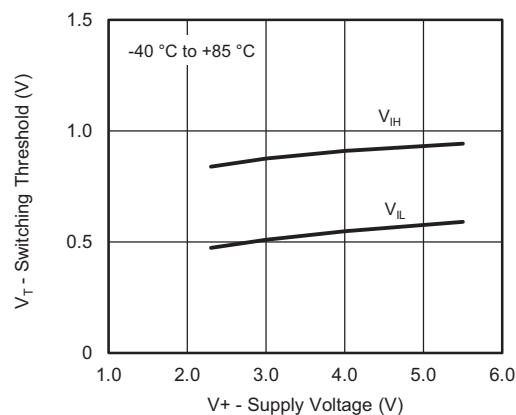
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

On-Resistance vs. V_D and Supply Voltage

Loss, Off-Isolation, Crosstalk vs. Audio Frequency
 $V_+ = 5.5\text{ V}$

On-Resistance vs. Analog Voltage and Temperature

Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

Loss, Off-Isolation, Crosstalk vs. Audio Frequency
 $V_+ = 3.3\text{ V}$

THD+N vs. Frequency



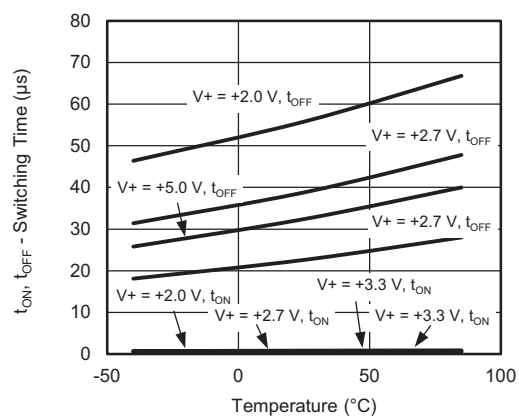
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



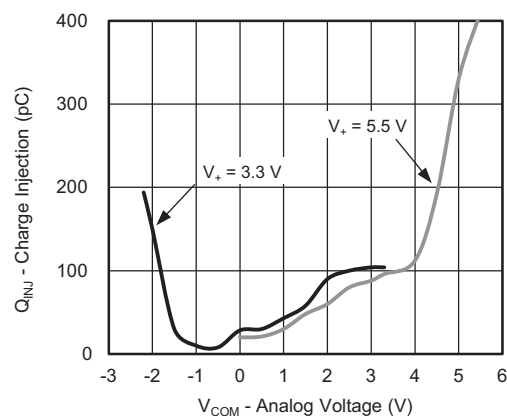
THD+N vs. Frequency



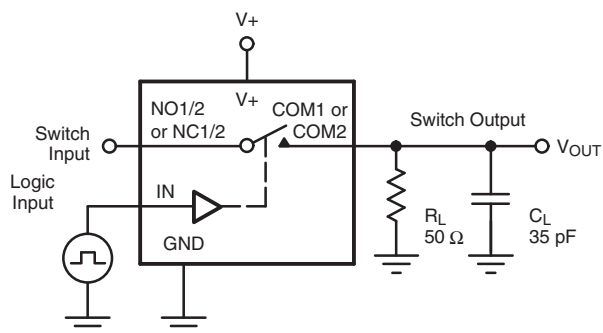
Switching Threshold vs. Supply Voltage



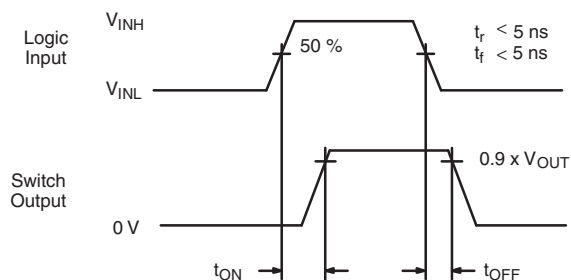
Switching Time vs. Temperature and Supply Voltage



Charge Injection vs. Analog Voltage

TEST CIRCUITS

 C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Fig. 1 - Switching Time


Logic "1" = Switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

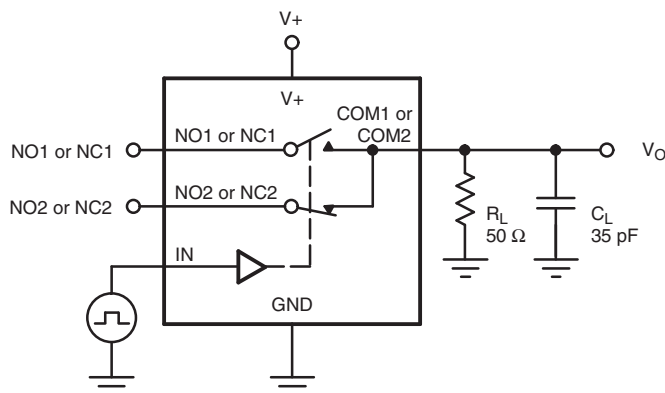
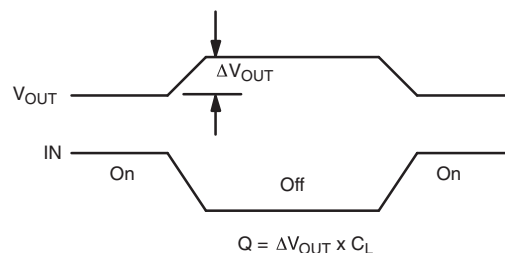
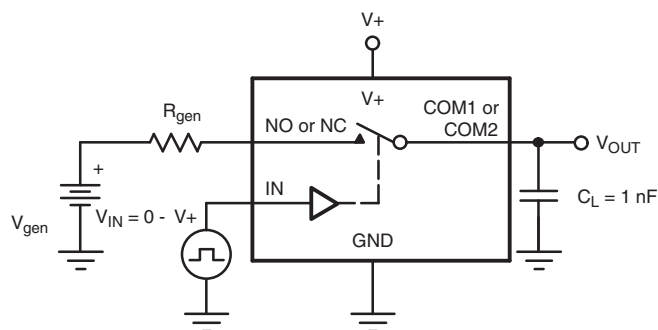
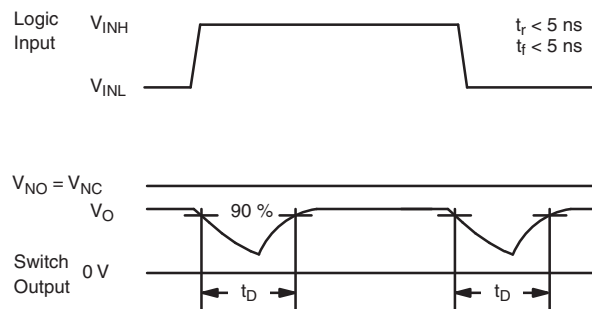
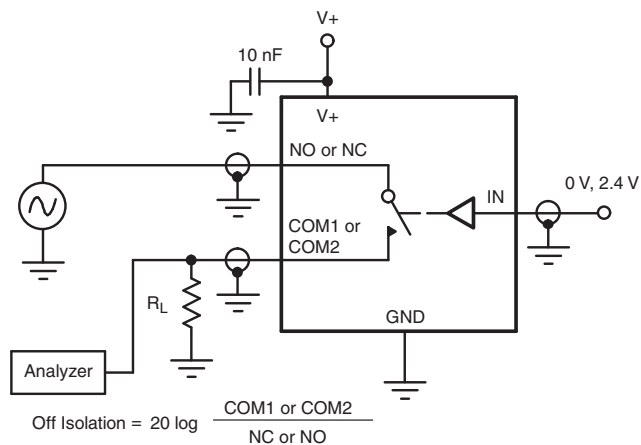
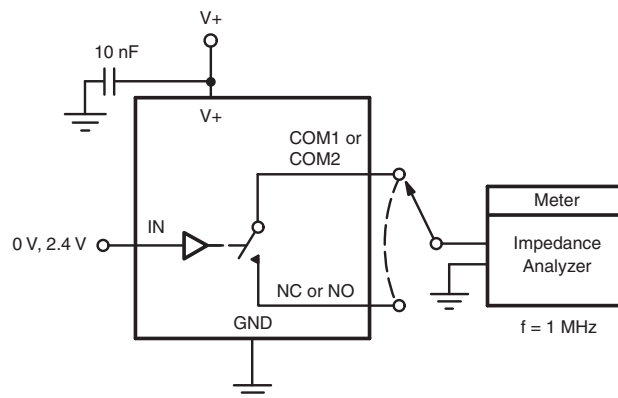

 C_L (includes fixture and stray capacitance)

Fig. 2 - Break-Before-Make Interval


IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

TEST CIRCUITS

Fig. 4 - Off-Isolation

Fig. 5 - Channel Off/On Capacitance

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