

Scope

The present specifications shall apply to a 3 phase brushless motor driver IC, SI-6635M.

The present specifications shall apply to SI-6635M which is performed RoHS instructions.

The present specifications, which shows in Japanese and English, shall be prior to Japanese.

Outline

Type	Monolithic integrated circuit
Structure	Plastic molded (transfer mold)
Applications	3 phase brushless motor driver (Sinusoidal Current Control)

Absolute maximum ratings

Items	Symbol	Condition	Limit	Unit
Power supply voltage	V_{BB}		-0.3~38	V
Output voltage ^{※1}	V_{OUT}		-0.5~ V_{BB}	V
Output current ^{※2}	$I_{OUT(Ave)}$		±2	A
	$I_{OUT(Peak)}$	tw<500msec/Duty<10%	±4	A
Open drain output sink current	I_{OD}	FG/FLAG	10	mA
Logic input voltage	$V_{IN(Logic)}$		-0.3~5.5	V
Logic output voltage	$V_{OUT(Logic)}$	FG/FLAG	-0.3~5.5	V
Analog input voltage	$V_{IN(Analog)}$		-0.3~6	V
Sense voltage	V_{SENSE}		±0.5	V
Package power dissipation	PD	SK evaluation board	4.1	W
Maximum junction temperature	T_J		150	°C
Storage temperature	T_{stg}		-40~150	°C
Ambient temperature	T_A		-20~85	°C

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified junction temperature (T_J).

※1 Output voltage can not be over 38V.

※2 Peak current is guaranteed by design.

Electrical characteristics

Recommended Operating Range

Items	Symbol	Limit		Unit	Remark
		Min	Max		
Power supply voltage	V_{BB}	10	30	V	In normal operation
Logic input voltage	$V_{IN(Logic)}$	0	5.25	V	
Analog input voltage	$V_{IN(Analog)}$	0	5.25	V	
CLK input range	F_{CLK}	9.5	20	MHz	
Sense voltage	V_{SEN}	-0.5	0.5	V	
Package temperature	T_C	-20	105	°C	
Ambient temperature	T_A	-20	85	°C	

Note) Especially, care should be taken with output current on condition over recommended range and below absolute max rating. In this case, enough evaluation is needed with thermal design data below and application note to avoid the device being over absolute max rating for other item.

Electrical Characteristic ($T_a=25^\circ\text{C}$, $V_{BB}=24\text{V}$, Unless Otherwise Noted.)

Item	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Output Drivers						
VBB voltage range	V _{BB}	10	–	V _{BB0V}	V	In normal operation
Main power supply current	I _{BB}	5	–	25	mA	Opration state
		3	–	25	mA	Non-operation state with charge pump OFF, output OFF
Output ON resistance	R _{on}	0.1	0.2	0.3	Ω	I _{out} =2A
MOSFET diode forward volatge	V _F	0.3	1.15	2.0	V	I _{out} =2A
Control Logic						
VDD voltage range	V _{DD}	3.0	3.3	3.5	V	In operation
Logic input voltage	V _{IN(0)}	–	–	V _{DD} × 0.3	V	
	V _{IN(1)}	V _{DD} × 0.7	–	–	V	
Logic input current	I _{IN(0)}	–10	0	10	μ A	V _{IN(0)} , V _{IN} =0V
	I _{IN(1)}	–10	0	10	μ A	V _{IN(1)} , V _{IN} =5.5V, SDA/SCL
		45	–	145	μ A	V _{IN(1)} , V _{IN} =5.5V, ADRS1/ADRS2/BRKn
Internal PWM						
Sen pin input current	I _{Sen}	–10	0	10	μ A	V _{Sen} =0~0.5V
Sense voltage	V _{Sen}	0.21	0.25	0.29	V	With VREF=0.25V
Current sensing filter time	t _{LPFSen}	0.5	2	4	μ s	Guaranteed by design

- Typ data is for reference only.
- Negative current is defined as coming out of the specified pin.

Electrical Characteristic(continued) ($T_a=25^{\circ}\text{C}$, $V_{BB}=24\text{V}$, Unless Otherwise Noted.)

Item	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		

Protection

Flag output saturation voltage	$V_{FI(ON)}$	0.08	0.45	0.7	V	$I_{FG}=2\text{mA}$
Flag output pin ON current	$I_{FI(ON)}$	5	7.5	25	mA	$V_{FI}=2\text{V}$
Flag output leak current	$I_{FI(OFF)}$	-1	0	50	μA	$V_{FG}=5.5\text{V}$
OCP sensing voltage	V_{OCPLS}	0.7	1.2	2	V	LowSideMOSFET sensing (OUT-GND)
	V_{OCPHS}	0.3	0.8	1.8	V	HighSideMOSFET sensing (VBB-GND)
VBB overvoltage protection threshold voltage	V_{BBOV}	32	35	38	V	In V_{BB} voltage rising
VBB overvoltage protection hysteresis	$V_{BBOVhys}$	1.4	2	5.1	V	
Thermal protection operating temperature	T_{JTSD}	-	165	-	$^{\circ}\text{C}$	In temperature rising Guaranteed by design
Thermal protection hysteresis	$T_{JTSDhys}$	-	50	-	$^{\circ}\text{C}$	
VDD UVLO releasing voltage	V_{DDUV}	2.55	3.0	3.3	V	In V_{DD} voltage rising
VDD UVLO hysteresis	$V_{DDUVhys}$	0.15	0.25	0.35	V	
VBB UVLO releasing voltage	V_{BBUV}	6.5	9	9.75	V	In V_{BB} voltage rising
VBB UVLO hysteresis	$V_{BBUVhys}$	0.15	0.3	0.45	V	

FG

FG output saturation voltage	$V_{FG(sat)}$	0.08	0.45	0.7	V	$I_{FG}=2\text{mA}$
FG output pin ON current	$I_{FI(ON)}$	5	7.5	25	mA	$V_{FI}=2\text{V}$
FG output leak current	I_{FGlk}	-1	0	50	μA	$V_{FG}=5.5\text{V}$

Hall Logic

Hall input current	I_{HALL}	-2	-0.1	2	μA	$V_{IN}=0.2\sim 3.5\text{V}$
Common mode input voltage	V_{CMR}	0.2	-	4	V	
AC input voltage range	V_{HALL}	60	-	-	mV _{p-p}	
Hysteresis	V_{HYS}	20	40	V_{HALL}	mV	
Pulse removal filter	t_{pulse}	0.9	2	4	μs	
Hall input thresh voltage	$V_{HIC(1)}$	2.3	2.5	2.8	V	In applied voltage rising/ Hall IC input
Hall input hysteresis	$V_{HIC(1)HYS}$	20	40	60	mV	Hall IC input

FG amplifier

FG input bias current	I_{BFG}	-1	0	1	μA	
FG input offset voltage	V_{OSFG}	-60	-	60	mV	
FGO output leak current	I_{OH}	-110	-	10	μA	
FGO output L voltage	V_{OL}	0.05	-	0.6	V	$I=10\mu\text{A}$
FG amplifier bias voltage	V_{BFG}	2.2	2.5	2.8	V	
FG comparator hysteresis	V_{FGhys}	20	70	150	mV	

- Typ data is for reference only.
- Negative current is defined as coming out of the specified pin.

Serial Interface

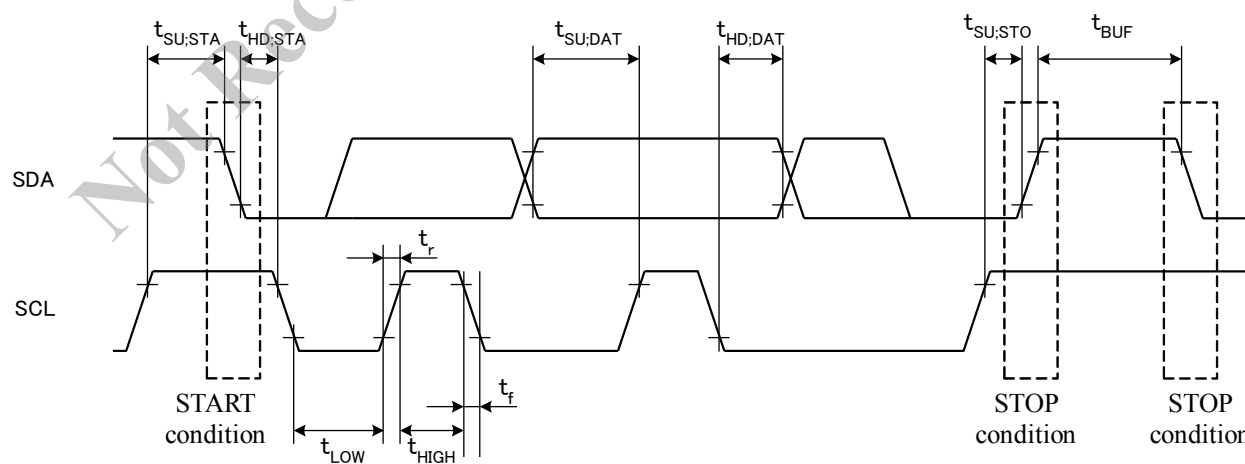
Electrical Characteristic(continued) ($T_a=25^{\circ}\text{C}$, $V_{BB}=24\text{V}$, Unless Otherwise Noted.)

Parameter	Symbol	Conditions	Ratings			
			Min.	Typ.	Max.	Unit
SCL Clock Frequency	f_{SCL}				400	kHz
Start Condition Hold Time	$t_{\text{HD:STA}}$		0.6			μs
Start Condition Set Up Time	$t_{\text{SU:STA}}$		0.6			μs
SCL Low Time	t_{LOW}		1.3			μs
SCL High Time	t_{HIGH}		0.6			μs
SDA Hold Time	$t_{\text{HD:DAT}}$		0		900	ns
SDA Set Up Time	$t_{\text{SU:DAT}}$		100			ns
Rising Time of SCL and SDA	t_r				300	ns
Falling Time of SCL and SDA	t_f				300	ns
Stop Condition Set Up Time	$t_{\text{SU:STO}}$		0.6			μs
Bus Free Time between Stop and Start Condition	t_{BUF}		1.3			μs

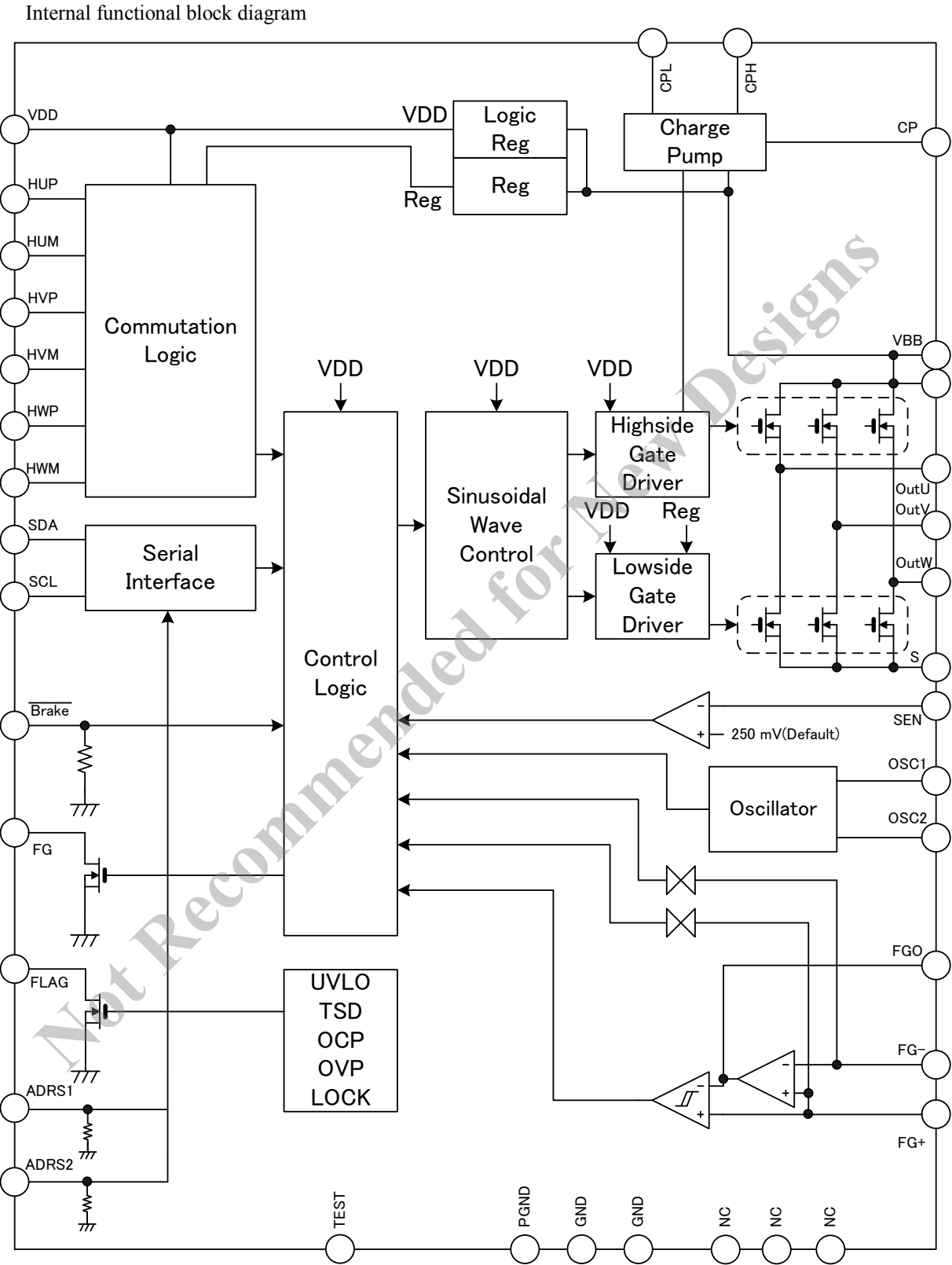
※All threshold voltage referred to $V_{\text{IH}}(\text{Min.})$ and $V_{\text{IL}}(\text{Max.})$ level.

※There are design guarantee values.

Serial Timing



Block diagram (Connection diagram)



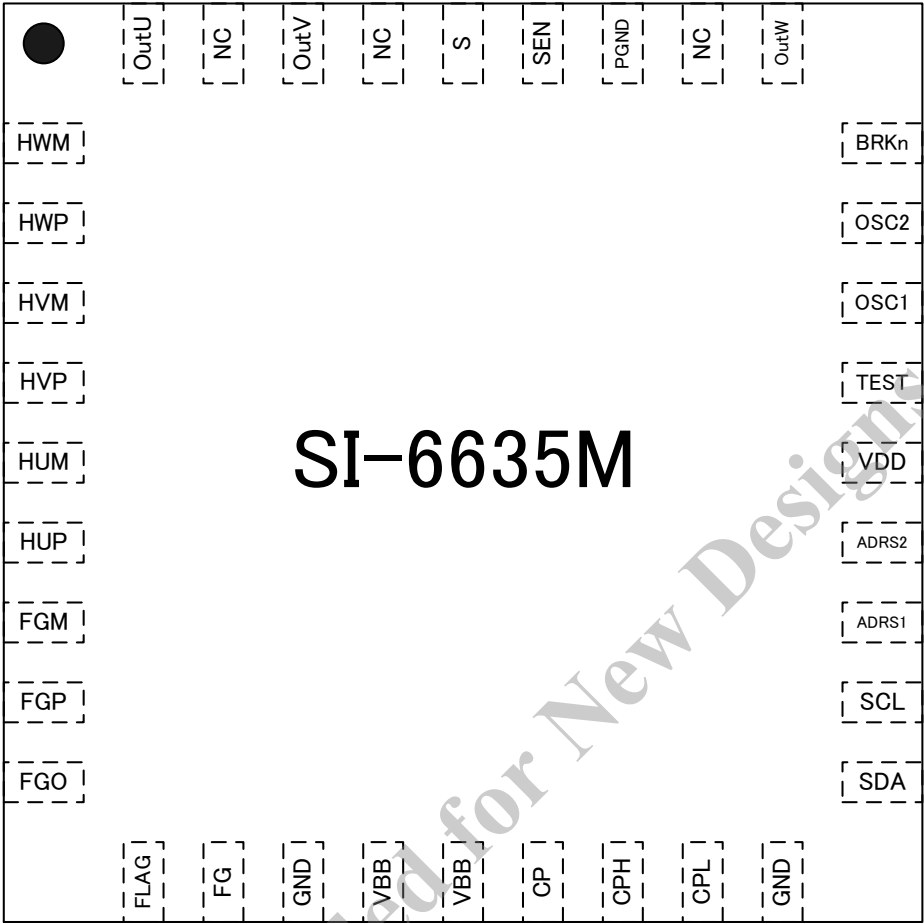
Pin Assignment (Terminal Functions)

1	HWM	Hall input W-
2	HWP	Hall input W+
3	HVM	Hall input V-
4	HVP	Hall input V+
5	HUM	Hall input U-
6	HUP	Hall input U+
7	FGM	Pattern FG input (-)/ Encoder input
8	FGP	Pattern FG input (+)/ Encoder input
9	FGO	Pattern FG feedback
10	FLAG	Output for protection detected
11	FG	FG signal output/ Error output for designated speed
12	GND	Ground
13	VBB	Motor power supply
14	VBB	Motor power supply
15	CP	Reservoir pin for charge pump
16	CPH	Reservoir pin for charge pump (High)
17	CPL	Reservoir pin for charge pump (Low)
18	GND	Ground
19	SDA	Serial interface (data)
20	SCL	Serial interface (clock)
21	ADRS1	Device address setting (most significant bit)
22	ADRS2	Device address setting (least significant bit)
23	VDD	Ceramic capacitor connection for internal regulator
24	TEST	for test
25	OSC1	for ceramic oscillator connection/ External clock input
26	OSC2	for ceramic oscillator connection
27	BRKn	Brake input
28	OUTW	Output for W phase
29	N.C.	No connection
30	PGND	Power ground
31	SEN	Current sensing input
32	S	Source pin
33	N.C.	No connection
34	OUTV	Output for V phase
35	N.C.	No connection
36	OUTU	Output for U phase

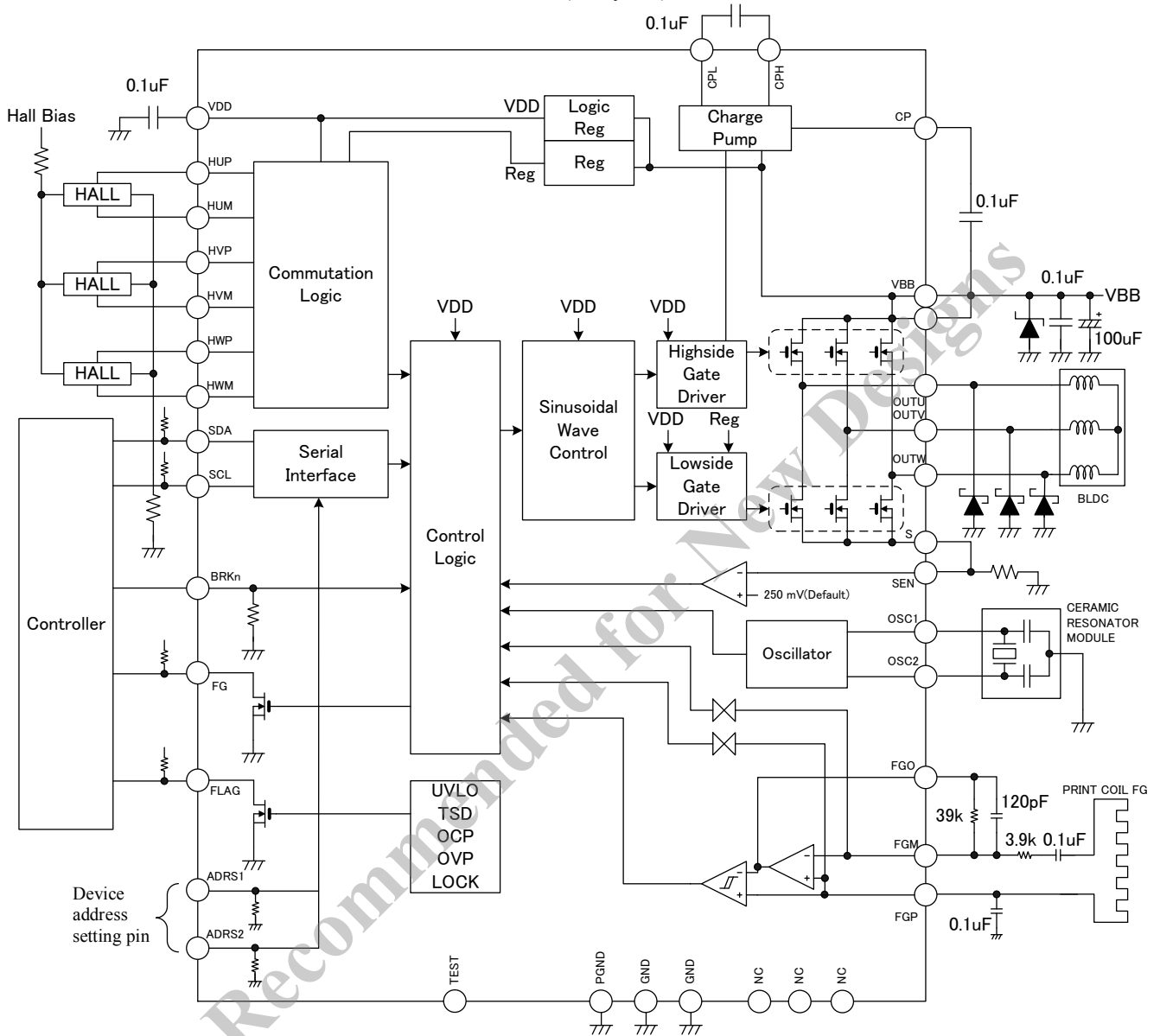
※ Both VBB pins should be connected to VBB line on PCB.

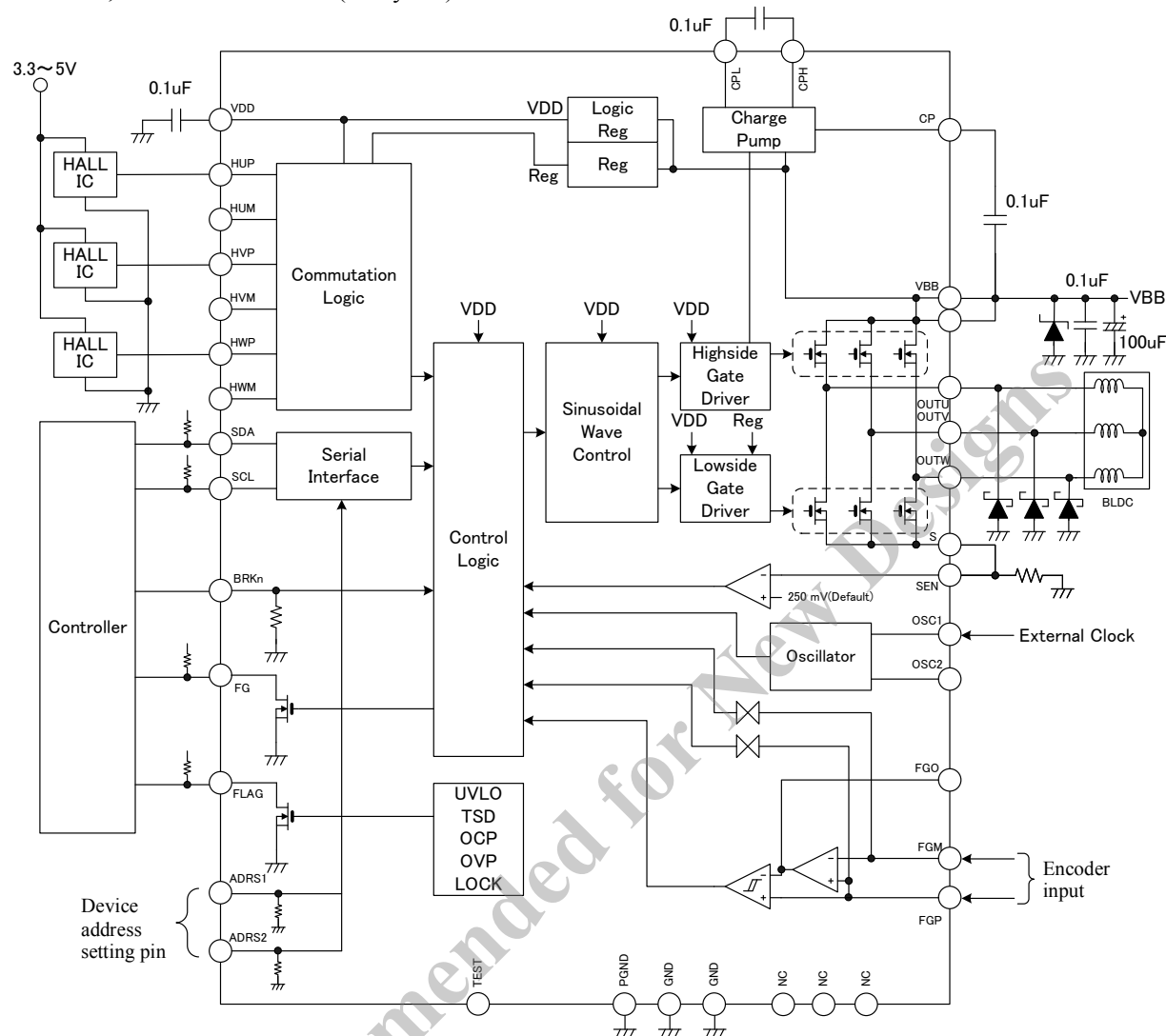
※ GND pins and PGND pin should be connected to GND line on PCB.

Pin assignment diagram



Example application circuit(Evaluation Board Circuit)

Ceramic resonator module, Hall element and Print coil FG (set by I²C)

External clock, Hall IC and Encoder (set by I²C)

※1 : The capacitance on VBB or VDD is used as close to the device as possible.

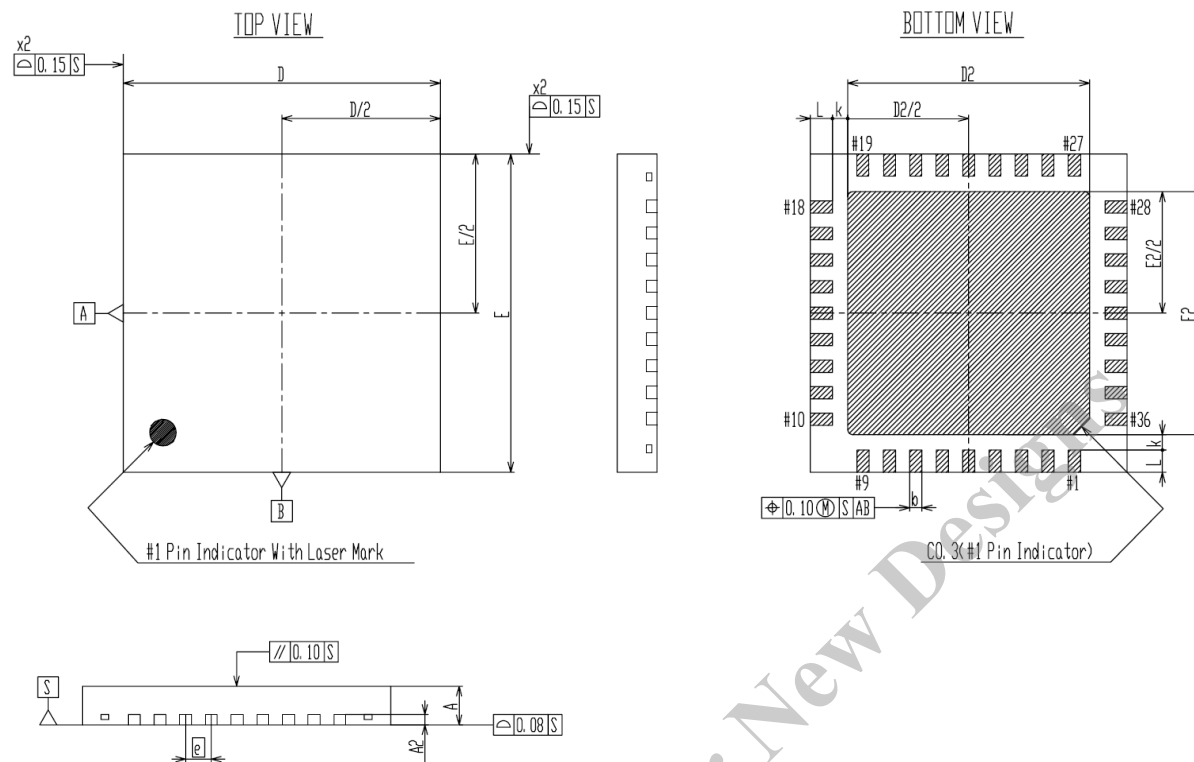
※2 : Care should be taken for power dissipation for SEN/S resistance.

☆ Precaution to avoid the noise on V_{DD} line.

Switching noise from PCB traces, where high current flows, to the V_{DD} line should be minimized because the noise level more than 0.3V on the V_{DD} line may cause malfunctioning operation.

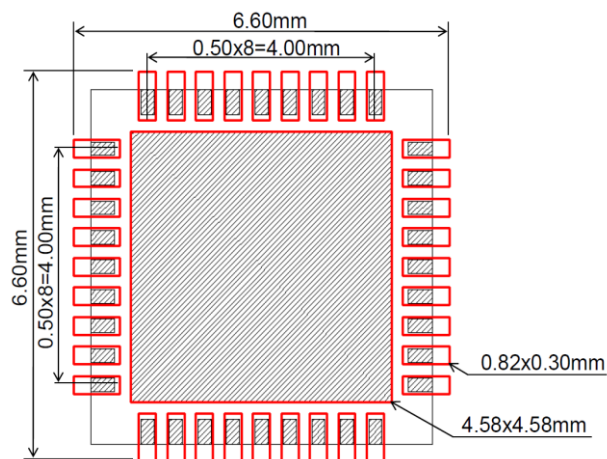
7 Package information

7-1 Package type, physical dimensions and recommendation foot print



Recommendation foot print (red line)

SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2	0.20 REF.		
b	0.18	0.23	0.28
D	5.90	6.00	6.10
D2	4.43	4.58	4.73
E	5.90	6.00	6.10
E2	4.43	4.58	4.73
e	0.50 BSC.		
k	0.25	—	—
L	0.32	0.42	0.52



Dimensions in millimeters

Material of terminal: Cu

Treatment of terminal : Ni + Pd +Au (Pb Free)

7-2 Appearance

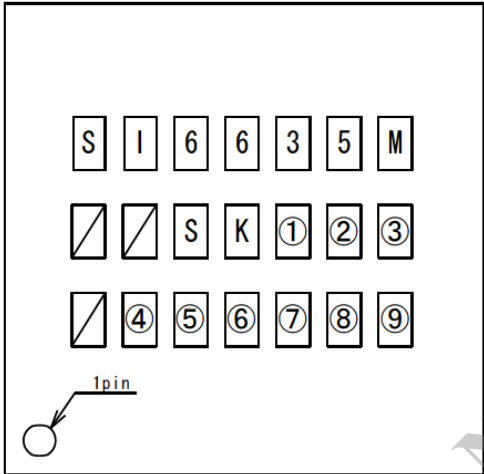
The body shall be clean and shall not bear any stain, rust or flaw.

7-3 Marking

The type number and lot number shall be clearly marked by laser so that cannot be erased easily.

7-4 Blanding

SI-6635M Marking Specification



Discrimination	Mark No	Contents
Year	①	The last digit of year
Month	②	Month by number or alphabet when assembly is started [1-9] in case from January to September [O] in case October [N] in case November [D] in case December
Week	③	[1] in case from first to tenth [2] in case from eleven to twentieth [3] in case from twenty to first to thtry first
Casting order	④、⑤	Assembly entry order 1 to 9 to be used.”11” ~ “99” ("0" is excluded) *Unit of assembly entry order is per MIC lot
Registration code	⑥~⑨	The last three digit of MIC’s lot number + "T" mark

8 Packing specifications

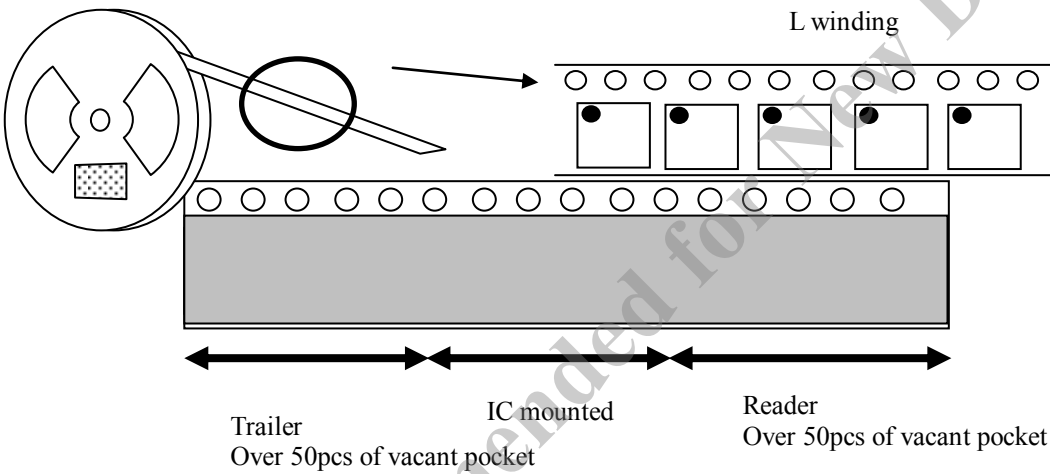
8-1. Container/Material/The number of parts per reel

Container is taping. the number of parts is 2500pcs per reel.
Remainder is packed with combination with next lot.

8-2. The material of taping

Material	
Emboss tape	The width of tape : 16mm
Reel	φ330 [mm]
laminate bag	Size : 0.075×380× 450 [mm]
Inner packing figure	Size : 340×360× 55 [mm]
Outer packing figure	Size : 350×370×230 [mm] 4 reels(max) per 1 outer box

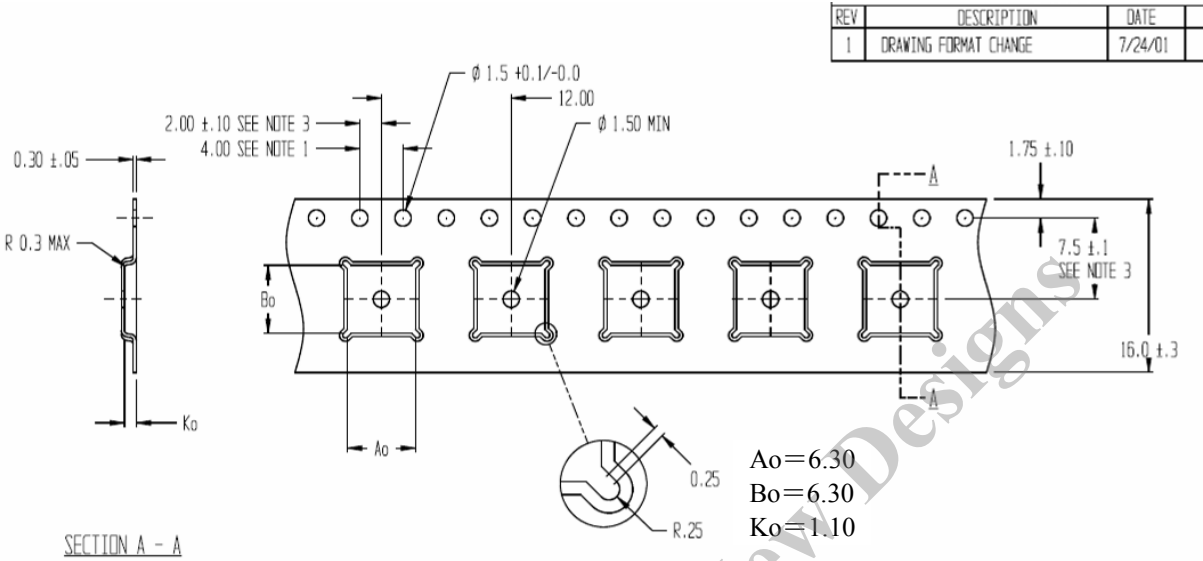
8-3. Emboss tape diagram



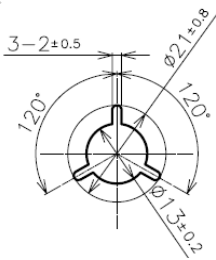
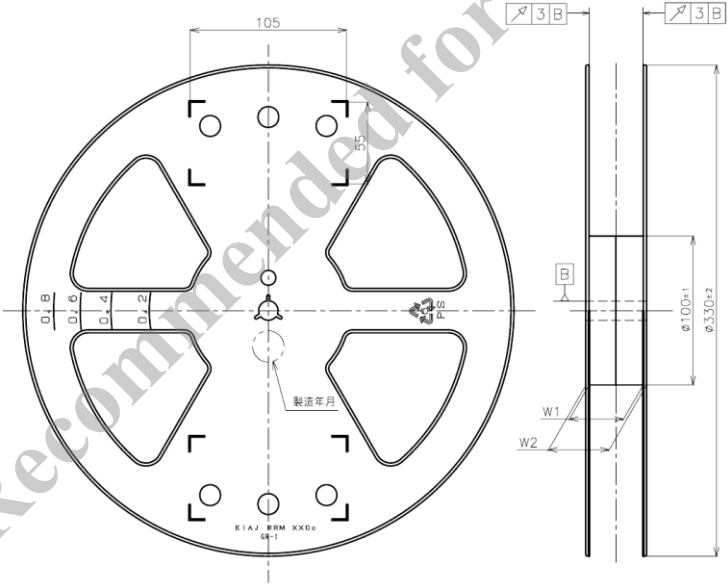
※ It is heat-sealed with cover tape in reader and trailer.

8-4. Dimension, material and diagram

8-4-1. Emboss tape



8-4-2. Reel



Detail drawing of shaft hole

Dimension in millimeter

• 8-5-1

Storage environment is below.

Temperature: 5 degrees-30 degrees

Humidity: 90% or below

Storage limitation is within 12month from packing date

8-5-2

If the above storage condition (8-5.1) is expired, the device is needed to have baking with 125 degrees for 20 hours. Also, Tape and reel are not guaranteed with the temperature and time condition.

If the device should be baked, it is needed to use container with "heatproof" or temperature to cover baking condition. And the container is needed to have static electricity control.

Not Recommended for New Designs

9 Cautions and warnings

Input/output (SDA, SCL, FG, FLAG, Brake, ADRS1, ADRS2, TEST)

- Be sure to prevent the logic input (SDA, SCL, for 2-wire serial) from being "OPEN".
※In case some of the logic inputs stay "OPEN", a malfunction may occur due to external noises.
- Logic input (Brake, ADRS1, ADRS2) has internal 78k ohm (typ) pull-down resistor.
Please take care that current source/sink capacity of external microcontroller if use.
- TEST terminal should be used as open or connected to GND.
- When the open-drain output (FG, FLAG) is not used, be sure to keep it "OPEN" or GND.
※In case it is connected to VDD, it may cause the device's deterioration or/and breakdown.

Schottky should be needed between each OUT pin and GND(Please see 6. Example application circuit).

About the protection circuit operation

This product has protection circuits (motor coil short-circuit and overheating).

These protection circuits work with detecting the thing that excessive energy joins the driver.

Therefore, it is not possible to protect it when the energy caused by the motor coil short-circuit is outside the tolerance of the driver.

Notice

This driver has MOS inputs. Please notice as following contents.

- When static electricity is a problem, care should be taken to properly control the room humidity. This is particularly true in the winter when static electricity is most troublesome.
- Care should be taken with device leads and with assembly sequencing to avoid applying static charges to IC leads. PC board pins should be shorted together to keep them at the same potential to avoid this kind of trouble.

10. other

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In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature (T_j) affects the reliability significantly.
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