

610762 ✓ 9328 011168 ✓  
93L28

## DUAL 8-BIT SHIFT REGISTER

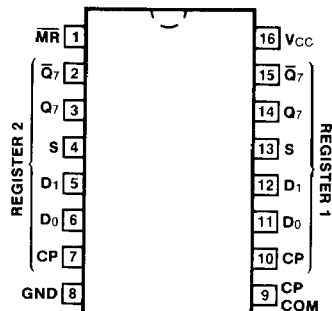
**DESCRIPTION** — The '28 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

- **2-INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**

**ORDERING CODE:** See Section 9

| PKGS            | PIN OUT | COMMERCIAL GRADE                                                                       | MILITARY GRADE                                                                             | PKG TYPE |
|-----------------|---------|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|----------|
|                 |         | $V_{CC} = +5.0 \text{ V} \pm 5\%$ ,<br>$T_A = 0^\circ \text{C to } +70^\circ \text{C}$ | $V_{CC} = +5.0 \text{ V} \pm 10\%$ ,<br>$T_A = -55^\circ \text{C to } +125^\circ \text{C}$ |          |
| Plastic DIP (P) | A       | 9328PC, 93L28PC                                                                        |                                                                                            | 9B       |
| Ceramic DIP (D) | A       | 9328DC, 93L28DC                                                                        | 9328DM, 93L28DM                                                                            | 6B       |
| Flatpak (F)     | A       | 9328FC, 93L28FC                                                                        | 9328FM, 93L28FM                                                                            | 4L       |

### CONNECTION DIAGRAM PINOUT A



**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

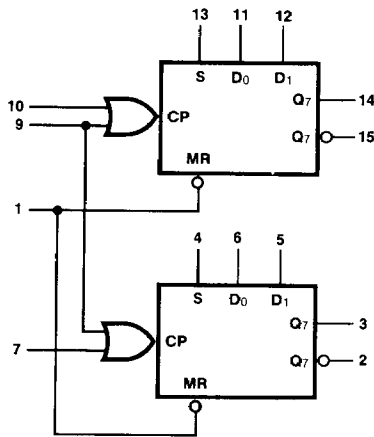
| PIN NAMES                       | DESCRIPTION                                       | 93XX (U.L.)<br>HIGH/LOW | 93L (U.L.)<br>HIGH/LOW   |
|---------------------------------|---------------------------------------------------|-------------------------|--------------------------|
| S                               | Data Select Input                                 | 2.0/2.0                 | 1.0/0.5                  |
| D <sub>0</sub> , D <sub>1</sub> | Data Inputs                                       | 1.0/1.0                 | 0.5/0.25                 |
| CP                              | Clock Pulse Input (Active HIGH)<br>Common (Pin 9) | 3.0/3.0                 | 1.5/0.75                 |
|                                 | Separate (Pins 7 and 10)                          | 1.5/1.5                 | 0.75/0.375               |
| MR                              | Master Reset Input (Active LOW)                   | 1.0/1.0                 | 0.5/0.25                 |
| Q <sub>7</sub>                  | Last Stage Output                                 | 20/10                   | 10/5.0                   |
| $\bar{Q}_7$                     | Complementary Output                              | 20/10                   | (3.0)<br>10/5.0<br>(3.0) |

**FUNCTIONAL DESCRIPTION** — The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs  $D_0$  and  $D_1$  are controlled by the data select input (S) following the Boolean expression:

$$\text{Serial data in: } S_D = S D_0 + S D_1$$

An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

#### LOGIC SYMBOL



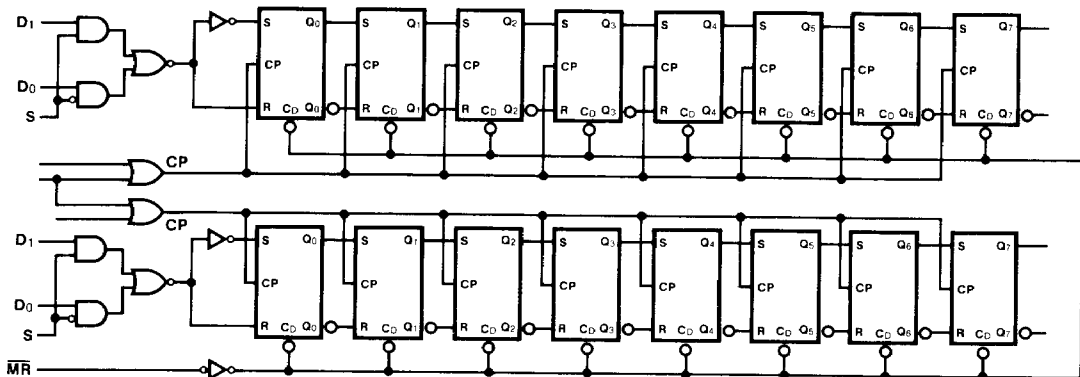
$V_{CC}$  = Pin 16  
GND = Pin 8

#### SHIFT SELECT TABLE

| INPUTS |       |       | OUTPUT          |
|--------|-------|-------|-----------------|
| S      | $D_0$ | $D_1$ | $Q_7 (t_n + 8)$ |
| L      | L     | X     | L               |
| L      | H     | X     | H               |
| H      | X     | L     | L               |
| H      | X     | H     | H               |

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
 $n + 8$  = Indicates state after eight clock pulse

#### LOGIC DIAGRAM



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL          | PARAMETER            | 93XX |     | 93L  |     | UNITS | CONDITIONS            |
|-----------------|----------------------|------|-----|------|-----|-------|-----------------------|
|                 |                      | Min  | Max | Min  | Max |       |                       |
| I <sub>CC</sub> | Power Supply Current | 77   |     | 25.3 |     | mA    | V <sub>CC</sub> = Max |

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL                               | PARAMETER                                                     | 93XX                                             | 93L                    | UNITS | CONDITIONS      |
|--------------------------------------|---------------------------------------------------------------|--------------------------------------------------|------------------------|-------|-----------------|
|                                      |                                                               | C <sub>L</sub> = 15 pF<br>R <sub>L</sub> = 400 Ω | C <sub>L</sub> = 15 pF |       |                 |
|                                      |                                                               | Min    Max                                       | Min    Max             |       |                 |
| f <sub>max</sub>                     | Maximum Shift Right Frequency                                 | 20                                               | 5.0                    | MHz   | Figs. 3-1, 3-8  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>CP to Q <sub>7</sub> or $\overline{Q}_7$ | 20<br>35                                         | 45<br>80               | ns    | Figs. 3-1, 3-8  |
| t <sub>PHL</sub>                     | Propagation Delay $\overline{MR}$ to Q <sub>7</sub>           | 50                                               | 110                    | ns    | Figs. 3-1, 3-16 |

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

| SYMBOL                                   | PARAMETER                                      | 93XX |     | 93L |     | UNITS | CONDITIONS |
|------------------------------------------|------------------------------------------------|------|-----|-----|-----|-------|------------|
|                                          |                                                | Min  | Max | Min | Max |       |            |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup Time HIGH or LOW<br>D <sub>n</sub> to CP | 20   | 20  | 30  | 30  | ns    | Fig. 3-6   |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold Time HIGH or LOW<br>D <sub>n</sub> to CP  | 0    | 0   | 0   | 0   | ns    |            |
| t <sub>w</sub> (H)<br>t <sub>w</sub> (L) | Clock Pulse Width HIGH<br>or LOW               | 25   | 25  | 55  | 55  | ns    |            |
| t <sub>w</sub> (L)                       | $\overline{MR}$ Pulse Width with CP HIGH       | 30   |     | 60  |     | ns    | Fig. 3-16  |
| t <sub>w</sub> (L)                       | $\overline{MR}$ Pulse Width with CP LOW        | 40   |     | 70  |     | ns    |            |
| t <sub>rec</sub>                         | Recovery Time $\overline{MR}$ to CP            | 33   |     |     |     | ns    | Fig. 3-16  |