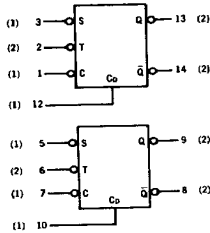


DUAL J-K FLIP-FLOPS

PLASTIC mW MRTL MC700P/800P series

MC776P • MC876P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



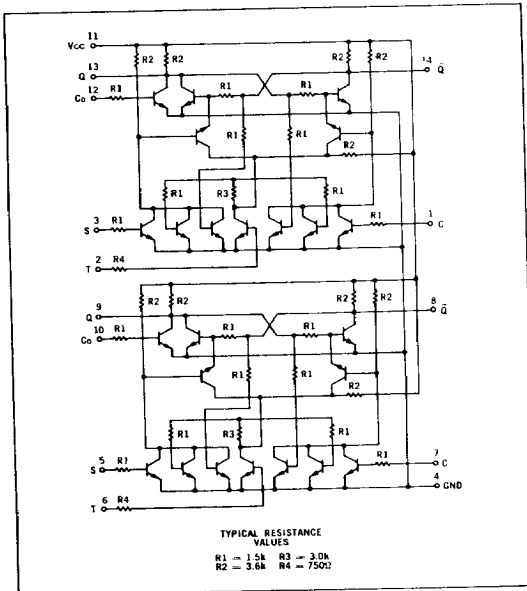
$f_{max} \dots 3 \text{ MHz min}$
 $P_o \dots 41 \text{ mW (Only Clock Input High)}$
 $29 \text{ mW (All Inputs Low)}$

NUMBER IN PARENTHESES INDICATES LOADING FACTOR

CLOCKED INPUT OPERATION

$t_{C \rightarrow Q}$	S	C	Q	\bar{Q}
1	1	1	0	1
2	1	0	1	0
3	0	1	0	1
4	0	0	Q	\bar{Q}

- ① Direct input (Co) must be low.
- ② The time period prior to the negative transition of the clock pulse is denoted t_c and the time period subsequent to this transition is denoted t_d .
- ③ Q is the state of the Q output in the time period t_c .



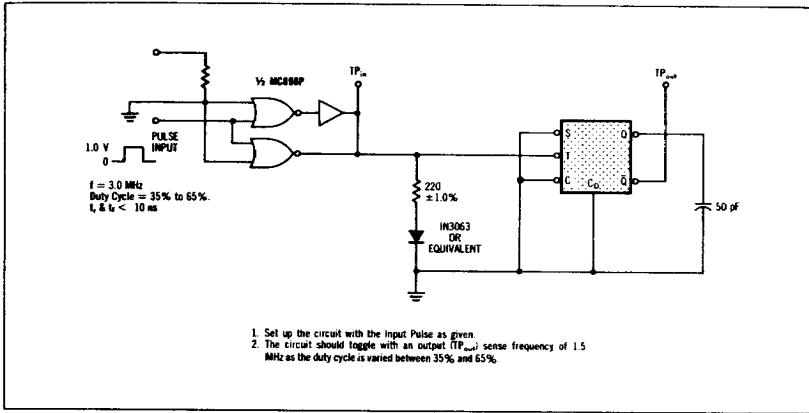
Characteristics	Pin Under Test	TEST VALUES													
		mVdc						µA							
		V _{in}	V _{out}	V _{sat}	V _{on}	V _{ce}	I _p	V _{in}	V _{out}	V _{sat}	V _{on}	V _{ce}	I _p		
© Test Temperature 0°C 0.880 0.850 1.80 0.500 3.60 270 +25°C 0.830 0.800 1.80 0.460 3.60 280 +75°C 0.740 0.710 1.80 0.400 3.60 270 +15°C 0.865 0.865 1.80 0.475 3.60 270 +25°C 0.850 0.850 1.80 0.460 3.60 270 +55°C 0.800 0.800 1.80 0.450 3.60 270															
Symbol	Pin Under Test	TEST VALUES													
		APPLIED TO PINS LISTED BELOW:													
		V _{in}	V _{out}	V _{sat}	V _{on}	V _{ce}	I _p	V _{in}	V _{out}	V _{sat}	V _{on}	V _{ce}	I _p		
Characteristics	Pin Under Test	TEST LIMITS													
		MC776P				MC776P				MC776P					
		8°C		+25°C		+75°C		+15°C		+25°C		+55°C		+55°C	
Input Current	I _{in} 2 I _{in} I _{in} I _{in}	1	150	-	140	Min	Max	Min	Max	Min	Max	Min	Max	Unit	µAdc
		2	300	-	280	-	300	-	300	-	300	-	300	-	150
		3	150	-	140	-	150	-	150	-	150	-	150	-	300
		12	150	-	140	-	150	-	150	-	150	-	150	-	150
Output Current	I _{A2}	13	320	-	300	-	320	-	320	-	320	-	320	-	µAdc
		14	-	-	-	-	-	-	-	-	-	-	-	-	µAdc
Output Voltage	V _{out}	13	400	-	350	-	400	-	300	-	300	-	320	-	mVdc
		13**	-	-	-	-	-	-	-	-	-	-	-	-	mVdc
		13**	-	-	-	-	-	-	-	-	-	-	-	-	mVdc
		14	-	-	-	-	-	-	-	-	-	-	-	-	mVdc
Saturation Voltage	V _{CE(sat)}	13	250	-	250	-	220	-	230	-	320	-	320	-	mVdc
		14	-	-	-	-	-	-	-	-	-	-	-	-	mVdc
Turn On Voltage	V _{on}	13**	850	-	800	-	865	-	850	-	800	-	800	-	mVdc
		13**	-	-	-	-	-	-	-	-	-	-	-	-	mVdc

ELECTRICAL CHARACTERISTICS
 Test procedures are shown for one flip-flop only.
 The other flip-flop is tested in the same manner.

* Click: Pulse to pin 2
 † Pin 13 = LOW: Set by a momentary ground prior to the application of the negative-going clock.
 ‡ Pin 14 = LOW: application of the negative-going clock.
 § ground thru diode (cathode to ground).
 ¶ Ground inputs of flip-flop not under test.
 Other pins not listed are left open.

MC776P, MC876P (continued)

TOGGLE MODE TEST CIRCUIT



CLOCK PULSE

MC776P		
T _A	V _L	V _H
15°C	0.475 V	0.915 V
25°C	0.460 V	0.900 V
55°C	0.430 V	0.850 V

MC876P		
T _A	V _L	V _H
0°C	0.50 V	0.900 V
25°C	0.46 V	0.850 V
75°C	0.40 V	0.760 V

All values are ± 2.0mV

CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

- Voltage applied to Clock pin is raised to V_H. t_r is not critical, but should be < 1.0 μs.
- Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
- Apply momentary ground (when applicable).
- Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
- Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.