

8-bit Microcontrollers

CMOS

New 8FX MB95430H Series

MB95F432H/F433H/F434H MB95F432K/F433K/F434K

■ DESCRIPTION

MB95430H is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

■ FEATURES

- F²MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

- Clock

- Selectable main clock source

Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)

External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)

Main CR clock (1/8/10/12.5 MHz $\pm$ 2%, maximum machine clock frequency: 12.5 MHz)

- Selectable subclock source

Sub-OSC clock (32.768 kHz)

External clock (32.768 kHz)

Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

- Timer

- 8/16-bit composite timer $\times$ 1 channel
- 16-bit PPG $\times$ 1 channel
- 16-bit free-running timer $\times$ 1 channel
- 16-bit output compare $\times$ 2 channels
- Time-base timer $\times$ 1 channel
- Watch prescaler $\times$ 1 channel

- UART/SIO $\times$ 1 channel

- Full duplex double buffer
- Capable of clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer

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For the information for microcontroller supports, see the following website.

<http://edevic.fujitsu.com/micom/en-support/>

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- I²C × 1 channel
 - Built-in wake-up function
- Voltage comparator × 4 channels
- Operational amplifier (OPAMP) × 1 channel
 - Software-select programmable gain
 - Software-select standalone option
 - Power down function included
- External interrupt × 8 channels
 - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
 - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter × 17 channels
 - 8-bit and 10-bit resolution can be chosen.
- Low power consumption (standby) modes
 - Stop mode
 - Sleep mode
 - Watch mode
 - Time-base timer mode
- I/O port
 - MB95F432H/F433H/F434H (maximum no. of I/O ports: 28)
 - General-purpose I/O ports (N-ch open drain) : 1
 - General-purpose I/O ports (CMOS I/O) : 27
 - MB95F432K/F433K/F434K (maximum no. of I/O ports: 29)
 - General-purpose I/O ports (N-ch open drain) : 2
 - General-purpose I/O ports (CMOS I/O) : 27
- On-chip debug
 - 1-wire serial control
 - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
 - Built-in hardware watchdog timer
 - Built-in software watchdog timer
- Low-voltage detection reset circuit (available only on MB95F432K/F433K/F434K)
 - Built-in low-voltage detector
- Clock supervisor counter
 - Built-in clock supervisor counter function
- Programmable port input voltage level
 - CMOS input level / hysteresis input level
- Dual operation Flash memory
 - The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
 - Protects the content of the Flash memory

■ PRODUCT LINE-UP

Part number	MB95F432H	MB95F433H	MB95F434H	MB95F432K	MB95F433K	MB95F434K
Parameter						
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	240 bytes	496 bytes	240 bytes	240 bytes	496 bytes
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected by software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (with machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 μs (with machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 28 • CMOS I/O : 27 • N-ch open drain: 1			• I/O ports (Max) : 29 • CMOS I/O : 27 • N-ch open drain: 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (with external clock frequency = 4 MHz)					
Hardware/software watchdog timer	• Reset generation cycle - Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
8/10-bit A/D converter	17 channels (Ch. 16 is the channel for OPAMP output.) 8-bit resolution and 10-bit resolution can be chosen.					
8/16-bit composite timer	1 channel • The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
External interrupt	8 channels • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from different standby modes.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
UART/SIO	1 channel • Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					

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Part number	MB95F432H	MB95F433H	MB95F434H	MB95F432K	MB95F433K	MB95F434K
Parameter						
I ² C	1 channel • Master/slave transmission and receiving • It has a bus error function, an arbitration function, a transmission direction detection function and a wake-up function. • It also has functions of generating and detecting repeated START conditions.					
16-bit PPG	• PWM mode and single-shot mode are available to use. • Ch. 0 can work with the multi-functional timer or individually.					
Output compare	• 1 channel of 16-bit free-running timer with a compare buffer • 2 channels of 16-bit output compare					
Voltage comparator	4 channels					
OPAMP	• This is an operational amplifier used in an induction heater. It contains 7 software (registers) select close loop gain selections for ground current sensing according to different sense resistor values. The OPAMP can also work as a standalone OPAMP. • It selects closed loop gain for ground current sensing according to different sense resistor values of a standalone OPAMP.					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, and write/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of write/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-32P-M30 DIP-32P-M06					

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number Package	MB95F432H	MB95F433H	MB95F434H	MB95F432K	MB95F433K	MB95F434K
FPT-32P-M30	O	O	O	O	O	O
DIP-32P-M06	O	O	O	O	O	O

O: Available

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON PRODUCT SELECTION

- Current consumption

When using the on-chip debug function, take account of the current consumption of flash program/erase.

For details of current consumption, see “■ ELECTRICAL CHARACTERISTICS”.

- Package

For details of information on each package, see “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSION”.

- Operating voltage

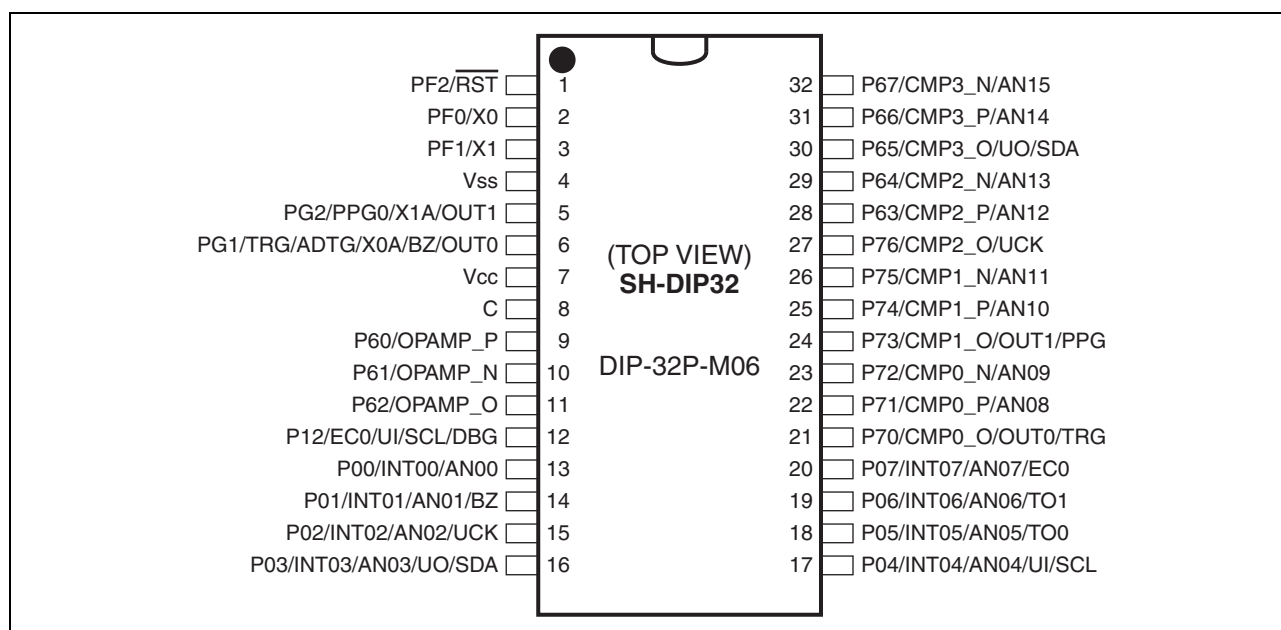
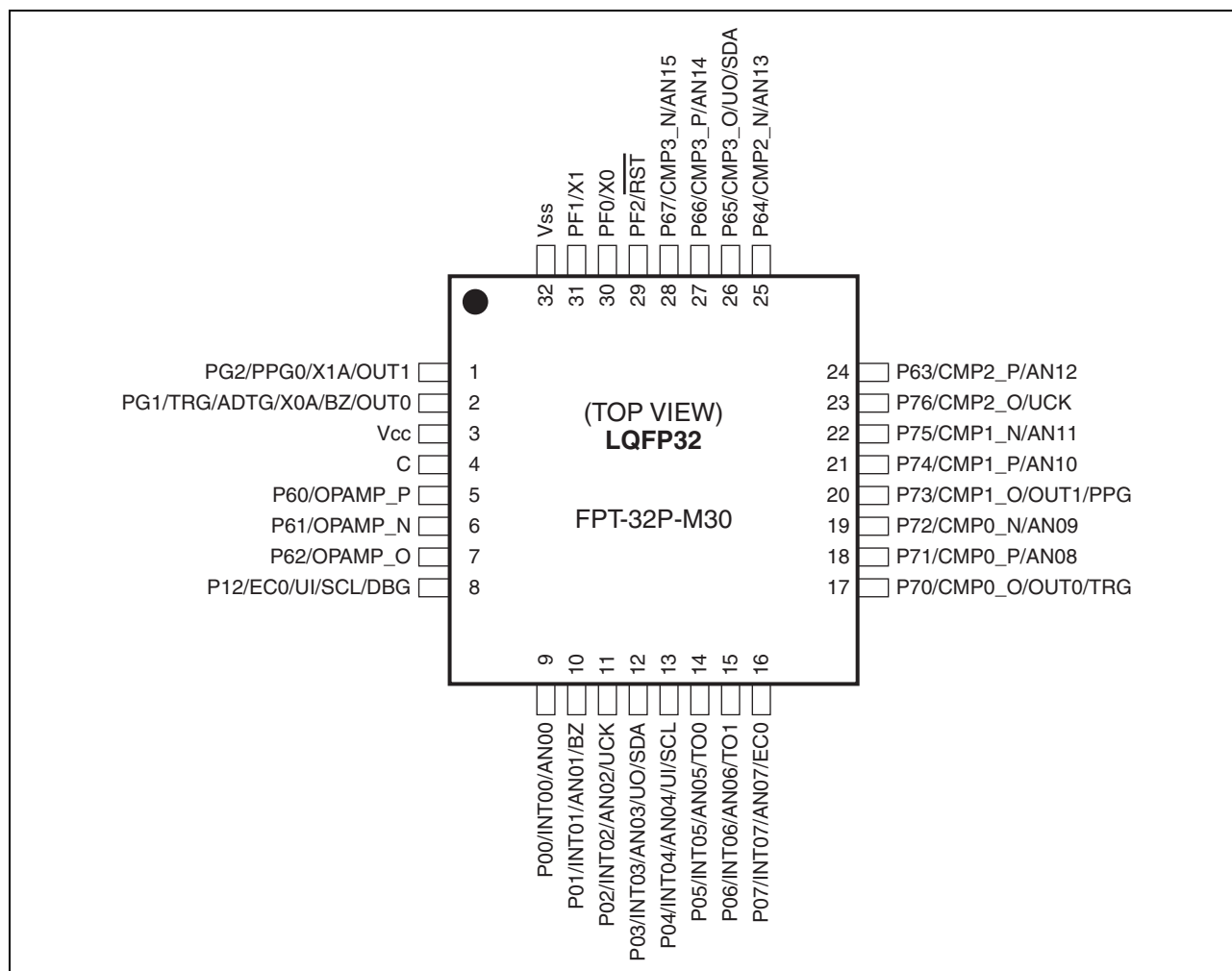
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “■ ELECTRICAL CHARACTERISTICS”.

- On-chip debug function

The on-chip debug function requires that V_{CC} , V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 29 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in the hardware manual of the MB95430H Series.

PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type*3	Function
LQFP32*1	SH-DIP32*2			
1	5	PG2	C	General-purpose I/O port
		PPG		16-bit PPG output pin
		X1A		Subclock I/O oscillation pin
		OUT1		Output compare ch. 1 output pin
2	6	PG1	C	General-purpose I/O port
		TRG		16-bit PPG trigger input pin
		ADTG		A/D converter trigger input pin
		X0A		Subclock I/O oscillation pin
		BZ		Buzzer output pin
		OUT0		Output compare ch. 0 output pin
3	7	V _{CC}	—	Power supply pin
4	8	C	—	Capacitor connection pin
5	9	P60	K	General-purpose I/O port
		OPAMP_P		Operational amplifier input pin
6	10	P61	K	General-purpose I/O port
		OPAMP_N		Operational amplifier input pin
7	11	P62	J	General-purpose I/O port
		OPAMP_O		Operational amplifier output pin
8	12	P12	H	General-purpose I/O port
		EC0		8/16-bit composite timer external clock input pin
		UI		UART/SIO data input pin
		SCL		I ² C clock I/O pin
		DBG		DBG input pin
9	13	P00	E	General-purpose I/O port
		INT00		External interrupt input pin
		AN00		A/D converter analog input pin
10	14	P01	E	General-purpose I/O port
		INT01		External interrupt input pin
		AN01		A/D converter analog input pin
		BZ		Buzzer output pin
11	15	P02	E	General-purpose I/O port
		INT02		External interrupt input pin
		AN02		A/D converter analog input pin
		UCK		UART/SIO clock I/O pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP32*1	SH-DIP32*2			
12	16	P03	F	General-purpose I/O port
		INT03		External interrupt input pin
		AN03		A/D converter analog input pin
		UO		UART/SIO data output pin
		SDA		I ² C data I/O pin
13	17	P04	F	General-purpose I/O port
		INT04		External interrupt input pin
		AN04		A/D converter analog input pin
		UI		UART/SIO data input pin
		SCL		I ² C clock I/O pin
14	18	P05	E	General-purpose I/O port
		INT05		External interrupt input pin
		AN05		A/D converter analog input pin
		TO0		Timer output pin
15	19	P06	E	General-purpose I/O port
		INT06		External interrupt input pin
		AN06		A/D converter analog input pin
		TO1		Timer output pin
16	20	P07	E	General-purpose I/O port
		INT07		External interrupt input pin
		AN07		A/D converter analog input pin
		EC0		8/16-bit composite timer external clock input pin
17	21	P70	D	General-purpose I/O port
		CMP0_O		Comparator ch. 0 output pin
		OUT0		Output compare ch. 0 output pin
		TRG		16-bit PPG trigger input pin
18	22	P71	I	General-purpose I/O port
		CMP0_P		Comparator ch. 0 positive input pin
		AN08		A/D converter analog input pin
19	23	P72	I	General-purpose I/O port
		CMP0_N		Comparator ch. 0 negative input pin
		AN09		A/D converter analog input pin
20	24	P73	D	General-purpose I/O port
		CMP1_O		Comparator ch. 1 output pin
		OUT1		Output compare ch. 1 output pin
		PPG		16-bit PPG output pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP32*1	SH-DIP32*2			
21	25	P74	I	General-purpose I/O port
		CMP1_P		Comparator ch. 1 positive input pin
		AN10		A/D converter analog input pin
22	26	P75	I	General-purpose I/O port
		CMP1_N		Comparator ch. 1 negative input pin
		AN11		A/D converter analog input pin
23	27	P76	D	General-purpose I/O port
		CMP2_O		Comparator ch. 2 output pin
		UCK		UART/SIO clock I/O pin
24	28	P63	I	General-purpose I/O port
		CMP2_P		Comparator ch. 2 positive input pin
		AN12		A/D converter analog input pin
25	29	P64	I	General-purpose I/O port
		CMP2_N		Comparator ch. 2 negative input pin
		AN13		A/D converter analog input pin
26	30	P65	L	General-purpose I/O port
		CMP3_O		Comparator ch. 3 output pin
		UO		UART/SIO data output pin
		SDA		I ² C data I/O pin
27	31	P66	I	General-purpose I/O port
		CMP3_P		Comparator ch. 3 positive input pin
		AN14		A/D converter analog input pin
28	32	P67	I	General-purpose I/O port
		CMP3_N		Comparator ch. 3 negative input pin
		AN15		A/D converter analog input pin
29	1	PF2	A	General-purpose I/O port
		$\overline{\text{RST}}$		Reset pin Dedicated reset pin in MB95F432H/F433H/F434H
30	2	PF0	B	General-purpose I/O port
		X0		Main clock I/O oscillation pin
31	3	PF1	B	General-purpose I/O port
		X1		Main clock I/O oscillation pin
32	4	V _{SS}	—	Power supply pin (GND)

*1: Package code: FPT-32P-M30

*2: Package code: DIP-32P-M06

*3: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control available

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Type	Circuit	Remarks
D	P-ch Digital output N-ch Standby control Hysteresis input	• CMOS output • Hysteresis input
E	R Pull-up control P-ch Digital output P-ch Digital output N-ch Analog input A/D control Standby control Hysteresis input	• CMOS output • Hysteresis input • Pull-up control available • Analog input
F	R Pull-up control P-ch I²C output control Digital output P-ch Digital output N-ch Analog input A/D control Standby control Hysteresis input CMOS input	• CMOS output • Hysteresis input • CMOS input • Pull-up control available • Analog input • N-ch open drain output (as I²C output)
G	R Pull-up control P-ch Digital output P-ch Digital output N-ch Standby control Hysteresis input	• CMOS output • Hysteresis input • Pull-up control available
H	Standby control Hysteresis input CMOS input Digital output N-ch	• N-ch open drain output • Hysteresis input • CMOS input

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Type	Circuit	Remarks
I	P-ch P-ch N-ch Analog input for A/D Analog input for VC Analog input control Standby control Hysteresis input	- CMOS output - Hysteresis input
J	P-ch P-ch N-ch Analog output Analog output control Standby control Hysteresis input	- CMOS output - Hysteresis input
K	P-ch P-ch N-ch Analog input Analog input control Standby control Hysteresis input	- CMOS output - Hysteresis input
L	P-ch P-ch N-ch I²C output control Digital output Digital output Standby control Hysteresis input CMOS input	- CMOS output - Hysteresis input - CMOS input - N-ch open drain output (as I²C output)

■ NOTES ON DEVICE HANDLING

- Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "1. Absolute Maximum Ratings" of "■ ELECTRICAL CHARACTERISTICS" is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

■ PIN CONNECTION

- Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 k Ω . Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 μ F as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

- DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The DBG pin should not stay at "L" level after power-on until the reset output is released.

- $\overline{RST}$ pin

Connect the $\overline{RST}$ pin directly to an external pull-up resistor.

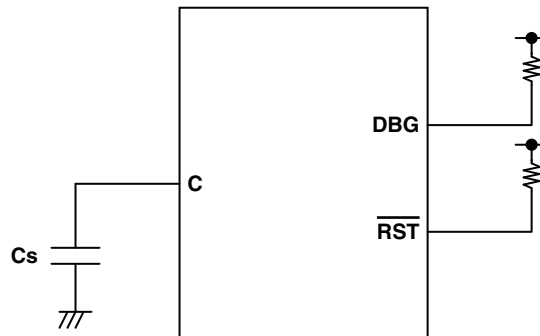
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{RST}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The $\overline{RST}$ /PF2 pin functions as the reset input/output pin after power-on. In addition, the reset output of the $\overline{RST}$ /PF2 pin can be enabled by the RSTOE bit in the SYSC1 register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC1 register.

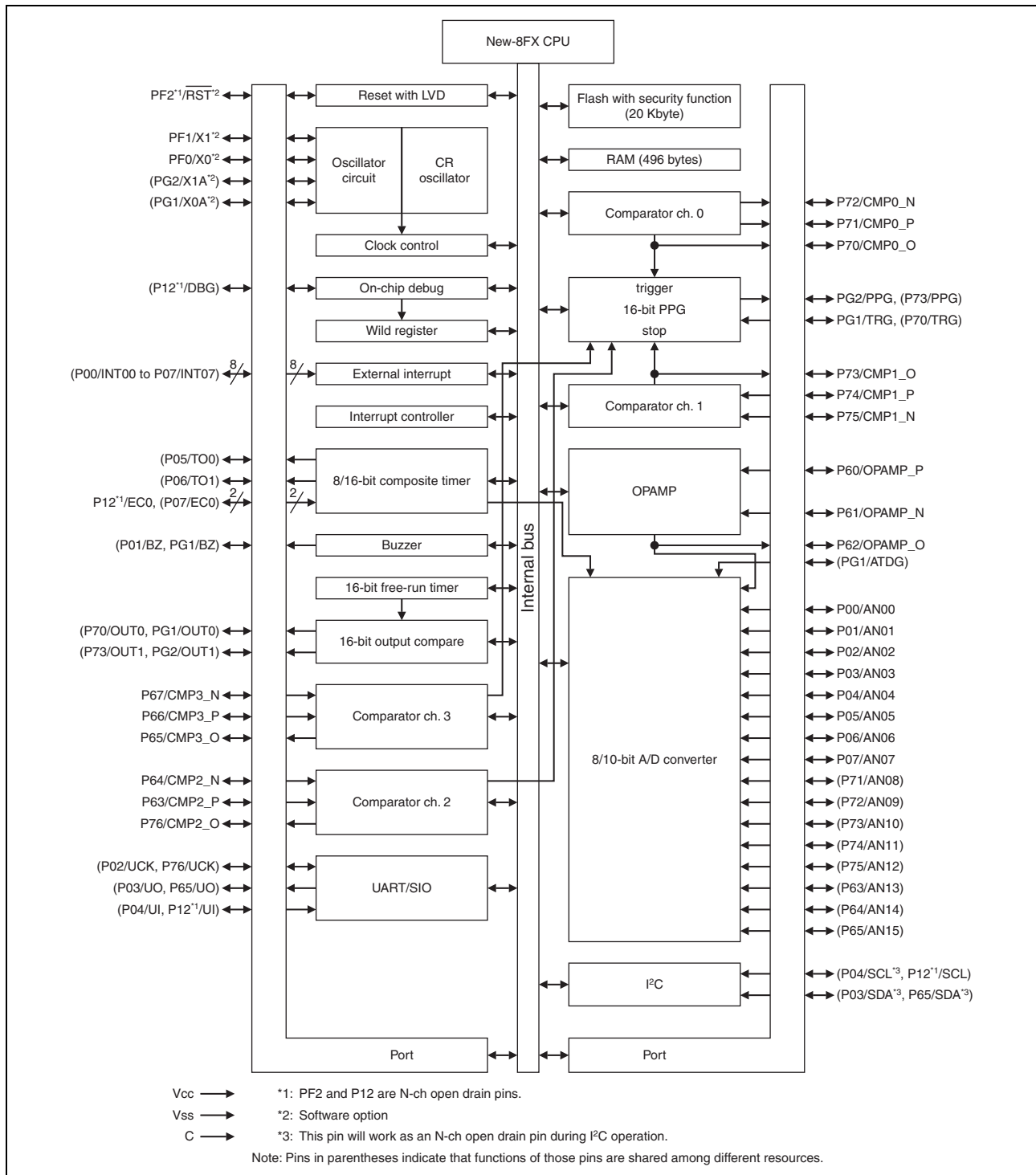
- C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_s . For the connection to a smoothing capacitor C_s , see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_s and the distance between C_s and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG/ $\overline{RST}$ /C pins connection diagram



■ BLOCK DIAGRAM



■ CPU CORE

• Memory Space

The memory space of the MB95430H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95430H Series are shown below.

• Memory Maps

MB95F432H/F432K		MB95F433H/F433K		MB95F434H/F434K	
0000 _H	I/O	0000 _H	I/O	0000 _H	I/O
0080 _H	Access prohibited	0080 _H	Access prohibited	0080 _H	Access prohibited
0090 _H	RAM 240 bytes	0090 _H	RAM 240 bytes	0090 _H	RAM 496 bytes
0100 _H	Register	0100 _H	Register	0100 _H	Register
0180 _H	Access prohibited	0180 _H	Access prohibited	0200 _H	Access prohibited
0F80 _H	Extended I/O	0F80 _H	Extended I/O	0F80 _H	Extended I/O
1000 _H	Access prohibited	1000 _H	Access prohibited	1000 _H	Access prohibited
B000 _H	Flash 4 Kbyte	B000 _H	Flash 4 Kbyte	B000 _H	Flash 20 Kbyte
C000 _H	Access prohibited	C000 _H	Access prohibited		
F000 _H	Flash 4 Kbyte	E000 _H	Flash 8 Kbyte		
FFFF _H		FFFF _H		FFFF _H	

■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000 _H	PDR0	Port 0 data register	R/W	00000000 _B
0001 _H	DDR0	Port 0 direction register	R/W	00000000 _B
0002 _H	PDR1	Port 1 data register	R/W	00000000 _B
0003 _H	DDR1	Port 1 direction register	R/W	00000000 _B
0004 _H	—	(Disabled)	—	—
0005 _H	WATR	Oscillation stabilization wait time setting register	R/W	11111111 _B
0006 _H	—	(Disabled)	—	—
0007 _H	SYCC	System clock control register	R/W	0000X011 _B
0008 _H	STBC	Standby control register	R/W	00000XXX _B
0009 _H	RSRR	Reset source register	R/W	000XXXXX _B
000A _H	TBTC	Time-base timer control register	R/W	00000000 _B
000B _H	WPCR	Watch prescaler control register	R/W	00000000 _B
000C _H	WDTC	Watchdog timer control register	R/W	00XX0000 _B
000D _H	SYCC2	System clock control register 2	R/W	XX100011 _B
000E _H to 0015 _H	—	(Disabled)	—	—
0016 _H	PDR6	Port 6 data register	R/W	00000000 _B
0017 _H	DDR6	Port 6 direction register	R/W	00000000 _B
0018 _H	PDR7	Port 7 data register	R/W	00000000 _B
0019 _H	DDR7	Port 7 direction register	R/W	00000000 _B
0020 _H to 0027 _H	—	(Disabled)	—	—
0028 _H	PDRF	Port F data register	R/W	00000000 _B
0029 _H	DDRF	Port F direction register	R/W	00000000 _B
002A _H	PDRG	Port G data register	R/W	00000000 _B
002B _H	DDRG	Port G direction register	R/W	00000000 _B
002C _H	PUL0	Port 0 pull-up register	R/W	00000000 _B
002D _H to 0034 _H	—	(Disabled)	—	—
0035 _H	PULG	Port G pull-up register	R/W	00000000 _B
0036 _H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000 _B
0037 _H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000 _B
0038 _H	BUZZ	Buzzer control register	R/W	00000000 _B
0039 _H	—	(Disabled)	—	—

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Address	Register abbreviation	Register name	R/W	Initial value
003A _H	CMR0	Voltage comparator control register ch. 0	R/W	000X0001 _B
003B _H	CMR1	Voltage comparator control register ch. 1	R/W	000X0001 _B
003C _H	CMR2	Voltage comparator control register ch. 2	R/W	000X0001 _B
003D _H	CMR3	Voltage comparator control register ch. 3	R/W	000X0001 _B
003E _H	OPCR	OPAMP control register	R/W	00000011 _B
003F _H to 0041 _H	—	(Disabled)	—	—
0042 _H	PCNTH0	16-bit PPG status control register upper ch. 0	R/W	00000000 _B
0043 _H	PCNTL0	16-bit PPG status control register lower ch. 0	R/W	00000000 _B
0044 _H	PTGS0	16-bit PPG trigger source control register ch. 0	R/W	00000000 _B
0045 _H	—	(Disabled)	—	—
0046 _H	OCUOC	16-bit output compare stop trigger control register	R/W	00000000 _B
0047 _H	—	(Disabled)	—	—
0048 _H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000 _B
0049 _H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000 _B
004A _H	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000 _B
004B _H	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000 _B
004C _H , 004D _H	—	(Disabled)	—	—
004E _H	SYSC2	System control register 2	R/W	00000000 _B
004F _H	—	(Disabled)	—	—
0050 _H	IBCR00	I ² C bus control register 0	R/W	00000000 _B
0051 _H	IBCR10	I ² C bus control register 1	R/W	00000000 _B
0052 _H	IBSR0	I ² C bus status register	R/W	00000000 _B
0053 _H	IDDR0	I ² C data register	R/W	00000000 _B
0054 _H	IAAR0	I ² C address register	R/W	00000000 _B
0055 _H	ICCR0	I ² C clock control register	R/W	00000000 _B
0056 _H	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000 _B
0057 _H	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000 _B
0058 _H	SSR0	UART/SIO serial status and data register ch. 0	R/W	00000001 _B
0059 _H	TDR0	UART/SIO serial output data register ch. 0	R/W	00000000 _B
005A _H	RDR0	UART/SIO serial input data register ch. 0	R	00000000 _B
005B _H	—	(Disabled)	—	—
005C _H	TCDTH	16-bit free-running timer data register (upper)	R/W	00000000 _B
005D _H	TCDTL	16-bit free-running timer data register (lower)	R/W	00000000 _B
005E _H	CPCLR _H	16-bit free-running timer compare clear register (upper)	R	11111111 _B
005F _H	CPCLR _L	16-bit free-running timer compare clear register (lower)	R	11111111 _B

(Continued)

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Address	Register abbreviation	Register name	R/W	Initial value
0060 _H	TCCSH	16-bit free-running timer control status register (upper)	R/W	01000000 _B
0061 _H	TCCSL	16-bit free-running timer control status register (lower)	R/W	00000000 _B
0062 _H	ETCCSH	16-bit free-running timer extended control status register (upper)	R/W	00000000 _B
0063 _H	ETCCSL	16-bit free-running timer extended control status register (lower)	R/W	00000000 _B
0064 _H	OCCP0H	16-bit output compare channel 0 register (upper)	R	00000000 _B
0065 _H	OCCP0L	16-bit output compare channel 0 register (lower)	R	00000000 _B
0066 _H	OCCP1H	16-bit output compare channel 1 register (upper)	R	00000000 _B
0067 _H	OCCP1L	16-bit output compare channel 1 register (lower)	R	00000000 _B
0068 _H	OCSH	16-bit output compare control status register (upper)	R/W	00000000 _B
0069 _H	OCSL	16-bit output compare control status register (lower)	R/W	00000000 _B
006A _H	OCMCR	16-bit output compare mode control register	R/W	00000000 _B
006B _H	EOCS	16-bit output compare extended control status register	R/W	00000000 _B
006C _H	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 _B
006D _H	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 _B
006E _H	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000 _B
006F _H	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000 _B
0070 _H	—	(Disabled)	—	—
0071 _H	FSR2	Flash memory status register 2	R/W	00000000 _B
0072 _H	FSR	Flash memory status register	R/W	000X0000 _B
0073 _H	SWRE0	Flash memory sector write control register 0	R/W	00000000 _B
0074 _H	FSR3	Flash memory status register 3	R	0000XXXX _B
0075 _H	—	(Disabled)	—	—
0076 _H	WREN	Wild register address compare enable register	R/W	00000000 _B
0077 _H	WROR	Wild register data test setting register	R/W	00000000 _B
0078 _H	—	(Disabled)	—	—
0079 _H	ILR0	Interrupt level setting register 0	R/W	11111111 _B
007A _H	ILR1	Interrupt level setting register 1	R/W	11111111 _B
007B _H	ILR2	Interrupt level setting register 2	R/W	11111111 _B
007C _H	ILR3	Interrupt level setting register 3	R/W	11111111 _B
007D _H	ILR4	Interrupt level setting register 4	R/W	11111111 _B
007E _H	ILR5	Interrupt level setting register 5	R/W	11111111 _B
007F _H to 0F7F _H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0F80 _H	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000 _B
0F81 _H	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000 _B
0F82 _H	WRDR0	Wild register data setting register ch. 0	R/W	00000000 _B
0F83 _H	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000 _B
0F84 _H	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000 _B
0F85 _H	WRDR1	Wild register data setting register ch. 1	R/W	00000000 _B
0F86 _H	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000 _B
0F87 _H	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000 _B
0F88 _H	WRDR2	Wild register data setting register ch. 2	R/W	00000000 _B
0F89 _H	WRARH3	Wild register address setting register (upper) ch. 3	R/W	00000000 _B
0F8A _H	WRARL3	Wild register address setting register (lower) ch. 3	R/W	00000000 _B
0F8B _H	WRDR3	Wild register data setting register ch. 3	R/W	00000000 _B
0F8C _H to 0F91 _H	—	(Disabled)	—	—
0F92 _H	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000 _B
0F93 _H	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000 _B
0F94 _H	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000 _B
0F95 _H	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000 _B
0F96 _H	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000 _B
0F97 _H to 0FA9 _H	—	(Disabled)	—	—
0FAA _H	PDCRH0	16-bit PPG down counter register (upper) ch. 0	R/W	00000000 _B
0FAB _H	PDCRL0	16-bit PPG down counter register (lower) ch. 0	R/W	00000000 _B
0FAC _H	PCSRH0	16-bit PPG cycle setting buffer register (upper) ch. 0	R/W	11111111 _B
0FAD _H	PCSRL0	16-bit PPG cycle setting buffer register (lower) ch. 0	R/W	11111111 _B
0FAE _H	PDUTH0	16-bit PPG duty setting buffer register (upper) ch. 0	R/W	11111111 _B
0FAF _H	PDUTL0	16-bit PPG duty setting buffer register (lower) ch. 0	R/W	11111111 _B
0FB0 _H to 0FBD _H	—	(Disabled)	—	—
0FBE _H	PSSR0	UART/SIO prescaler select register ch. 0	R/W	00000000 _B
0FBF _H	BRSR0	UART/SIO baud rate setting register ch. 0	R/W	00000000 _B
0FC0 _H , 0FC1 _H	—	(Disabled)	—	—
0FC2 _H	AIDRH	A/D input disable register (upper)	R/W	00000000 _B
0FC3 _H	AIDRL	A/D input disable register (lower)	R/W	00000000 _B
0FC4 _H to 0FE3 _H	—	(Disabled)	—	—

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Address	Register abbreviation	Register name	R/W	Initial value
0FE4 _H	CRT _H	Main CR clock trimming register (upper)	R/W	0XXXXXXXX _B
0FE5 _H	CRT _L	Main CR clock trimming register (lower)	R/W	00XXXXXXXX _B
0FE6 _H , 0FE7 _H	—	(Disabled)	—	—
0FE8 _H	SYSC1	System configuration register 1	R/W	11000011 _B
0FE9 _H	CMCR	Clock monitoring control register	R/W	00000000 _B
0FEA _H	CMDR	Clock monitoring data register	R	00000000 _B
0FEB _H	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXX _B
0FEC _H	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXXX _B
0FED _H	—	(Disabled)	—	—
0FEE _H	ILSR	Input level select register	R/W	00000000 _B
0FEF _H	WICR	Interrupt pin control register	R/W	01000000 _B
0FF0 _H to 0FFF _H	—	(Disabled)	—	—

• R/W access symbols

R/W : Readable / Writable

R : Read only

W : Write only

• Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 0	IRQ00	FFFA _H	FFFB _H	L00 [1:0]	High ↑ ↓ Low
External interrupt ch. 4					
External interrupt ch. 1	IRQ01	FFF8 _H	FFF9 _H	L01 [1:0]	
External interrupt ch. 5					
External interrupt ch. 2	IRQ02	FFF6 _H	FFF7 _H	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4 _H	FFF5 _H	L03 [1:0]	
External interrupt ch. 7					
UART/SIO	IRQ04	FFF2 _H	FFF3 _H	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0 _H	FFF1 _H	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE _H	FFEF _H	L06 [1:0]	
Output compare ch. 0 match	IRQ07	FFEC _H	FFED _H	L07 [1:0]	
Output compare ch. 1 match	IRQ08	FFEA _H	FFEB _H	L08 [1:0]	
—	IRQ09	FFE8 _H	FFE9 _H	L09 [1:0]	
Voltage comparator ch. 0	IRQ10	FFE6 _H	FFE7 _H	L10 [1:0]	
Voltage comparator ch. 1	IRQ11	FFE4 _H	FFE5 _H	L11 [1:0]	
Voltage comparator ch. 2	IRQ12	FFE2 _H	FFE3 _H	L12 [1:0]	
Voltage comparator ch. 3	IRQ13	FFE0 _H	FFE1 _H	L13 [1:0]	
16-bit free-running timer (compare match/zero-detect/overflow)	IRQ14	FFDE _H	FFDF _H	L14 [1:0]	
16-bit PPG	IRQ15	FFDC _H	FFDD _H	L15 [1:0]	
I ² C	IRQ16	FFDA _H	FFDB _H	L16 [1:0]	
—	IRQ17	FFD8 _H	FFD9 _H	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6 _H	FFD7 _H	L18 [1:0]	
Time-base timer	IRQ19	FFD4 _H	FFD5 _H	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 _H	FFD3 _H	L20 [1:0]	
—	IRQ21	FFD0 _H	FFD1 _H	L21 [1:0]	
—	IRQ22	FFCE _H	FFCF _H	L22 [1:0]	
Flash memory	IRQ23	FFCC _H	FFCD _H	L23 [1:0]	

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6$	V	
Input voltage*1	V_i	$V_{SS} - 0.3$	$V_{SS} + 6$	V	*2
Output voltage*1	V_o	$V_{SS} - 0.3$	$V_{SS} + 6$	V	*2
Maximum clamp current	I_{CLAMP}	-2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	ΣI_{CLAMP}	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{OL1}	—	15	mA	Other than P05 and P06
	I_{OL2}		15		P05 and P06
“L” level average current	I_{OLAV1}	—	4	mA	Other than P05 and P06 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05 and P06 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH1}	—	-15	mA	Other than P05 and P06
	I_{OH2}		-15		P05 and P06
“H” level average current	I_{OHAV1}	—	-4	mA	Other than P05 and P06 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		-8		P05 and P06 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	-100	mA	
“H” level total average output current	ΣI_{OHAV}	—	-50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	-40	+85	°C	
Storage temperature	T_{stg}	-55	+150	°C	

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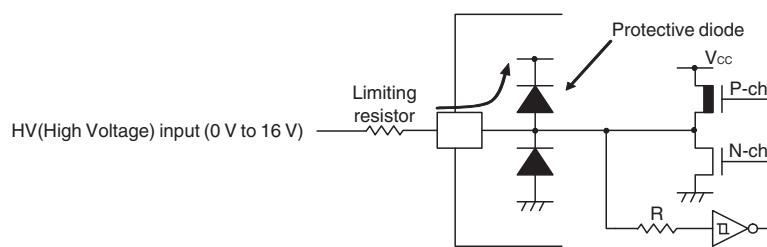
*1: The parameter is based on $V_{SS} = 0.0\text{ V}$.

*2: V_I and V_O must not exceed $V_{CC} + 0.3\text{ V}$. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P00 to P07, P60 to P67, P70 to P76, PF0 and PF1

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit

- Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

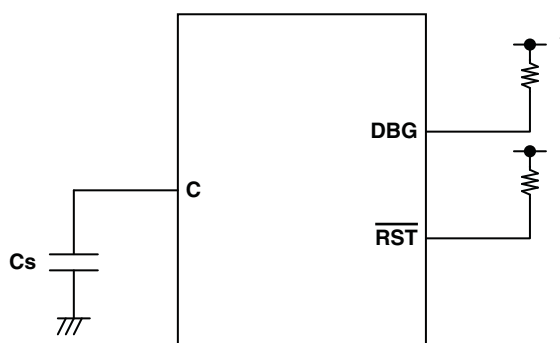
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V _{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C _S	0.022	1	μF	*3	
Operating temperature	T _A	−40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: This value becomes 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

• DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/EC0/UI/SCL/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ ³	Max		
"H" level input voltage	V _{IHI}	P03, P04, P12, P65	*1	0.7 V _{CC}	—	V _{CC} + 0.3	V	When CMOS input level (hysteresis input) is selected
	V _{IHS}	P00 to P07, P12, P60 to P67, P70 to P76, PF0, PF1, PG1, PG2	*1	0.8 V _{CC}	—	V _{CC} + 0.3	V	Hysteresis input
	V _{IHM}	PF2	—	0.7 V _{CC}	—	V _{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V _{IL}	P03, P04, P12, P65	*1	V _{SS} - 0.3	—	0.3 V _{CC}	V	When CMOS input level (hysteresis input) is selected
	V _{ILS}	P00 to P07, P12, P60 to P67, P70 to P76, PF0, PF1, PG1, PG2	*1	V _{SS} - 0.3	—	0.2 V _{CC}	V	Hysteresis input
	V _{ILM}	PF2	—	V _{SS} - 0.3	—	0.3 V _{CC}	V	Hysteresis input
Open-drain output application voltage	V _D	P03, P04, P12, P65, PF2	—	V _{SS} - 0.3	—	V _{SS} + 5.5	V	P03, P04 and P65 are open-drain output pins when assigned as the SDA/SCL pin of I ² C.
"H" level output voltage	V _{OH1}	Output pins other than P05, P06, P12 and PF2	I _{OH} = -4 mA	V _{CC} - 0.5	—	—	V	
	V _{OH2}	P05, P06	I _{OH} = -8 mA	V _{CC} - 0.5	—	—	V	
"L" level output voltage	V _{OL1}	Output pins other than P05 and P06	I _{OL} = 4 mA	—	—	0.4	V	
	V _{OL2}	P05, P06	I _{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I _{LI}	All input pins	0.0 V < V _I < V _{CC}	-5	—	+5	μA	When pull-up resistance is disabled
Pull-up resistance	R _{PULL}	P00 to P07, PG1, PG2	V _I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled
Input capacitance	C _{IN}	Other than V _{CC} and V _{SS}	f = 1 MHz	—	5	15	pF	

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(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ ^{*3}	Max		
Power supply current ^{*2}	I _{CC}	V _{CC} (External clock operation)	V _{CC} = 5.5 V F _{CH} = 32 MHz F _{MP} = 16 MHz Main clock mode (divided by 2)	—	11.9	13.7	mA	Except during Flash memory writing and erasing
				—	17.9	21.8	mA	During Flash memory writing and erasing
				—	13.6	15.9	mA	At A/D conversion
				—	12.3	14.2	mA	When the voltage comparator is operating
				—	12.3	15.3	mA	When the OPAMP is operating
	I _{CCS}		V _{CC} = 5.5 V F _{CH} = 32 MHz F _{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.1	6.5	mA	
	I _{CCCL}		V _{CC} = 5.5 V F _{CL} = 32 kHz F _{MPL} = 16 kHz Subclock mode (divided by 2) T _A = +25°C	—	59.2	83	μA	
	I _{CCLS}		V _{CC} = 5.5 V F _{CL} = 32 kHz F _{MPL} = 16 kHz Subsleep mode (divided by 2) T _A = +25°C	—	7.8	11.3	μA	
	I _{CCCT}		V _{CC} = 5.5 V F _{CL} = 32 kHz Watch mode Main stop mode T _A = +25°C	—	4.2	6.5	μA	
	I _{CCMCR}		V _{CC} = 5.5 V F _{CRH} = 12.5 MHz F _{MP} = 12.5 MHz Main CR clock mode	—	9.5	11.5	mA	
	I _{CCSCR}	V _{CC}	V _{CC} = 5.5 V Sub-CR clock mode (divided by 2) T _A = +25°C	—	107.4	146.3	μA	

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(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ ^{*3}	Max		
Power supply current ^{*2}	I _{CCTS}	V _{CC} (External clock operation)	V _{CC} = 5.5 V F _{CH} = 32 MHz Time-base timer mode T _A = +25°C	—	0.9	1.2	mA	
	I _{CCH}		V _{CC} = 5.5 V Substop mode T _A = +25°C	—	3.0	4.8	μA	
	I _{LVD}	V _{CC}	Current consumption for low-voltage detection circuit only	—	26.8	39.7	μA	
	I _{CRH}		Current consumption for the main CR oscillator	—	0.2	0.4	mA	
	I _{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	8.0	18	μA	

*1: The input levels of P04 can be switched between "CMOS input level" and "hysteresis input level". The input level selection register (ILSR) is used to switch between the two input levels.

*2: • The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.

• See "4. AC Characteristics: (1) Clock Timing" for F_{CH} and F_{CL}.

• See "4. AC Characteristics: (2) Source Clock/Machine Clock" for F_{MP} and F_{MPL}.

*3: V_{CC} = 5.0 V, T_A = 25°C

4. AC Characteristics

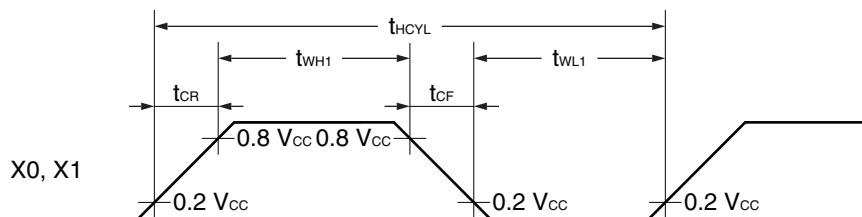
(1) Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F _{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1: open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
	F _{CRH}	—	—	12.25	12.5	12.75	MHz	Operating conditions: • The main CR clock is used. • T _A = -10°C to +85°C
				9.8	10	10.2	MHz	
				7.84	8	8.16	MHz	
				0.98	1	1.02	MHz	
				12.1875	12.5	12.8125	MHz	Operating conditions: • The main CR clock is used. • T _A = -40°C to -10°C
				9.75	10	10.25	MHz	
				7.8	8	8.2	MHz	
				0.975	1	1.025	MHz	
	F _{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F _{CRL}	—	—	50	100	200	kHz	When the sub-CR clock is used
Clock cycle time	t _{H CYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1: open	83.4	—	1000	ns	When the external clock is used
		X0, X1	*	30.8	—	1000	ns	
	t _{L CYL}	X0A, X1A	—	—	30.5	—	μs	When the subclock is used
Input clock pulse width	t _{WH1}	X0	X1: open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
	t _{WL1}	X0, X1	*	12.4	—	—	ns	
	t _{WH2} t _{WL2}	X0A	—	—	15.2	—	μs	
Input clock rise time and fall time	t _{CR}	X0	X1: open	—	—	5	ns	When the external clock is used
	t _{CF}	X0, X1	*	—	—	5	ns	
CR oscillation start time	t _{CRHWK}	—	—	—	—	80	μs	When the main CR clock is used
	t _{CRLWK}	—	—	—	—	10	μs	When the sub-CR clock is used

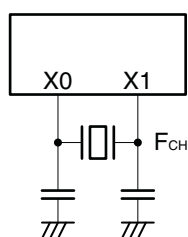
*: The external clock signal is input to X0 and the inverted external clock signal to X1.

- Input waveform generated when an external clock (main clock) is used

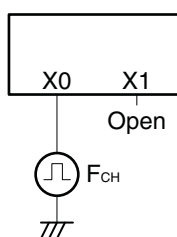


- Figure of main clock input port external connection

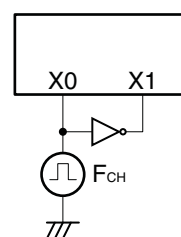
When a crystal oscillator or a ceramic oscillator is used



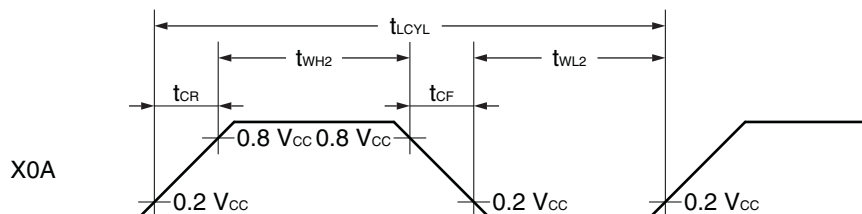
When the external clock is used (X1 is open)



When the external clock is used

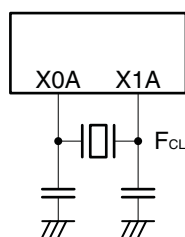


- Input waveform generated when an external clock (subclock) is used

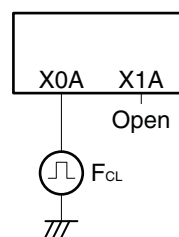


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When the external clock is used



(2) Source Clock/Machine Clock

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t _{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F _{CH} = 32.5 MHz, divided by 2 Max: F _{CH} = 1 MHz, divided by 2
			80	—	1000	ns	When the main CR clock is used Min: F _{CRH} = 12.5 MHz Max: F _{CRH} = 1 MHz
			—	61	—	μs	When the sub-oscillation clock is used F _{CL} = 32.768 kHz, divided by 2
			—	20	—	μs	When the sub-CR clock is used F _{CRL} = 100 kHz, divided by 2
Source clock frequency	F _{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	12.5	MHz	When the main CR clock is used
	F _{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F _{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t _{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F _{SP} = 16.25 MHz, no division Max: F _{SP} = 0.5 MHz, divided by 16
			80	—	16000	ns	When the main CR clock is used Min: F _{SP} = 12.5 MHz Max: F _{SP} = 1 MHz, divided by 16
			61	—	976.5	μs	When the sub-oscillation clock is used Min: F _{SPL} = 16.384 kHz, no division Max: F _{SPL} = 16.384 kHz, divided by 16
			20	—	320	μs	When the sub-CR clock is used Min: F _{SPL} = 50 kHz, no division Max: F _{SPL} = 50 kHz, divided by 16
Machine clock frequency	F _{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	12.5	MHz	When the main CR clock is used
	F _{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F _{CRL} = 100 kHz

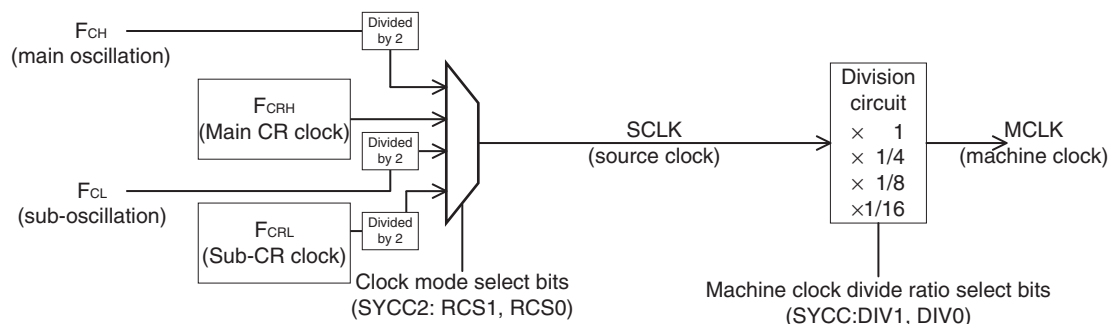
*1: This is the clock before it is divided according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). This source clock is divided to become a machine clock according to the divide ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

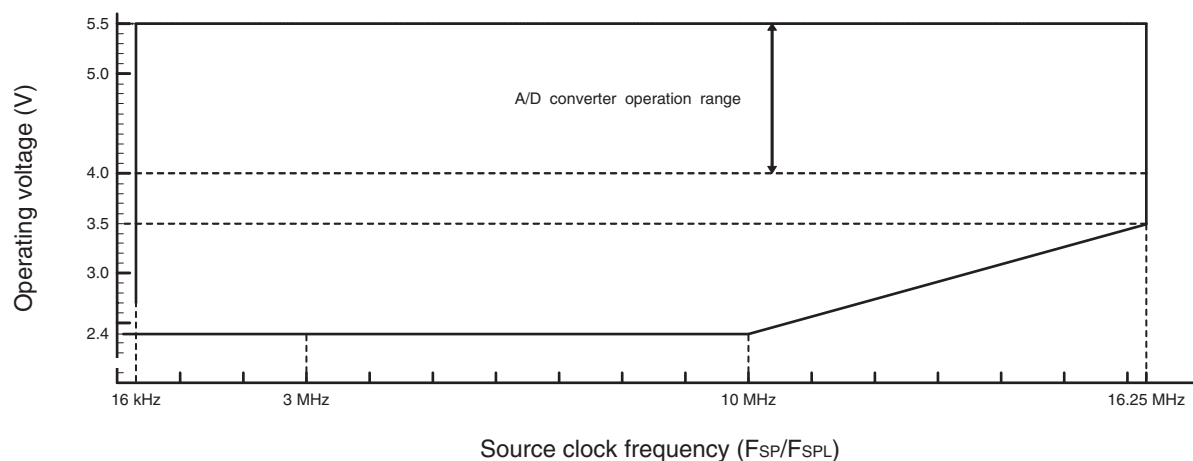
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

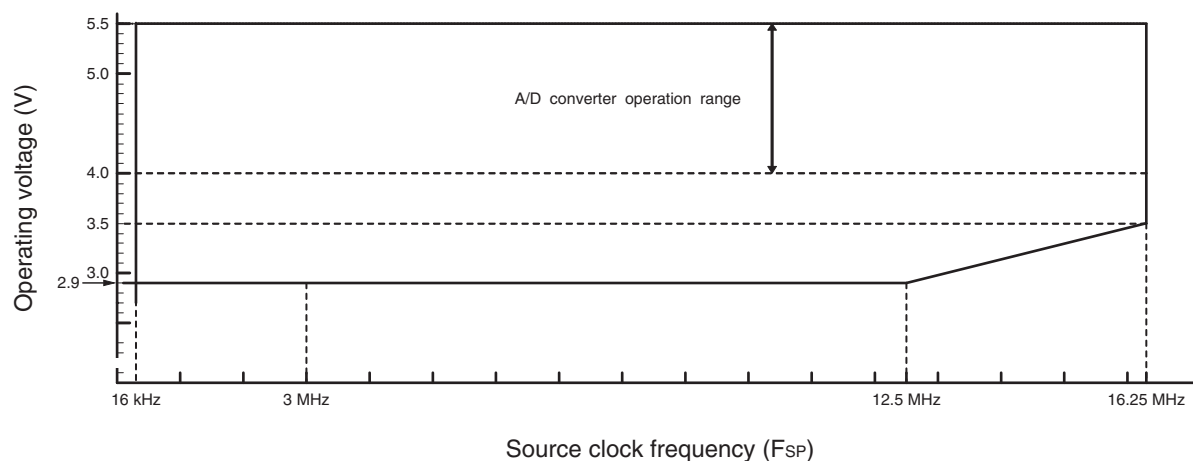
- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (When $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)
MB95430H (without the on-chip debug function)



- Operating voltage - Operating frequency (When $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)
MB95430H (with the on-chip debug function)



(3) External Reset

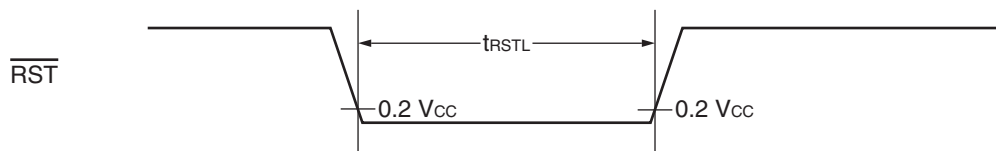
($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{\text{RST}}$ "L" level pulse width	t_{RSTL}	$2 t_{\text{MCLK}}^{*1}$	—	ns	In normal operation
		Oscillation time of the oscillator ^{*2} + 100	—	μs	In stop mode, subclock mode, subsleep mode, watch mode, and power-on
		100	—	μs	In time-base timer mode

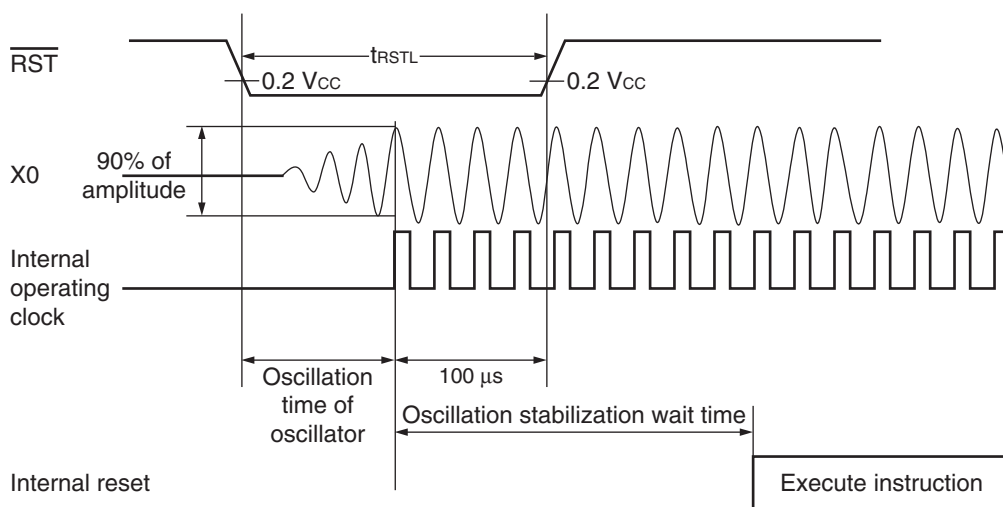
*1: See "(2) Source Clock/Machine Clock" for t_{MCLK} .

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of μs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several μs and several ms.

- In normal operation



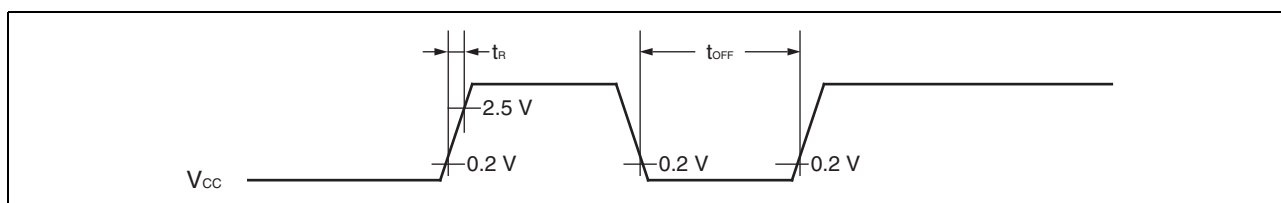
- In stop mode, subclock mode, subsleep mode, watch mode and power-on



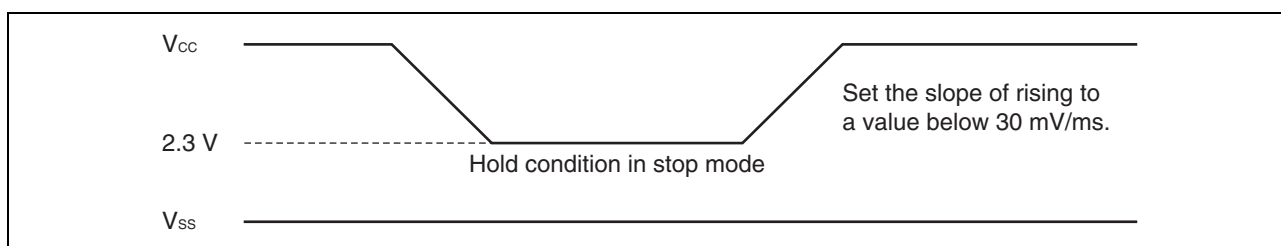
(4) Power-on Reset

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t _R	—	—	50	ms	
Power supply cutoff time	t _{OFF}	—	1	—	ms	Wait time until power-on



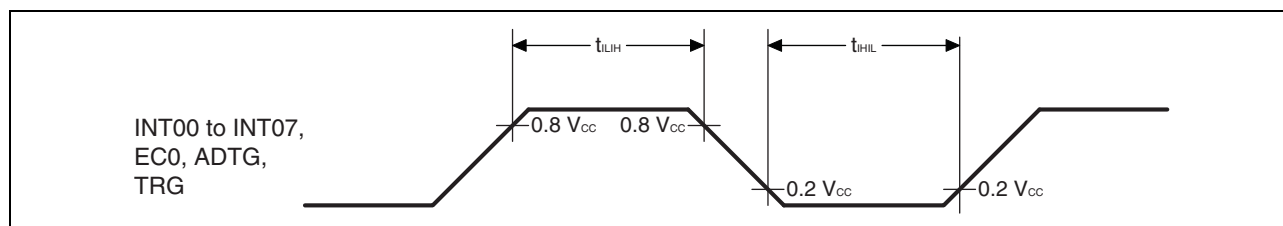
Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



(5) Peripheral Input Timing

(V_{CC} = 5.0 V $\pm$ 10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input "H" pulse width	t _{LIH}	INT00 to INT07, EC0, ADTG,	2 t _{MCLK} *	—	ns
Peripheral input "L" pulse width	t _{HIL}	TRG	2 t _{MCLK} *	—	ns

*: See "(2) Source Clock/Machine Clock" for t_{MCLK}.

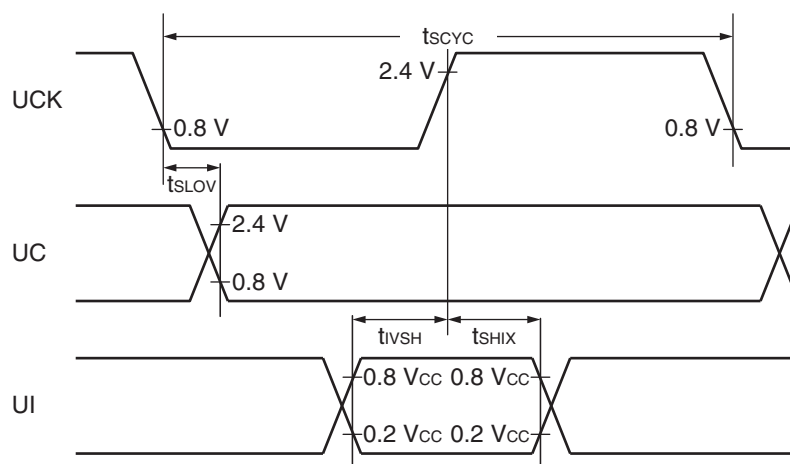
(6) UART/SIO, Serial I/O Timing

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

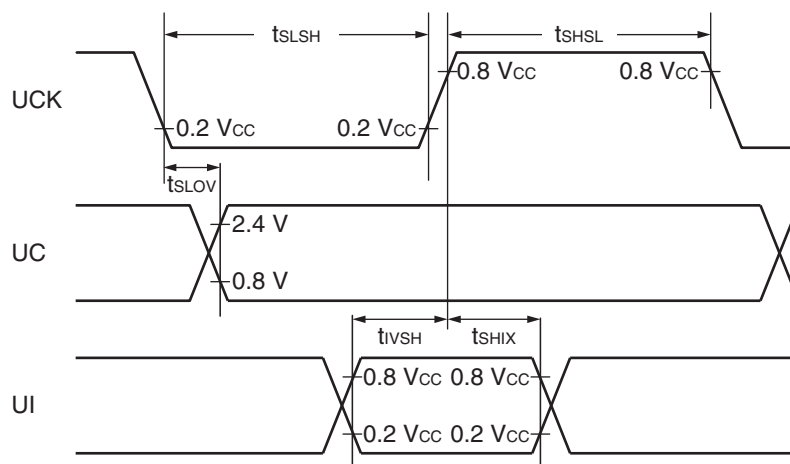
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	UCK	Internal clock operation	4 t _{MCLK} *	—	ns
UCK ↓ → UO time	t _{SLOV}	UCK, UO		-190	+190	ns
Valid UI → UCK ↑	t _{IVSH}	UCK, UI		2 t _{MCLK} *	—	ns
UCK ↑ → valid UI hold time	t _{SHIX}	UCK, UI		2 t _{MCLK} *	—	ns
Serial clock "H" pulse width	t _{SHSL}	UCK	External clock operation	4 t _{MCLK} *	—	ns
Serial clock "L" pulse width	t _{SLSH}	UCK		4 t _{MCLK} *	—	ns
UCK ↓ → UO time	t _{SLOV}	UCK, UO		—	190	ns
Valid UI → UCK ↑	t _{IVSH}	UCK, UI		2 t _{MCLK} *	—	ns
UCK ↑ → valid UI hold time	t _{SHIX}	UCK, UI		2 t _{MCLK} *	—	ns

*: See "(2) Source Clock/Machine Clock" for t_{MCLK}.

• Internal shift clock mode



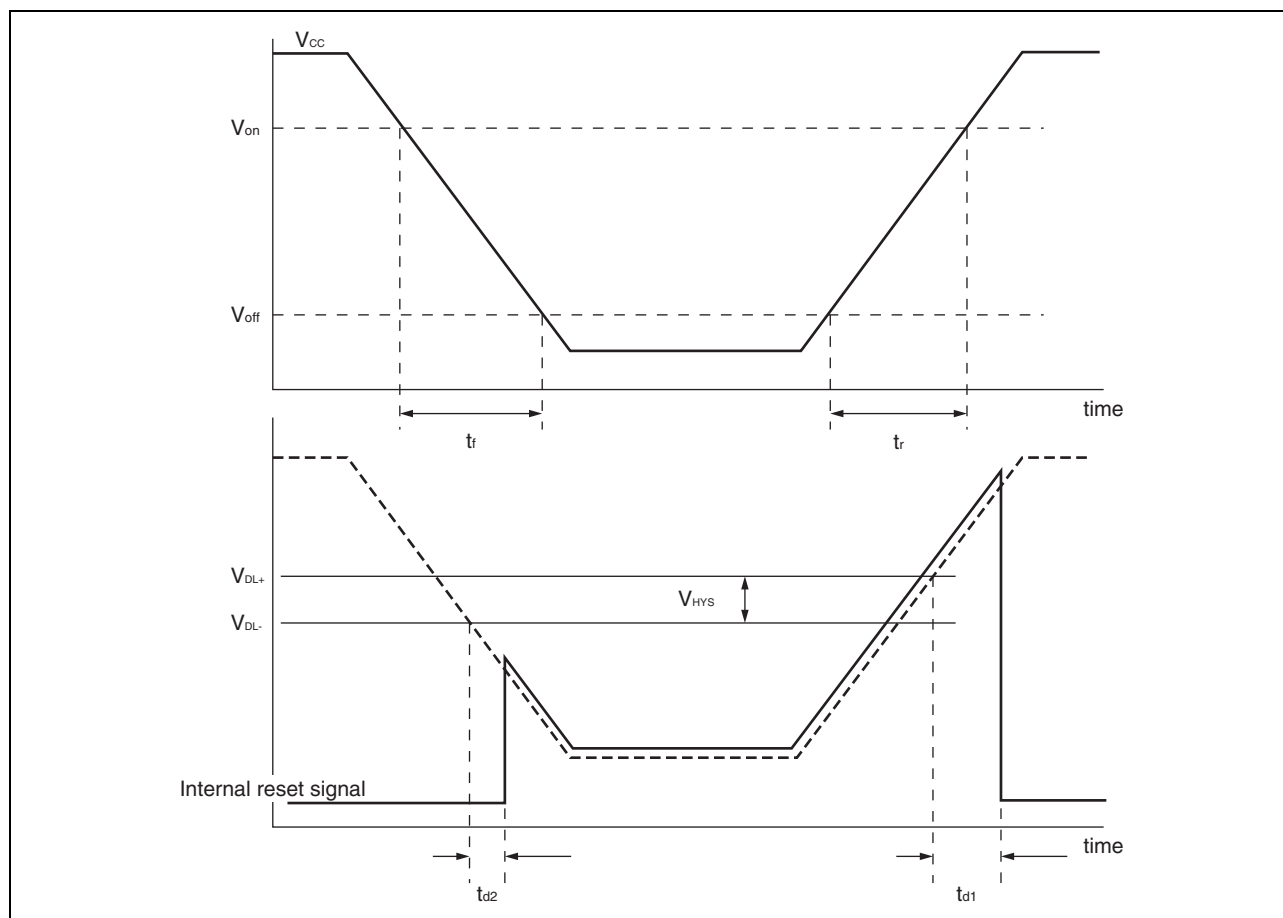
• External shift clock mode



(7) Low-voltage Detection

($V_{SS} = 0.0\text{ V}$, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	3000	—	—	μs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	μs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	μs	
Reset detection delay time	t_{d2}	—	—	20	μs	



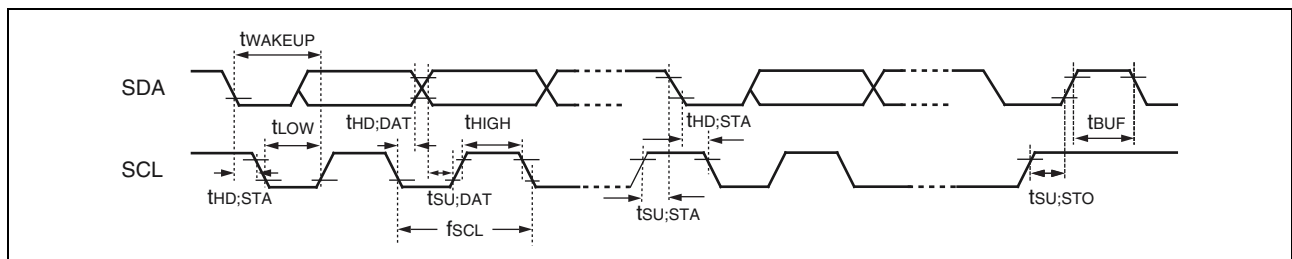
(8) I²C Timing(V_{CC} = 5.0 V ±10%, A V_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	SCL	R = 1.7 kΩ, C = 50 pF ^{*1}	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	t _{HD;STA}	SCL, SDA		4.0	—	0.6	—	μs
SCL clock “L” width	t _{LOW}	SCL		4.7	—	1.3	—	μs
SCL clock “H” width	t _{HIGH}	SCL		4.0	—	0.6	—	μs
(Repeated) START condition setup time SCL ↑ → SDA ↓	t _{SU;STA}	SCL, SDA		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓↑	t _{HD;DAT}	SCL, SDA		0	3.45 ^{*2}	0	0.9 ^{*3}	μs
Data setup time SDA ↓↑ → SCL ↑	t _{SU;DAT}	SCL, SDA		0.25	—	0.1	—	μs
STOP condition setup time SCL ↑ → SDA ↑	t _{SU;STO}	SCL, SDA		4	—	0.6	—	μs
Bus free time between STOP condition and START condition	t _{BUF}	SCL, SDA		4.7	—	1.3	—	μs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum t_{HD;DAT} in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" (t_{LOW}) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of t_{SU;DAT} ≥ 250ns is fulfilled.



(Continued)

(V_{CC} = 5.0 V $\pm$ 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock "L" width	t _{LOW}	SCL	R = 1.7 k Ω , C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock "H" width	t _{HIGH}	SCL		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	t _{HD;STA}	SCL, SDA		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	t _{SU;STO}	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	t _{SU;STA}	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t _{BUF}	SCL, SDA		$(2 nm + 4)t_{MCLK} - 20$	—	ns	
Data hold time	t _{HD;DAT}	SCL, SDA		$3 t_{MCLK} - 20$	—	ns	Master mode
Data setup time	t _{SU;DAT}	SCL, SDA		$(-2 + nm/2)t_{MCLK} - 20$	$(-1 + nm/2)t_{MCLK} + 20$	ns	Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	t _{SU;INT}	SCL		$(nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL $\downarrow$. Maximum value is applied to the interrupt at the 8th SCL $\downarrow$.

(Continued)

(Continued)

(V_{CC} = 5.0 V $\pm$ 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock "L" width	t _{LOW}	SCL	R = 1.7 k Ω , C = 50 pF*1	4 t _{MCLK} - 20	—	ns	At reception
SCL clock "H" width	t _{HIGH}	SCL		4 t _{MCLK} - 20	—	ns	At reception
START condition detection	t _{HD;STA}	SCL, SDA		2 t _{MCLK} - 20	—	ns	Undetected when 1 t _{MCLK} is used at reception
STOP condition detection	t _{SU;STO}	SCL, SDA		2 t _{MCLK} - 20	—	ns	Undetected when 1 t _{MCLK} is used at reception
RESTART condition detection condition	t _{SU;STA}	SCL, SDA		2 t _{MCLK} - 20	—	ns	Undetected when 1 t _{MCLK} is used at reception
Bus free time	t _{BUF}	SCL, SDA		2 t _{MCLK} - 20	—	ns	At reception
Data hold time	t _{HD;DAT}	SCL, SDA		2 t _{MCLK} - 20	—	ns	At slave transmission mode
Data setup time	t _{SU;DAT}	SCL, SDA		t _{LOW} - 3 t _{MCLK} - 20	—	ns	At slave transmission mode
Data hold time	t _{HD;DAT}	SCL, SDA		0	—	ns	At reception
Data setup time	t _{SU;DAT}	SCL, SDA		t _{MCLK} - 20	—	ns	At reception
SDA $\downarrow$ $\rightarrow$ SCL $\uparrow$ (at wakeup function)	t _{WAKEUP}	SCL, SDA		Oscillation stabilization wait time +2 t _{MCLK} - 20	—	ns	

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: • See "(2) Source Clock/Machine Clock" for t_{MCLK}.

- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I²C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I²C clock control register (ICCR0).
- The actual timing of I²C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.

• Standard-mode:

m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.

The usable frequencies of the machine clock are determined by the settings of m and n as shown below.

(m, n) = (1, 8)	: 0.9 MHz < t _{MCLK} $\leq$ 1 MHz
(m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4)	: 0.9 MHz < t _{MCLK} $\leq$ 2 MHz
(m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8)	: 0.9 MHz < t _{MCLK} $\leq$ 4 MHz
(m, n) = (1, 98), (5, 22), (6, 22), (7, 22)	: 0.9 MHz < t _{MCLK} $\leq$ 10 MHz
(m, n) = (8, 22)	: 0.9 MHz < t _{MCLK} $\leq$ 16.25 MHz

• Fast-mode:

m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.

The usable frequencies of the machine clock are determined by the settings of m and n as shown below.

(m, n) = (1, 8)	: 3.3 MHz < t _{MCLK} $\leq$ 4 MHz
(m, n) = (1, 22), (5, 4)	: 3.3 MHz < t _{MCLK} $\leq$ 8 MHz
(m, n) = (1, 22), (6, 4), (7, 4), (8, 4)	: 3.3 MHz < t _{MCLK} $\leq$ 10 MHz
(m, n) = (5, 8)	: 3.3 MHz < t _{MCLK} $\leq$ 16.25 MHz

(9) Voltage Compare Timing

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Voltage range	CMPn_P, CMPn_N (n = 0,1,2,3)	0	—	V _{CC} - 1.3	V	
Offset voltage	CMPn_P, CMPn_N (n = 0,1,2,3)	-10	—	+10	mV	
Delay time	CMPn_O (n = 0,1,2,3)	—	650	1210	ns	5 mV overdrive
		—	140	420	ns	50 mV overdrive
Power down delay	CMPn_O (n = 0,1,2,3)	—	—	1210	ns	Power down recovery PD: 1 → 0
		0	—	—	ns	Power down effective PD: 0 → 1 Output: "H" level
Power up stabilization time	CMPn_O (n = 0,1,2,3)	—	—	1210	ns	Output stabilization time at power up

(9) Operational Amplifier Timing

• Open Loop Configuration

(V_{CC} = 4.0 V to 5.5 V, T_A = -40°C to +85°C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Input voltage range	OPAMP_P, OPAMP_N	0.1	—	1.5	V	
Output voltage range	OPAMP_O	0.1	—	V _{CC} - 0.1	V	
Output resistor load	OPAMP_O	220	—	—	kΩ	Minimum driving resistor value
Output capacitor load	OPAMP_O	—	—	20	pF	AD loading (maximum ESR = 10k)
Offset voltage	OPAMP_O	—	—	10	mV	
Open loop bandwidth	OPAMP_O	3	—	—	MHz	
Open loop gain	OPAMP_O	75	85	—	dB	AD loading
Common mode rejection ratio	OPAMP_O	60	—	—	dB	AD loading
Power supply rejection ratio	OPAMP_O	65	—	—	dB	
Power down recovery time	OPAMP_O	—	—	200	μs	
Slew rate	OPAMP_O	0.3	—	—	V/μs	
Large signal response	OPAMP_O	—	—	6	μs	
Small signal response	OPAMP_O	—	—	500	ns	
Output stabilization time	OPAMP_O	—	—	60	μs	After values of RES0-RES2 change

• Closed Loop Configuration

($V_{CC} = 4.0\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Input voltage range (10x, 20x, 60x)	OPAMP_P, OPAMP_N	0.09	—	—	V	
Input voltage range (30x, 40x, 50x)	OPAMP_P, OPAMP_N	0.10	—	—	V	
Maximum input voltage range (10x, 20x, 30x, 40x, 50x, 60x)	OPAMP_P, OPAMP_N	—	—	V_{CC}/Gain	V	
Output voltage range	OPAMP_O	0.1	—	$V_{CC} - 0.1$	V	
Output capacitor load	OPAMP_O	—	—	20	pF	AD loading (maximum ESR = 10k)
Closed loop bandwidth	OPAMP_O	1	—	—	MHz	AD loading
Closed loop gain	OPAMP_O	10	—	60	V/V	Selectable
Closed loop gain error* (10x, 20x, 30x, 40x, 50x)	OPAMP_O	—	—	$\pm 10\%$	—	
Closed loop gain error* (60x)	OPAMP_O	—	—	$\pm 15\%$	—	
Power down recovery time	OPAMP_O	—	—	200	μs	
Slew rate	OPAMP_O	0.3	—	—	V/ μs	
Large signal response	OPAMP_O	—	—	6	μs	
Small signal response	OPAMP_O	—	—	500	ns	
Output stabilization time	OPAMP_O	—	—	60	μs	After values of RES0- RES2 change

*: Gain error = $1 - (\text{actual gain} / \text{design gain})$

5. A/D Converter

(1) A/D Converter Electrical Characteristics

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

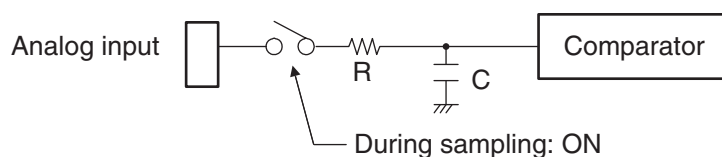
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		-3	—	+3	LSB	
Linearity error		-2.5	—	+2.5	LSB	
Differential linear error		-1.9	—	+1.9	LSB	
Zero transition voltage	V _{OT}	V _{SS} - 1.5 LSB	V _{SS} + 0.5 LSB	V _{SS} + 2.5 LSB	V	
Full-scale transition voltage	V _{FST}	V _{CC} - 4.5 LSB	V _{CC} - 2 LSB	V _{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	μs	4.5 V ≤ V _{CC} ≤ 5.5 V
		1.8	—	16500	μs	4.0 V ≤ V _{CC} < 4.5 V
Sampling time	—	0.6	—	∞	μs	4.5 V ≤ V _{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	μs	4.0 V ≤ V _{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I _{AIN}	-0.3	—	+0.3	μA	
Analog input voltage	V _{AIN}	V _{SS}	—	V _{CC}	V	

(2) Notes on Using the A/D Converter

• External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 μF to the analog input pin.

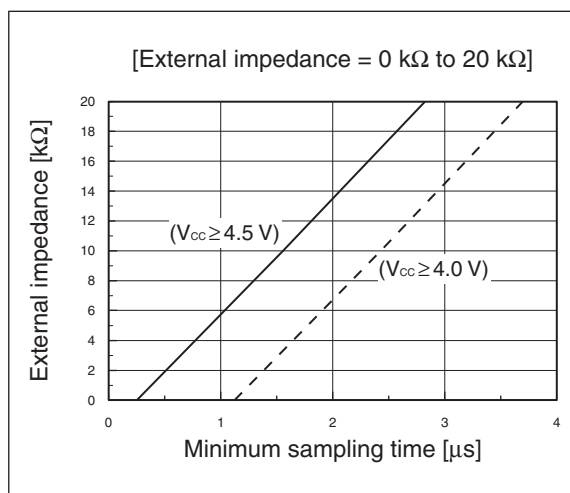
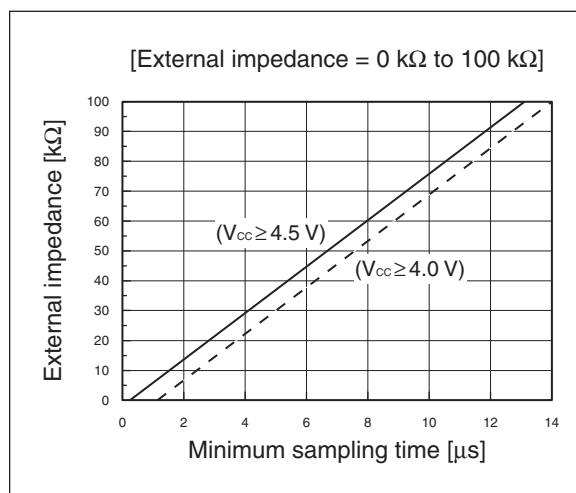
• Analog input equivalent circuit



V_{CC}	R	C
$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	1.95 k Ω (Max)	17 pF (Max)
$4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$	8.98 k Ω (Max)	17 pF (Max)

Note: The values are reference values.

• Relationship between external impedance and minimum sampling time



• A/D conversion error

As $V_{CC} - V_{SS}$ decreases, the A/D conversion error increases proportionately.

(3) Definitions of A/D Converter Terms

- Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.

- Linearity error (unit: LSB)

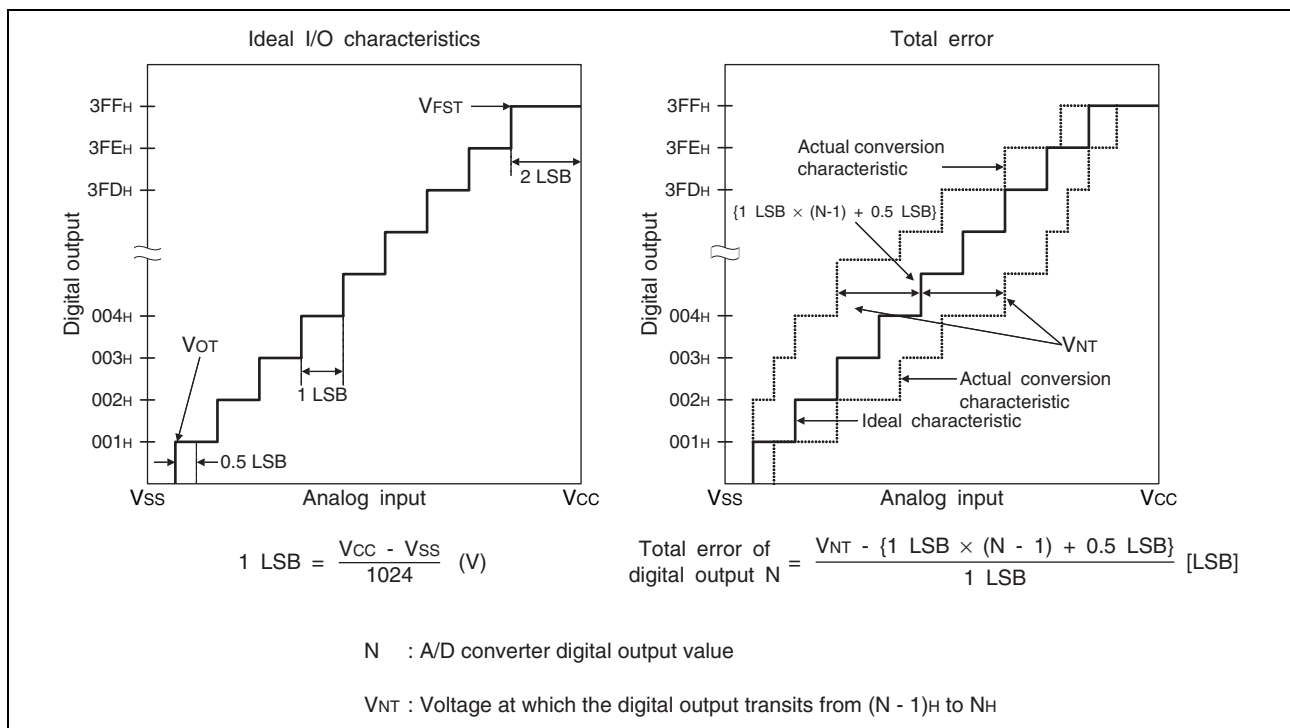
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00 0000 0000" $\leftrightarrow$ "00 0000 0001") of a device to the full-scale transition point ("11 1111 1111" $\leftrightarrow$ "11 1111 1110") of the same device.

- Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

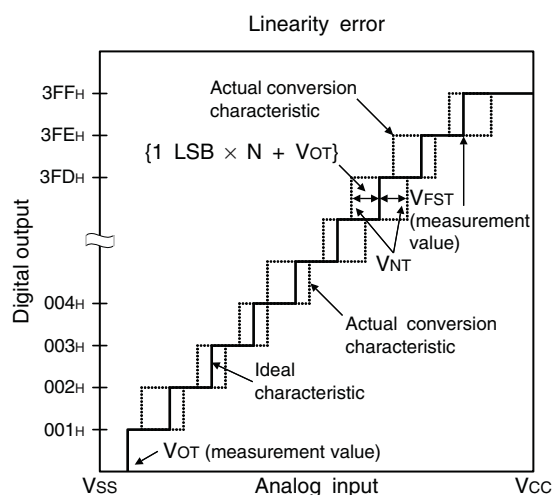
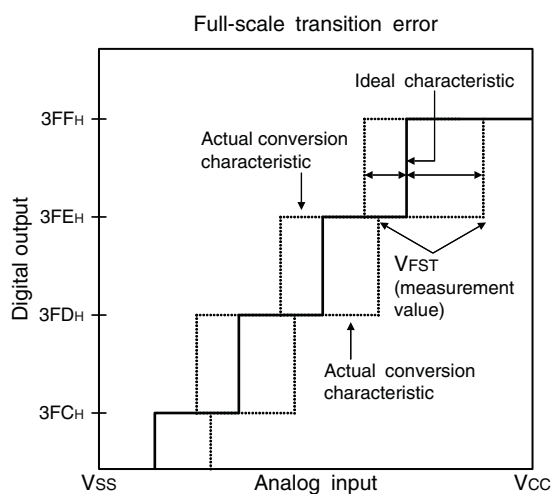
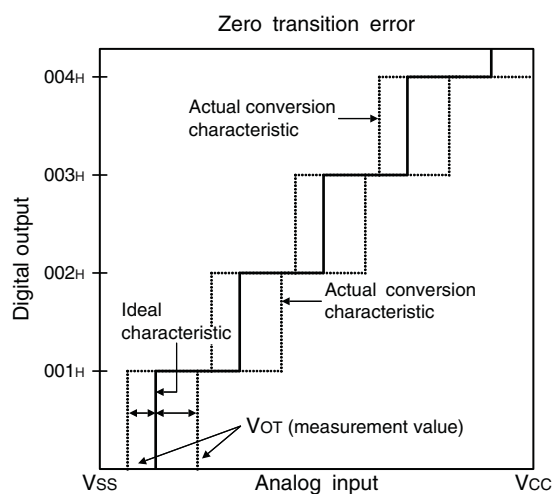
- Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.

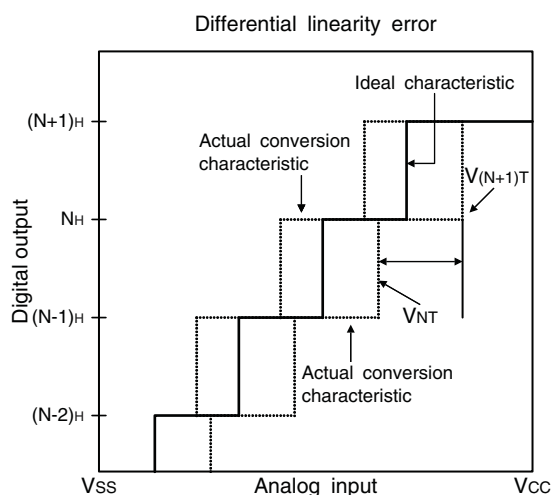


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$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$



$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

$V_{OT}(\text{ideal value}) = V_{SS} + 0.5 \text{ LSB [V]}$

$V_{FST}(\text{ideal value}) = V_{CC} - 2 \text{ LSB [V]}$

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2 ^{*1}	0.5 ^{*2}	s	The time of writing 00 _H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5 ^{*1}	7.5 ^{*2}	s	The time of writing 00 _H prior to erasure is excluded.
Byte writing time	—	21	6100 ^{*2}	μs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	3.0	—	5.5	V	
Flash memory data retention time	20 ^{*3}	—	—	year	Average T _A = +85°C

*1: T_A = +25°C, V_{CC} = 5.0 V, 100000 cycles

*2: T_A = +85°C, V_{CC} = 3.0 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

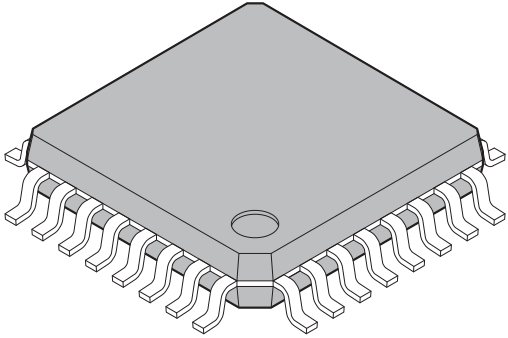
■ MASK OPTIONS

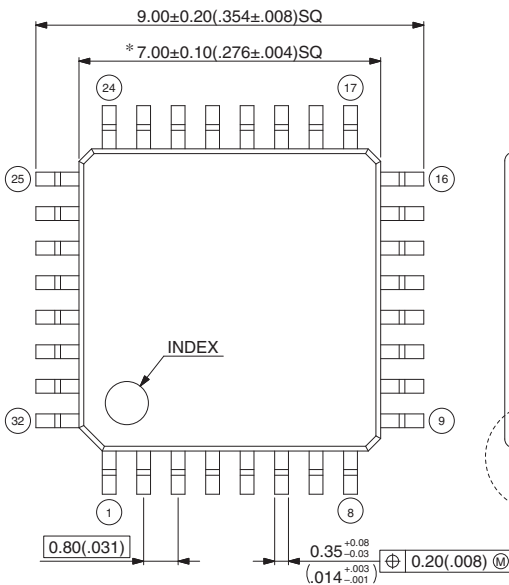
No.	Part Number	MB95F432H MB95F433H MB95F434H	MB95F432K MB95F433K MB95F434K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

■ ORDERING INFORMATION

Part Number	Package
MB95F432HPMC-G-SNE2 MB95F432KPMC-G-SNE2 MB95F433HPMC-G-SNE2 MB95F433KPMC-G-SNE2 MB95F434HPMC-G-SNE2 MB95F434KPMC-G-SNE2	32-pin plastic LQFP (FPT-32P-M30)
MB95F432HP-G-SH-SNE2 MB95F432KP-G-SH-SNE2 MB95F433HP-G-SH-SNE2 MB95F433KP-G-SH-SNE2 MB95F434HP-G-SH-SNE2 MB95F434KP-G-SH-SNE2	32-pin plastic SH-DIP (DIP-32P-M06)

■ PACKAGE DIMENSION

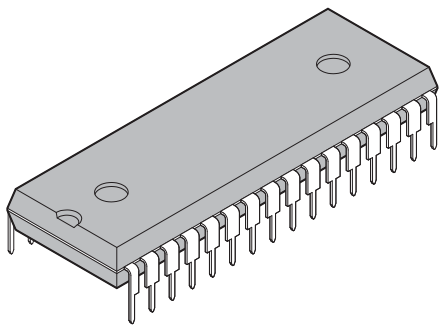
 32-pin plastic LQFP (FPT-32P-M30)	Lead pitch	0.80 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.60 mm MAX

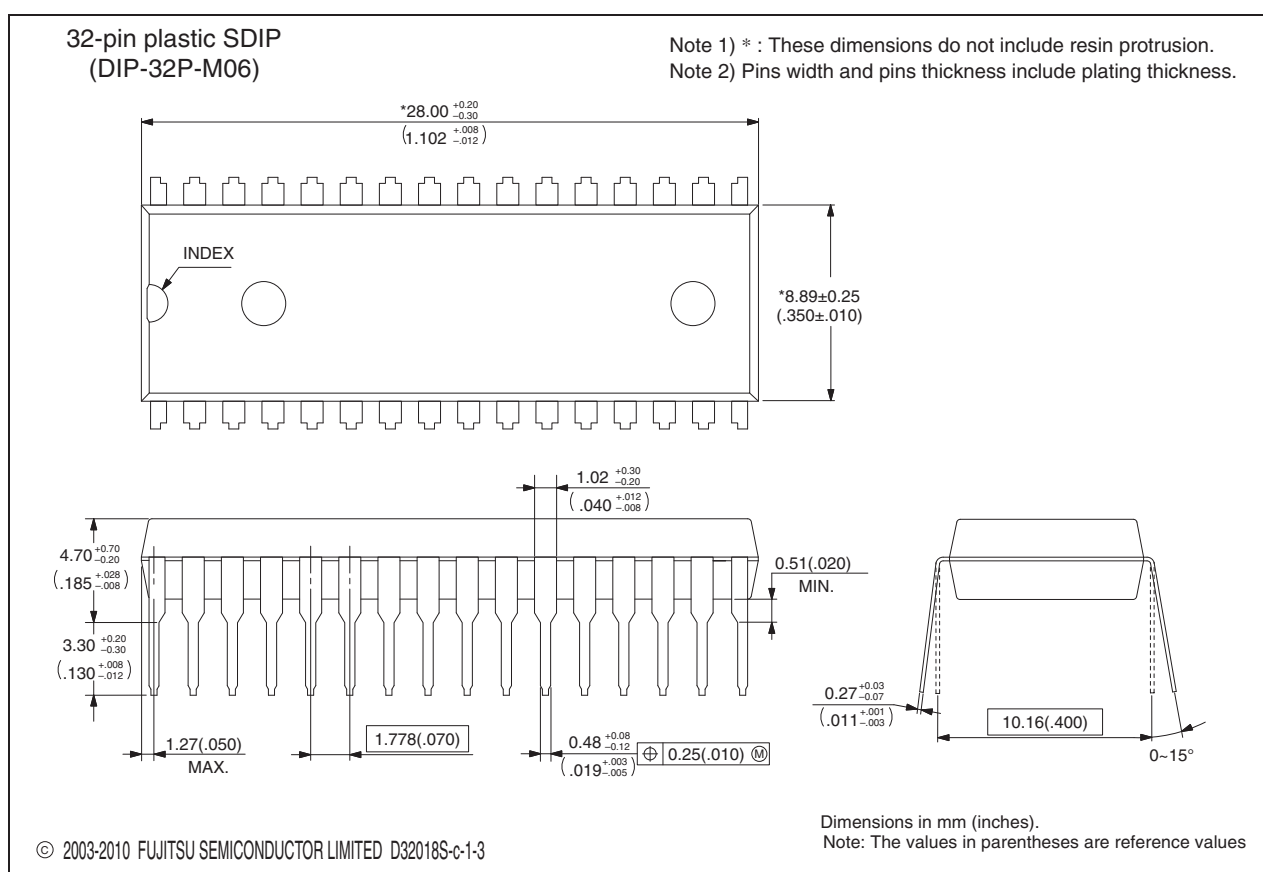
32-pin plastic LQFP (FPT-32P-M30)  9.00±0.20(354±.008)SQ * 7.00±0.10(276±.004)SQ INDEX 0.80(.031) 0.13^{+0.05}_{-0.03} (.005^{+0.002}_{-.001}) 0.10(.004) 0.35^{+0.08}_{-0.03} (.014^{+0.003}_{-.001}) 0.20(.008)Ⓜ	Note 1) * : These dimensions do not include resin protrusion. Note 2) Pins width and pins thickness include plating thickness. Note 3) Pins width do not include tie bar cutting remainder.

Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

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32-pin plastic SDIP  (DIP-32P-M06)	Lead pitch	1.778 mm
	Low space	10.16 mm
	Sealing method	Plastic mold



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MEMO

MEMO

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