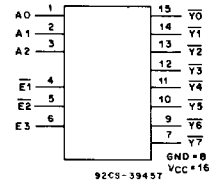
CD54AC138/3A
CD54ACT138/3A

3-to-8-Line Decoder/Demultiplexer Inverting

The RCA CD54AC138/3A and CD54ACT138/3A are 3-to-8-line decoders/demultiplexers that utilize the new RCA ADVANCED CMOS LOGIC technology.

The CD54AC138/3A and CD54ACT138/3A are supplied in 16-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Package Specifications
See Section 11, Fig. 11

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Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				+25		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (MSI) I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
A0 - A2	0.83
$\overline{E1}$, $\overline{E2}$	1
E3	0.42

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54AC/ACT138	7,9-15	1-6,8	16	7,9-15	8	1-6,16
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	25 kHz
CD54AC/ACT138	—	4,5,8	7,9-15	3,6,16	2	1

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54AC138/3A
CD54ACT138/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delay An to Output	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4.6 3.3	138 15.4 11•	ns
$\overline{E1}$, $\overline{E2}$ to Output	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.2 3	125 14 10•	ns
E3 to Output	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.6 3.3	138 15.4 11•	ns
Power Dissipation Capacitance	C_{PD}§	—	110 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delay An to Output	t_{PLH} t_{PHL}	5†	3.6	12•	ns
$\overline{E1}$, $\overline{E2}$ to Output	t_{PLH} t_{PHL}	5	3.2	10.5•	ns
E3 to Output	t_{PLH} t_{PHL}	5	3.3	11•	ns
Power Dissipation Capacitance	C_{PD}§	—	110 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§C_{PD} is used to determine the dynamic power consumption per package.
For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

CD54AC139/3A
CD54ACT139/3A

Dual 2-to-4-Line Decoder/Demultiplexer

The RCA CD54AC139/3A and CD54ACT139/3A are dual 2-to-4-line decoders/demultiplexers that utilize the new RCA ADVANCED CMOS LOGIC technology. These devices contain two independent binary to one-of-four decoders, each with a single active-LOW enable input ($\overline{1E}$ or $\overline{2E}$). Data on the select inputs (1A0 and 1A1 or 2A0 and 2A1) cause one of the four normally HIGH outputs to go LOW.

If the enable input is HIGH, all four outputs remain HIGH. For demultiplexer operation, the enable input is the data input. The enable input also functions as a chip select when these devices are cascaded.

The CD54AC139/3A and CD54ACT139/3A are supplied in 16-lead dual-in-line ceramic packages (F suffix).