For:joe

Printed on:Fri, Aug 27, 1999 08:30:42

Document:mc74f283rev5ltb

Last saved on:Wed, Aug 25, 1999 11:53:22

4-BIT BINARY FULL ADDER (With Fast Carry)

The MC54/74F283 high-speed 4-bit binary full adder with internal carry lookahead, accepts two 4-bit binary words (A_0 – A_3 , B_0 – B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0 – S_3) and the Carry output (C_4) from the most significant bit. The F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

FUNCTIONAL DESCRIPTION

The F283 adds two 4-bit binary words (A plus B) plus the incoming carry C_0 . The binary sum appears on the Sum (S_0 – S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

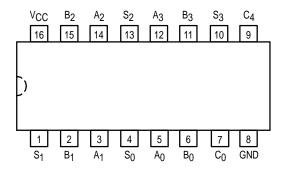
$$20 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3)$$

= $S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$
Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0 , A_0 , B_0 can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure A. Note that if C_0 is not used it must be tied LOW for active-HIGH logic or tied HIGH for active-LOW logic.

Due to pin limitations, the intermediate carries of the F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure B shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A₃, B₃) LOW makes S₃ dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure C shows a way of dividing the F283 into a 2-bit and a 1-bit adder. The third stage adder (A₂, B₂, S₂) is used merely as a means of getting a carry (C₁₀) signal into the fourth stage (via A2 and B2) and bringing out the carry from the second stage on S2. Note that as long as A2 and B2 are the same, whether HIGH or LOW, they do not influence S2. Similarly, when A2 and B2 are the same the carry into the third stage does not influence the carry out of the third stage. Figure D shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S₀, S₁ and S₂ present a binary number equal to the number of inputs I₁-I₅ that are true. Figure E shows one method of implementing a 5-input majority gate. When three or more of the inputs I₁-I₅ are true, the output M5 is true.

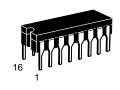
CONNECTION DIAGRAM



MC54/74F283

4-BIT BINARY FULL ADDER (With Fast Carry)

FASTTM **SCHOTTKY TTL**



J SUFFIX CERAMIC CASE 620-09



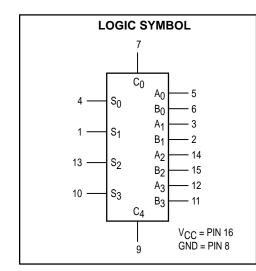
N SUFFIX PLASTIC CASE 648-08



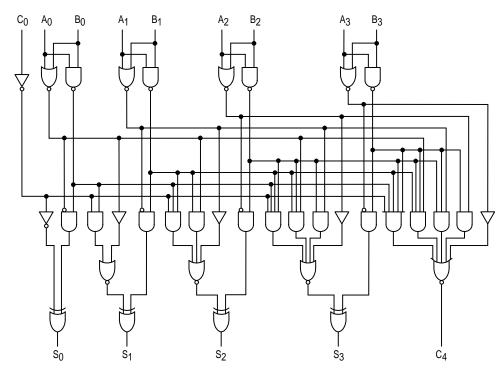
D SUFFIX SOIC CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ Ceramic MC74FXXXN Plastic MC74FXXXD SOIC



LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

	1 111111 1111111										
Symbol	Parameter		Min	Тур	Max	Unit					
VCC	Supply Voltage	54, 74	4.5	5.0	5.5	V					
T _A	Operating Ambient Temperature Benge	54	-55	25	125	°C					
	Operating Ambient Temperature Range	74	0	25	70	-0	Н				
ЮН	Output Current — High	54, 74	_	_	-1.0	mA	Ц				
lOL	Output Current — Low	54, 74	_	_	20	mA					

Figure A. Active-HIGH versus Active-LOW Interpretation

	C ₀	A ₀	A ₁	A ₂	А3	В0	В ₁	В2	В3	S ₀	S ₁	S ₂	S ₃	C ₄
Logic Levels	L	L	Н	L	Н	Н	L	L	Н	Η	Н	L	L	Н
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

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A₀ B₀ A₁ B₁ A₂ B₂ A₃ B₃ C₀ C₄ S₀ S₁ S₂ S₃ C₃

Figure B. 3-Bit Adder

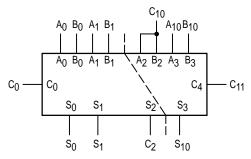


Figure C. 2-Bit and 1-Bit Adders

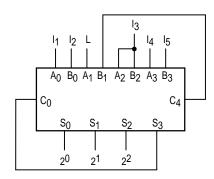


Figure D. 5-Input Encoder

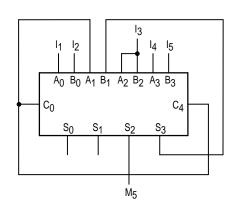


Figure E. 5-Input Majority Gate

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

			Limits						
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions			
VIH	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage			
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage			
VIK	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
Vон	Output HIGH Voltage	54, 74	2.5	3.4		V	$I_{OH} = -1.0 \text{ mA}$	V _{CC} = 4.5 V	
		74	2.7	3.4		V	$I_{OH} = -1.0 \text{ mA}$	V _{CC} = 4.75 V	
V _{OL}	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN	
	La mart LII QUI Quarrant				20	μΑ	V _{IN} = 2.7 V	Vaa MAY	
lΗ	Input HIGH Current			100	μΑ	V _{IN} = 7.0 V	VCC = MAX		
l _{IL}	Input LOW Current C ₀ Input			-0.6	mA	VIN = 0.5 V	VCC = MAX		
	A and B Inputs			-1.2	mA]			
los	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX	
Icc	Power Supply Current			36	55	mA	Inputs = 4.5 V	V _{CC} = MAX	

NOTES:

- 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

			54/74F		5	4F	7		
		$T_A = +25^{\circ}C$ $V_{CC} = +5.0 \text{ V}$ $C_L = 50 \text{ pF}$			V _{CC} = 5	to +125°C .0 V ±10% 50 pF	$T_A = 0 \text{ to } +70^{\circ}\text{C}$ $V_{CC} = 5.0 \text{ V } \pm 10\%$ $C_L = 50 \text{ pF}$		
Symbol	Parameter	Min	Тур	Max	Min	Max	Min	Max	Unit
tPLH	Propagation Delay	3.5	7.0	9.5	3.5	14	3.5	10.5	ns
tPHL	C ₀ to S _n	4.0	7.0	9.5	4.0	14	4.0	10.5	
tPLH	Propagation Delay	3.0	7.0	9.5	3.0	14	3.0	10.5	ns
tPHL	A _n or B _n to S _n	3.5	7.0	9.5	3.5	14	3.5	10.5	
^t PLH	Propagation Delay	3.5	5.7	7.5	3.5	10.5	3.5	8.5	ns
^t PHL	C ₀ to C ₄	3.0	5.4	7.0	3.0	10	3.0	8.0	
tPLH	Propagation	3.0	5.7	7.5	3.0	10.5	3.0	8.5	ns
tPHL	A _n or B _n to C ₄	3.0	5.3	7.0	3.0	10	3.0	8.0	

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