

**FEATURES:**

- 0.5 MICRON CMOS Technology
- Typical  $t_{SK(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4 $\mu$ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in TSSOP package

**DRIVE FEATURES:**

- Balanced Output Drivers:  $\pm 12mA$
- Low Switching Noise

**APPLICATIONS:**

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

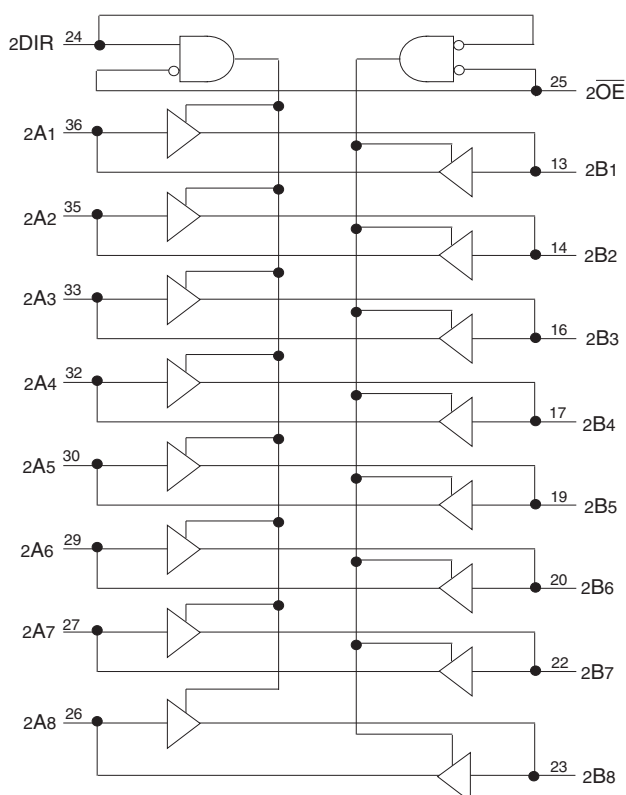
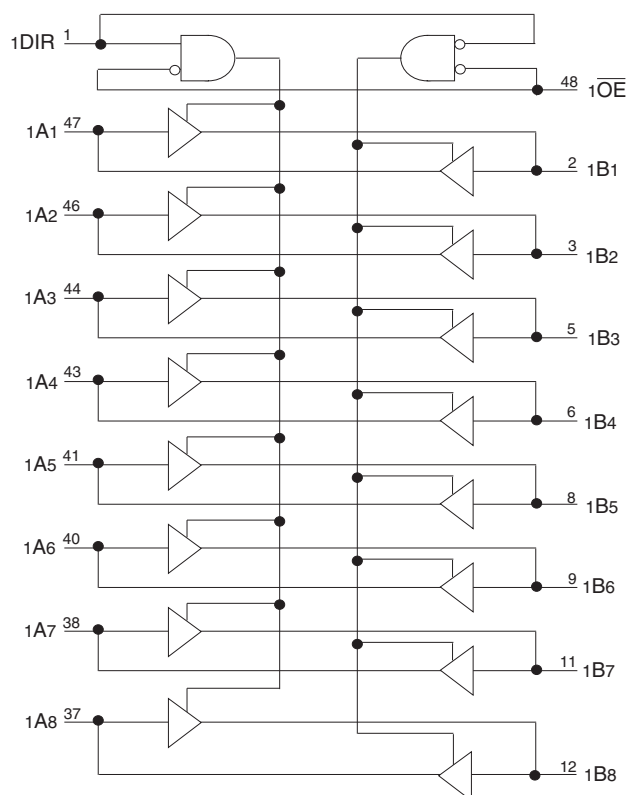
**DESCRIPTION:**

This 16-bit bus transceiver is built using advanced dual metal CMOS technology. The ALVCHR162245 device is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

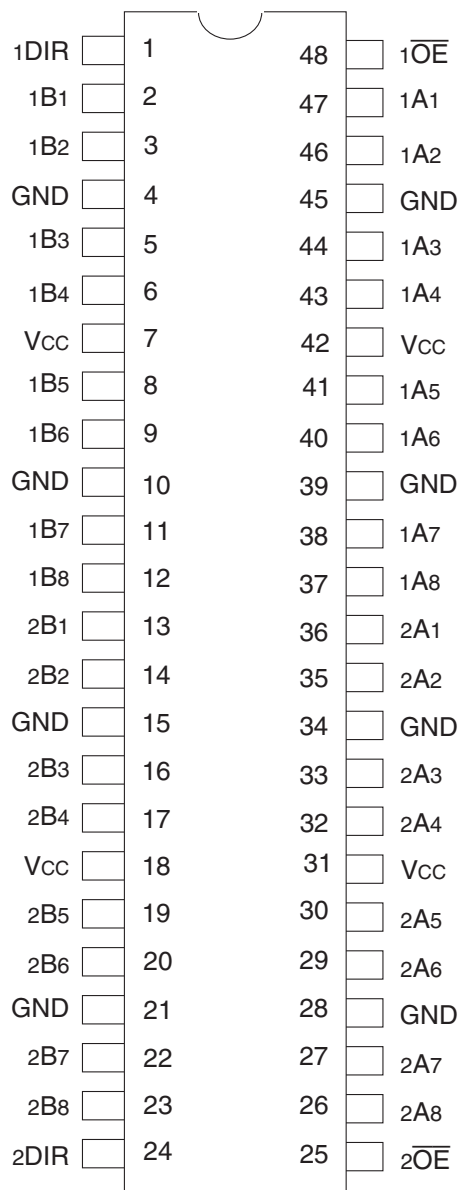
This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The ALVCHR162245 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive  $\pm 12mA$  at the designated threshold levels.

The ALVCHR162245 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

**FUNCTIONAL BLOCK DIAGRAM**


## PIN CONFIGURATION



TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IIK	Continuous Clamp Current, VI < 0 or VI > VCC	±50	mA
IOK	Continuous Clamp Current, VO < 0	-50	mA
ICC ISS	Continuous Current through each VCC or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

## CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COUT	Output Capacitance	VOUT = 0V	7	9	pF
CII/O	I/O Port Capacitance	VIN = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
xOE	Output Enable Inputs (Active LOW)
DIR	Direction Control Inputs
xAx <sup>(1)</sup>	Side A Inputs or 3-State Outputs
xBx <sup>(1)</sup>	Side B Inputs or 3-State Outputs

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE (EACH 8-BIT SECTION)<sup>(1)</sup>

Inputs		Outputs
xOE	xDIR	
L	L	Bus B data to A bus
L	H	Bus A data to B bus
H	X	High Z State

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		—	—	0.8	
$I_{IH}$	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OZL}$			$V_O = \text{GND}$	—	—	$\pm 10$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or $V_{CC}$		—	0.1	40	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ , other inputs at $V_{CC}$ or $\text{GND}$		—	—	750	$\mu\text{A}$

NOTE:

- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 3\text{V}$	$V_I = 2\text{V}$	-75	—	—	$\mu\text{A}$
			$V_I = 0.8\text{V}$	75	—	—	
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	-45	—	—	$\mu\text{A}$
			$V_I = 0.7\text{V}$	45	—	—	
$I_{BHHO}$ $I_{BHL0}$	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $3.6\text{V}$	—	—	$\pm 500$	$\mu\text{A}$

NOTES:

- Pins with Bus-Hold are identified in the pin description.
- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = -4mA	1.9	—	
			IOH = -6mA	1.7	—	
		VCC = 2.7V	IOH = -4mA	2.2	—	
			IOH = -8mA	2	—	
		VCC = 3V	IOH = -6mA	2.4	—	
			IOH = -12mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3V	IOL = 6mA	—	0.55	
			IOL = 12mA	—	0.8	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

## OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	24	32	pF
CPD	Power Dissipation Capacitance Outputs disabled		4	5	

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH	Propagation Delay	1	4.9	—	4.7	1	4.2	ns
tPHL	xAx to xBx or xBx to xAx							
tPZH	Output Enable Time	1	6.8	—	6.7	1	5.6	ns
tPZL	xOE to xAx or xBx							
tPHZ	Output Disable Time	1	6.3	—	5.7	1	5.5	ns
tPLZ	xOE to xAx or xBx							
tsk(o)	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

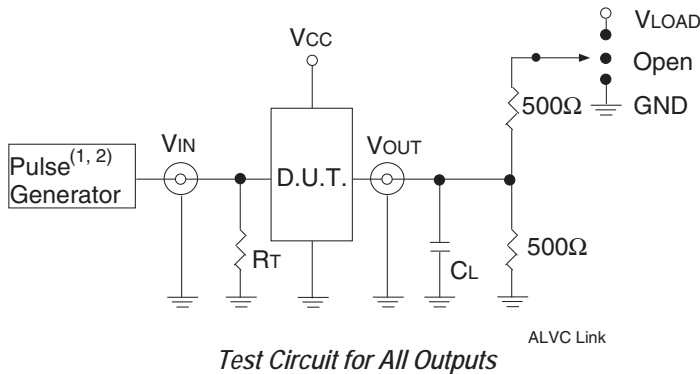
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. TA = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
$V_{LOAD}$	6	6	$2 \times V_{CC}$	V
$V_{IH}$	2.7	2.7	$V_{CC}$	V
$V_T$	1.5	1.5	$V_{CC} / 2$	V
$V_{LZ}$	300	300	150	mV
$V_{HZ}$	300	300	150	mV
$C_L$	50	50	30	pF



#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.

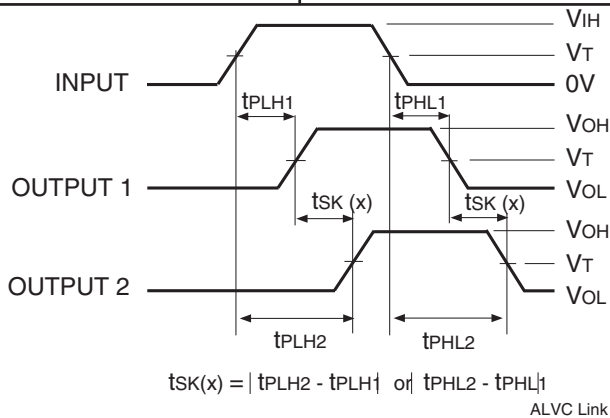
$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2\text{ns}$ ;  $t_f \leq 2\text{ns}$ .

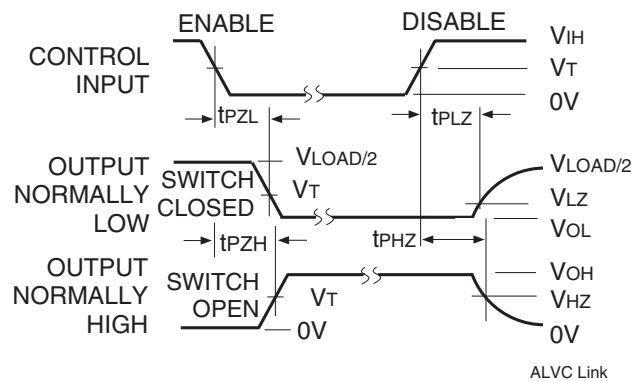
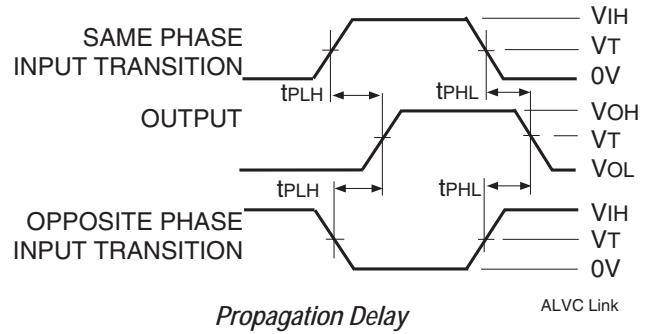
### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	$V_{LOAD}$
Disable High Enable High	GND
All Other Tests	Open



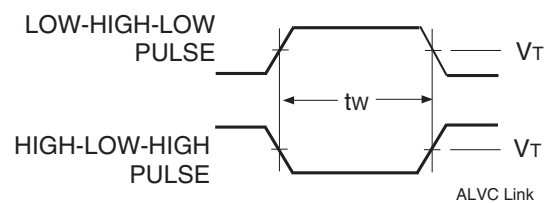
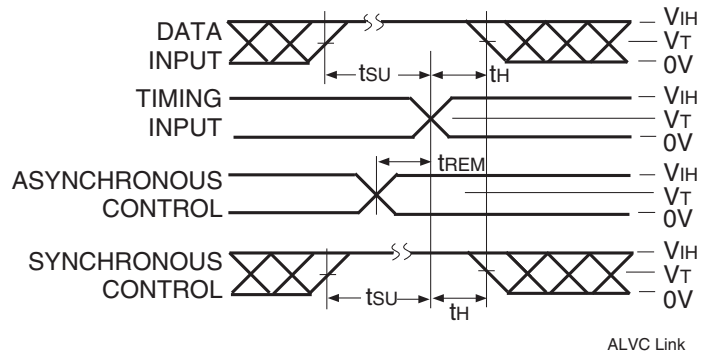
#### NOTES:

1. For  $t_{SK}(a)$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $t_{SK}(b)$  OUTPUT1 and OUTPUT2 are in the same bank.



#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



XX	ALVC	X	XX	XXX	XX	X		
Temp. Range	Bus-Hold	Family	Device Type	Package				
							Blank	Tube
							8	Tape and Reel
							PAG	Thin Shrink Small Outline Package - Green
							245	16-Bit Bus Transceiver with 3-State Outputs
							R162	Double-Density with Resistors, $\pm 12\text{mA}$
							H	Bus-Hold
							74	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

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