Monolithic JFET-Input Operational Amplifiers

PM-155A/PM-156A/PM-157A

FEATURES

All Devices

- **Low Input Bias and Offset Currents**
- **Low Input Offset Voltage** **1.0mV**
- **Low Input Offset Voltage Drift** ..... **3.0μV/° C**
- **Low Input Noise Current** ..... **0.01pA/√Hz**
- **High Common-Mode Rejection Ratio** **100dB**

PM-155 (Only) ..... **LF155 Replacement**

- **Low Supply Current** **2mA**

PM-156 (Only) ..... **LF156 Replacement**

- **High Slew Rate** **12V/μsec**
- **Fast Settling to ±0.01%** **4.0μsec**

PM-157 (Only) ..... **LF157 Replacement**

- **Wide-Bandwidth Decompensated (A_{VCL} = 5 Min)** ... **20MHz**
- **High Slew Rate** **45V/μsec**
- **Fast Settling to ±0.01%** **4.0μsec**

GENERAL DESCRIPTION

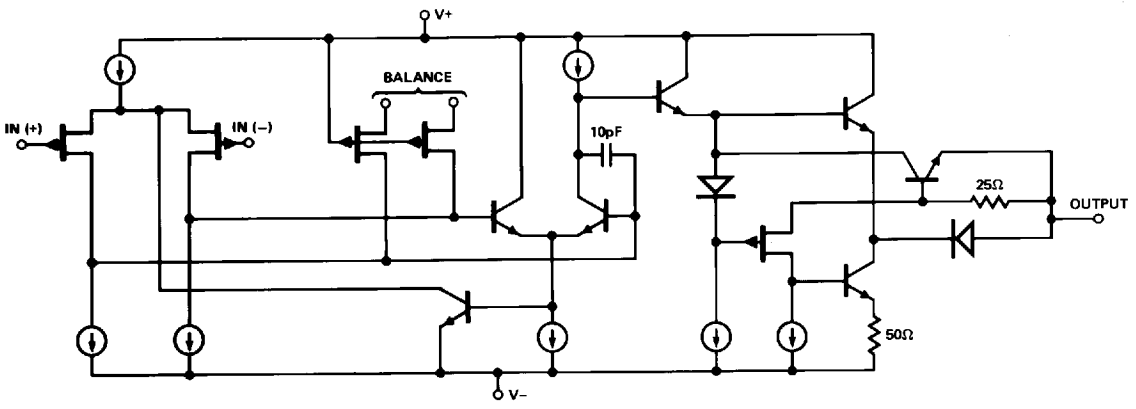
The PM JFET-input series provides low input current, high slew rate, and direct interchangeability with LF155, 156, and 157 types. These operational amplifiers use a new process which allows fabrication of matched JFET transistors and standard bipolar transistors on the same chip. High accuracy and low cost make the PM JFET-input series useful in new designs and as replacements for modular and hybrid types. Unlike many designs, nulling the input offset voltage does not degrade common-mode rejection ratio or input offset voltage drift. Low input voltage noise and current noise plus a low 1/f noise corner frequency allow these amplifiers to be used in a variety of low noise, wide-bandwidth applications.

Dynamic specifications for the PM-155 include a slew rate of 5V/μs, a 2.5MHz gain bandwidth product, and settling time to within ±0.01% of final value in 5.0μs. The PM-156 has a slew rate of 12V/μs and a settling time of 4.0μs to ±0.01% of final value.

The PM-157 is a very fast decompensated device. This results in a 45V/μs slew rate, a 20MHz gain bandwidth product, and a settling time of 4.0μs. Decompensation requires a minimum closed-loop gain of five because of stability considerations.

For improved performance, see the OP-15/OP-16/OP-17 data sheet. For duals, see the OP-215 data sheet.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157, PM-355A, PM-356A, PM-357A ..... ±22V
Operating Temperature Range
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157 ..... −55°C to +125°C
PM-355A, PM-356A, PM-357A ..... 0°C to +70°C
Maximum Junction Temperature (T_j)
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157 ..... +150°C
PM-355A, PM-356A, PM-357A ..... +100°C
Differential Input Voltage
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157, PM-355A, PM-356A, PM-357A ..... ±40V
Input Voltage
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157, PM-355A, PM-356A, PM-357A ..... ±20V

Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) .... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
20-Contact LCC (RC)	98	38	°C/W

NOTES:
1. The absolute maximum negative input voltage is equal to the negative power supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, and LCC packages.

ELECTRICAL CHARACTERISTICS at $\pm 15V \le V_S \le \pm 20V$, $-55°C \le T_A \le +125°C$ and $T_{HIGH} = +125°C$ for PM-155A, PM-156A and PM-157A, $0°C \le T_A \le +70°C$ and $T_{HIGH} = +70°C$ for PM-355A, PM-356A and PM-357A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155A/ PM-156A/ PM-157A MIN	TYP	MAX	PM-355A/ PM-356A/ PM-357A MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	1.4	2.5	—	1.2	2.3	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	3	5	—	3	5	µV/°C
Change in Input Offset Drift with V_{OS} Adjust	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	$R_S = 50\Omega$	—	0.5	—	—	0.5	—	µV/°C per mV
Input Offset Current	I_{OS}	$T_j \le T_{HIGH}$ (Note 1)	—	4.0	10	—	0.4	1.0	nA
Input Bias Current	I_B	$T_j \le T_{HIGH}$ (Note 1)	—	±10	±25	—	±2	±5	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$	25	75	—	25	75	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12	— —	±12 ±10	±13 ±12	— —	V
Input Voltage Range	IVR	$V_S = \pm 15V$	±10.4	+15.1 −12.0	—	±10.4	+15.1 −12.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	—	10	57	µV/V

NOTES:
1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS at $\pm 15V \leq V_S \leq \pm 20V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		PM-155A/ PM-156A/ PM-157A MIN	TYP	MAX	PM-355A/ PM-356A/ PM-357A MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	1	2	—	1	2	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)		—	3	10	—	3	10	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)		—	±30	±50	—	±30	±50	pA
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$		50	200	—	50	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm 15V$	PM-155	—	2	4	—	2	4	mA
			PM-156/PM-157	—	5	7	—	5	7	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	3	5	—	3	5	—	V/μs
			PM-156	10	12	—	10	12	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	40	45	—	40	45	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	—	2.5	—	—	2.5	—	MHz
			PM-156	4.0	4.5	—	4.0	4.5	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	15	20	—	15	20	—	
Settling Time (to ±0.01%)	t_S	$V_S = \pm 15V$ (Note 2)	PM-155	—	5.0	—	—	4.0	—	μs
			PM-156	—	4.0	—	—	1.5	—	
		$V_S = \pm 15V$ (Note 3)	PM-157	—	4.0	—	—	1.5	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, f = 10Hz	PM-155	—	25	—	—	25	—	nV/√Hz
		$R_S = 100\Omega$, f = 1000Hz		—	20	—	—	20	—	
		$R_S = 100\Omega$, f = 10Hz	PM-156/PM-157	—	15	—	—	15	—	
		$R_S = 100\Omega$, f = 1000Hz		—	12	—	—	12	—	
Input Noise Current	i_n	f = 100Hz, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	pA/√Hz
		f = 1000Hz, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}			—	3	—	—	3	—	pF

NOTES:

1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS at $\pm 15V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ for PM-155, PM-156 and PM-157, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155 PM-156 PM-157 MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	4	7	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	5	—	µV/°C
Change In Input Offset Drift With V_{OS} Adjust.	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	$R_S = 50\Omega$	—	0.5	—	µV/°C per mV
Input Offset Current	I_{OS}	$T_j \leq T_{HIGH}$ (Note 1)	—	8	20	nA
Input Bias Current	I_B	$T_j \leq T_{HIGH}$ (Note 1)	—	±2	±50	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 2k\Omega$	25	75	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12	— —	V
Input Voltage Range	IVR	$V_S = \pm 15V$	±10.4	+15.1 −12.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	µV/V

NOTES:

1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$, $T_j = +125°C$.
2. Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

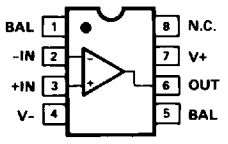
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	8-PIN HERMETIC DIP	LCC	OPERATING TEMPERATURE RANGE
2.0	PM155AJ*	PM155AZ/883	PM155ARC/883	MIL
	PM156AJ*	PM156AZ*	PM156ARC/883	
	PM157AJ/883	PM157AZ*	—	
2.0	PM355AJ	PM355AZ	—	COM
	PM356AJ	PM356AZ	—	
	PM357AJ	PM357AZ	—	
5.0	PM155J*	PM155Z*	—	MIL
	PM156J*	PM156Z*	—	
	PM157J*	PM157Z*	—	

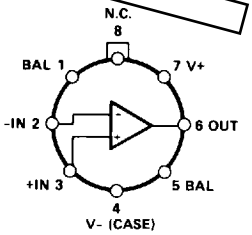
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

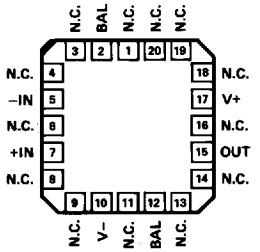
PIN CONNECTIONS



8-PIN HERMETIC DIP (Z-Suffix)



TO-99 (J-Suffix)



PM-155ARC/883, PM-156ARC/883 20-LEAD LCC (RC-Suffix)

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $\pm 15V \leq V_S \leq \pm 20V$ for PM-155, PM-156 and PM-157, unless otherwise noted.

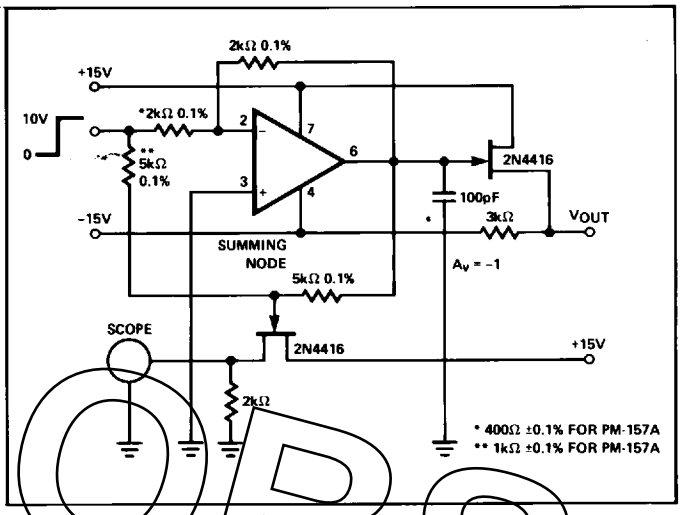
PARAMETER	SYMBOL	CONDITIONS		PM-155 PM-156 PM-157 MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	3	5	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)		—	3	20	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)		—	±30	±100	pA
Input Resistance	R_{IN}			—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$		50	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm 15V$	PM-155	—	2	4	mA
			PM-156/PM-157	—	5	7	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	—	5	—	V/μs
			PM-156	7.5	12	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	30	40	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	—	2.5	—	MHz
			PM-156	—	5	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	—	20	—	
Settling Time (to ±0.01%)	t_S	$V_S = \pm 15V$ (Note 2)	PM-155	—	5	—	μs
			PM-156	—	4	—	
		$V_S = \pm 15V$ (Note 3)	PM-157	—	4	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, f = 100Hz	PM-155	—	25	—	nV/√Hz
		$R_S = 100\Omega$, f = 1000Hz		—	20	—	
		$R_S = 100\Omega$, f = 100Hz	PM-156/PM-157	—	15	—	
		$R_S = 100\Omega$, f = 1000Hz		—	12	—	
Input Noise Current	i_n	f = 100Hz, $V_S = \pm 15V$		—	0.01	—	pA/√Hz
		f = 1000Hz, $V_S = \pm 15V$					
Input Capacitance	C_{IN}			—	3	—	pF

NOTES:

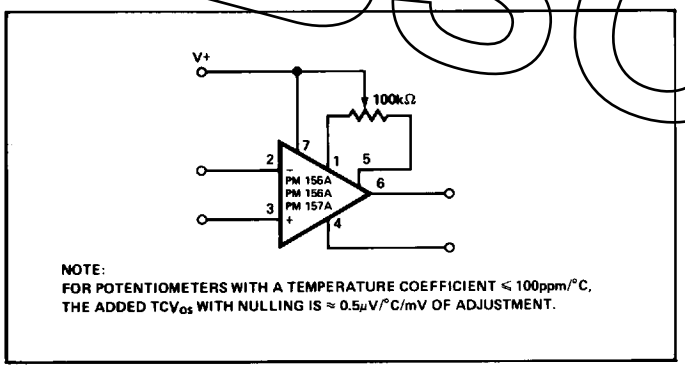
1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

BASIC CONNECTIONS

SETTLING-TIME TEST CIRCUIT

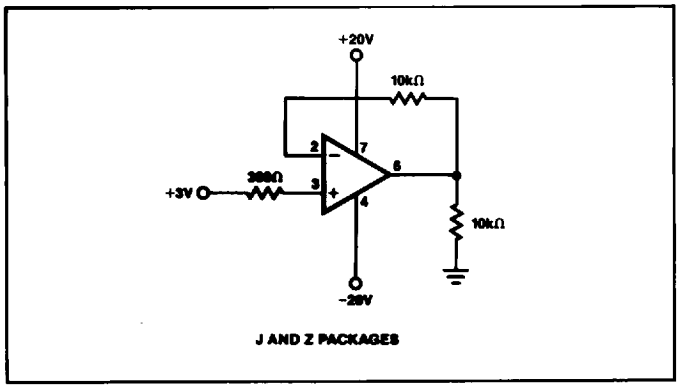


INPUT OFFSET VOLTAGE NULLING



NOTE:
FOR POTENTIOMETERS WITH A TEMPERATURE COEFFICIENT ≤ 100ppm/°C, THE ADDED TCV_{OS} WITH NULLING IS ≈ 0.5μV/°C/mV OF ADJUSTMENT.

BURN-IN CIRCUIT



J AND Z PACKAGES

APPLICATIONS INFORMATION

INPUT VOLTAGE CONSIDERATIONS

The PM series JFET input stages can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than V- can result in a destroyed unit.

If both inputs exceed the negative common-mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common-mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common-mode voltage range.

Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

POWER SUPPLY CONSIDERATIONS

Power supply polarity reversal can result in a destroyed unit.

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input. This minimizes "pick-up" and increases the frequency of the feedback pole by minimizing the capacitance from input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device to AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain. Consequently, the pole has negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the inverting input of the op amp. The capacitor value should be such that the RC time constant of the capacitor and feedback resistor is greater than, or equal to, the original feedback-pole time constant.