



F²MC-16LX CY90930 Series 16-bit Proprietary Microcontroller

The CY90930 series is a family of general-purpose Cypress 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16L families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Features

■ Clock

Built-in PLL clock frequency multiplication circuit.
Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed.

■ 16-bit input capture (8 channels)

Detects rising, falling, or both edges.
16-bit capture register $\times$ 8
The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

■ 16-bit reload timer (4 channels)

16-bit reload timer operation (select toggle output or one-shot output)
Selectable event count function

■ Real time watch timer (main clock)

Operates directly from oscillator clock.
Interrupt can be generated by second/minute/hour/date counter overflow.

■ PPG timer (6 channels)

Output pins (6 channels), external trigger input pin (1 channel)
Operation clock frequencies : f_{CP} , $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$

■ Delay interrupt

Generates interrupt for task switching.
Interrupts to CPU can be generated/cleared by software setting.

■ External interrupts (8 channels)

8-channel independent operation
Interrupt source setting available : "L" to "H" edge/ "H" to "L" edge/ "L" level/ "H" level.

■ 8/10-bit A/D converter (24 channels)

Conversion time : 3 μ s (at f_{CP} = 32 MHz)
External trigger activation available (P50/INT0/ADTG)
Internal timer activation available (16-bit reload timer 1)

■ UART(LIN/SCI) (4 channels)

Equipped with full duplex double buffer
Clock-asynchronous or clock-synchronous serial transfer is available.

■ CAN interface (1 channel).

Conforms to CAN specifications version 2.0 Part A and B.
Automatic resend in case of error.
Automatic transfer in response to remote frame.
16 prioritized message buffers for data and ID
Multiple message support
Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
Supports up to 1 Mbps
CAN wakeup function (RX connected to INT0 internally)

■ LCD controller/driver (32 segment $\times$ 4 common)

Segment driver and command driver with direct LCD panel (display) drive capability

■ Reset on detection of low voltage/program loop

Automatic reset when low voltage is detected.
Program looping detection function

■ Stepping motor controller (4 channels)

High current output for each channel $\times$ 4
Synchronized 8/10-bit PWM for each channel $\times$ 2

■ Sound generator (2 channels)

8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at f_{CP} = 32 MHz)
Tone frequencies : PWM frequency /2/, divided by (reload frequency +1)

■ Input/output ports

General-purpose input/output port (CMOS output) 93 ports

■ Function for port input level selection

Automotive/CMOS-Schmitt

■ Flash memory security function

Protects the contents of Flash memory (Flash memory product only)

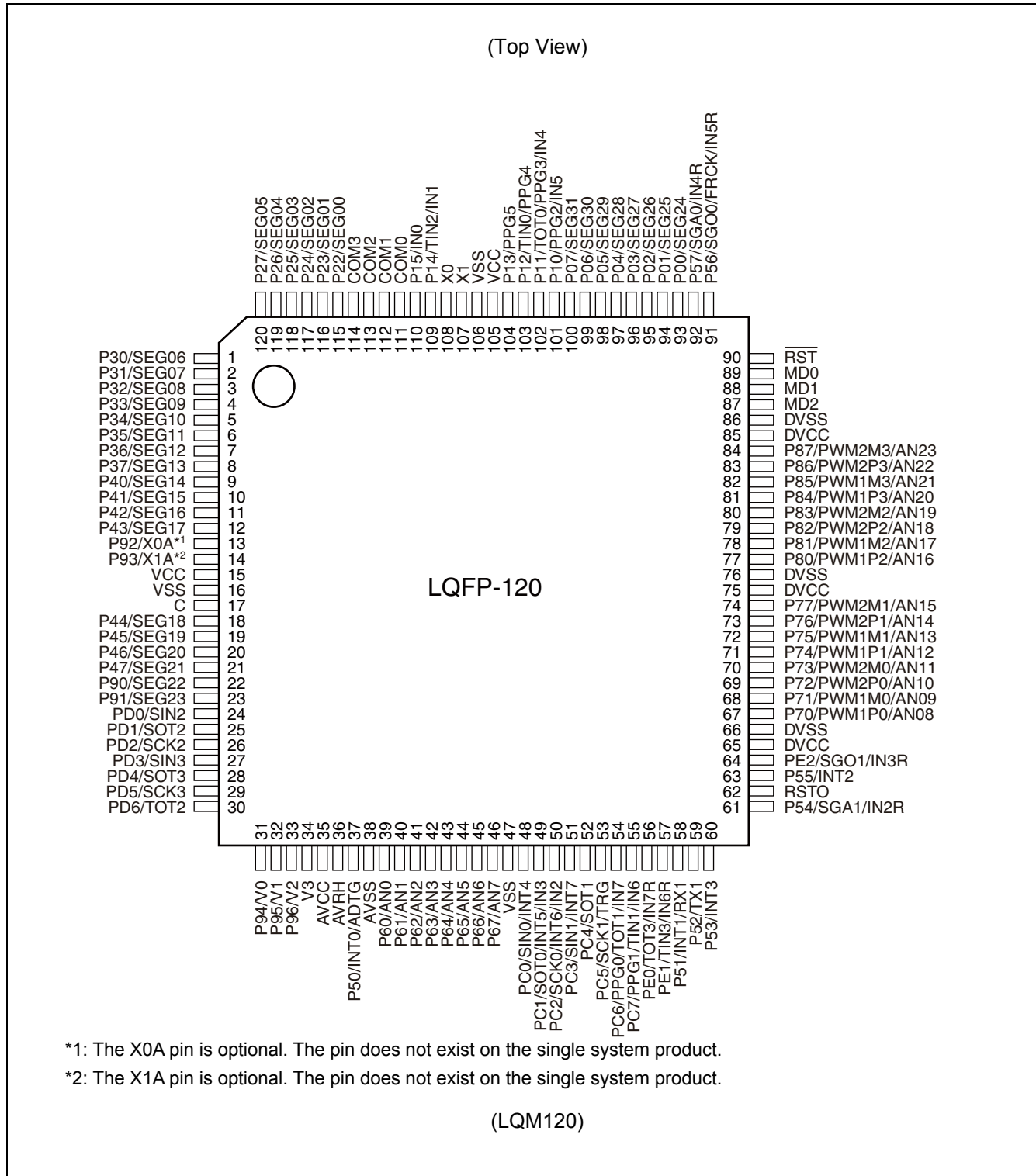
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1. Product Lineup

Part Number Parameter	CY90F931	CY90F931S	CY90931	CY90931S	CY90V930-102	CY90V930-101
Type	Flash memory		Mask ROM		Evaluation	
CPU	F ² MC-16LX CPU					
System clock	PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 6, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25ns (with 4 MHz oscillation clock × 8)					
Sub clock pins (X0A, X1A)	Yes	No	Yes	No	Yes	No
ROM	Flash memory 128 Kbytes		Mask ROM 128 Kbytes		External	
RAM	8 Kbytes				30 Kbytes	
I/O port	91 ports	93 ports	91 ports	93 ports	91 ports	93 ports
LCD controller	32 segment × 4 common					
LIN-UART	UART(LIN/SCI) 4 channels					
CAN interface	1 channel					
16-bit input capture	8 channels					
16-bit reload timer	4 channels					
16-bit free-run timer	1 channel					
Real time watch timer	1 channel					
16-bit PPG timer	6 channels					
External interrupt	8 channels					
8/10-bit A/D converter	24 channels					
Low-voltage/CPU operating detection reset	Yes				No	
Stepping motor controller	4 channels					
Sound generator	2 channels					
Flash memory security	Yes		—			
Operating voltage	3.7 V to 5.5 V				4.5 V to 5.5 V	
Package	LQFP-120				PGA-299	

2. Pin Assignment



3. Pin Descriptions

Pin No.	Pin Name	I/O Circuit Type ^{*1}	Function
108	X0	A	High-speed oscillation input pin
107	X1		High-speed oscillation output pin
13	X0A	B	Low-speed oscillation input pin
	P92	I	General-purpose I/O port
14	X1A	B	Low-speed oscillation output pin
	P93	I	General-purpose I/O port
90	RST	C	Reset input pin
93	P00	F	General-purpose I/O port
	SEG24		LCD controller/driver segment output pin
94	P01	F	General-purpose I/O port
	SEG25		LCD controller/driver segment output pin
95	P02	F	General-purpose I/O port
	SEG26		LCD controller/driver segment output pin
96	P03	F	General-purpose I/O port
	SEG27		LCD controller/driver segment output pin
97	P04	F	General-purpose I/O port
	SEG28		LCD controller/driver segment output pin
98	P05	F	General-purpose I/O port
	SEG29		LCD controller/driver segment output pin
99	P06	F	General-purpose I/O port
	SEG30		LCD controller/driver segment output pin
100	P07	F	General-purpose I/O port
	SEG31		LCD controller/driver segment output pin
101	P10	I	General-purpose I/O port
	PPG2		16-bit PPG ch.2 output pin
	IN5		Input capture ch.5 trigger input pin
102	P11	I	General-purpose I/O port
	TOT0		16-bit reload timer ch.0 TOT output pin
	PPG3		16-bit PPG ch.3 output pin
	IN4		Input capture ch.4 trigger input pin
103	P12	I	General-purpose I/O port
	TIN0		16-bit reload timer ch.0 TIN input pin
	PPG4		16-bit PPG ch.4 output pin
104	P13	I	General-purpose I/O port
	PPG5		16-bit PPG ch.5 output pin
109	P14	I	General-purpose I/O port
	TIN2		16-bit reload timer ch.2 TIN input pin
	IN1		Input capture ch.1 trigger input pin

Pin No.	Pin Name	I/O Circuit Type ^{*1}	Function
110	P15	I	General-purpose I/O port
	IN0		Input capture ch.0 trigger input pin
111	COM0	P	LCD controller/driver common output pin
112	COM1	P	LCD controller/driver common output pin
113	COM2	P	LCD controller/driver common output pin
114	COM3	P	LCD controller/driver common output pin
115	P22	F	General-purpose I/O port
	SEG00		LCD controller/driver segment output pin
116	P23	F	General-purpose I/O port
	SEG01		LCD controller/driver segment output pin
117	P24	F	General-purpose I/O port
	SEG02		LCD controller/driver segment output pin
118	P25	F	General-purpose I/O port
	SEG03		LCD controller/driver segment output pin
119	P26	F	General-purpose I/O port
	SEG04		LCD controller/driver segment output pin
120	P27	F	General-purpose I/O port
	SEG05		LCD controller/driver segment output pin
1	P30	F	General-purpose I/O port
	SEG06		LCD controller/driver segment output pin
2	P31	F	General-purpose I/O port
	SEG07		LCD controller/driver segment output pin
3	P32	F	General-purpose I/O port
	SEG08		LCD controller/driver segment output pin
4	P33	F	General-purpose I/O port
	SEG09		LCD controller/driver segment output pin
5	P34	F	General-purpose I/O port
	SEG10		LCD controller/driver segment output pin
6	P35	F	General-purpose I/O port
	SEG11		LCD controller/driver segment output pin
7	P36	F	General-purpose I/O port
	SEG12		LCD controller/driver segment output pin
8	P37	F	General-purpose I/O port
	SEG13		LCD controller/driver segment output pin
9	P40	F	General-purpose I/O port
	SEG14		LCD controller/driver segment output pin
10	P41	F	General-purpose I/O port
	SEG15		LCD controller/driver segment output pin
11	P42	F	General-purpose I/O port
	SEG16		LCD controller/driver segment output pin

Pin No.	Pin Name	I/O Circuit Type *1	Function
12	P43	F	General-purpose I/O port
	SEG17		LCD controller/driver segment output pin
18	P44	F	General-purpose I/O port
	SEG18		LCD controller/driver segment output pin
19	P45	F	General-purpose I/O port
	SEG19		LCD controller/driver segment output pin
20	P46	F	General-purpose I/O port
	SEG20		LCD controller/driver segment output pin
21	P47	F	General-purpose I/O port
	SEG21		LCD controller/driver segment output pin
37	P50	I	General-purpose I/O port
	INT0		INT0 external interrupt input pin
	ADTG		A/D converter external trigger input pin
58	P51	I	General-purpose I/O port
	INT1		INT1 external interrupt input pin
	RX1		CAN interface 1 RX input pin
59	P52	I	General-purpose I/O port
	TX1		CAN interface 1 TX output pin
60	P53	I	General-purpose I/O port
	INT3		INT3 external interrupt input pin
61	P54	I	General-purpose I/O port
	SGA1		Sound generator ch.1 SGA output pin
	IN2R		Input capture ch.2 trigger input pin
63	P55	I	General-purpose I/O port
	INT2		INT2 external interrupt input pin
91	P56	I	General-purpose I/O port
	SGO0		Sound generator ch.0 SGO output pin
	FRCK		Free-run timer clock input pin
	IN5R		Input capture ch.5 trigger input pin
92	P57	I	General-purpose I/O port
	SGA0		Sound generator ch.0 SGA output pin
	IN4R		Input capture ch.4 trigger input pin
39	P60	H	General-purpose I/O port
	AN0		A/D converter input pin
40	P61	H	General-purpose I/O port
	AN1		A/D converter input pin
41	P62	H	General-purpose I/O port
	AN2		A/D converter input pin
42	P63	H	General-purpose I/O port
	AN3		A/D converter input pin

Pin No.	Pin Name	I/O Circuit Type ^{*1}	Function
43	P64	H	General-purpose I/O port
	AN4		A/D converter input pin
44	P65	H	General-purpose I/O port
	AN5		A/D converter input pin
45	P66	H	General-purpose I/O port
	AN6		A/D converter input pin
46	P67	H	General-purpose I/O port
	AN7		A/D converter input pin
67	P70	L	General-purpose output-only port
	PWM1P0		Stepping motor controller ch.0 output pin
	AN08		A/D converter input pin
68	P71	L	General-purpose output-only port
	PWM1M0		Stepping motor controller ch.0 output pin
	AN09		A/D converter input pin
69	P72	L	General-purpose output-only port
	PWM2P0		Stepping motor controller ch.0 output pin
	AN10		A/D converter input pin
70	P73	L	General-purpose output-only port
	PWM2M0		Stepping motor controller ch.0 output pin
	AN11		A/D converter input pin
71	P74	L	General-purpose output-only port
	PWM1P1		Stepping motor controller ch.1 output pin
	AN12		A/D converter input pin
72	P75	L	General-purpose output-only port
	PWM1M1		Stepping motor controller ch.1 output pin
	AN13		A/D converter input pin
73	P76	L	General-purpose output-only port
	PWM2P1		Stepping motor controller ch.1 output pin
	AN14		A/D converter input pin
74	P77	L	General-purpose output-only port
	PWM2M1		Stepping motor controller ch.1 output pin
	AN15		A/D converter input pin
77	P80	L	General-purpose output-only port
	PWM1P2		Stepping motor controller ch.2 output pin
	AN16		A/D converter input pin
78	P81	L	General-purpose output-only port
	PWM1M2		Stepping motor controller ch.2 output pin
	AN17		A/D converter input pin
79	P82	L	General-purpose output-only port
	PWM2P2		Stepping motor controller ch.2 output pin
	AN18		A/D converter input pin

Pin No.	Pin Name	I/O Circuit Type *1	Function
80	P83	L	General-purpose output-only port
	PWM2M2		Stepping motor controller ch.2 output pin
	AN19		A/D converter input pin
81	P84	L	General-purpose output-only port
	PWM1P3		Stepping motor controller ch.3 output pin
	AN20		A/D converter input pin
82	P85	L	General-purpose output-only port
	PWM1M3		Stepping motor controller ch.3 output pin
	AN21		A/D converter input pin
83	P86	L	General-purpose output-only port
	PWM2P3		Stepping motor controller ch.3 output pin
	AN22		A/D converter input pin
84	P87	L	General-purpose output-only port
	PWM2M3		Stepping motor controller ch.3 output pin
	AN23		A/D converter input pin
22	P90	F	General-purpose I/O port
	SEG22		LCD controller/driver segment output pin
23	P91	F	General-purpose I/O port
	SEG23		LCD controller/driver segment output pin
31	P94	G	General-purpose I/O port
	V0		LCD controller/driver reference power supply pin
32	P95	G	General-purpose I/O port
	V1		LCD controller/driver reference power supply pin
33	P96	G	General-purpose I/O port
	V2		LCD controller/driver reference power supply pin
34	V3	—	LCD controller/driver reference power supply pin
48	PC0	J	General-purpose I/O port
	SIN0		UART ch.0 serial data input pin
	INT4		INT4 external interrupt input pin
49	PC1	I	General-purpose I/O port
	SOT0		UART ch.0 serial data output pin
	INT5		INT5 external interrupt input pin
	IN3		Input capture ch.3 trigger input pin
50	PC2	I	General-purpose I/O port
	SCK0		UART ch.0 serial clock I/O pin
	INT6		INT6 external interrupt input pin
	IN2		Input capture ch.2 trigger input pin
51	PC3	J	General-purpose I/O port
	SIN1		UART ch.1 serial data input pin
	INT7		INT7 external interrupt input pin

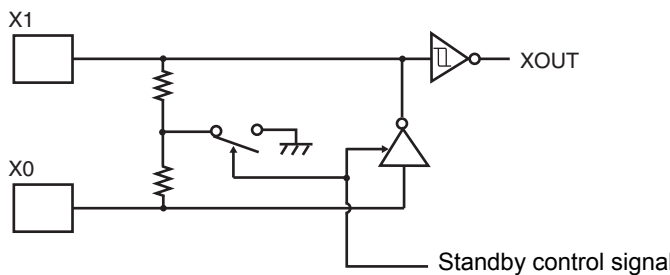
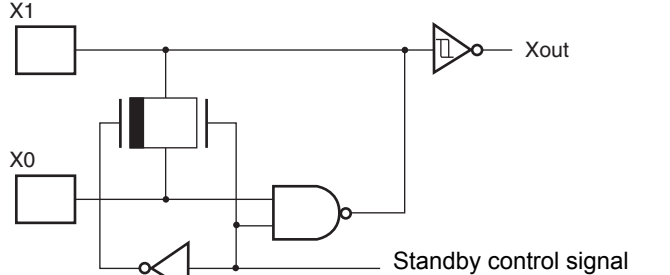
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52	PC4	I	General-purpose I/O port
	SOT1		UART ch.1 serial data output pin
53	PC5	I	General-purpose I/O port
	SCK1		UART ch.1 serial clock I/O pin
	TRG		16-bit PPG ch.0 to ch.5 external trigger input pin
54	PC6	I	General-purpose I/O port
	PPG0		16-bit PPG ch.0 output pin
	TOT1		16-bit reload timer ch.1 TOT output pin
	IN7		Input capture ch.7 trigger input pin
55	PC7	I	General-purpose I/O port
	PPG1		16-bit PPG ch.1 output pin
	TIN1		16-bit reload timer ch.1 TIN input pin
	IN6		Input capture ch.6 trigger input pin
24	PD0	J	General-purpose I/O port
	SIN2		UART ch.2 serial data input pin
25	PD1	I	General-purpose I/O port
	SOT2		UART ch.2 serial data output pin
26	PD2	F	General-purpose I/O port
	SCK2		UART ch.2 serial clock I/O pin
27	PD3	J	General-purpose I/O port
	SIN3		UART ch.3 serial data input pin
28	PD4	I	General-purpose I/O port
	SOT3		UART ch.3 serial data output pin
29	PD5	F	General-purpose I/O port
	SCK3		UART ch.3 serial clock I/O pin
30	PD6	I	General-purpose I/O port
	TOT2		16-bit reload timer ch.2 TOT output pin
56	PE0	I	General-purpose I/O port
	TOT3		16-bit reload timer ch.3 TOT output pin
	IN7R		Input capture ch.7 trigger input pin
57	PE1	I	General-purpose I/O port
	TIN3		16-bit reload timer ch.3 TIN input pin
	IN6R		Input capture ch.6 trigger input pin
64	PE2	I	General-purpose I/O port
	SGO1		Sound generator ch.1 SGO output pin
	IN3R		Input capture ch.3 trigger input pin
62	RSTO	N	Internal reset signal output pin
65, 75, 85	DVCC	—	Power supply input pins dedicated for high current output buffer
66, 76, 86	DVSS	—	Power supply GND pins dedicated for high current output buffer
35	AVCC	—	A/D converter dedicated power supply input pin
38	AVSS	—	A/D converter dedicated power supply GND pin

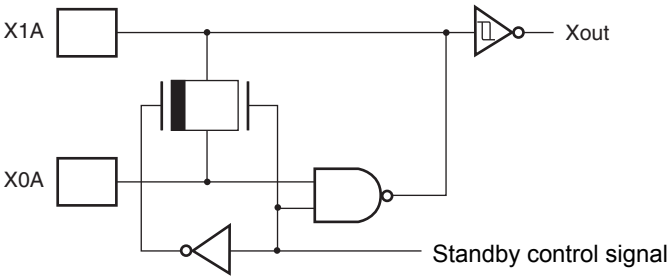
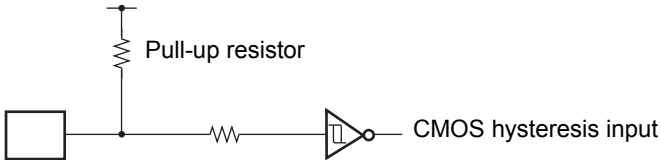
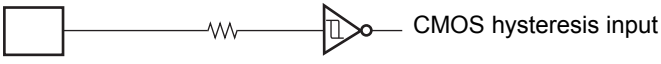
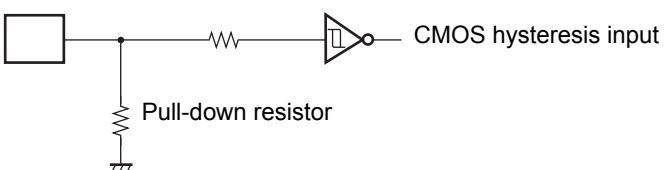
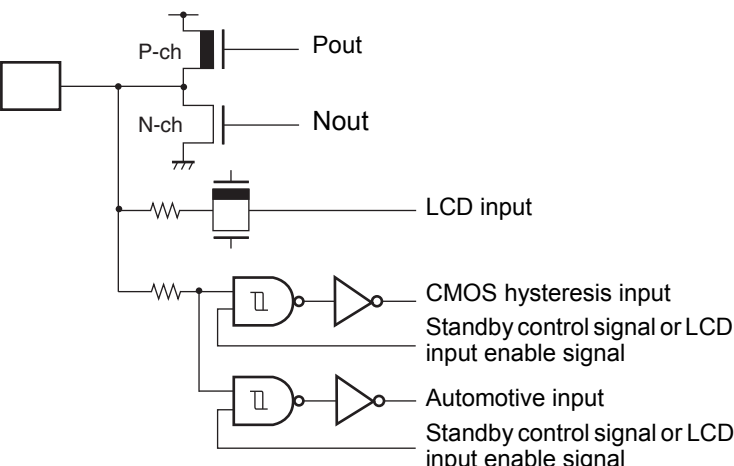
Pin No.	Pin Name	I/O Circuit Type ^{*1}	Function
36	AVRH	—	A/D converter Vref+ input pin. Vref- is fixed to AVSS.
89	MD0	D	Mode setting input pin. Connect to VCC pin.
88	MD1	D	Mode setting input pin. Connect to VCC pin.
87	MD2	D/E ^{*2}	Mode setting input pin. Connect to VSS pin.
17	C	—	External capacitor pin. Connect a 0.1 μ F capacitor between this pin and the VSS pin.
15, 105	VCC	—	Power supply input pins
16, 47, 106	VSS	—	GND power supply pins

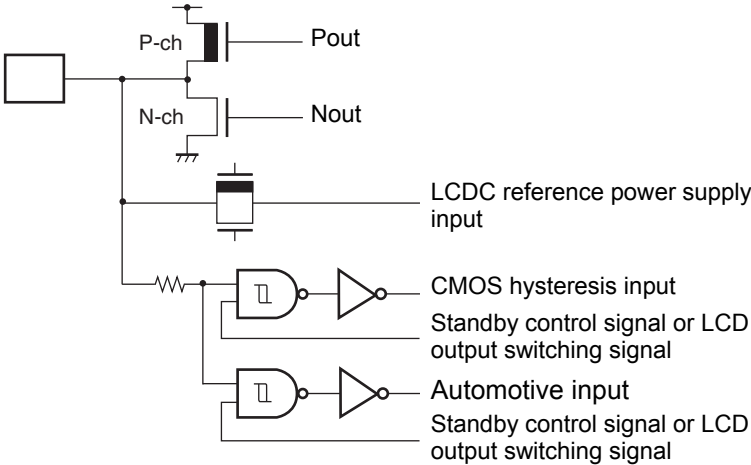
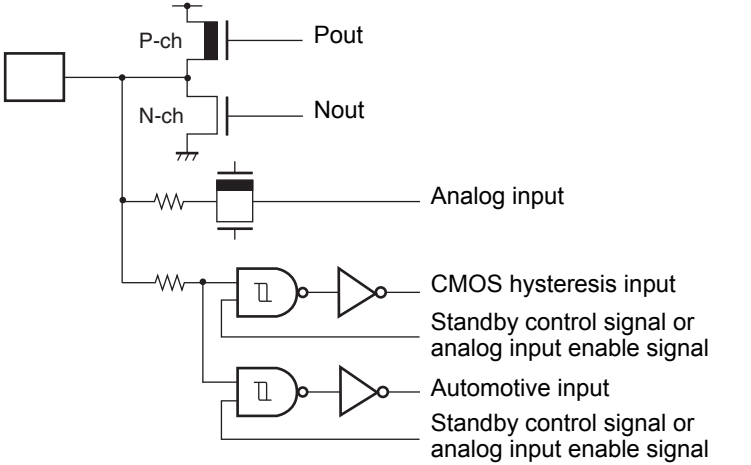
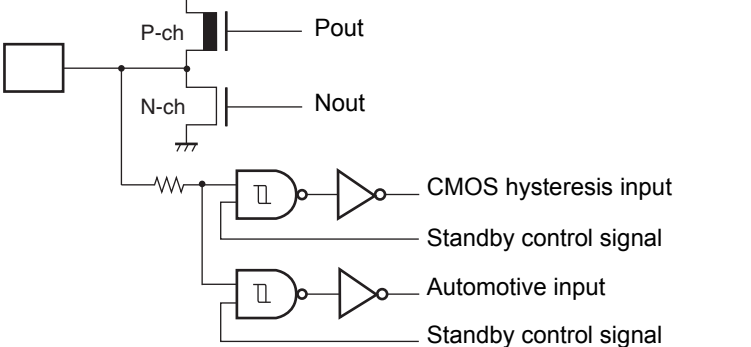
*1. For I/O circuit type, refer to [I/O Circuit Type](#).

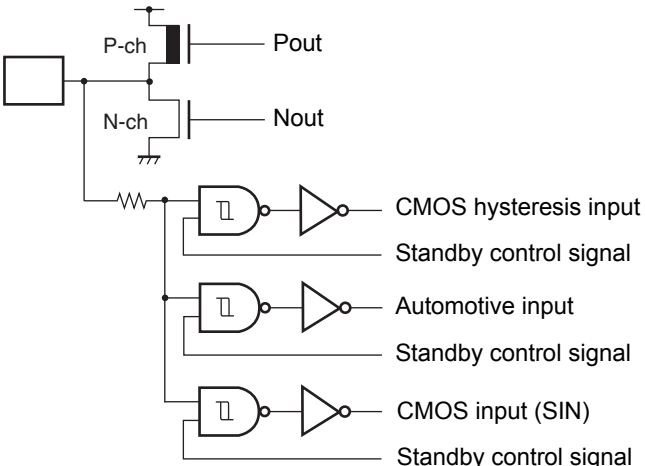
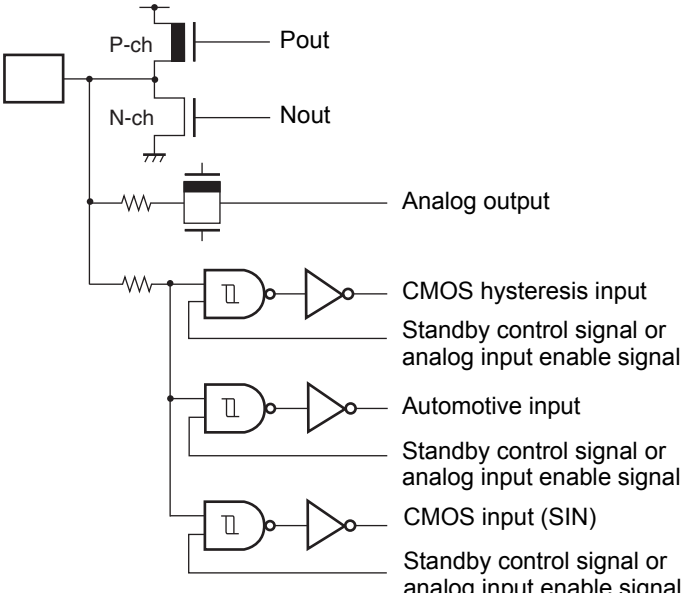
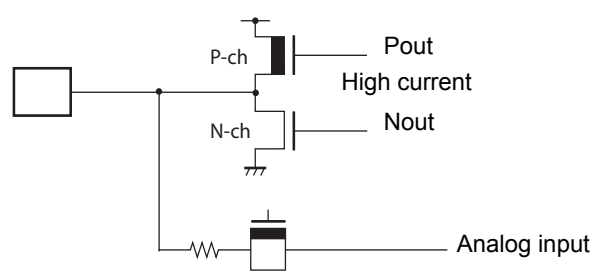
*2. The I/O circuit type is D for Flash memory products/Mask ROM products and E for evaluation products.

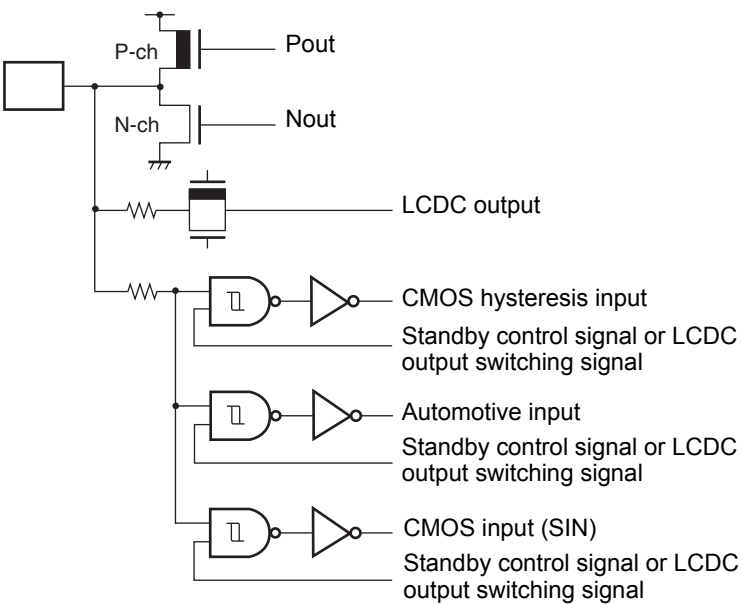
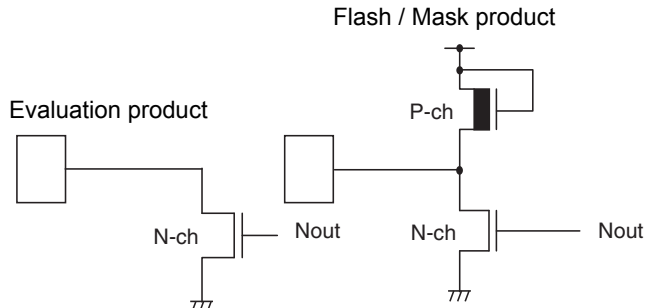
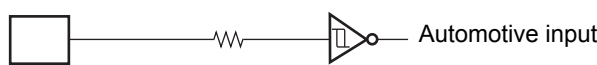
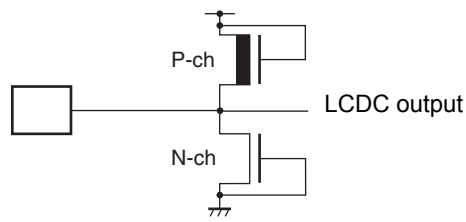
4. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation pin (Flash memory product, Mask ROM product) Oscillation feedback resistance : approx. 1 M Ω
		High-speed oscillation pin (Evaluation product) Oscillation feedback resistance : approx. 1 M Ω

Type	Circuit	Remarks
B		low-speed oscillation pin Oscillation feedback resistance : approx. 10 MΩ
C		Input-only pin (with pull-up resistance) ■ Attached pull-up resistor : approx. 50 kΩ ■ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$)
D		Input-only pin ■ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) Note: The MD2 pin of the Flash memory products uses this circuit type.
E		Input-only pin (with pull-down resistance) ■ Attached pull-down resistance : approx. 50 kΩ ■ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) Note: The MD2 pin of the Mask ROM products and the evaluation products uses this circuit type.
F		LCD output common general-purpose port ■ CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) ■ Hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) ■ Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)

Type	Circuit	Remarks
G		LCD reference power supply common general-purpose port ■ CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) ■ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) ■ Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)
H		A/D converter input common general-purpose port ■ CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) ■ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) ■ Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)
I		General-purpose port ■ CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) ■ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) ■ Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)

Type	Circuit	Remarks
J		General-purpose port (serial input) ■ CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) ■ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) ■ CMOS input (SIN) ($V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}$) ■ Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)
K		A/D converter input common general-purpose port (serial input) ■ CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) ■ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) ■ CMOS input (SIN) ($V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}$) ■ Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)
L		A/D converter input common and high current output port (SMC pin) CMOS output ($I_{OH}/I_{OL} = \pm 30 \text{ mA}$)

Type	Circuit	Remarks
M		LCDC output common general-purpose port (serial input)) ■ CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) ■ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) ■ CMOS input (SIN) ($V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}$) ■ Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$)
N		N-ch open-drain pin $I_{OL} = 4 \text{ mA}$
O		Input-only pin Automotive input $(V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})$
P		LCDC output pin (COM pin)

5. Handling Devices

Strictly Observe Maximum Rated Voltages (Preventing Latch-up)

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium or high withstand voltage pins, or if the voltage applied between VCC and VSS pins exceeds the rated voltage level. If a latch-up occurs, the power supply current may increase dramatically and may destroy semiconductor elements. When using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

When the analog system power supply is switched on or off, be careful not to apply the analog power supply (AV_{CC} , AV_{RH}), the analog input voltages and the power supply voltage for the high current output buffer pins (DVCC) in excess of the digital power supply voltage (V_{CC}).

Once the digital power supply voltage (V_{CC}) has been disconnected, the analog power supply (AV_{CC} , AV_{RH}) and the power supply voltage for the high current output buffer pins (DVCC) may be turned on in any sequence.

Supply Voltage Stabilization

Rapid fluctuations in the power supply voltage can cause malfunctions even if the V_{CC} power supply voltage remains within the warranted operating range. It is recommended that the power supply be stabilized such that ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) be limited to within 10% of the standard V_{CC} value, and that transient fluctuations due to power supply switching, etc. be limited to a rate of 0.1 V/ms or less.

Precautions when Turning the Power ON

In order to prevent the built-in step-down circuits from malfunctioning, the time taken for the voltage to rise (0.2 V to 2.7 V) during power-on should be less than 50 μ s.

Handling Unused Pins

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 k Ω .

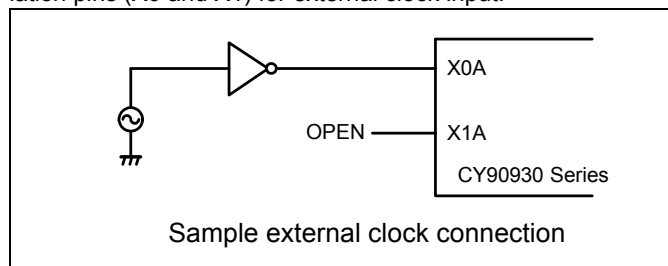
Unused input/output pins may be set to the output state and left open, or set to the input state and connected to a pull-up or pull-down resistance of 2 k Ω or more.

Handling A/D Converter Power Supply Pins

Even if the A/D converter is not used, the power supply pins should be connected such as $AV_{CC} = V_{CC}$, and $AV_{SS} = AV_{RH} = V_{SS}$.

Notes on Using an External Clock

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Furthermore, only the X0A pin should be driven when an external clock is used, with the X1A pin open as shown in the following diagram. Do not use high-speed oscillation pins (X0 and X1) for external clock input.



Notes on Operating in PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Cypress will not guarantee results of operations if such failure occurs.

Crystal Oscillator Circuit

Noise around the X0/X1 may cause this device to operate abnormally. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit do not cross the lines of other circuits while you design a printed circuit board.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

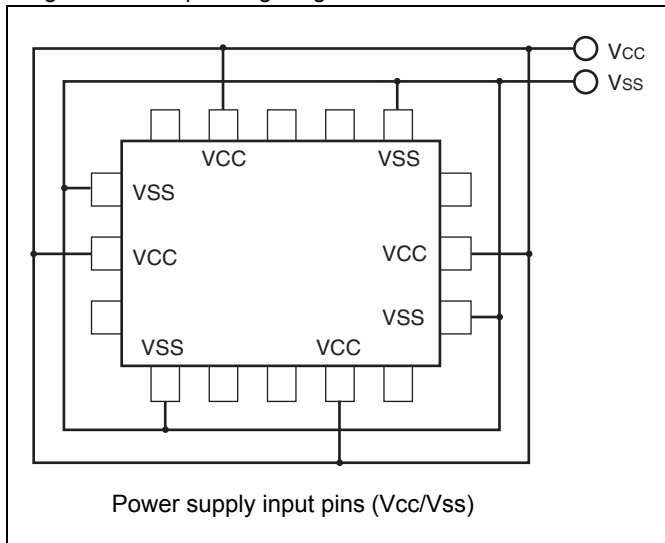
Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

Power Supply Pins

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to externally connect the VCC and VSS pins to the power supply and ground respectively.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are

connected to different voltages, even if those voltages are within the guaranteed operating ranges.



In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μ F bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

Sequence for Connecting the A/D Converter Power Supply and Analog Inputs

The A/D converter power supply (AV_{CC} , $AVRH$) and analog inputs (AN0 to AN23) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that $AVRH$ does not exceed AV_{CC} during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

Handling the Power Supply for High-current Output Buffer Pins (DVCC, DVSS)

*Flash memory Products/Mask ROM Products
(CY90F931/CY90F931S/CY90931/CY90931S)*

In the Flash memory products/Mask ROM products, the power supply for the high-current output buffer pins (DVCC, DVSS) is isolated from the digital power supply (V_{CC}). Therefore, DVcc can be set to a higher voltage than Vcc. If the power supply for the high-current output buffer pins (DVCC, DVSS) is supplied before the digital power supply (V_{CC}), however, care needs to be taken because it is possible that the port 7 or port 8 stepping motor outputs may momentarily output an "H" or "L" level during the DVcc rise. In order to prevent this, connect the digital power supply (V_{CC}) prior to connecting the power supply for the high-current output buffer pins.

Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power

supply pins for the high-current output buffer pins (DVCC, DVSS).

Evaluation Product (CY90V930-102/CY90V930-101)

In the evaluation products, the power supply for the high-current output buffer pins (DVCC, DVSS) is not isolated from the digital power supply (V_{CC}). Therefore, DVcc must be set to a lower voltage than Vcc. The power supply for the high-current output buffer pins (DVCC, DVSS) must always be applied after the digital power supply (V_{CC}) has been connected, and disconnected before the digital power supply (V_{CC}) is disconnected (the power supply for the high-current output buffer pins may also be connected and disconnected simultaneously with the digital power supply).

Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins (DVCC, DVSS).

Pull-up/pull-down Resistors

CY90930 series does not support internal pull-up/pull-down resistors. Use external components as necessary.

Precautions when Not Using a Sub Clock Signal

If the X0A and X1A pins are not connected to an oscillator, apply a pull-down resistance to the X0A pin and leave the X1A pin open.

Flash Memory Security Function

A security bit is located within the Flash memory region. The security function is activated by writing the protection code 01_H to the security bit.

Do not write the value 01_H to this address if you are not using the security function.

Please refer to following table for the address of the security bit.

	Flash Memory Size	Address for Security Bit
CY90F931 CY90F931S	Built-in 1 Mbit Flash Memory	FE0001 _H

Serial Communication

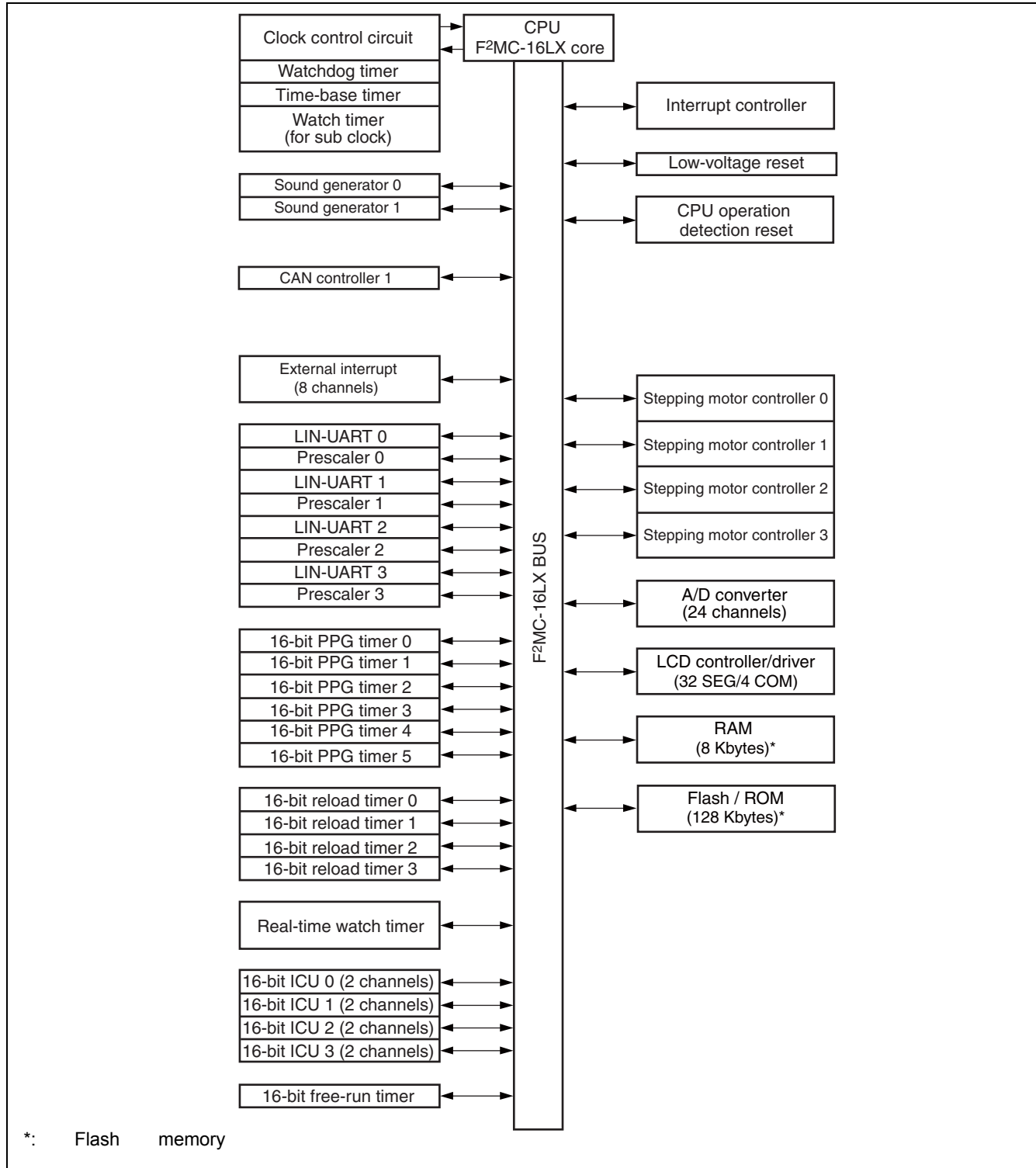
In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

Characteristic Difference between Flash Device and Mask ROM Device

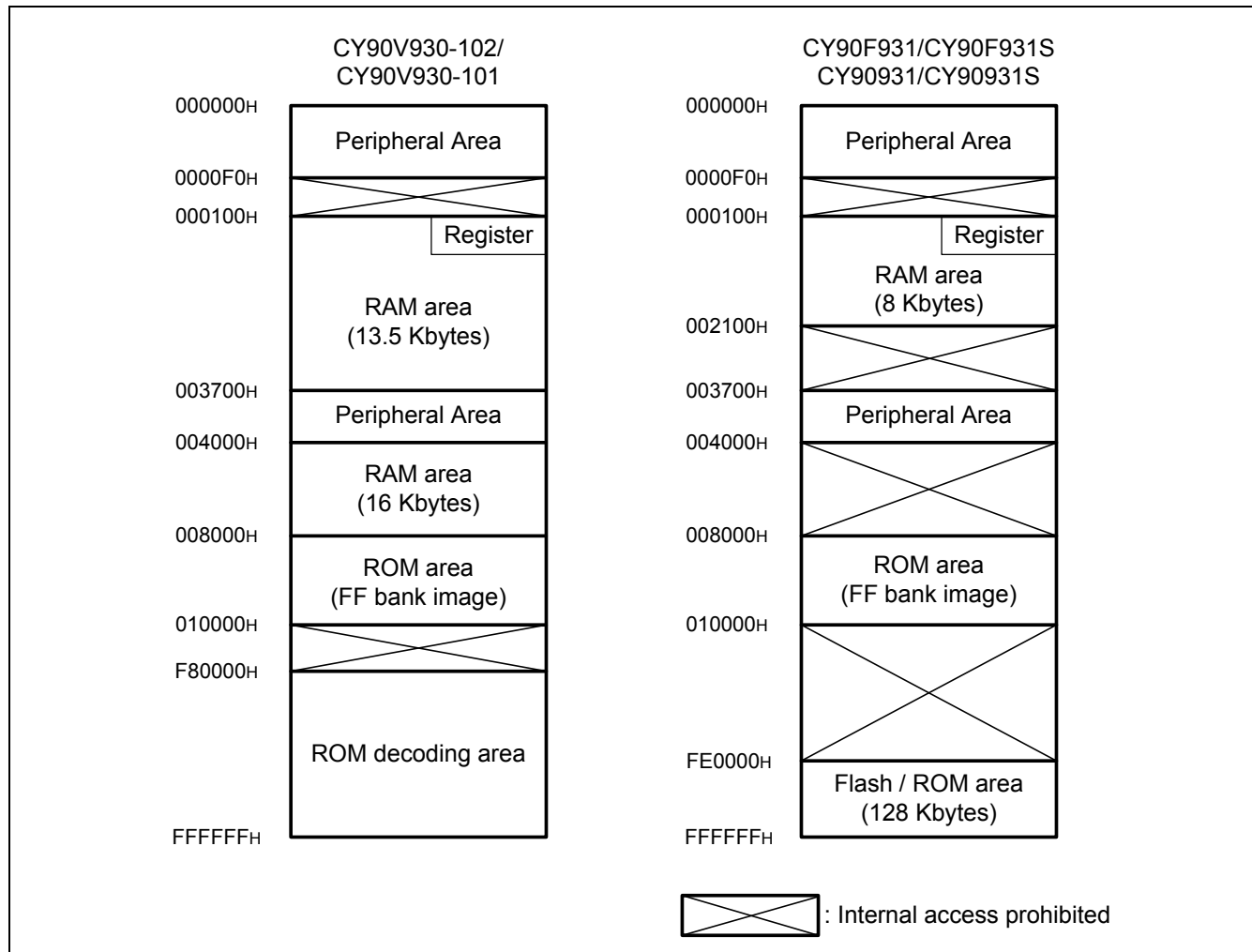
In the flash device and the mask ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

6. Block Diagram



7. Memory Map



Note: To select models without the ROM mirror function, refer to the "ROM Mirror Function Selection Module" in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the "far" modifier with the pointers. For example, when

an access is made to the address 00C000_H, the actual address to be accessed is FFC000_H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000_H to FFFFFFF_H appears in the image from 008000_H to 00FFF_H, it is recommended that ROM data tables be stored in the area from FF8000_H to FFFFFFF_H.

8. I/O Map

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
000000 _H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX _B
000001 _H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX _B
000002 _H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX _B
000003 _H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX _B
000004 _H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX _B
000005 _H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX _B
000006 _H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX _B
000007 _H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX _B
000008 _H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX _B
000009 _H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX _B
00000A _H , 00000B _H	(Disabled)				
00000C _H	Port C data register	PDRC	R/W	Port C	XXXXXXXX _B
00000D _H	Port D data register	PDRD	R/W	Port D	XXXXXXXX _B
00000E _H	Port E data register	PDRE	R/W	Port E	XXXXXXXX _B
00000F _H	(Disabled)				
000010 _H	Port 0 direction register	DDR0	R/W	Port 0	00000000 _B
000011 _H	Port 1 direction register	DDR1	R/W	Port 1	XX000000 _B
000012 _H	Port 2 direction register	DDR2	R/W	Port 2	000000XX _B
000013 _H	Port 3 direction register	DDR3	R/W	Port 3	00000000 _B
000014 _H	Port 4 direction register	DDR4	R/W	Port 4	00000000 _B
000015 _H	Port 5 direction register	DDR5	R/W	Port 5	00000000 _B
000016 _H	Port 6 direction register	DDR6	R/W	Port 6	00000000 _B
000017 _H	Port 7 direction register	DDR7	R/W	Port 7	00000000 _B
000018 _H	Port 8 direction register	DDR8	R/W	Port 8	00000000 _B
000019 _H	Port 9 direction register	DDR9	R/W	Port 9	X0000000 _B
00001A _H	Analog input enable	ADER6	R/W	Port 6, A/D	11111111 _B
00001B _H	Analog input enable	ADER7	R/W	Port7, A/D	11111111 _B
00001C _H	Port C direction register	DDRC	R/W	Port C	00000000 _B
00001D _H	Port D direction register	DDRD	R/W	Port D	X0000000 _B
00001E _H	Port E direction register	DDRE	R/W	Port E	XXXXX000 _B
00001F _H	Analog input enable	ADER8	R/W	Port8, A/D	11111111 _B
000020 _H	Lower A/D control status register	ADCS0	R/W	A/D converter	000XXXX0 _B
000021 _H	Higher A/D control status register	ADCS1	R/W		0000000X _B
000022 _H	Lower A/D data register	ADCR0	R		00000000 _B
000023 _H	Higher A/D data register	ADCR1	R		XXXXXX00 _B

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
000024 _H	Compare clear register	CPCLR	R/W	16-bit free-run timer	XXXXXXXX _B
000025 _H			R/W		XXXXXXXX _B
000026 _H	Timer data register	TCDT	R/W		00000000 _B
000027 _H			R/W		00000000 _B
000028 _H	Lower timer control status register	TCCSL	R/W		00000000 _B
000029 _H	Higher timer control status register	TCCSH	R/W		01X00000 _B
00002A _H	Lower PPG0 control status register	PCNTL0	R/W	16-bit PPG0	00000000 _B
00002B _H	Higher PPG0 control status register	PCNTH0	R/W		00000001 _B
00002C _H	Lower PPG1 control status register	PCNTL1	R/W	16-bit PPG1	00000000 _B
00002D _H	Higher PPG1 control status register	PCNTH1	R/W		00000001 _B
00002E _H	Lower PPG2 control status register	PCNTL2	R/W	16-bit PPG2	00000000 _B
00002F _H	Higher PPG2 control status register	PCNTH2	R/W		00000001 _B
000030 _H	External interrupt enable	ENIR	R/W	External interrupt	00000000 _B
000031 _H	External interrupt request	EIRR	R/W		00000000 _B
000032 _H	Lower external interrupt level	ELVRL	R/W		00000000 _B
000033 _H	Higher external interrupt level	ELVRH	R/W		00000000 _B
000034 _H	Serial mode register 0	SMR0	R/W, W	UART (LIN/SCI) 0	00000000 _B
000035 _H	Serial control register 0	SCR0	R/W, W		00000000 _B
000036 _H	Reception/transmission data register 0	RDR0/ TDR0	R/W		00000000 _B
000037 _H	Serial status register 0	SSR0	R/W, R		00001000 _B
000038 _H	Extended communication control register 0	ECCR0	R/W, R		000000XX _B
000039 _H	Extended status control register 0	ESCR0	R/W		00000100 _B
00003A _H	Baud rate generator register 00	BGR00	R/W		00000000 _B
00003B _H	Baud rate generator register 01	BGR01	R/W, R		00000000 _B
00003C _H to 000047 _H	(Disabled)				
000048 _H	Input capture input select register	ICISR	R/W	Input capture 0/1/2/3/4/5/6/7	00000000 _B
000049 _H	(Disabled)				
00004A _H to 00004F _H	(Disabled)				
000050 _H	Lower timer control status register 0	TMCSR0L	R/W	16-bit reload timer 0	00000000 _B
000051 _H	Higher timer control status register 0	TMCSR0H	R/W		XXX10000 _B
000052 _H	Timer register 0/reload register 0	TMR0/ TMRLR0	R/W		XXXXXXXX _B
000053 _H					XXXXXXXX _B
000054 _H	Lower timer control status register 1	TMCSR1L	R/W	16-bit reload timer 1	00000000 _B
000055 _H	Higher timer control status register 1	TMCSR1H	R/W		XXX10000 _B
000056 _H	Timer register 1/reload register 1	TMR1/ TMRLR1	R/W		XXXXXXXX _B
000057 _H					XXXXXXXX _B

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
000058 _H	LCD output control register 1	LOCR1	R/W	LCDC	1111111 _B
000059 _H	LCD output control register 2	LOCR2	R/W		0000000 _B
00005A _H	Lower sound control register 0	SGCRL0	R/W	Sound generator 0	0000000 _B
00005B _H	Higher sound control register 0	SGCRH0	R/W		0XXXX100 _B
00005C _H	Frequency data register 0	SGFR0	R/W		XXXXXXXX _B
00005D _H	Amplitude data register 0	SGAR0	R/W		0000000 _B
00005E _H	Decrement grade register 0	SGDR0	R/W		XXXXXXXX _B
00005F _H	Tone count register 0	SGTR0	R/W		XXXXXXXX _B
000060 _H	Input capture register 0	IPCP0	R	Input capture 0/1	XXXXXXXX _B
000061 _H					XXXXXXXX _B
000062 _H	Input capture register 1	IPCP1	R		XXXXXXXX _B
000063 _H					XXXXXXXX _B
000064 _H	Input capture register 2	IPCP2	R	Input capture 2/3	XXXXXXXX _B
000065 _H					XXXXXXXX _B
000066 _H	Input capture register 3	IPCP3	R		XXXXXXXX _B
000067 _H					XXXXXXXX _B
000068 _H	Input capture control status 0/1	ICS01	R/W	Input capture 0/1	0000000 _B
000069 _H	Input capture edge register 0/1	ICE01	R/W		XXX0X0XX _B
00006A _H	Input capture control status 2/3	ICS23	R/W	Input capture 2/3	0000000 _B
00006B _H	Input capture edge register 2/3	ICE23	R/W		XXXXXXXX _B
00006C _H	Lower LCD control register	LCRL	R/W	LCD controller/driver	0001000 _B
00006D _H	Higher LCD control register	LCRH	R/W		0000000 _B
00006E _H	Low voltage/CPU operation detection reset control register	LVRC	R/W	Low voltage/CPU operation detection reset	0011000 _B
00006F _H	ROM mirror	ROMM	W	ROM mirror	XXXXXXXX1 _B
000070 _H to 00007F _H	Area reserved for CAN Controller 1(See CAN Controllers).				
000080 _H	PWM control register 0	PWC0	R/W	Stepping motor controller 0	00000X0 _B
000081 _H	(Disabled)				
000082 _H	PWM control register 1	PWC1	R/W	Stepping motor controller 1	00000X0 _B
000083 _H	(Disabled)				
000084 _H	PWM control register 2	PWC2	R/W	Stepping motor controller 2	00000X0 _B
000085 _H	(Disabled)				
000086 _H	PWM control register 3	PWC3	R/W	Stepping motor controller 3	00000X0 _B
000087 _H	(Disabled)				
000088 _H	LCD output control register 3	LOCR3	R/W	LCDC	XXXXX111 _B
000089 _H	(Disabled)				

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
00008A _H	A/D setting register 0	ADSR0	R/W	A/D converter	00000000 _B
00008B _H	A/D setting register 1	ADSR1	R/W		00000000 _B
00008C _H	Port input level select 0	PIL0	R/W	Port input level select	00000000 _B
00008D _H	Port input level select 1	PIL1	R/W		XXXX0000 _B
00008E _H	Port input level select 2	PIL2	R/W		XXXX0000 _B
00008F _H to 00009D _H	(Disabled)				
00009E _H	Program address detection control register	PACSR	R/W	Address match detection	XXXX0X0X _B
00009F _H	Delayed Interrupt source generation /Release Register	DIRR	R/W	Delay interrupt	XXXXXXXX0 _B
0000A0 _H	Power saving mode control register	LPMCR	R/W	Power saving control circuit	00011000 _B
0000A1 _H	Clock select register	CKSCR	R/W, R		11111100 _B
0000A2 _H to 0000A7 _H	(Disabled)				
0000A8 _H	Watchdog timer control register	WDTC	R, W	Watchdog timer	XXXXX111 _B
0000A9 _H	Time-base timer control register	TBTC	R/W, W	Time-base timer	1XX00100 _B
0000AA _H	Watch timer control register	WTC	R/W, W, R	Watch timer (sub clock)	10001000 _B
0000AB _H to 0000AD _H	(Disabled)				
0000AE _H	Flash memory control status register	FMCS	R/W	Flash interface	000X0000 _B
0000AF _H	(Disabled)				
0000B0 _H	Interrupt control register 00	ICR00	R/W	Interrupt controller	00000111 _B
0000B1 _H	Interrupt control register 01	ICR01	R/W		00000111 _B
0000B2 _H	Interrupt control register 02	ICR02	R/W		00000111 _B
0000B3 _H	Interrupt control register 03	ICR03	R/W		00000111 _B
0000B4 _H	Interrupt control register 04	ICR04	R/W		00000111 _B
0000B5 _H	Interrupt control register 05	ICR05	R/W		00000111 _B
0000B6 _H	Interrupt control register 06	ICR06	R/W		00000111 _B
0000B7 _H	Interrupt control register 07	ICR07	R/W		00000111 _B
0000B8 _H	Interrupt control register 08	ICR08	R/W		00000111 _B
0000B9 _H	Interrupt control register 09	ICR09	R/W		00000111 _B
0000BA _H	Interrupt control register 10	ICR10	R/W		00000111 _B
0000BB _H	Interrupt control register 11	ICR11	R/W		00000111 _B
0000BC _H	Interrupt control register 12	ICR12	R/W		00000111 _B
0000BD _H	Interrupt control register 13	ICR13	R/W		00000111 _B
0000BE _H	Interrupt control register 14	ICR14	R/W		00000111 _B
0000BF _H	Interrupt control register 15	ICR15	R/W		00000111 _B
0000C0 _H to 0000C3 _H	(Disabled)				

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
0000C4 _H	Serial mode register 1	SMR1	R/W, W	UART (LIN/SCI) 1	00000000 _B
0000C5 _H	Serial control register 1	SCR1	R/W, W		00000000 _B
0000C6 _H	Reception/transmission data register 1	RDR1/TDR1	R/W		00000000 _B
0000C7 _H	Serial status register 1	SSR1	R/W, R		00001000 _B
0000C8 _H	Extended communication control register 1	ECCR1	R/W, R		000000XX _B
0000C9 _H	Extended status control register 1	ESCR1	R/W		00000100 _B
0000CA _H	Baud rate generator register 10	BGR10	R/W		00000000 _B
0000CB _H	Baud rate generator register 11	BGR11	R/W, R		00000000 _B
0000CC _H	Lower watch timer control register	WTCRL	R/W	Real-time watch timer	000XXXX0 _B
0000CD _H	Middle watch timer control register	WTCRM	R/W		00000000 _B
0000CE _H	Higher watch timer control register	WTCRH	R/W		XXXXXX00 _B
0000CF _H	PLL/Sub clock control register	PSCCR	W	PLL/Sub clock	XXXX0000 _B
0000D0 _H	Input capture control status 4/5	ICS45	R/W	Input capture 4/5	00000000 _B
0000D1 _H	Input capture edge register 4/5	ICE45	R/W, R		XXXXXXXX _B
0000D2 _H	Input capture control status 6/7	ICS67	R/W	Input capture 6/7	00000000 _B
0000D3 _H	Input capture edge register 6/7	ICE67	R/W, R		XXX0X0XX _B
0000D4 _H	Lower timer control status register 2	TMCSR2L	R/W	16-bit reload timer 2	00000000 _B
0000D5 _H	Higher timer control status register 2	TMCSR2H	R/W		XXX10000 _B
0000D6 _H	Lower timer control status register 3	TMCSR3L	R/W	16-bit reload timer 3	00000000 _B
0000D7 _H	Higher timer control status register 3	TMCSR3H	R/W		XXX10000 _B
0000D8 _H	Lower sound control register 1	SGCRL1	R/W	Sound generator 1	00000000 _B
0000D9 _H	Higher sound control register 1	SGCRH1	R/W		0XXXX100 _B
0000DA _H	Lower PPG3 control status register	PCNTL3	R/W	16-bit PPG3	00000000 _B
0000DB _H	Higher PPG3 control status register	PCNTH3	R/W		00000001 _B
0000DC _H	Lower PPG4 control status register	PCNTL4	R/W	16-bit PPG4	00000000 _B
0000DD _H	Higher PPG4 control status register	PCNTH4	R/W		00000001 _B
0000DE _H	Lower PPG5 control status register	PCNTL5	R/W	16-bit PPG5	00000000 _B
0000DF _H	Higher PPG5 control status register	PCNTH5	R/W		00000001 _B
0000E0 _H	Serial mode register 2	SMR2	R/W, W	UART (LIN/SCI) 2	00000000 _B
0000E1 _H	Serial control register 2	SCR2	R/W, W		00000000 _B
0000E2 _H	Reception/transmission data register 2	RDR2/TDR2	R/W		00000000 _B
0000E3 _H	Serial status register 2	SSR2	R/W, R		00001000 _B
0000E4 _H	Extended communication control register 2	ECCR2	R/W, R		000000XX _B
0000E5 _H	Extended status control register 2	ESCR2	R/W		00000100 _B
0000E6 _H	Baud rate generator register 20	BGR20	R/W		00000000 _B
0000E7 _H	Baud rate generator register 21	BGR21	R/W, R		00000000 _B

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
0000E8 _H	Serial mode register 3	SMR3	R/W, W	UART (LIN/SCI) 3	00000000 _B
0000E9 _H	Serial control register 3	SCR3	R/W, W		00000000 _B
0000EA _H	Reception/transmission data register 3	RDR3/TDR3	R/W		00000000 _B
0000EB _H	Serial status register 3	SSR3	R/W, R		00001000 _B
0000EC _H	Extended communication control register 3	ECCR3	R/W, R		000000XX _B
0000ED _H	Extended status control register 3	ESCR3	R/W		00000100 _B
0000EE _H	Baud rate generator register 30	BGR30	R/W		00000000 _B
0000EF _H	Baud rate generator register 31	BGR31	R/W, R		00000000 _B
001FF0 _H	Program address detection register 0	PADR0	R/W	Address match detection	XXXXXXXX _B
001FF1 _H	Program address detection register 1	PADR0	R/W		XXXXXXXX _B
001FF2 _H	Program address detection register 2	PADR0	R/W		XXXXXXXX _B
001FF3 _H	Program address detection register 3	PADR1	R/W		XXXXXXXX _B
001FF4 _H	Program address detection register 4	PADR1	R/W		XXXXXXXX _B
001FF5 _H	Program address detection register 5	PADR1	R/W		XXXXXXXX _B
003700 _H to 0037FF _H	(Disabled)				
003800 _H to 0038FF _H	(Disabled)				
003900 _H to 00391F _H	(Disabled)				
003920 _H	PPG0 down counter register	PDCR0	R	16-bit PPG0	11111111 _B
003921 _H					11111111 _B
003922 _H	PPG0 cycle setting register	PCSR0	W		11111111 _B
003923 _H					11111111 _B
003924 _H	PPG0 duty setting register	PDUT0	W		00000000 _B
003925 _H					00000000 _B
003926 _H	PPG0 output division setting register	PPGDIV0	R/W, R		11111100 _B
003927 _H	(Disabled)				
003928 _H	PPG1 down counter register	PDCR1	R	16-bit PPG1	11111111 _B
003929 _H					11111111 _B
00392A _H	PPG1 cycle setting register	PCSR1	W		11111111 _B
00392B _H					11111111 _B
00392C _H	PPG1 duty setting register	PDUT1	W		00000000 _B
00392D _H					00000000 _B
00392E _H	PPG1 output division setting register	PPGDIV1	R/W, R		11111100 _B
00392F _H	(Disabled)				

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
003930 _H	PPG2 down counter register	PDCR2	R	16-bit PPG2	11111111 _B
003931 _H					11111111 _B
003932 _H	PPG2 cycle setting register	PCSR2	W		11111111 _B
003933 _H					11111111 _B
003934 _H	PPG2 duty setting register	PDUT2	W		00000000 _B
003935 _H					00000000 _B
003936 _H	PPG2 output division setting register	PPGDIV2	R/W, R		11111100 _B
003937 _H to 00393F _H	(Disabled)				
003940 _H	Input capture register 4	IPCP4	R	Input capture 4/5	XXXXXXXX _B
003941 _H					XXXXXXXX _B
003942 _H	Input capture register 5	IPCP5	R		XXXXXXXX _B
003943 _H					XXXXXXXX _B
003944 _H	Input capture register 6	IPCP6	R	Input capture 6/7	XXXXXXXX _B
003945 _H					XXXXXXXX _B
003946 _H	Input capture register 7	IPCP7	R		XXXXXXXX _B
003947 _H					XXXXXXXX _B
003948 _H to 00394F _H	(Disabled)				
003950 _H	Timer register 2/Reload register 2	TMR2/ TMRLR2	R/W	16-bit reload timer 2	XXXXXXXX _B
003951 _H					XXXXXXXX _B
003952 _H	Timer register 3/Reload register 3	TMR3/ TMRLR3	R/W	16-bit reload timer 3	XXXXXXXX _B
003953 _H					XXXXXXXX _B
003954 _H to 003957 _H	(Disabled)				
003958 _H	Sub second data register	WTBR	R/W	Real time watch timer	XXXXXXXX _B
003959 _H					XXXXXXXX _B
00395A _H					XXXXXXXX _B
00395B _H	Second data register	WTSR	R/W		XX000000 _B
00395C _H	Minute data register	WTMR	R/W		XX000000 _B
00395D _H	Hour data register	WTHR	R/W		XXX00000 _B
00395E _H	Day data register	WTDR	R/W		00X00001 _B
00395F _H	(Disabled)				

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
003960 _H	LCD display RAM	VRAM	R/W	LCD controller/driver	XXXXXXXX _B
003961 _H					XXXXXXXX _B
003962 _H					XXXXXXXX _B
003963 _H					XXXXXXXX _B
003964 _H					XXXXXXXX _B
003965 _H					XXXXXXXX _B
003966 _H					XXXXXXXX _B
003967 _H					XXXXXXXX _B
003968 _H					XXXXXXXX _B
003969 _H					XXXXXXXX _B
00396A _H					XXXXXXXX _B
00396B _H					XXXXXXXX _B
00396C _H					XXXXXXXX _B
00396D _H					XXXXXXXX _B
00396E _H					XXXXXXXX _B
00396F _H					XXXXXXXX _B
003970 _H to 003973 _H	(Disabled)				
003974 _H	Frequency data register 1	SGFR1	R/W	Sound generator 1	XXXXXXXX _B
003975 _H	Amplitude data register 1	SGAR1	R/W		00000000 _B
003976 _H	Decrement grade register 1	SGDR1	R/W		XXXXXXXX _B
003977 _H	Tone count register 1	SGTR1	R/W		XXXXXXXX _B
003978 _H to 00397F _H	(Disabled)				
003980 _H	PWM1 compare register 0	PWC10	R/W	Stepping motor controller 0	XXXXXXXX _B
003981 _H					XXXXXXXX _B
003982 _H	PWM2 compare register 0	PWC20	R/W		XXXXXXXX _B
003983 _H					XXXXXXXX _B
003984 _H	PWM1 select register 0	PWS10	R/W		00000000 _B
003985 _H	PWM2 select register 0	PWS20	R/W		X0000000 _B
003986 _H , 003987 _H	(Disabled)				
003988 _H	PWM1 compare register 1	PWC11	R/W	Stepping motor controller 1	XXXXXXXX _B
003989 _H					XXXXXXXX _B
00398A _H	PWM2 compare register 1	PWC21	R/W		XXXXXXXX _B
00398B _H					XXXXXXXX _B
00398C _H	PWM1 select register 1	PWS11	R/W		00000000 _B
00398D _H	PWM2 select register 1	PWS21	R/W		X0000000 _B
00398E _H , 00398F _H	(Disabled)				

Address	Register Name	Symbol	Read/Write	Resource Name	Initial Value
003990 _H	PWM1 compare register 2	PWC12	R/W	Stepping motor controller 2	XXXXXXXX _B
003991 _H					XXXXXXXX _B
003992 _H	PWM2 compare register 2	PWC22	R/W		XXXXXXXX _B
003993 _H					XXXXXXXX _B
003994 _H	PWM1 select register 2	PWS12	R/W		00000000 _B
003995 _H	PWM2 select register 2	PWS22	R/W		X0000000 _B
003996 _H , 003997 _H	(Disabled)				
003998 _H	PWM1 compare register 3	PWC13	R/W	Stepping motor controller 3	XXXXXXXX _B
003999 _H					XXXXXXXX _B
00399A _H	PWM2 compare register 3	PWC23	R/W		XXXXXXXX _B
00399B _H					XXXXXXXX _B
00399C _H	PWM1 select register 3	PWS13	R/W		00000000 _B
00399D _H	PWM2 select register 3	PWS23	R/W		X0000000 _B
00399E _H to 0039A5 _H	(Disabled)				
0039A6 _H	Flash write control register 0	FWR0	R/W	Flash I/F	00000000 _B
0039A7 _H	Flash write control register 1	FWR1			00000000 _B
0039A8 _H to 0039BF _H	(Disabled)				
0039C0 _H to 0039DF _H	(Disabled)				
0039E0 _H to 0039FF _H	(Disabled)				
003A00 _H to 003AFF _H	(Disabled)				
003B00 _H to 003BFF _H	Area reserved for CAN Controller 1(See CAN Controllers).				
003C00 _H to 003CFF _H	(Disabled)				
003D00 _H to 003DFF _H	Area reserved for CAN Controller 1(See CAN Controllers).				
003E00 _H to 003EFF _H	(Disabled)				
003F00 _H to 003FFF _H	(Disabled)				

9. CAN Controllers

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers

- 29-bit ID and 8-byte data
- Multi-level message buffer configuration

- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

Table 1: List of Control Registers(1)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003D00 _H	Control status register	CSR	R/W, R	00---000 _B
003D01 _H				0----0-1 _B
003D02 _H	Last event indicator register	LEIR	R/W	----- _B
003D03 _H				000-0000 _B
003D04 _H	RX/TX error counter	RTEC	R	00000000 _B
003D05 _H				00000000 _B
003D06 _H	Bit timing register	BTR	R/W	-1111111 _B
003D07 _H				11111111 _B

Table 2: List of Control Registers(2)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
000070 _H	Message buffer valid register	BVALR	R/W	00000000 _B
000071 _H				00000000 _B
000072 _H	Transmit request register	TREQR	R/W	00000000 _B
000073 _H				00000000 _B
000074 _H	Transmit cancel register	TCANR	W	00000000 _B
000075 _H				00000000 _B
000076 _H	Transmit complete register	TCR	R/W	00000000 _B
000077 _H				00000000 _B
000078 _H	Receive complete register	RCR	R/W	00000000 _B
000079 _H				00000000 _B
00007A _H	Remote request receive register	RRTRR	R/W	00000000 _B
00007B _H				00000000 _B
00007C _H	Receive overrun register	ROVRR	R/W	00000000 _B
00007D _H				00000000 _B
00007E _H	Receive interrupt enable register	RIER	R/W	00000000 _B
00007F _H				00000000 _B
003D08 _H	IDE register	IDER	R/W	XXXXXXXX _B
003D09 _H				XXXXXXXX _B

Table 2: List of Control Registers(2)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003D0A _H	Transmit RTR register	TRTRR	R/W	00000000 _B
003D0B _H				00000000 _B
003D0C _H	Remote frame receive wait register	RFWTR	R/W	XXXXXXXX _B
003D0D _H				XXXXXXXX _B
003D0E _H	Transmit interrupt enable register	TIER	R/W	00000000 _B
003D0F _H				00000000 _B
003D10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX _B
003D11 _H				XXXXXXXX _B
003D12 _H				XXXXXXXX _B
003D13 _H				XXXXXXXX _B
003D14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX _B
003D15 _H				XXXXXXXX _B
003D16 _H				XXXXXX--- _B
003D17 _H				XXXXXXXX _B
003D18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX _B
003D19 _H				XXXXXXXX _B
003D1A _H				XXXXXX--- _B
003D1B _H				XXXXXXXX _B

Table 3: List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003B00 _H to 003B1F _H	General-purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
003B20 _H	ID register 0	IDR0	R/W	XXXXXXXX _B
003B21 _H				XXXXXXXX _B
003B22 _H				XXXXXX--- _B
003B23 _H				XXXXXXXX _B
003B24 _H	ID register 1	IDR1	R/W	XXXXXXXX _B
003B25 _H				XXXXXXXX _B
003B26 _H				XXXXXX--- _B
003B27 _H				XXXXXXXX _B
003B28 _H	ID register 2	IDR2	R/W	XXXXXXXX _B
003B29 _H				XXXXXXXX _B
003B2A _H				XXXXXX--- _B
003B2B _H				XXXXXXXX _B

Table 3: List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003B2C _H	ID register 3	IDR3	R/W	XXXXXXXX _B
003B2D _H				XXXXXXXX _B
003B2E _H				XXXXXX--- _B
003B2F _H				XXXXXXXX _B
003B30 _H	ID register 4	IDR4	R/W	XXXXXXXX _B
003B31 _H				XXXXXXXX _B
003B32 _H				XXXXXX--- _B
003B33 _H				XXXXXXXX _B
003B34 _H	ID register 5	IDR5	R/W	XXXXXXXX _B
003B35 _H				XXXXXXXX _B
003B36 _H				XXXXXX--- _B
003B37 _H				XXXXXXXX _B
003B38 _H	ID register 6	IDR6	R/W	XXXXXXXX _B
003B39 _H				XXXXXXXX _B
003B3A _H				XXXXXX--- _B
003B3B _H				XXXXXXXX _B
003B3C _H	ID register 7	IDR7	R/W	XXXXXXXX _B
003B3D _H				XXXXXXXX _B
003B3E _H				XXXXXX--- _B
003B3F _H				XXXXXXXX _B
003B40 _H	ID register 8	IDR8	R/W	XXXXXXXX _B
003B41 _H				XXXXXXXX _B
003B42 _H				XXXXXX--- _B
003B43 _H				XXXXXXXX _B
003B44 _H	ID register 9	IDR9	R/W	XXXXXXXX _B
003B45 _H				XXXXXXXX _B
003B46 _H				XXXXXX--- _B
003B47 _H				XXXXXXXX _B
003B48 _H	ID register 10	IDR10	R/W	XXXXXXXX _B
003B49 _H				XXXXXXXX _B
003B4A _H				XXXXXX--- _B
003B4B _H				XXXXXXXX _B
003B4C _H	ID register 11	IDR11	R/W	XXXXXXXX _B
003B4D _H				XXXXXXXX _B
003B4E _H				XXXXXX--- _B
003B4F _H				XXXXXXXX _B

Table 3: List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003B50 _H	ID register 12	IDR12	R/W	XXXXXXXX _B
003B51 _H				XXXXXXXX _B
003B52 _H				XXXXXX--- _B
003B53 _H				XXXXXXXX _B
003B54 _H	ID register 13	IDR13	R/W	XXXXXXXX _B
003B55 _H				XXXXXXXX _B
003B56 _H				XXXXXX--- _B
003B57 _H				XXXXXXXX _B
003B58 _H	ID register 14	IDR14	R/W	XXXXXXXX _B
003B59 _H				XXXXXXXX _B
003B5A _H				XXXXXX--- _B
003B5B _H				XXXXXXXX _B
003B5C _H	ID register 15	IDR15	R/W	XXXXXXXX _B
003B5D _H				XXXXXXXX _B
003B5E _H				XXXXXX--- _B
003B5F _H				XXXXXXXX _B

Table 4: List of Message Buffers (DLC Registers)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003B60 _H	DLC register 0	DLCR0	R/W	----XXXX _B
003B61 _H				
003B62 _H	DLC register 1	DLCR1	R/W	----XXXX _B
003B63 _H				
003B64 _H	DLC register 2	DLCR2	R/W	----XXXX _B
003B65 _H				
003B66 _H	DLC register 3	DLCR3	R/W	----XXXX _B
003B67 _H				
003B68 _H	DLC register 4	DLCR4	R/W	----XXXX _B
003B69 _H				
003B6A _H	DLC register 5	DLCR5	R/W	----XXXX _B
003B6B _H				
003B6C _H	DLC register 6	DLCR6	R/W	----XXXX _B
003B6D _H				
003B6E _H	DLC register 7	DLCR7	R/W	----XXXX _B
003B6F _H				
003B70 _H	DLC register 8	DLCR8	R/W	----XXXX _B
003B71 _H				

Table 4: List of Message Buffers (DLC Registers)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003B72 _H	DLC register 9	DLCR9	R/W	----XXXX _B
003B73 _H				
003B74 _H	DLC register 10	DLCR10	R/W	----XXXX _B
003B75 _H				
003B76 _H	DLC register 11	DLCR11	R/W	----XXXX _B
003B77 _H				
003B78 _H	DLC register 12	DLCR12	R/W	----XXXX _B
003B79 _H				
003B7A _H	DLC register 13	DLCR13	R/W	----XXXX _B
003B7B _H				
003B7C _H	DLC register 14	DLCR14	R/W	----XXXX _B
003B7D _H				
003B7E _H	DLC register 15	DLCR15	R/W	----XXXX _B
003B7F _H				

Table 5: List of Message Buffers (Data register)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003B80 _H to 003B87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
003B88 _H to 003B8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003B90 _H to 003B97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003B98 _H to 003B9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
003BA0 _H to 003BA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
003BA8 _H to 003BAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
003BB0 _H to 003BB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
003BB8 _H to 003BBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B

Table 5: List of Message Buffers (Data register)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
003BC0 _H to 003BC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
003BC8 _H to 003BCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
003BD0 _H to 003BD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
003BD8 _H to 003BDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
003BE0 _H to 003BE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
003BE8 _H to 003BEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
003BF0 _H to 003BF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
003BF8 _H to 003BFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

10. Interrupt Sources, Interrupt Vectors, And Interrupt Control Registers

Interrupt Source	EI ² OS Corresponding	Interrupt Vector			Interrupt Control Register		Priority ^{*1}
		Number		Address	ICR	Address	
Reset	×	#08	08 _H	FFFFDC _H	—	—	High ↑ ↓ Low
INT9 instruction	×	#09	09 _H	FFFFD8 _H	—	—	
Exception processing	×	#10	0A _H	FFFFD4 _H	—	—	
—	×	#11	0B _H	FFFFD0 _H	ICR00	0000B0 _H	
—	×	#12	0C _H	FFFFCC _H			
CAN1 received	×	#13	0D _H	FFFFC8 _H	ICR01	0000B1 _H ^{*2}	
CAN1 transmitted/node status/	×	#14	0E _H	FFFFC4 _H			
Input capture 0	△	#15	0F _H	FFFFC0 _H	ICR02	0000B2 _H ^{*2}	
DTP/ external interrupt - ch.0/ch.1 detected	△	#16	10 _H	FFFFBC _H			
Reload timer 0	△	#17	11 _H	FFFFB8 _H	ICR03	0000B3 _H ^{*2}	
Reload timer 2	△	#18	12 _H	FFFFB4 _H			
Input capture 1	△	#19	13 _H	FFFFB0 _H	ICR04	0000B4 _H ^{*2}	
DTP/ external interrupt - ch.2/ch.3 detected	△	#20	14 _H	FFFFAC _H			
Input capture 2	△	#21	15 _H	FFFFA8 _H	ICR05	0000B5 _H ^{*2}	
Reload timer 3	△	#22	16 _H	FFFFA4 _H			
Input capture 3/4/5/6/7	△	#23	17 _H	FFFFA0 _H	ICR06	0000B6 _H ^{*2}	
DTP/ external interrupt - ch.4/ ch.5 detected UART3 RX	△	#24	18 _H	FFFF9C _H			
PPG timer 0	△	#25	19 _H	FFFF98 _H	ICR07	0000B7 _H ^{*2}	
DTP/ external interrupt - ch.6/ ch.7 detected UART3 TX	△	#26	1A _H	FFFF94 _H			
PPG timer 1	△	#27	1B _H	FFFF90 _H	ICR08	0000B8 _H ^{*2}	
Reload timer 1	△	#28	1C _H	FFFF8C _H			
PPG timer 2/3/4/5	○	#29	1D _H	FFFF88 _H	ICR09	0000B9 _H ^{*2}	
Real time watch timer / Watch timer (Sub clock)	×	#30	1E _H	FFFF84 _H			
Free-run timer overflow/clear	×	#31	1F _H	FFFF80 _H	ICR10	0000BA _H ^{*2}	
A/D converter conversion complete	○	#32	20 _H	FFFF7C _H			
Sound generator 0/1	×	#33	21 _H	FFFF78 _H	ICR11	0000BB _H ^{*2}	
Time-base timer	×	#34	22 _H	FFFF74 _H			
UART2 RX	○	#35	23 _H	FFFF70 _H	ICR12	0000BC _H ^{*2}	
UART2 TX	△	#36	24 _H	FFFF6C _H			

Interrupt Source	EI ² OS Corresponding	Interrupt Vector			Interrupt Control Register		Priority ^{*1}
		Number		Address	ICR	Address	
UART 1 RX	◎	#37	25 _H	FFFF68 _H	ICR13	0000BD _H ^{*2}	High ↑ ↕ ↓ Low
UART 1 TX	△	#38	26 _H	FFFF64 _H			
UART 0 RX	◎	#39	27 _H	FFFF60 _H	ICR14	0000BE _H ^{*2}	
UART 0 TX	△	#40	28 _H	FFFF5C _H			
Flash memory status	×	#41	29 _H	FFFF58 _H	ICR15	0000BF _H ^{*2}	
Delay interrupt generator module	×	#42	2A _H	FFFF54 _H			

*1: Priority applies when interrupts of the same level are generated.

*2:

Peripheral functions that share the ICR register have the same interrupt level.

If the extended intelligent I/O service (EI²OS) is used with peripheral functions that share the ICR register, only one of the peripheral functions that share the register can be used.

When the extended intelligent I/O service (EI²OS) is specified or one of the peripheral functions that shares the ICR register, interrupts cannot be used from the other peripheral functions that share the register.

⊙ : Usable, and has extended intelligent I/O services (EI²OS) stop function

○ : Usable

△ : Usable when interrupt sources sharing ICR are not in use

× : Unusable

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage ^{*1}	V _{CC}	V _{SS} - 0.3	V _{SS} + 6.0	V	
	AV _{CC}	V _{SS} - 0.3	V _{SS} + 6.0	V	AV _{CC} = V _{CC} ^{*2}
	AVRH	V _{SS} - 0.3	V _{SS} + 6.0	V	AV _{CC} ≥ AVRH ^{*2}
	DV _{CC}	V _{SS} - 0.3	V _{SS} + 6.0	V	DV _{CC} = V _{CC} ^{*2}
Input voltage ^{*1}	V _I	V _{SS} - 0.3	V _{CC} + 0.3	V	^{*3}
Output voltage ^{*1}	V _O	V _{SS} - 0.3	V _{CC} + 0.3	V	
Maximum clamp current	I _{CLAMP}	- 4	+ 4	mA	^{*4}
Total maximum clamp current	Σ I _{CLAMP}	—	40	mA	^{*4}
“L” level maximum output current ^{*5}	I _{OL1}	—	15	mA	Except P70 to P77 and P80 to P87
	I _{OL2}	—	40	mA	P70 to P77 and P80 to P87
“L” level average output current ^{*6}	I _{OLAV1}	—	4	mA	Except P70 to P77 and P80 to P87
	I _{OLAV2}	—	30	mA	P70 to P77 and P80 to P87
“L” level maximum total output current	Σ I _{OL1}	—	100	mA	Except P70 to P77 and P80 to P87
	Σ I _{OL2}	—	330	mA	P70 to P77 and P80 to P87
“L” level average total output current	Σ I _{OLAV1}	—	50	mA	Except P70 to P77 and P80 to P87
	Σ I _{OLAV2}	—	250	mA	P70 to P77 and P80 to P87
“H” level maximum output current	I _{OH1} ^{*5}	—	-15	mA	Except P70 to P77 and P80 to P87
	I _{OH2} ^{*5}	—	-40	mA	P70 to P77 and P80 to P87

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
“H” level average output current	I_{OHAV1}^{*6}	—	–4	mA	Except P70 to P77 and P80 to P87
	I_{OHAV2}^{*6}	—	–30	mA	P70 to P77 and P80 to P87
“H” level maximum total output current	ΣI_{OH1}	—	–100	mA	Except P70 to P77 and P80 to P87
	ΣI_{OH2}	—	–330	mA	P70 to P77 and P80 to P87
“H” level average total output current	ΣI_{OHAV1}^{*7}	—	–50	mA	Except P70 to P77 and P80 to P87
	ΣI_{OHAV2}^{*7}	—	–250	mA	P70 to P77 and P80 to P87
Power consumption	P_D	—	490	mW	
Operating temperature	T_A	– 40	+ 105	°C	
Storage temperature	T_{STG}	– 55	+ 150	°C	

*1: The parameter is based on VSS = AVSS = DVSS = 0.0 V.

*2: AVCC, AVRH must not exceed VCC, and AVRH must not exceed AVCC.

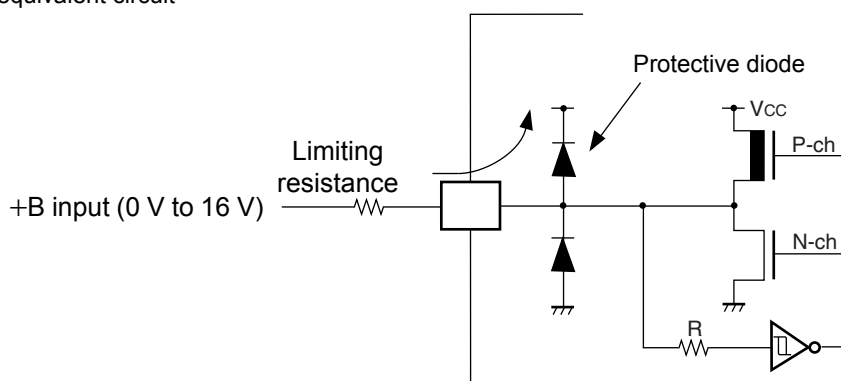
When using an evaluation product, DVCC must not exceed VCC (however, DVCC can be set to a higher voltage than VCC when using a Flash memory product/Mask ROM product).

*3: If the input current or the maximum input current is limited using external components, ICLAMP is the applicable rating instead of VI.

*4:

- Applicable to pins: P00 to P07, P10 to P15, P22 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the microcontroller may partially malfunction on power supplied through the +B signal pin.
- Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
- Care must be taken not to leave +B input pins open.
- Note that analog system input/output pins (LCD common pins, comparator input pins, etc.) cannot accept +B signal inputs.
- Sample recommended circuit:

■ Input/output equivalent circuit



*5: Maximum output current is defined as the peak value of current through any one of the corresponding pins

*6: Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

*7: Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.

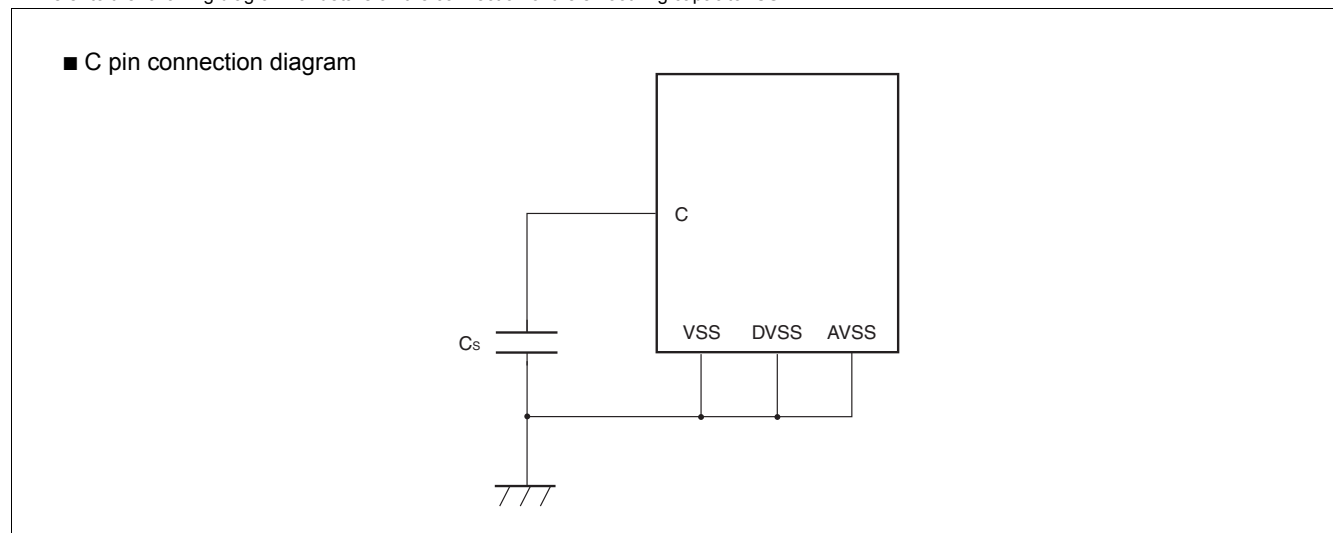
WARNING Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

11.2 Recommended Operating Conditions

$(V_{SS} = DV_{SS} = AV_{SS} = 0.0 \text{ V})$

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}, AV_{CC}, DV_{CC}	3.7	5.5	V	The low voltage detection reset operates when the power supply voltage reaches $4.0 \text{ V} \pm 0.3 \text{ V}$.
		3.7	5.5	V	Maintain stop operation status The low voltage detection reset operates when the power supply voltage reaches $4.0 \text{ V} \pm 0.3 \text{ V}$.
Smoothing capacitor ^{*1}	C_S	0.1	1.0	μF	Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the VCC pin.
Operating temperature	T_A	- 40	+ 105	$^{\circ}\text{C}$	

*1: Refer to the following diagram for details on the connection of the smoothing capacitor C_S .



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

11.3 DC Characteristics

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	V_{IHA}	—	—	$0.8 V_{CC}$	—	—	V	Pin inputs if Automotive input levels are selected
	V_{IHS}	—	—	$0.8 V_{CC}$	—	—	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{IHC}	—	—	$0.7 V_{CC}$	—	—	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
“L” level input voltage	V_{ILA}	—	—	—	—	$0.5 V_{CC}$	V	Pin inputs if Automotive input levels are selected
	V_{ILS}	—	—	—	—	$0.2 V_{CC}$	V	Pin inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	—	—	$0.3 V_{CC}$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
Power supply current ^{*1}	I_{CC}	V_{CC}	Maximum operating frequency $F_{CP} = 32 \text{ MHz}$, normal operation	—	30	40	mA	
			Maximum operating frequency $F_{CP} = 32 \text{ MHz}$, writing Flash memory	—	40	55	mA	
	I_{CCS}		Operating frequency $F_{CP} = 32 \text{ MHz}$, sleep mode	—	12	20	mA	
	I_{CTS}		Operating frequency $F_{CP} = 2 \text{ MHz}$, time-base timer mode	—	0.6	1.0	mA	
	I_{CTSPLL}		Operating frequency $F_{CP} = 32 \text{ MHz}$, PLL timer mode, External frequency = 4 MHz	—	2.5	4	mA	
	I_{CCL}		Operating frequency $F_{CP} = 8 \text{ kHz}$, $T_A = +25^\circ\text{C}$, Sub clock operation	—	170	340	μA	
	I_{CCLS}		Operating frequency $F_{CP} = 8 \text{ kHz}$, $T_A = +25^\circ\text{C}$, Sub sleep operation	—	—	270	μA	
	I_{CCT}		Operating frequency $F_{CP} = 8 \text{ kHz}$, $T_A = +25^\circ\text{C}$, Watch mode	—	—	250	μA	
	I_{CCH}		$T_A = +25^\circ\text{C}$, Stop mode	—	—	170	μA	
Input leakage current	I_{IL}	All input pins	$V_{CC} = DV_{CC} = AV_{CC} = 5.5 \text{ V}$, $V_{SS} < V_I < V_{CC}$	—	—	10	μA	

(V_{CC} = 5.0 V ±10%, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V, T_A = -40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input capacitance 1	C _{IN1}	All pins except VCC, VSS, DVCC, DVSS, AVCC, AVSS, C, P70 to P77, P80 to P87	—	—	—	15	pF	
Input capacitance 2	C _{IN2}	P70 to P77, P80 to P87	—	—	—	45	pF	
Pull-up resistance	R _{UP}	RST	—	—	—	100	kΩ	
Pull-down resistance	R _{DOWN}	MD2	—	—	—	100	kΩ	Excluding Flash memory product
General-purpose output “H” voltage	V _{OH1}	All pins except P70 to P77, P80 to P87	V _{CC} = 4.5 V, I _{OH} = -4.0 mA	V _{CC} - 0.5	—	—	V	
Stepping motor output “H” voltage	V _{OH2}	P70 to P77, P80 to P87	V _{CC} = 4.5 V, I _{OH} = -30.0 mA	V _{CC} - 0.5	—	—	V	
General-purpose output “L” voltage	V _{OL1}	All pins except P70 to P77, P80 to P87	V _{CC} = 4.5 V, I _{OL} = 4.0 mA	—	—	0.4	V	
Stepping motor output “L” voltage	V _{OL2}	P70 to P77, P80 to P87	V _{CC} = 4.5 V, I _{OL} = 30.0 mA	—	—	0.55	V	
Stepping motor output phase variation “H”	ΔV _{OH}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V _{CC} = 4.5 V, I _{OH} = -30.0 mA, maximum deviation V _{OH2}	—	—	90	mV	
Stepping motor output phase variation “L”	ΔV _{OL}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3	V _{CC} = 4.5 V, I _{OL} = 30.0 mA, maximum deviation V _{OL2}	—	—	90	mV	
LCD internal divider resistance	R _{LCD}	Between V0 and V1, Between V1 and V2, Between V2 and V3	—	6.25	12.5	25	kΩ	Evaluation
				8.75	12.5	17.0	kΩ	Flash/Mask ROM
LCDC leakage current	I _{LCDC}	V0 to V3, COMm (m = 0 to 3), SEGn, (n = 00 to 31)	—	—	—	5.0	μA	

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
LCD output impedance	Rvcom	COMn (n = 0 to 3)	—	—	—	4.5	k Ω	
	Rvseg	SEGn (n = 00 to 31)	—	—	—	17	k Ω	

*1: Power supply current values are assumed by an external clock supplied from the X1 pin. Users must be aware that power supply current levels differ depending on whether an external clock or oscillator is used.

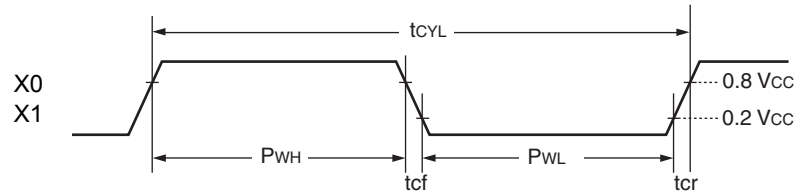
11.4 AC Characteristics

11.4.1 Clock Timing

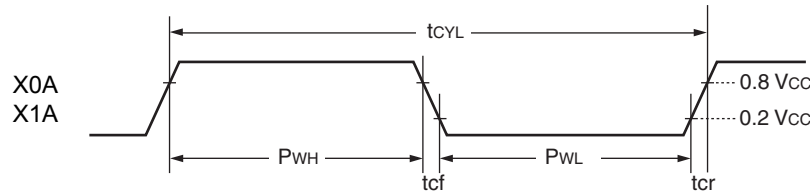
($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Pin Name	Condi- tions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	1/2 (PLL stopped) When using the oscillator circuit
				4	—	32	MHz	PLL multiplied by 1
				3	—	16	MHz	PLL multiplied by 2
				3	—	10.7	MHz	PLL multiplied by 3
				3	—	8	MHz	PLL multiplied by 4
				3	—	5.33	MHz	PLL multiplied by 6
				3	—	4	MHz	PLL multiplied by 8
	F_{LC}	X0A, X1A		—	32.768	—	kHz	
Clock cycle time	t_{CYL}	X0, X1		62.5	—	333	ns	
	t_{LCYL}	X0A, X1A		—	30.5	—	μs	
Internal operating clock frequency	F_{CP}	—		1.5	—	32	MHz	Using main clock (PLL clock)
	F_{LCP}	—		—	8.192	—	kHz	Using sub clock
Internal operating clock cycle time	t_{CP}	—		31.25	—	666	ns	Using main clock (PLL clock)
	t_{LCP}	—		—	122.1	—	μs	Using sub clock

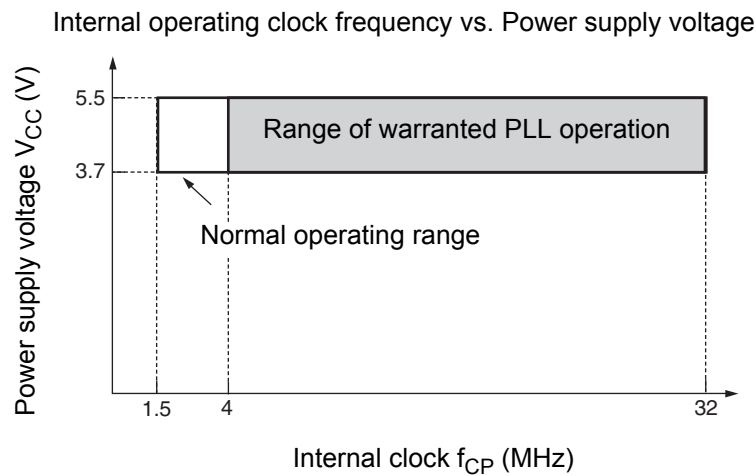
■ X0, X1 clock timing



■ X0A, X1A clock timing

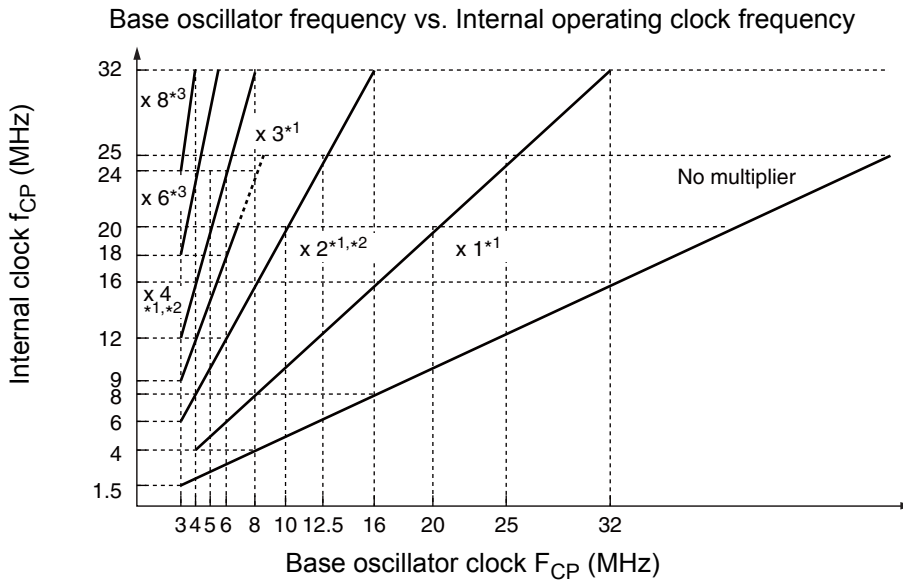


■ Guaranteed PLL Operation Range



Notes:

- For PLL 1 × only, use with $t_{cp} = 4$ MHz or greater.
- Refer to “11.5. A/D Converter (1) Electrical Characteristics” for details on the A/D converter operating frequency.



*1: When the PLL multiplier is $\times 1$, $\times 2$, $\times 3$ or $\times 4$ and the internal clock is $20 \text{ MHz} < f_{CP} \leq 32 \text{ MHz}$, set DIV2 bit = "1"*4, CS2 bit = "1" in the PSCCR register.

[Example] When using a base oscillator frequency of 24 MHz at PLL $\times 1$:

CKSCR register : CS1 bit = "0", CS0 bit = "0"

PSCCR register : DIV2 bit = "1"*4, CS2 bit = "1"

[Example] When using a base oscillator frequency of 6 MHz at PLL $\times 3$:

CKSCR register : CS1 bit = "1", CS0 bit = "0"

PSCCR register : DIV2 bit = "1"*4, CS2 bit = "1"

*2: When the PLL multiplier is $\times 2$ or $\times 4$ and the internal clock is $20 \text{ MHz} < f_{CP} \leq 32 \text{ MHz}$, the following settings are also supported.

PLL $\times 2$: CKSCR register : CS1 bit = "0", CS0 bit = "0"

PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"

PLL $\times 4$: CKSCR register : CS1 bit = "0", CS0 bit = "1"

PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"

*3: When the PLL multiplier is set to $\times 6$ or $\times 8$, set "DIV2 bit = "0"*4 CS2 bit = "1" and "PLL2 bit = 1" in the PSCCR register.

[Example] When using a base oscillator frequency of 4 MHz at PLL $\times 6$:

CKSCR register : CS1 bit = "1", CS0 bit = "0"

PSCCR register : DIV2 bit = "0"*4, CS2 bit = "1"

[Example] When using a base oscillator frequency of 3 MHz at PLL $\times 8$:

CKSCR register : CS1 bit = "1", CS0 bit = "1"

PSCCR register : DIV2 bit = "0"*4, CS2 bit = "1"

Note: The DIV2 bit is assigned to bit 9 of the PSCCR register and the CS2 bit is assigned to bit 8 of the PSCCR register. Both bits have a default value of "0".

11.4.2 Reset Input

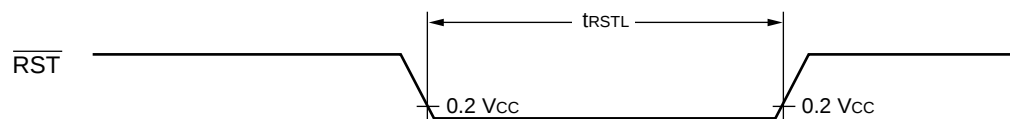
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	RST	10	—	μs	During normal operation
			Oscillator oscillation time ¹ + $100\text{ }\mu\text{s}$	—	ms	In stop mode
			100	—	μs	In time-base timer mode
Width of Reset input removal			1	—	μs	—

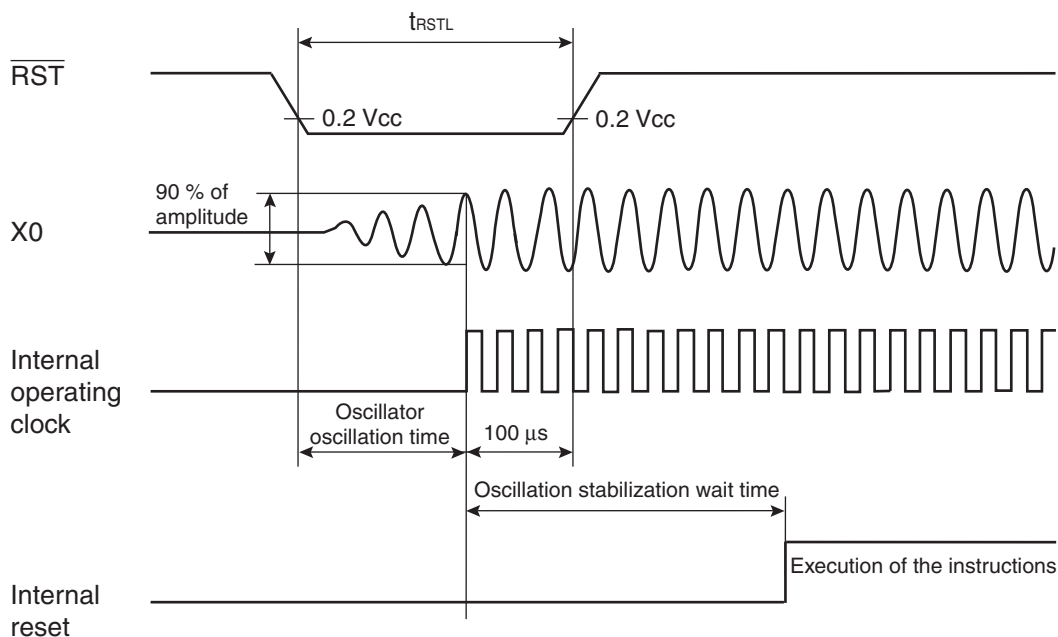
1. The oscillation time of the oscillator is the time taken to reach 90% of the amplitude. The oscillation time of a crystal oscillator is between several ms and tens of ms. The oscillation time of a ceramic oscillator is between hundreds of μs and several ms. The oscillation time of an external clock is 0 ms.

Note: t_{CP} is the internal operating clock cycle time. (Unit: ns)

■ During normal operation



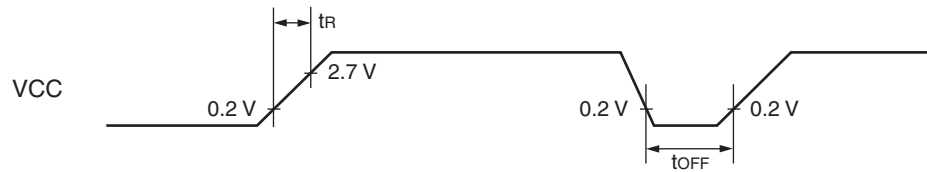
■ In stop mode and power-on



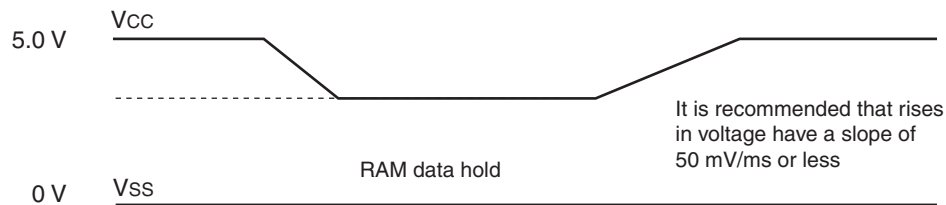
11.4.3 Power-on Reset

($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C to } +105^\circ\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	VCC	—	0.05	30	ms	
Power supply cutoff time	t_{OFF}			1	—	ms	Waiting time until power-on



Note: Extreme variations in power supply voltage may trigger a power-on reset. When the power supply voltage is changed during operation, it is recommended that increases in voltage are smoothed out as shown in the following diagram. The PLL clock of the device should not be in use when varying the voltage. However, the PLL clock may continue to be used if the rate of the voltage drop is 1 V/s or less.



11.4.4 UART0/1/2/3 (LIN/SCI)

Bit Setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C _L = 80 pF + 1TTL	5 t _{CP}	—	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↑	t _{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t _{CP} + 80	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXI}			0	—	ns
Serial clock “L” pulse width	t _{SLSH}	SCK0 to SCK3	External shift clock mode output pin C _L = 80 pF + 1TTL	3 t _{CP} – t _R	—	ns
Serial clock “H” pulse width	t _{SHSL}			t _{CP} + 10	—	ns
SCK ↓ → SOT delay time	t _{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t _{CP} + 60	ns
Valid SIN → SCK ↑	t _{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXE}			t _{CP} + 30	—	ns
SCK ↓ time	t _F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t _R			—	10	ns

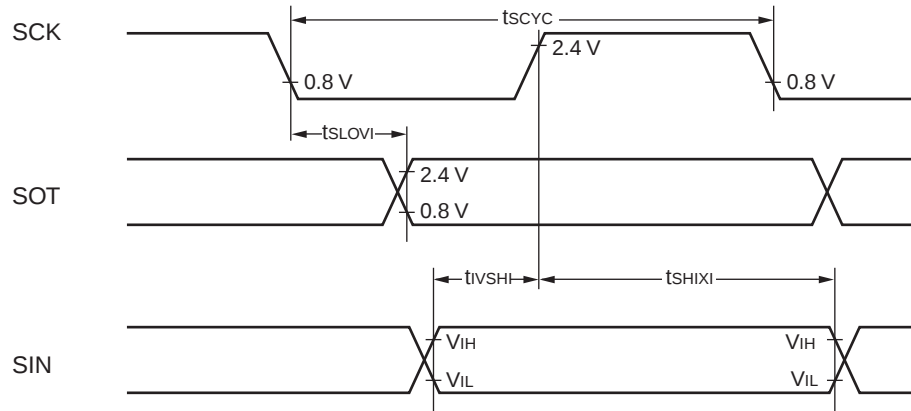
Notes:

- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters.

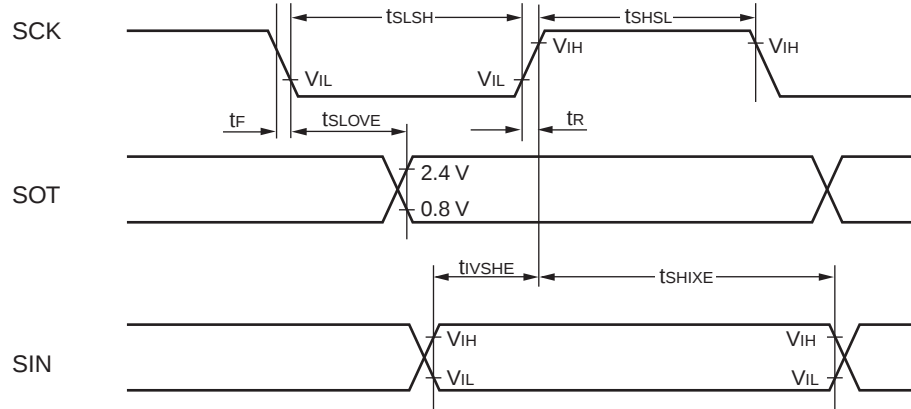
These parameters are shown in "CY90930 series hardware manual".

- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. See [Clock Timing](#).

■ Internal shift clock mode



■ External shift clock mode



Bit Setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=0

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin C _L = 80 pF + 1TTL	5 t _{CP}	—	ns
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		– 50	+ 50	ns
Valid SIN → SCK ↓	t _{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t _{CP} + 80	—	ns
SCK ↓ → valid SIN hold time	t _{SLIXI}			0	—	ns
Serial clock “H” pulse width	t _{SHSL}	SCK0 to SCK3	External shift clock mode output pin C _L = 80 pF + 1TTL	3 t _{CP} – t _R	—	ns
Serial clock “L” pulse width	t _{SLSH}			t _{CP} + 10	—	ns
SCK ↑ → SOT delay time	t _{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t _{CP} + 60	ns
Valid SIN → SCK ↓	t _{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↓ → valid SIN hold time	t _{SLIXE}			t _{CP} + 30	—	ns
SCK ↓ time	t _F	SCK0 to SCK3		—	10	ns
SCK ↑ time	t _R			—	10	ns

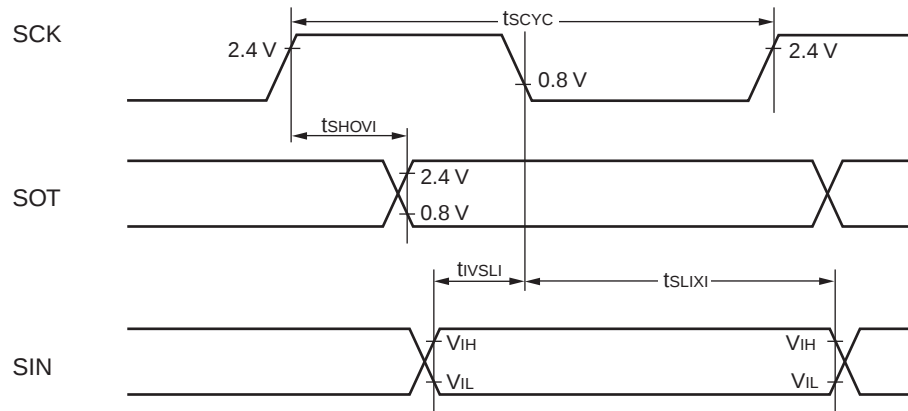
Notes:

- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters.

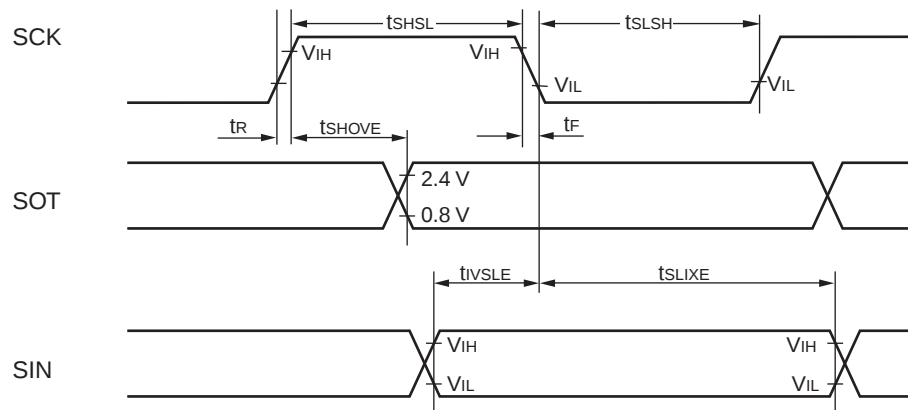
These parameters are shown in "CY90930 series hardware manual".

- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. See [Clock Timing](#).

■ Internal shift clock mode



■ External shift clock mode



Bit Setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=1

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

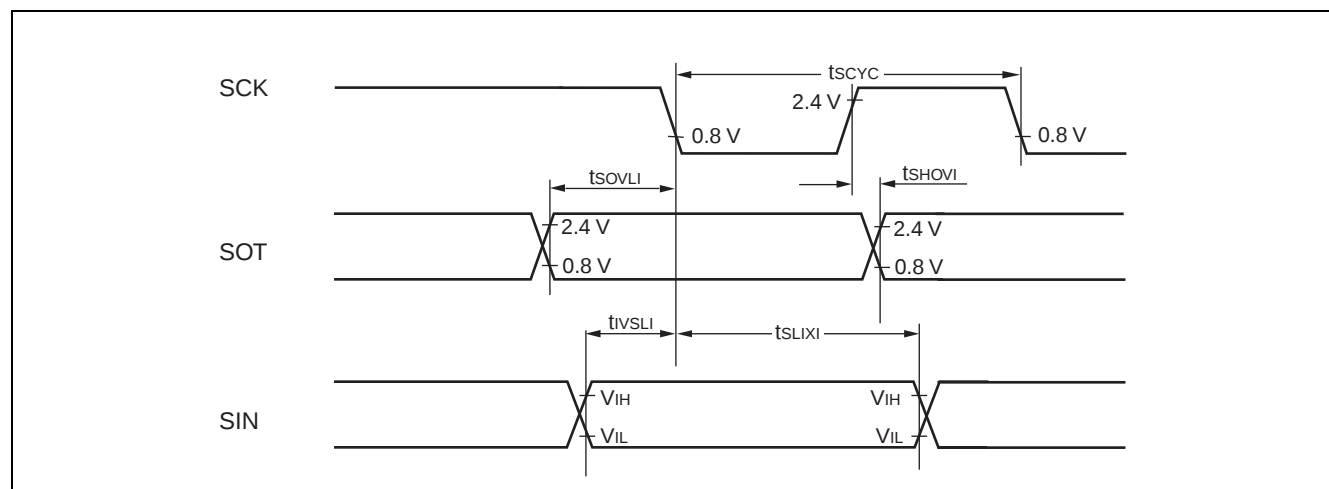
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin $C_L = 80\text{ pF} + 1\text{ TTL}$	$5\ t_{CP}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		- 50	+ 50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\downarrow \rightarrow$ valid SIN hold time	t_{SLIXI}			0	—	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		$3\ t_{CP} - 70$	—	ns

Notes:

- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters.

These parameters are shown in “CY90930 series hardware manual”.

- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. See [Clock Timing](#).



Bit Setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

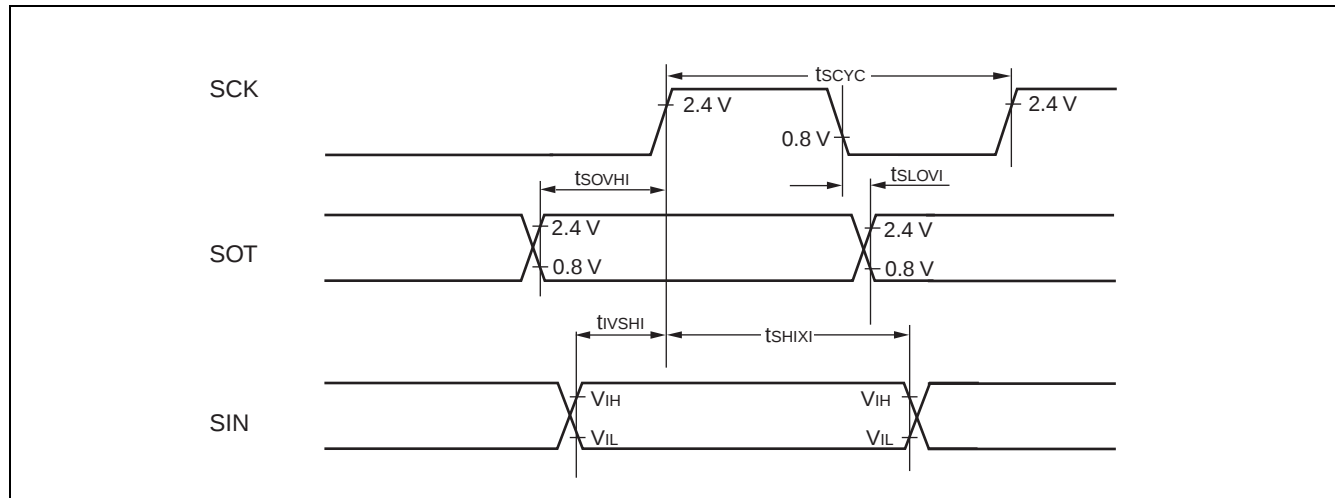
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pin $C_L = 80\text{ pF} + 1\text{ TTL}$	$5\ t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		- 50	+ 50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SOT0 to SOT3		0	—	ns
SOT $\rightarrow$ SCK $\uparrow$ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		$3\ t_{CP} - 70$	—	ns

Notes:

■ Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “CY90930 series hardware manual”.

■ C_L is the load capacitance connected to the pin during testing.

■ t_{CP} is the internal operating clock cycle time. See [Clock Timing](#).



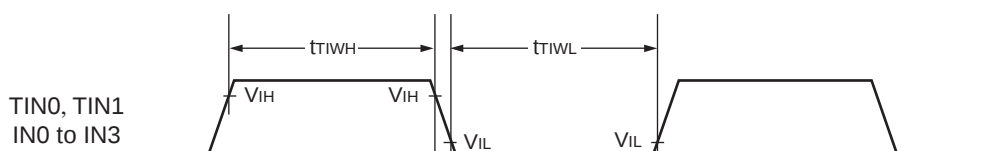
11.4.5 Timer Input Timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, TIN1, IN0 to IN3	—	$4\ t_{CP}$	—	ns

Note: t_{CP} is the internal operating clock cycle time. See [Clock Timing](#).

■ Timer input timing



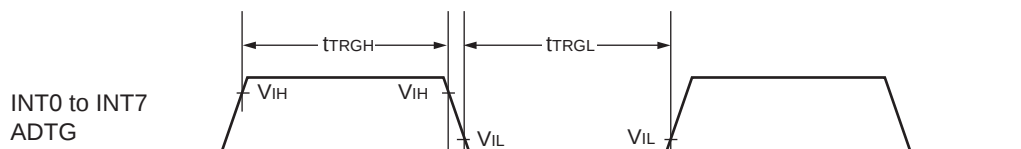
11.4.6 Trigger Input Timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}	INT0 to INT7	—	200	—	ns	During normal operation
	t_{TRGL}	ADTG	—	$t_{CP} + 200$	—	ns	

Note: t_{CP} is the internal operating clock cycle time. See [Clock Timing](#).

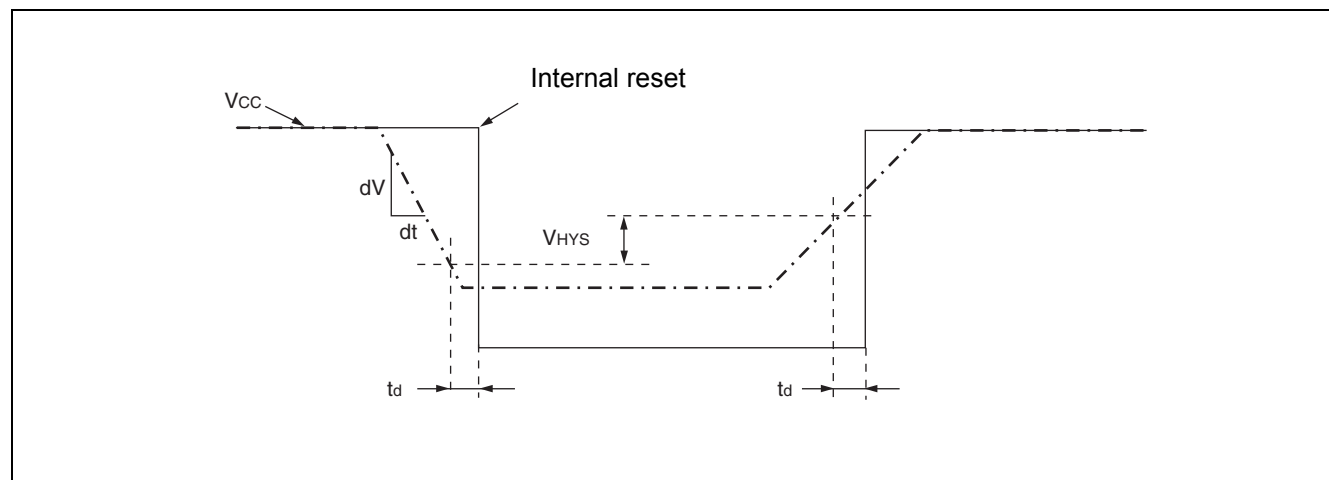
■ Trigger input timing



11.4.7 Low Voltage Detection

(V_{SS} = AV_{SS} = 0.0 V, T_A = -40 °C to +105 °C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Detection voltage	V _{DL}	VCC	—	3.7	4.0	4.3	V	Flash memory product/Mask ROM product, during voltage drop
Hysteresis width	V _{HYS}	VCC	—	169	—	—	mV	Flash memory product/Mask ROM product, during voltage rise
Power supply voltage change rate	dV/dt	VCC	—	- 0.1	—	+ 0.1	V/μs	Flash memory product/Mask ROM product, dV/dt at low voltage reset
				-0.004	—	+ 0.004	V/μs	Flash memory product/Mask ROM product, dV/dt at standard value of low voltage detection/release voltage
Detection delay time	t _d	—	—	—	—	3.2	μs	Flash memory product/Mask ROM product, when dV/dt ≤ 0.004 V/μs



11.5 A/D Converter

11.5.1 Electrical Characteristics

($V_{CC} = AV_{CC} = AVRH = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	– 3.0	—	+ 3.0	LSB	
Non-linear error	—	—	– 2.5	—	+ 2.5	LSB	
Differential linear error	—	—	– 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN23	$AV_{SS} - 1.5\text{ LSB}$	$AV_{SS} + 0.5\text{ LSB}$	$AV_{SS} + 2.5\text{ LSB}$	V	1 LSB = $(AVRH - AV_{SS}) / 1024$
Full scale transition voltage	V_{FST}	AN0 to AN23	$AVRH - 3.5\text{ LSB}$	$AVRH - 1.5\text{ LSB}$	$AVRH + 0.5\text{ LSB}$	V	
Sampling time	t_{SMP}	—	0.4	—	16500	μs	4.5 V $\leq$ AVCC $\leq$ 5.5 V
			1.0				4.0 V $\leq$ AVCC $\leq$ 4.5 V
Compare time	t_{CMP}	—	0.66	—	—	μs	4.5 V $\leq$ AVCC $\leq$ 5.5 V
			2.2				4.0 V $\leq$ AVCC $\leq$ 4.5 V
A/D conversion time	t_{CNV}	—	1.44	—	—	μs	*1
Analog port input current	I_{AIN}	AN0 to AN23	– 1.0	—	+ 1.0	μA	
Analog input voltage	V_{AIN}	AN0 to AN23	0	—	AVRH	V	
Reference voltage	AV+	AVRH	$AV_{SS} + 2.7$	—	AV_{CC}	V	
Power supply current	I_A	AVCC	—	2.3	6.0	mA	
	I_{AH}		—	—	5	μA	*2
Reference voltage supply current	I_R	AVRH	—	—	900	μA	$V_{AVRH} = 5.0\text{ V}$
	I_{RH}		—	—	5	μA	*2
Inter-channel variation	—	AN0 to AN23	—	—	4	LSB	

*1: The time per channel (4.5 V $\leq$ AVCC $\leq$ 5.5 V, and internal operating frequency = 32 MHz).

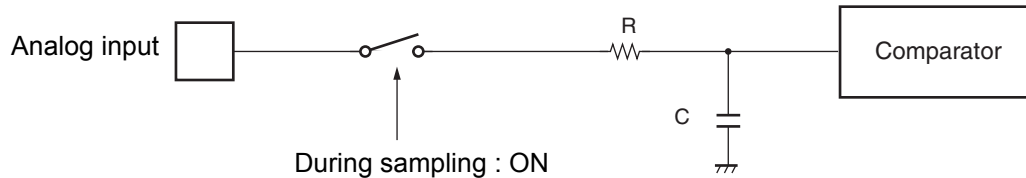
*2: Defined as supply current (when VCC = AVCC = AVRH = 5.0 V) with A/D converter not operating, and CPU in stop mode.

Notes on the External Impedance and Sampling Time of Analog Inputs

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard,

consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

■ Analog input equivalent circuit



CY90F931/CY90F931S/CY90931/CY90931S

R	C
$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V} : 2.6\text{ k}\Omega\text{ (Max)}$	8.5 pF (Max)
$4.0\text{ V} \leq AV_{CC} \leq 4.5\text{ V} : 12.1\text{ k}\Omega\text{ (Max)}$	8.5 pF (Max)

CY90V930-102/CY90V930-101

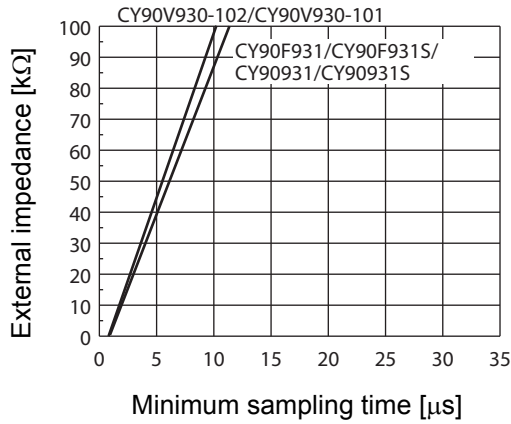
R	C
$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V} : 2.0\text{ k}\Omega\text{ (Max)}$	14.4 pF (Max)
$4.0\text{ V} \leq AV_{CC} \leq 4.5\text{ V} : 8.2\text{ k}\Omega\text{ (Max)}$	14.4 pF (Max)

Note : The values are reference values.

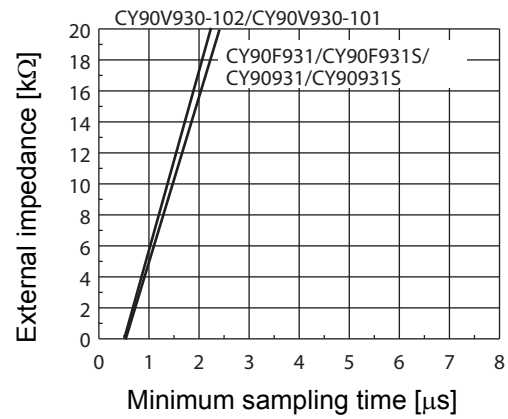
■ The relationship between the external impedance and minimum sampling time

■ At $4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$

(External impedance = 0 k Ω to 100 k Ω)

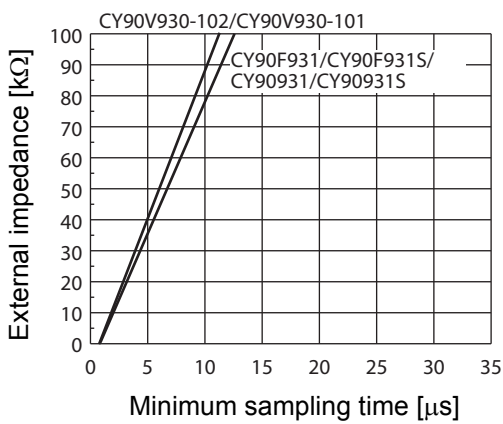


(External impedance = 0 k Ω to 20 k Ω)

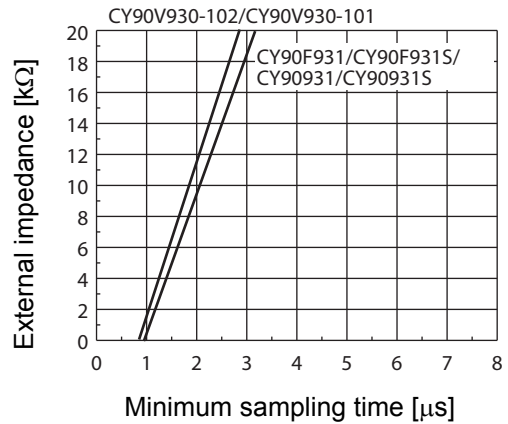


■ At $4.0\text{ V} \leq AV_{CC} \leq 4.5\text{ V}$

(External impedance = 0 k Ω to 100 k Ω)



(External impedance = 0 k Ω to 20 k Ω)

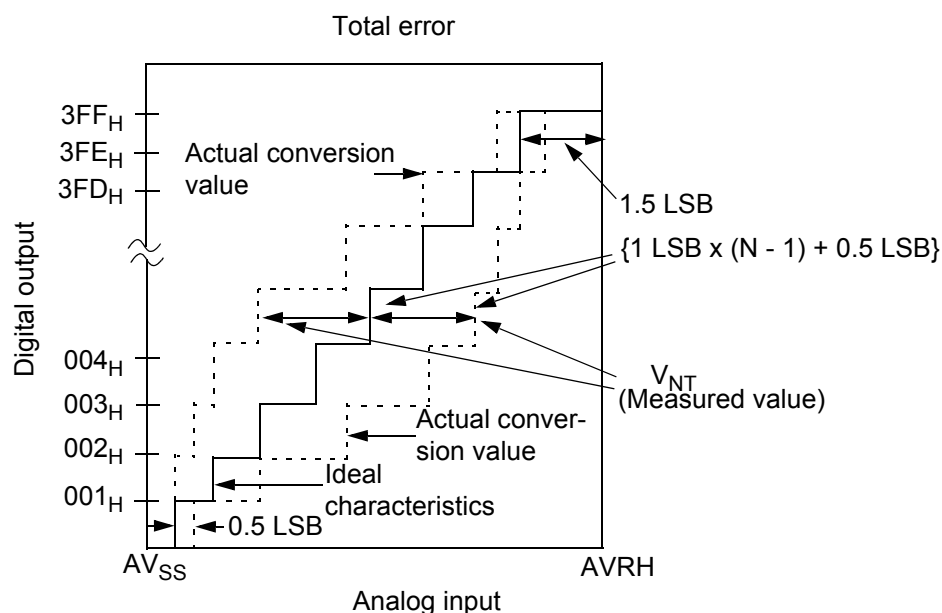


About Errors

As $|AV_{RH} - AV_{SS}|$ becomes smaller, the relative errors grow larger.

11.5.2 Definition of Terms

Resolution	: Analog changes that are identifiable by the A/D converter.
Non-Linear error	: The deviation of the straight line connecting the transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics.
Differential linear error	: The deviation from the ideal value of the input voltage needed to change the output code by 1 LSB.
Total error	: The total error is the difference between the actual value and the theoretical value, and includes transition error/full-scale transition error and linear error.



$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

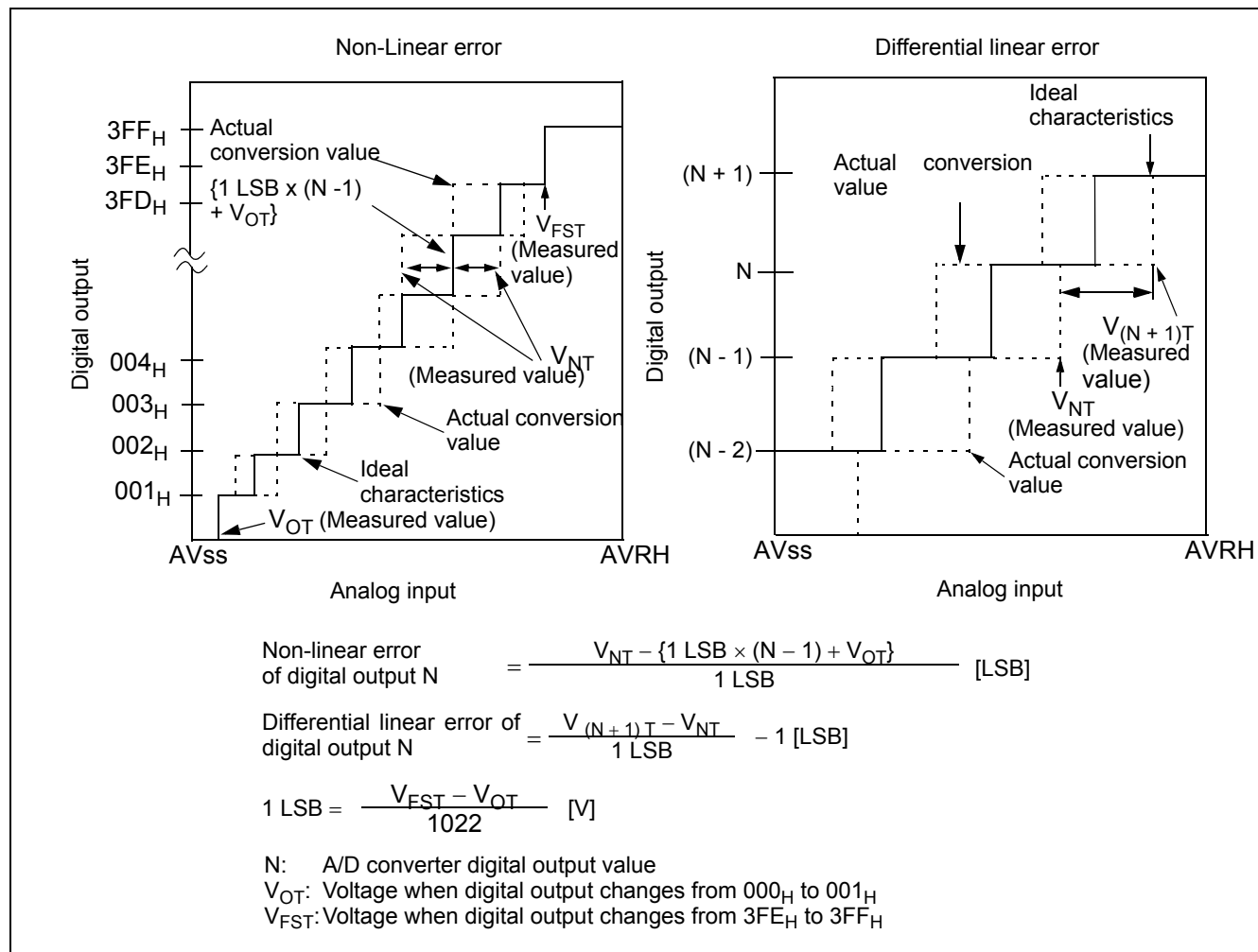
$$1 \text{ LSB (Ideal)} = \frac{AV_{RH} - AV_{SS}}{1024} \quad [\text{V}]$$

N : A/D converter digital output value

$$V_{OT} \text{ (Ideal)} = AV_{SS} + 0.5 \text{ LSB} \quad [\text{V}]$$

$$V_{FST} \text{ (Ideal)} = AV_{RH} - 1.5 \text{ LSB} \quad [\text{V}]$$

V_{NT} : Voltage when the digital output changes from (N - 1) to N



11.6 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T _A = + 25 °C, V _{CC} = 5.0 V	—	0.9	3.6	s	Excludes pre-programming before erase
Word (16-bit width) programming time		—	23	370	μs	Excludes system-level overhead
Chip programming time	T _A = + 25 °C, V _{CC} = 5.0 V	—	3.4	55	s	
Erase/program cycle	—	10000	—	—	cycle	
Flash memory data retention time	Average T _A = + 85 °C	20	—	—	year	*1

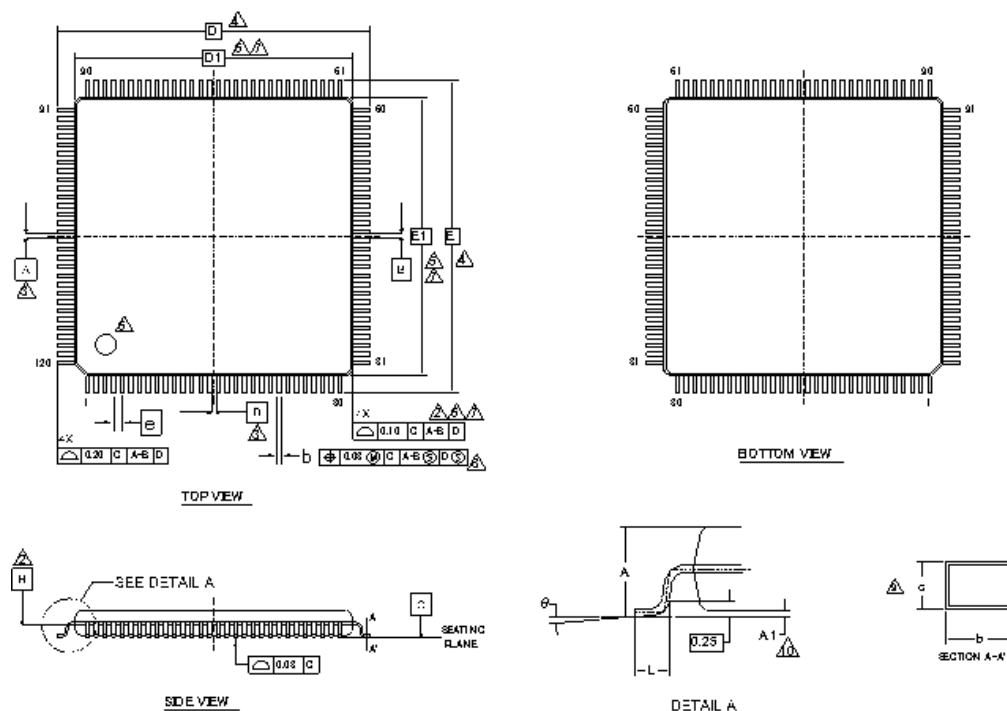
*1: This value is calculated from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C).

12. Ordering Information

Part number	Package	Remarks
CY90F931PMC-GS-UJE1 CY90931PMC-GSE1	120-pin plastic LQFP (LQM120)	

13. Package Dimension

Package Type	Package Code
LQFP 120	LQM120



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC		
D1	18.00 BSC		
e	0.50 BSC		
E	18.00 BSC		
E1	18.00 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. D TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN IDENTIFIERS ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS C1 AND E1 ARE DETERMINED AT THE LARGEST 1-A JIB OF THE BODY EXCLUDING MOLD FLASH AND GAUGING SURFACES, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE WAFER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.27mm MAXIMUM BY MORE THAN 0.05mm. DAMBER CANNOT BE LOCATED ON THE LOWER RADII OF THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

11. JEDOC SPECIFICATION NO. RFF-1A4

002-16172 **

PACKAGE OUTLINE, 120 LEAD LQFP
18.0x18.0x1.7mm LQM120 REV#4

14. Major Changes

Spansion Publication Number: **DS07-13754-3E**

Page	Section	Change Results
13	■ I/O CIRCUIT TYPE	Corrected the circuit type A and B.
21	■ HANDLING DEVICES	Added the following items. Serial communication Characteristic difference between flash device and mask ROM device
49	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristic	Added the item for "LCD output impedance".
Rev. *A		
	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
4 59 60	2. Pin Assignments 12. Ordering Information 13. Package Dimension	Package description modified to JEDEC description. (before) FPT-120P-M21 (after) LQM120
59	12. Ordering Information	Deleted the following parts number. - MB90F931SPMC - MB90931SPMC - MB90V930-102 (for evaluation) - MB90V930-101 (for evaluation) Revised the following parts number. (before) - MB90F931PMC - MB90931PMC (after) - CY90F931PMC-GS-UJE1 - CY90931PMC-GSE1

NOTE: Please see "Document History" for later revised information.

Document History

Document Title: CY90931/931S, CY90F931/F931S, CY90V930-101/V930-102, F ² MC-16LX CY90930 Series, 16-bit Proprietary Microcontroller Document Number: 002-07953				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	TORS	09/17/2010	Migrated to Cypress and assigned document number 002-07953. No change to document contents or format.
*A	6279258	GSHI	08/13/2018	Updated to Cypress template. Revised the following items: 2. Pin Assignments 12. Ordering Information 13. Package Dimension For details, please see 14. Major Changes.

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