

Smart Power-Management Integrated Circuit for Camera Module Application

General Description

The RT5112 device is a smart power management IC which includes a low-quiescent-current HCOT Buck converter, a ACOT Boost converter and four high PSRR low dropout regulators (LDO). One can control the channel power sequence, output voltage level and DVS slew rate by setting registers via I²C interface. The output voltage OVP/UVP, OCP and OTP protection are built in the RT5112. The RT5112 is available in a WL-CSP-25B 2.2x2.3 (BSC) package.

Applications

- Camera Module
- Optical Module
- SSD

Ordering Information

RT5112□

Package Type

WSC : WL-CSP-25B 2.2x2.3 (BSC)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Features

System Control

- Hardware Enable Pin
- I²C Controlled Interface
- Programmable Channel Power Sequence
- IRQ Output for Indication
- Over-Voltage Protection
- Under-Voltage Protection
- Over-Current Protection
- Over-Temperature Protection
- Available in a WL-CSP-25B 2.2x2.3 (BSC) Package

High Efficiency Buck Converter

- Wide 2.5V to 5.5V Operating Input Range
- Programmable Output Voltage from 0.6V to 3.3V with 12.5mV/Step
- Maximum Continuous Load Current : 1.2A
- HCOT Control Operation
- Low Quiescent Current

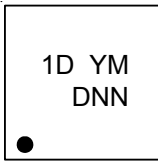
Flexible Boost Converter

- Wide 2.5V to 4.4V Operating Input Range
- Programmable Output Voltage from 4.5 V to 5.5V with 25mV/Step
- Maximum Continuous Load Current : 1A
- ACOT Control Operation
- Low Quiescent Current

Four Low Dropout Regulators

- Wide 1.9V to 5.5V Operating Input Range
- Programmable Output Voltage from 0.6V to 3.775V with 25mV/Step
- High PSRR : 70dB @ 1kHz, 40dB @ 100kHz with LDO1 / LDO2
- High PSRR : 50dB @ 1kHz, 40dB @ 10kHz with LDO3 / LDO4
- 300mA Low Dropout Voltage Regulators
- Low Quiescent Current

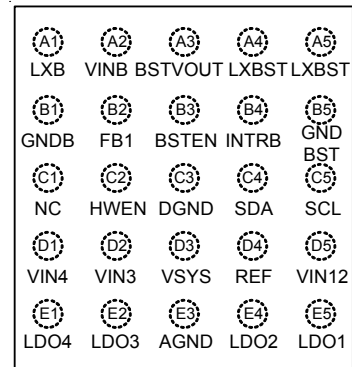
Marking Information



1D : Product Code
YMDNN : Date Code

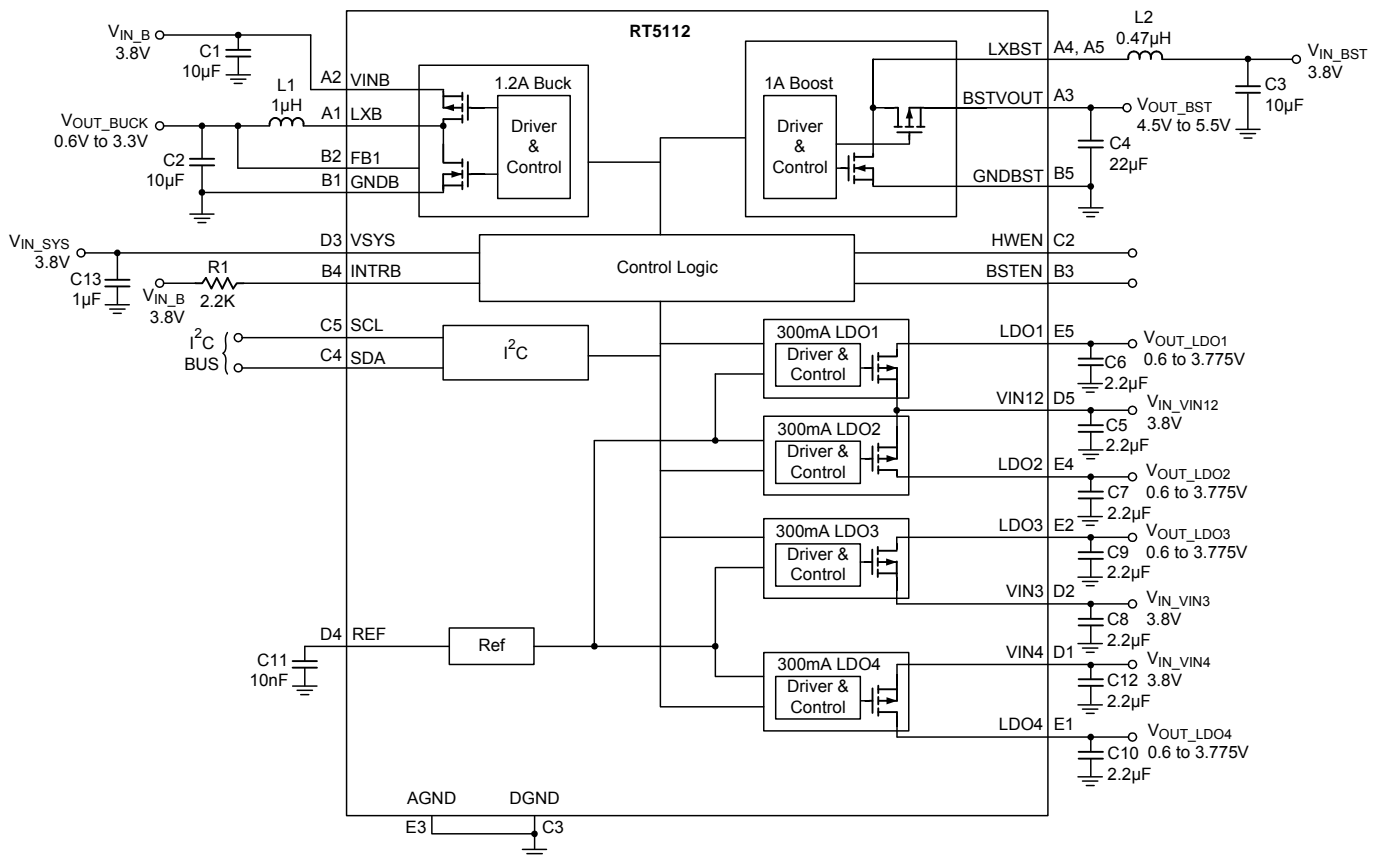
Pin Configuration

(TOP VIEW)



WL-CSP-25B 2.2 x 2.3 (BSC)

Typical Application Circuit



Component List of Evaluation Board

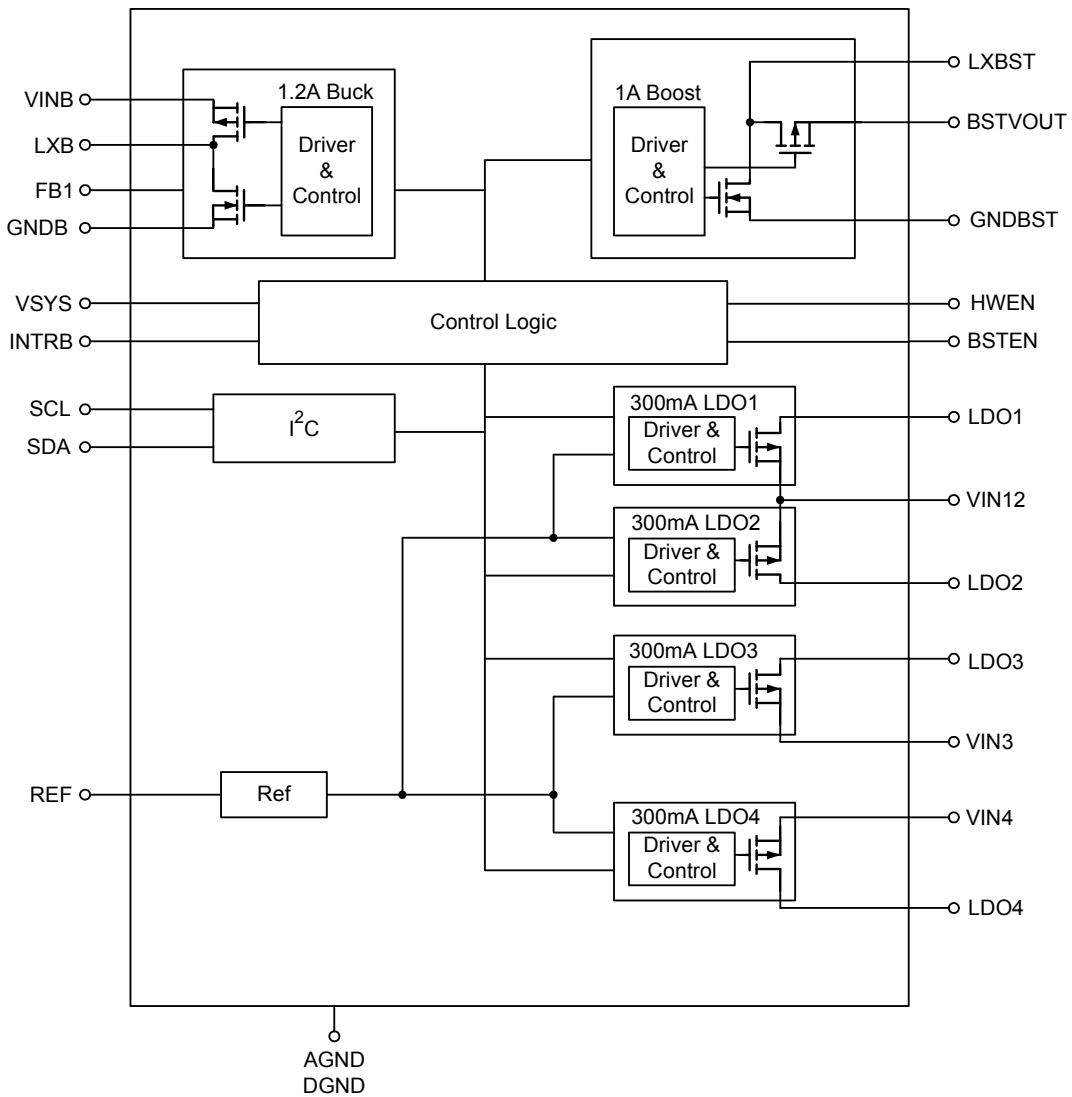
| Reference | Qty | Part Number | Description | Package | Manufacturer |
|-----------------|-----|---------------------|--------------------------------|---------|--------------|
| C1, C2, C3 | 1 | JMK105CBJ106MV-F | 10 μ F/X5R/6.3V | 0402 | TAIYO YUDEN |
| C4 | 1 | JMK107BBJ226MA-T | 22 μ F/X5R/6.3V | 0603 | TAIYO YUDEN |
| C5, C8, C12 | 1 | JMK105BJ225KV-F | 2.2 μ F/X5R/6.3V | 0402 | TAIYO YUDEN |
| C6, C7, C9, C10 | 1 | GRM033R60J225ME47D | 2.2 μ F/X5R/6.3V | 0201 | MURATA |
| C11 | 1 | LMK105BJ103KV-F | 10nF/X5R/6.3V | 0402 | TAIYO YUDEN |
| C13 | 1 | LMK063BBJ105MPLF | 1 μ F/X5R/10V | 0201 | TAIYO YUDEN |
| L1 | 1 | MEKK2016T1R0M | 1 μ H/3.1A/50m Ω | 2016 | TAIYO YUDEN |
| L2 | 1 | DFE201210S-R47MH=P2 | 0.47 μ H/3.4A/32m Ω | 2012 | MURATA |

Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---------|----------|--|
| A1 | LXB | Buck switch output. Connect this pin to an inductor with a wide PCB trace. |
| A2 | VINB | Supply voltage input of Buck. The IC operates from a 2.5V to 5.5V input rail. It requires a 10 μ F decouple ceramic capacitor. Connect this pin to input voltage with a wide PCB trace. |
| A3 | BSTVOUT | Boost output pin. PCB trace length from BSTVOUT to the output filter capacitor should be as short and wide as possible. It requires a 22 μ F decouple ceramic capacitor. BSTVOUT is completely disconnected from LXBST when Boost is at off state. |
| A4, A5 | LXBST | Boost switch output. Connect this pin to an inductor with a wide PCB trace and keep the PCB trace length as short and wide as possible to reduce EMI and voltage spike. |
| B1 | GNDB | Buck power ground. |
| B2 | FB1 | Feedback of Buck. Directly connect the Buck's output to this pin. |
| B3 | BSTEN | Boost enable control input. |
| B4 | INTRB | Interrupt output. Open drain output. When interrupt happens, interrupt pin is pulled down. |
| B5 | GNDBST | Boost power ground. |
| C1 | NC | NC internal connection and should keep floating state. |
| C2 | HWEN | Chip enable control input. |
| C3 | DGND | Digital ground. |
| C4 | SDA | I ² C data pin. |
| C5 | SCL | I ² C clock signal input. |
| D1 | VIN4 | LDO4 power supply input. It requires a 2.2 μ F decouple ceramic capacitor. |
| D2 | VIN3 | LDO3 power supply input. It requires a 2.2 μ F decouple ceramic capacitor. |
| D3 | VSYS | System analog power supply. It requires a 1 μ F decouple ceramic capacitor. It also connected to V _{INB} externally. |

| Pin No. | Pin Name | Pin Function |
|---------|----------|--|
| D4 | REF | Internal reference output. It requires a 10nF decouple ceramic capacitor. |
| D5 | VIN12 | LDO1 and 2 power supply input. It requires a 2.2μF decouple ceramic capacitor. |
| E1 | LDO4 | LDO4 output. It requires a 2.2μF decouple ceramic capacitor. |
| E2 | LDO3 | LDO3 output. It requires a 2.2μF decouple ceramic capacitor. |
| E3 | AGND | Analog ground. |
| E4 | LDO2 | LDO2 output. It requires a 2.2μF decouple ceramic capacitor. |
| E5 | LDO1 | LDO1 output. It requires a 2.2μF decouple ceramic capacitor. |

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VSYS, VINB, VIN12, VIN3, VIN4, BSTVOUT, LDO1, LDO2, LDO3, LDO4, FB1, REF, SCL, SDA, HWEN, BSTEN, INTRB, LXB, LXBST ----- -0.3V to 6.5V
- LXB, LXBST (< 20ns) ----- -2V to 9V
- Power Dissipation, P_D @ T_A = 25°C
 WL-CSP-25B 2.2x2.3 (BSC) ----- 3.05W
- Package Thermal Resistance (Note 2)
 WL-CSP-25B 2.2x2.3 (BSC), θ_{JA} ----- 32.7°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 HBM (Human Body Mode) ----- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage V_{IN_B}, V_{sys} ----- 2.5V to 5.5V
- Supply Voltage V_{IN_BST} ----- 2.5V to V_{OUT_BST} - 0.1V
- Supply Voltage V_{IN_VIN12}, V_{IN_VIN3}, V_{IN_VIN4} ----- 1.9V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---------------------|--|-----|------|------|------|
| System Parameter | | | | | | |
| Quiescent Current | I _{QTATOL} | HWEN = BSTEN = H, V _{IN_SYS} = V _{IN_B} = V _{IN_BST} = V _{IN_VIN12} = V _{IN_VIN3} = V _{IN_VIN4} = 3.8V, LDO/Buck/Boost on, no load, automode -40°C to 85°C | -- | 106 | 138 | μA |
| | I _{QLDO} | HWEN = H, V _{IN_SYS} = V _{IN_VIN12} = V _{IN_VIN3} = V _{IN_VIN4} = 3.8V, LDO on, no load, automode | -- | 95 | 118 | |
| | I _{QBASE} | HWEN = H, V _{IN_SYS} = V _{IN_B} = 3.8V, all power regulators are off | -- | 7 | 10 | |
| | I _{QBOOST} | HWEN = L, BSTEN = H, V _{IN_SYS} = V _{IN_B} = V _{IN_BST} = 3.8V, only Boost active, no load, automode | -- | 12 | 20 | |
| Leakage Current | I _{LEAK} | Leak current, HWEN = BSTEN = L, V _{IN_SYS} = V _{IN_B} = V _{IN_BST} = V _{IN_VIN12} = V _{IN_VIN3} = V _{IN_VIN4} = 2.5V to 5.5V, -40°C to 85°C | -- | -- | 1.5 | μA |
| V _{sys} Under-Voltage Lockout Threshold Rising | UVLO | | -- | 2.35 | 2.45 | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---------------------------|--|-----|------------------------------|-----|------|
| Hysteresis Voltage of UVLO | UVLO_H | | -- | 100 | -- | mV |
| HWEN and BSTEN Control | | | | | | |
| HWEN and BSTEN Low Level Input Voltage | V _{IL} | | -- | -- | 0.4 | V |
| HWEN and BSTEN High Level Input Voltage | V _{IH} | | 1.2 | -- | -- | V |
| HWEN and BSTEN Pull Down Resistor | R _{EN} | | -- | 1 | - | MΩ |
| Step Down Buck Converter (V_{IN_B} = 3.8V, C1 = C2 = 10μF, L1 = 1μH) | | | | | | |
| Input Voltage Range | V _{IN_B} | | 2.5 | -- | 5.5 | V |
| Output Voltage Range | V _{OUT_BUCK} | | 0.6 | -- | 3.3 | V |
| Output Voltage Step | | | -- | 12.5 | -- | mV |
| Output Voltage Accuracy | V _{OUT_ACC_BUCK} | All output range of V _{OUT_BUCK} , I _{OUT} = I _{OUT(MAX)} | -2 | -- | 2 | % |
| Switching Frequency | f _{SW_BUCK} | V _{OUT_BUCK} = 1.1V, operating under CCM | 2 | 2.5 | 3 | MHz |
| P-Channel MOSFET On Resistance | R _{ON_HG_BUCK} | From VINB pin to LXB pin | -- | 150 | 200 | mΩ |
| N-Channel MOSFET On Resistance | R _{ON_LG_BUCK} | From LXB pin to GNDB pin | -- | 70 | 140 | mΩ |
| Maximum Duty Cycle | D _{MAX_BUCK} | | -- | -- | 100 | % |
| Output Discharge Resistor | R _{DIS_BUCK} | | 80 | 100 | 140 | Ω |
| Over-Voltage Rising Threshold Detection | OVP_R_BUCK | | -- | V _{OUT_BUCK} x 120% | -- | V |
| Over-Voltage Falling Threshold Detection | OVP_F_BUCK | | -- | V _{OUT_BUCK} x 109% | -- | V |
| Under-Voltage Rising Threshold Detection | UVP_R_BUCK | | -- | V _{OUT_BUCK} x 92% | -- | V |
| Under-Voltage Falling Threshold Detection | UVP_F_BUCK | | -- | V _{OUT_BUCK} x 80% | -- | V |
| FB1 Leakage Current | I _{FB_LK} | Buck disable, 0x0B[7] = 0 (Buck discharge disable), V _{IN_B} = 5.5V, V _{LXB} = 5.5V, V _{FB1} = 5.5V | 0 | 50 | 100 | nA |
| Switch Leakage Current | I _{LXB_LK} | Buck disable, 0x0B[7] = 0 (Buck discharge disable), V _{IN_B} = 5.5V, V _{LXB} = 0 or 5.5V | 0 | -- | 1 | μA |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|------------------------|--|-----|------------------------------|-----|------------|
| UG Peak Current Limit | $I_{CL_peak_BUCK}$ | $2.5V \leq V_{IN_B} \leq 5.5V$ | 1.5 | 2 | 2.5 | A |
| LG Valley Current Limit | $I_{CL_valley_BUCK}$ | $V_{IN_B} = 3.6V$ | 1 | 1.5 | 2 | A |
| LG Negative Current Limit | $I_{NCL_NEG_BUCK}$ | $V_{IN_B} = 3.6V$, CCM | 0.5 | -- | 3 | A |
| Minimum On Time | $t_{MIN_ON_BUCK}$ | $V_{IN_B} = 3.6V$, $V_{OUT_BUCK} = 1.8V$ | 167 | 200 | 250 | ns |
| Minimum Off Time | $t_{MIN_OFF_BUCK}$ | $V_{IN_B} = V_{OUT_BUCK} = 3.3V$ | 20 | 40 | 60 | ns |
| Step Up Boost Converter ($V_{IN_BST} = 3.8V$, $C3 = 10\mu F$, $C4 = 22\mu F$, $L2 = 0.47\mu H$) | | | | | | |
| Input Voltage Range | V_{IN_BST} | | 2.5 | -- | 4.4 | V |
| Output Voltage Range | V_{OUT_BST} | | 4.5 | 5 | 5.5 | V |
| Output Voltage Step | | | -- | 25 | -- | mV |
| DC Output Voltage Accuracy | $V_{OUT_ACC_BST}$ | All output range of V_{OUT_BST} , $I_{OUT} = I_{OUT(MAX)}$ | -2 | -- | 2 | % |
| Switching Frequency | f_{SW_BST} | $V_{OUT_BST} = 5V$, operating under CCM | 2 | 3 | 3.6 | MHz |
| Shutdown Current | I_{SHDN_BST} | HWEN = BSTEN = 0V, from V_{IN_BST} to GND | -- | -- | 0.5 | μA |
| Reverse Leakage Current | I_{LEAK_BST} | BSTEN = 0, $V_{OUT_BST} = 5V$, from V_{OUT_BST} to GND, 0x0B[5] = 0 | -- | -- | 1.5 | μA |
| P-Channel MOSFET On Resistance | $R_{ON_HG_BST}$ | From LXBST pin to BSTOUT pin | -- | 95 | 120 | m Ω |
| N-Channel MOSFET On Resistance | $R_{ON_LG_BST}$ | From LXBST pin to PGND pin | -- | 100 | 130 | m Ω |
| Output Discharge Resistor | R_{DIS_BST} | | 60 | 100 | 140 | Ω |
| Over-Voltage Rising Threshold Detection | OVP_R_BST | | -- | $V_{OUT_BST} \times 117\%$ | -- | V |
| Over-Voltage Falling Threshold Detection | OVP_F_BST | | -- | $V_{OUT_BST} \times 106\%$ | -- | V |
| Under-Voltage Rising Threshold Detection | UVP_R_BST | | -- | $V_{OUT_BST} \times 92.3\%$ | -- | V |
| Under-Voltage Falling Threshold Detection | UVP_F_BST | | -- | $V_{OUT_BST} \times 80\%$ | -- | V |
| Switch Leakage Current | I_{LXBST_LK} | BSTEN = 0V, $V_{IN_BST} = V_{LX_BST} = 5.5V$, $V_{OUT_BST} = 0V$ | -- | 100 | 200 | nA |
| Linear Charge Current Limit | I_{LC_BST} | $V_{IN_BST} = 2.5$ to $4.4V$, $V_{OUT_BST} = 4.5V$ to $5.5V$ | -- | 0.4 | -- | A |
| | $I_{LC_OTW_BST}$ | Over OTW protection 120°C | -- | 0.1 | -- | |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|--|------|---|-------|----------|
| Inductor Valley Current Limit | $I_{CL_valley_BST}$ | $V_{OUT_BST} = 5V$ | 2.5 | 2.8 | 3.1 | A |
| Low Dropout Voltage Regulator LDO1 and LDO2 ($V_{IN_VIN12} = V_{OUT_LDO1}/V_{OUT_LDO2} + 1V$, $V_{HWEN} = 1.2V$, $I_{OUT} = 1mA$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 2.2\mu F$) | | | | | | |
| Input Voltage Range | V_{IN_VIN12} | | 1.9 | -- | 5.5 | V |
| Output Voltage Range | $V_{OUT_LDO1}/$ | | 0.6 | 2.8 | 3.775 | V |
| Output Voltage Step | V_{OUT_LDO2} | | -- | 25 | -- | mV |
| Maximum Output Current | $I_{OUT_LDO1}/$ I_{OUT_LDO2} | | 300 | -- | -- | mA |
| Soft-Start Time | $t_{SS_LDO1}/$ t_{SS_LDO2} | Time from $V_{OUT_LDO1} /$ V_{OUT_LDO2} start rising to 90% nominal value, $V_{OUT_LDO1} /$ $V_{OUT_LDO2} = 2.8V$, no load | -- | -- | 150 | μs |
| DC Output Voltage Accuracy | $V_{OUT_ACC_LDO1}/$ $V_{OUT_ACC_LDO2}$ | All output range of $V_{OUT_LDO1} /$ V_{OUT_LDO2} , $I_{OUT} = I_{OUT(MAX)}$ | -2 | -- | 2 | % |
| Load Regulation | $V_{LOAD_REG_LDO1}/$ $V_{LOAD_REG_LDO2}$ | $I_{OUT} = 0$ to $I_{OUT(MAX)}$ | -0.5 | -- | 0.5 | % |
| Line Regulation | $V_{LINE_REG_LDO1}/$ $V_{LINE_REG_LDO2}$ | $I_{OUT} = 50mA$ to $300mA$, V_{IN_VIN12} $= 3.0V$ to $4.4V$, $V_{OUT_LDO1} /$ $V_{OUT_LDO2} = 2.8V$ | -0.5 | -- | 0.5 | % |
| Dropout Voltage | $V_{DROP_LDO1}/$ V_{DROP_LDO2} | $I_{OUT} = 300mA$, $V_{OUT_LDO1} /$ $V_{OUT_LDO2} = 2.8V$ (Note 5) | -- | -- | 250 | mV |
| Output Discharge Resistor | $R_{DIS_LDO1}/$ R_{DIS_LDO2} | | -- | 10 | -- | Ω |
| Over-Voltage Rising Threshold Detection | $OVP_R_LDO1/$ OVP_R_LDO2 | | -- | $V_{OUT_LDO1}/$ V_{OUT_LDO2} $\times 120\%$ | -- | V |
| Over-Voltage Falling Threshold Detection | $OVP_F_LDO1/$ OVP_F_LDO2 | | -- | $V_{OUT_LDO1}/$ V_{OUT_LDO2} $\times 110\%$ | -- | V |
| Under-Voltage Rising Threshold Detection | $UVP_R_LDO1/$ UVP_R_LDO2 | | -- | $V_{OUT_LDO1}/$ V_{OUT_LDO2} $\times 90\%$ | -- | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|--|---|------|---|-------|------|
| Under-Voltage Falling Threshold Detection | UVP_F_LDO1/ UVP_F_LDO2 | | -- | V _{OUT_LDO1} / V _{OUT_LDO2} x 80% | -- | V |
| Quiescent Current | I _{Q_LDO1} /I _{Q_LDO2} | HWEN = 1.2V, I _{OUT} = 0mA | -- | 22 | 27 | μA |
| | | HWEN = 0.3V (disable) | -- | 0.1 | 1 | |
| Short Circuit Current Limit | I _{sc_LDO1} / I _{sc_LDO2} | | 360 | -- | -- | mA |
| Current Limit | I _{Limt_LDO1} / I _{Limt_LDO2} | 0x01[3:2] = 11 (LDO1 current limit = 360mA), 0x02[3:2] = 11 (LDO2 current limit = 360mA) | 360 | 415 | 470 | mA |
| Short Protection On Timer | t _{scp_ON_LDO1} / t _{scp_ON_LDO2} | | -- | 2 | -- | ms |
| Short Protection Off Timer | t _{scp_OFF_LDO1} / t _{scp_OFF_LDO2} | | -- | 40 | -- | ms |
| Low Dropout Voltage Regulator LDO3 and LDO4 (V_{IN_VIN3}/V_{IN_VIN4} = V_{OUT_LDO3}/V_{OUT_LDO4} + 1V, V_{HWEN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 2.2μF, C_{OUT} = 2.2μF) | | | | | | |
| Input Voltage Range | V _{IN_VIN3} / V _{IN_VIN4} | | 1.9 | -- | 5.5 | V |
| Output Voltage Range | V _{OUT_LDO3} / V _{OUT_LDO4} | | 0.6 | 1.8 | 3.775 | V |
| Output Voltage Step | | | -- | 25 | -- | mV |
| Maximum Output Current | I _{OUT_LDO3} / I _{OUT_LDO4} | | 300 | -- | -- | mA |
| Soft-Start Time | t _{SS_LDO3} / t _{SS_LDO4} | Time from V _{OUT_LDO3} / V _{OUT_LDO4} start rising to 90% nominal value, V _{OUT_LDO3} / V _{OUT_LDO4} = 1.8V, no load | -- | -- | 150 | μs |
| DC Output Voltage Accuracy | V _{OUT_ACC_LDO3} / V _{OUT_ACC_LDO4} | All output range of V _{OUT_LDO3} / V _{OUT_LDO4} , I _{OUT} = I _{OUT(MAX)} | -2 | -- | 2 | % |
| Load Regulation | V _{LOAD_REG_LDO3} / V _{LOAD_REG_LDO4} | I _{OUT} = 0 to I _{OUT(MAX)} | -0.5 | -- | 0.5 | % |
| Line Regulation | V _{LINE_REG_LDO3} / V _{LINE_REG_LDO4} | I _{OUT} = 50mA/300mA, V _{IN_VIN3} / V _{IN_VIN4} = 3.0 to 4.4V, V _{OUT_LDO3} / V _{OUT_LDO4} = 1.8V | -0.5 | -- | 0.5 | % |
| Dropout Voltage | V _{DROP_LDO3} / V _{DROP_LDO4} | I _{OUT} = 300mA, V _{OUT_LDO3} / V _{OUT_LDO4} = 1.8V (Note 5) | -- | -- | 150 | mV |
| Output Discharge Resistor | R _{DIS_LDO3} / R _{DIS_LDO4} | | -- | 10 | -- | Ω |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|-----|--|-----|---------|
| Over-Voltage Rising Threshold Detection | OVP_R_LDO3/ OVP_R_LDO4 | | -- | $V_{OUT_LDO3}/V_{OUT_LDO4} \times 120\%$ | -- | V |
| Over-Voltage Falling Threshold Detection | OVP_F_LDO3/ OVP_F_LDO4 | | -- | $V_{OUT_LDO3}/V_{OUT_LDO4} \times 110\%$ | -- | V |
| Under-Voltage Rising Threshold Detection | UVP_R_LDO3/ UVP_R_LDO4 | | -- | $V_{OUT_LDO3}/V_{OUT_LDO4} \times 90\%$ | -- | V |
| Under-Voltage Falling Threshold Detection | UVP_F_LDO3/ UVP_F_LDO4 | | -- | $V_{OUT_LDO3}/V_{OUT_LDO4} \times 80\%$ | -- | V |
| Quiescent Current | I_{Q_LDO3}/I_{Q_LDO4} | HWEN = 1.2V, $I_{OUT} = 0mA$ | -- | 22 | 27 | μA |
| | | HWEN = 0.3V (disable) | -- | 0.1 | 1 | |
| Short Circuit Current Limit | I_{sc_LDO3}/I_{sc_LDO4} | | 360 | -- | -- | mA |
| Current Limit | $I_{Limt_LDO3}/I_{Limt_LDO4}$ | 0x03[3:2] = 11 (LDO3 current limit = 360mA), 0x04[3:2] = 11 (LDO4 current limit = 360mA) | 360 | 415 | 470 | mA |
| Short Protection On Timer | $t_{scp_ON_LDO3}/t_{scp_ON_LDO4}$ | | -- | 2 | -- | ms |
| Short Protection Off Timer | $t_{scp_OFF_LDO3}/t_{scp_OFF_LDO4}$ | | -- | 40 | -- | ms |
| I²C Characteristics | | | | | | |
| SCL, SDA Low Input Voltage | $V_{I^2C_IL}$ | | -- | -- | 0.4 | V |
| SCL, SDA High Input Voltage | $V_{I^2C_IH}$ | | 1.2 | -- | -- | V |
| SCL, SDA Low Output Voltage | $V_{I^2C_OL}$ | | -- | -- | 0.4 | V |
| I ² C CLK Frequency | f_{SCL} | | 1 | -- | -- | MHz |
| I ² C Work Voltage | $V_{I^2C_int}$ | | -- | 1.8 | -- | V |
| Input Current Each IO Pin | $I_{IN_I^2C}$ | | -10 | -- | 10 | μA |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|------------------|----------------|-----------------|-----|-----|-----|------|
| Data Hold Time | $t_{DH_I^2C}$ | | 30 | -- | -- | ns |
| Data Set-Up Time | $t_{DS_I^2C}$ | | 70 | -- | -- | ns |

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at $T_A = 25^\circ\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

System Characteristics

The following system specifications are guaranteed by designed and are not performed in production testing. ($T_A = 25^\circ\text{C}$, unless otherwise specified.)

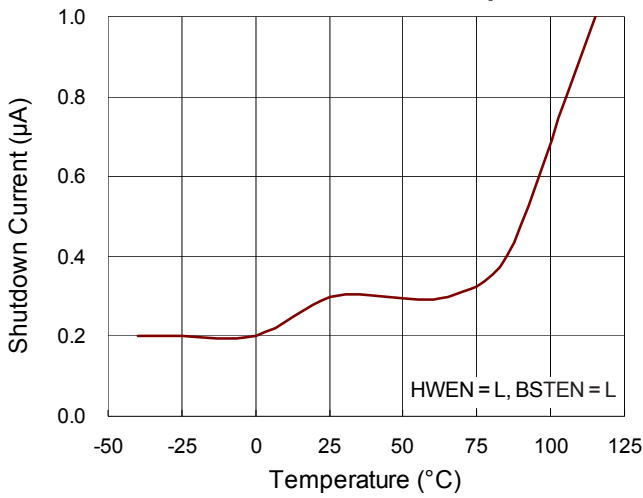
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|-----------------------|--|-----|-----|-----|------------------|
| System Parameter | | | | | | |
| Over-Temperature Warning | OTW | | 115 | 125 | 135 | $^\circ\text{C}$ |
| Over-Temperature Warning Hysteresis | OTW_H | | -- | 20 | -- | $^\circ\text{C}$ |
| Over-Temperature Protection | OTP | | 130 | 140 | 150 | $^\circ\text{C}$ |
| Over-Temperature Protection Hysteresis | OTP_H | 0x0A[4:3] = 01 | -- | 20 | -- | $^\circ\text{C}$ |
| HWEN and BSTEN Control | | | | | | |
| HWEN Turn On Delay | t_{HWEN_ON} | HWEN = H to I^2C operation available | -- | 50 | -- | μs |
| HWEN Turn Off Delay | t_{HWEN_OFF} | HWEN = L to I^2C operation stop | -- | 50 | -- | μs |
| BSTEN Turn On Delay | t_{BSTEN_ON} | BSTEN to Boost voltage start rising | -- | 225 | -- | μs |
| BSTEN Turn Off Delay | t_{BSTEN_OFF} | BSTEN off to Boost switch stop | -- | 16 | -- | μs |
| Step Down Buck Converter ($V_{IN_B} = 3.8\text{V}$, $C1 = C2 = 10\mu\text{F}$, $L1 = 1\mu\text{H}$) | | | | | | |
| Maximum Output Current | I_{OUT_BUCK} | | 1.2 | -- | -- | A |
| Load Regulation | $V_{LOAD_REG_BUCK}$ | CCM, $V_{OUT_BUCK} = 1.1\text{V}$ | -- | -- | 1.5 | % |
| Line Regulation | $V_{LINE_REG_BUCK}$ | CCM, $I_{OUT} = 50/300/1200\text{mA}$, $V_{OUT_BUCK} = 1.1\text{V}$, $V_{IN_B} = 3.0\text{V}$ to 4.4V | -- | -- | 1.5 | % |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|---------------------------|---|-----|-----|-----|------|
| Output Ripple | V _{RIPPLE_BUCK} | CCM, I _{OUT} = 300mA, V _{OUT_BUCK} = 1.1V, V _{IN_B} < 4.35V | -- | -- | 10 | mV |
| | | PFM, V _{OUT_BUCK} = 1.1V, V _{IN_B} < 4.35V | -- | 30 | 40 | |
| Soft-Start Time | t _{SS_BUCK} | 0x09[7:6] = 10, time from V _{OUT_BUCK} = 0V rising to 90% nominal value, V _{OUT_BUCK} = 1.1V, no load | -- | 235 | -- | μs |
| Load Transient | V _{TRAN_BUCK} | V _{OUT_BUCK} = 1.1V, 20 to 80% I _{OUT(MAX)} , 1μs, recovery time < 10μs | -- | -- | 70 | mV |
| Efficiency | Eff _{BUCK} | V _{OUT_BUCK} = 1.1V, I _{OUT} = 200mA to 600mA | 85 | -- | -- | % |
| Step Up Boost Converter (V_{IN_BST} = 3.8V, C₃ = 10μF, C₄ = 22μF, L₂ = 0.47μH) | | | | | | |
| Maximum Output Current | I _{OUT_BST} | V _{IN_BST} = 2.8V, V _{OUT_BST} = 5V | 1 | -- | -- | A |
| Soft-Start Time | t _{SS_BST} | 0x05[5:4] = 00, time from V _{OUT_BST} = 0V rising to 90% nominal value, V _{OUT_BST} = 5V, no load | -- | -- | 580 | μs |
| Start Up Time | t _{START_BST} | Time from BSTEN = H to V _{OUT_BST} rising to 90% nominal value, V _{OUT_BST} = 5V, no load | -- | -- | 700 | μs |
| Load Regulation | V _{LOAD_REG_BST} | CCM, V _{OUT_BST} = 5V | -- | -- | 1.5 | % |
| Line Regulation | V _{LINE_REG_BST} | CCM, I _{OUT} = 50/1000mA, V _{IN_BST} = 3V to 4.4V, V _{OUT_BST} = 5V | -- | -- | 1.5 | % |
| Output Ripple | V _{RIPPLE_BST} | CCM, I _{OUT} = 500mA, V _{IN_BST} = 3.4V to 4.4V, V _{OUT_BST} = 5V | -- | -- | 40 | mV |
| | | PFM, V _{IN_BST} = 3.4V to 4.4V, V _{OUT_BST} = 5V | -- | 40 | 80 | |
| Load Transient | V _{TRAN_BST} | V _{OUT_BST} = 5V, 20 to 80% I _{OUT(MAX)} , 2μs, recovery time < 30μs | -- | 100 | 150 | mV |
| Power Efficiency | Eff _{BST} | V _{OUT_BST} = 5V, V _{IN_BST} = 3.4V, I _{OUT_BST} = 10mA | -- | 88 | -- | % |
| | | V _{OUT_BST} = 5V, V _{IN_BST} = 3.4V, I _{OUT_BST} = 600mA | -- | 90 | -- | |
| | | V _{OUT_BST} = 5V, V _{IN_BST} = 3.4V, I _{OUT_BST} = 1A | -- | 84 | -- | |
| Linear Charge Hiccup On Time | t _{LC_ON} | During linear charge state | -- | 10 | -- | ms |

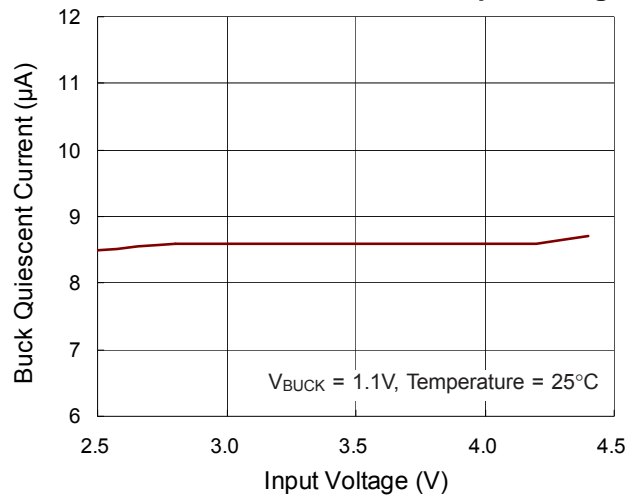
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-------------------------------------|--|-----|-----|-----|---------|
| Linear Charge Hiccup Off Time | t_{LC_OFF} | Restart linear charge | -- | 100 | -- | ms |
| ABS Output Over-Voltage Rising Threshold | OVP_R_ABS_BST | Stop switch | -- | 6.5 | -- | V |
| ABS Output Over-Voltage Falling Threshold | OVP_F_ABS_BST | Start switch | -- | 5.8 | -- | V |
| Low Dropout Voltage Regulator LDO1 and LDO2 ($V_{IN_VIN12} = V_{OUT_LDO1}/V_{OUT_LDO2} + 1V$, $V_{HWEN} = 1.2V$, $I_{OUT} = 1mA$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 2.2\mu F$) | | | | | | |
| Output Ripple Voltage | $V_{RIPPLE_LDO1}/V_{RIPPLE_LDO2}$ | $I_{OUT} = 0$ to $I_{OUT(MAX)}$, $V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V$ | -- | -- | 10 | mV |
| Load Transient | $V_{TRAN_LDO1}/V_{TRAN_LDO2}$ | $I_{OUT} = 1mA$ to $150mA$, $150mA/\mu s$, $V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V$ | -- | -- | 50 | mV |
| Power Supply Rejection Ratio | PSRR_LDO1/ PSRR_LDO2 | $V_{IN_VIN12} = 3.4V$, $f = 1kHz$, $I_{OUT} = 100mA$, $V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V$ | 70 | -- | -- | dB |
| | | $V_{IN_VIN12} = 3.4V$, $f = 100kHz$, $I_{OUT} = 100mA$, $V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V$ | 40 | -- | -- | |
| Output Noise Voltage | e_{N_LDO1}/e_{N_LDO2} | 100Hz to 100kHz, $I_{OUT} = 100mA$, $V_{OUT_LDO1}/V_{OUT_LDO2} = 2.8V$ | -- | 50 | -- | μV |
| Low Dropout Voltage Regulator LDO3 and LDO4 ($V_{IN_VIN3}/V_{IN_VIN4} = V_{OUT_LDO3}/V_{OUT_LDO4} + 1V$, $V_{HWEN} = 1.2V$, $I_{OUT} = 1mA$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 2.2\mu F$) | | | | | | |
| Output Ripple Voltage | $V_{RIPPLE_LDO3}/V_{RIPPLE_LDO4}$ | $I_{OUT} = 0$ to $I_{OUT(MAX)}$, $V_{OUT_LDO3}/V_{OUT_LDO4} = 1.8V$ | -- | -- | 10 | mV |
| Load Transient | $V_{TRAN_LDO3}/V_{TRAN_LDO4}$ | $I_{OUT} = 1mA$ to $150mA$, $150mA/\mu s$, $V_{OUT_LDO3}/V_{OUT_LDO4} = 1.8V$ | -- | -- | 50 | mV |
| Power Supply Rejection Ratio | PSRR_LDO3/ PSRR_LDO4 | $V_{IN_VIN3} / V_{IN_VIN4} = 1.95V$, $f = 1kHz$, $I_{OUT} = 100mA$, $V_{OUT_LDO3}/V_{OUT_LDO4} = 1.8V$ | 50 | -- | -- | dB |
| | | $V_{IN_VIN3} / V_{IN_VIN4} = 1.95V$, $f = 10kHz$, $I_{OUT} = 100mA$, $V_{OUT_LDO3}/V_{OUT_LDO4} = 1.8V$ | 40 | -- | -- | |
| Output Noise Voltage | e_{N_LDO3}/e_{N_LDO4} | 100Hz to 100kHz, $I_{OUT} = 100mA$, $V_{OUT_LDO3}/V_{OUT_LDO4} = 1.8V$ | -- | 50 | -- | μV |

Typical Operating Characteristics

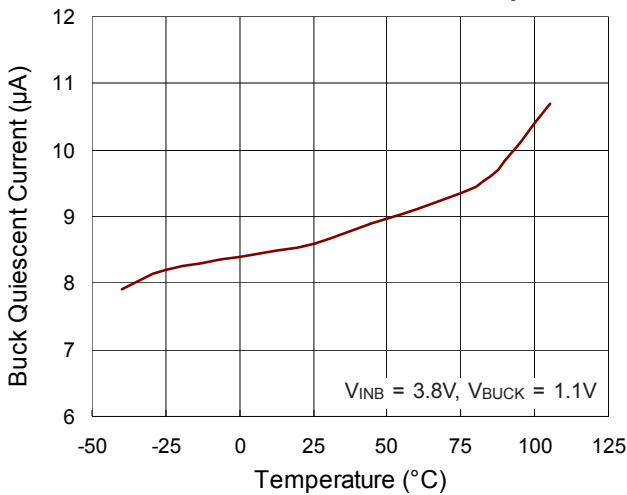
Shutdown Current vs. Temperature



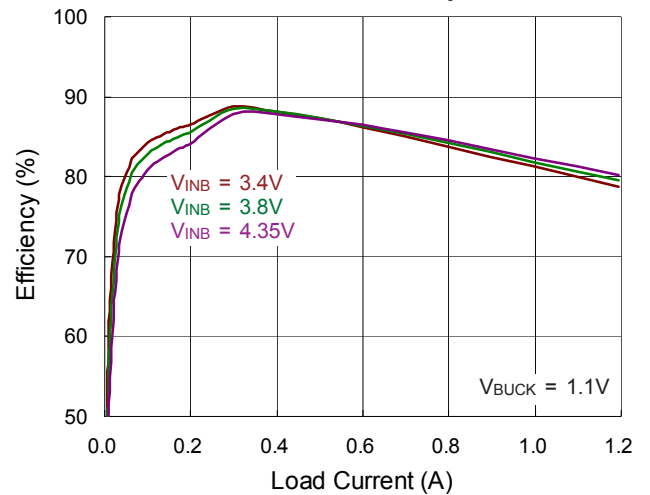
Buck Quiescent Current vs. Input Voltage



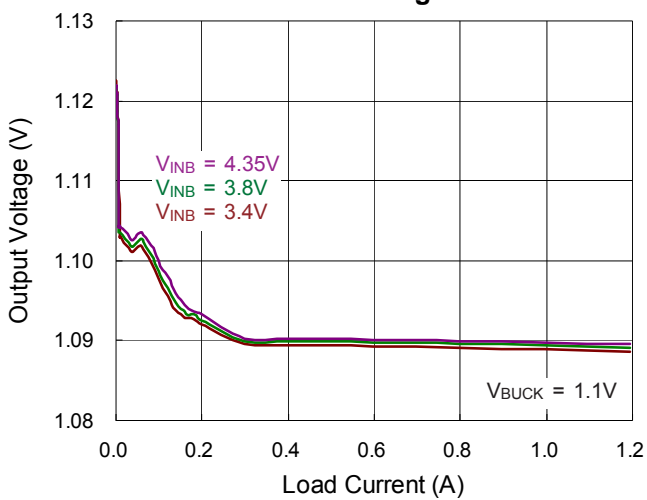
Buck Quiescent Current vs. Temperature



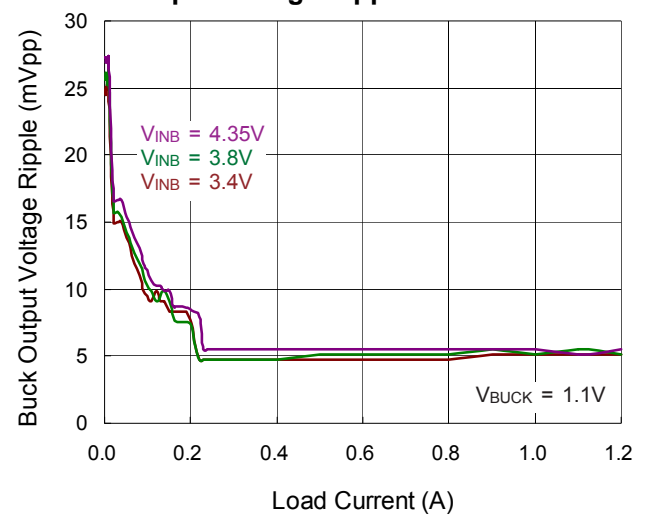
Buck Efficiency



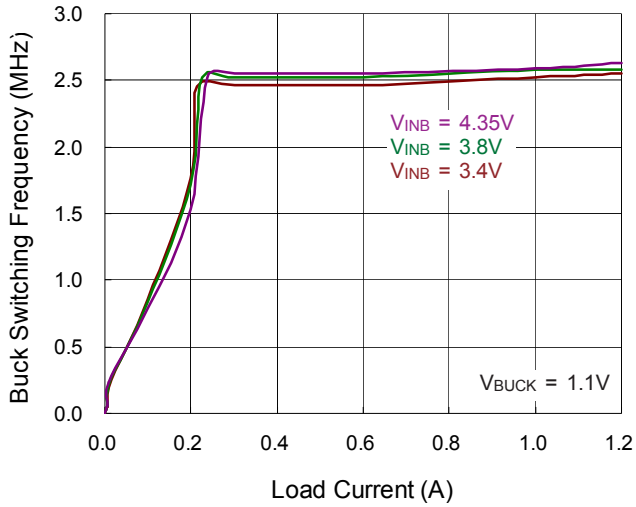
Buck Load Regulation



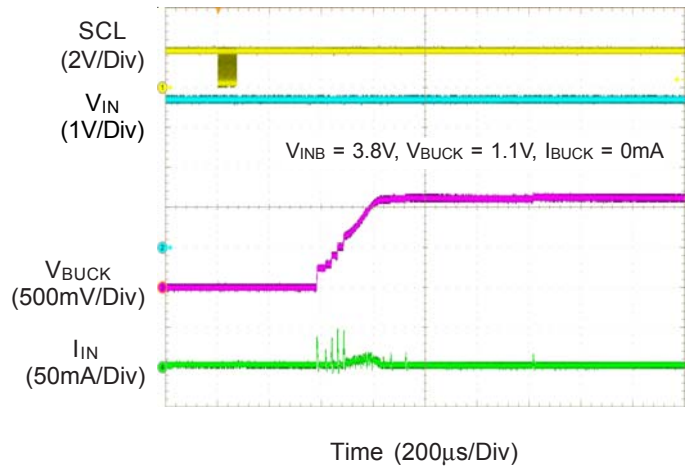
Buck Output Voltage Ripple vs. Load Current



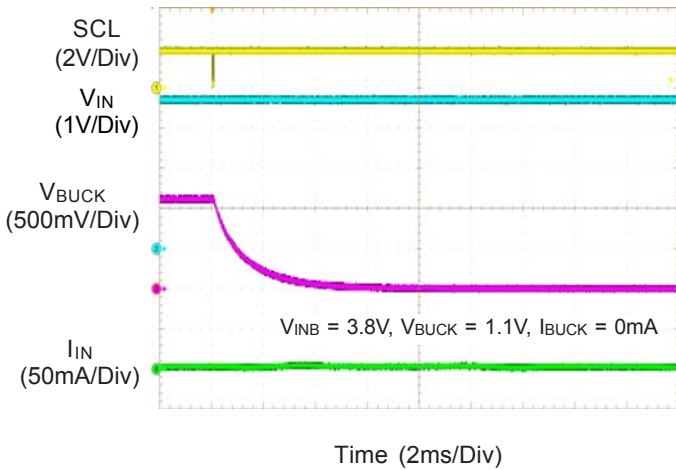
Buck Switching Frequency vs. Load Current



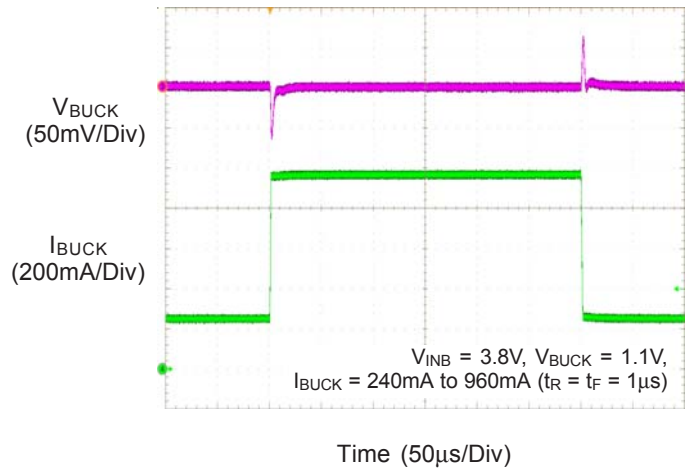
Buck Power On



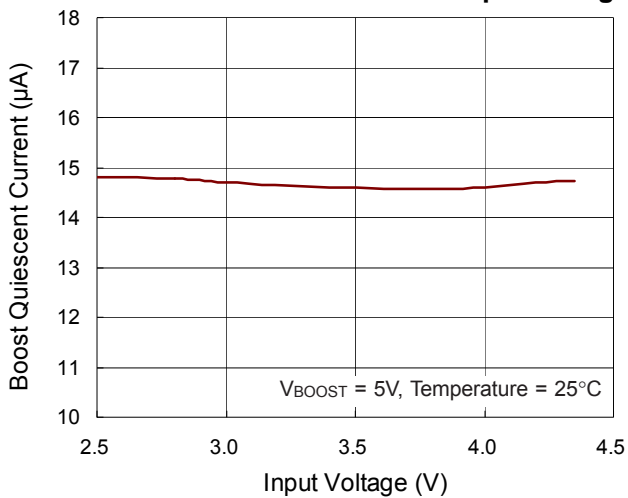
Buck Power Off



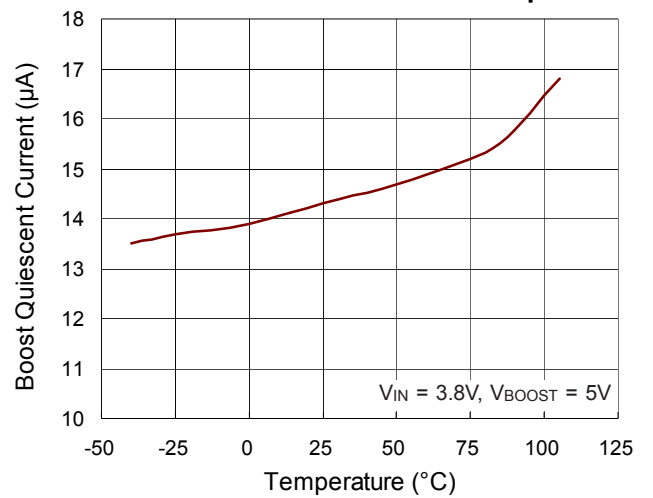
Buck Load Transient



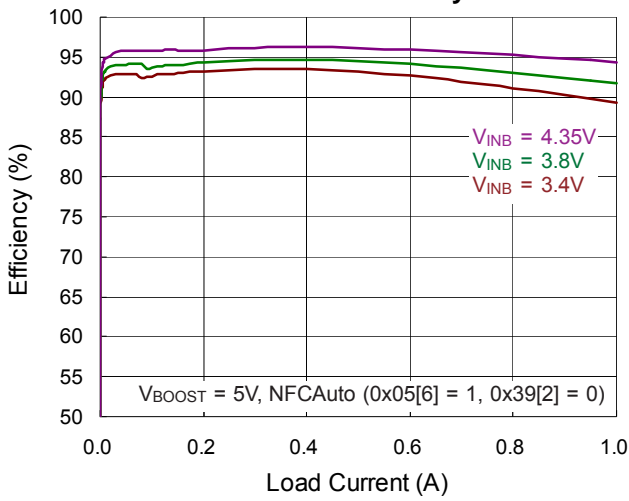
Boost Quiescent Current vs. Input Voltage



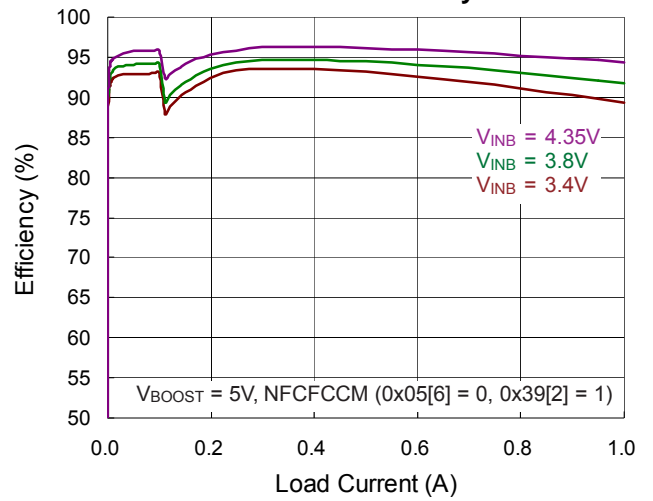
Boost Quiescent Current vs. Temperature



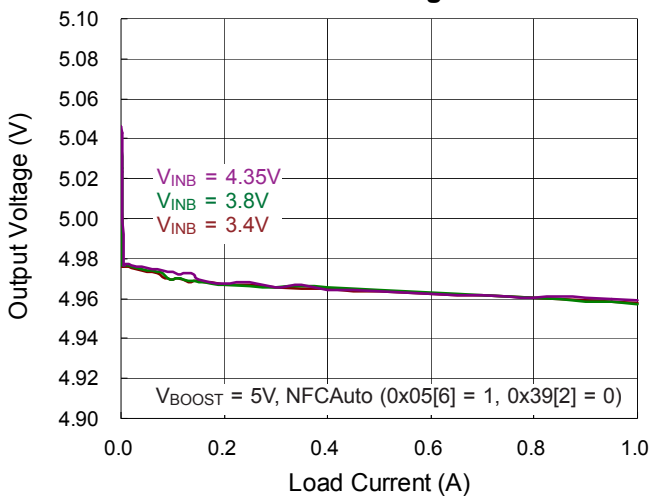
Boost Efficiency



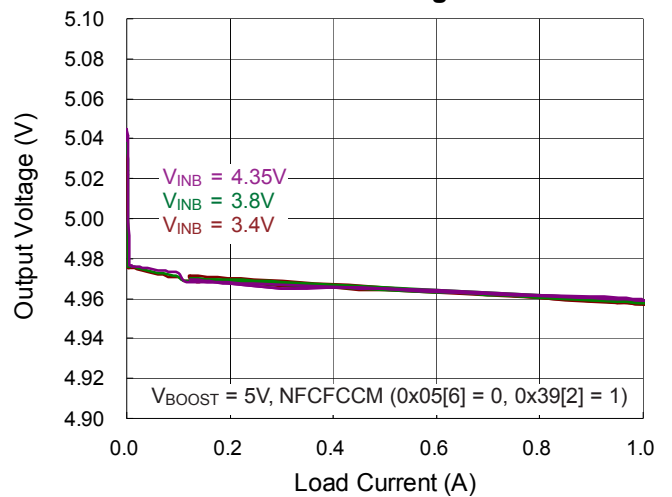
Boost Efficiency



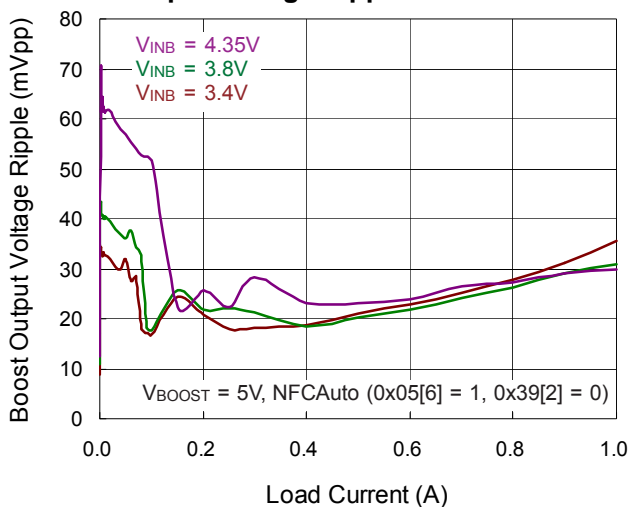
Boost Load Regulation



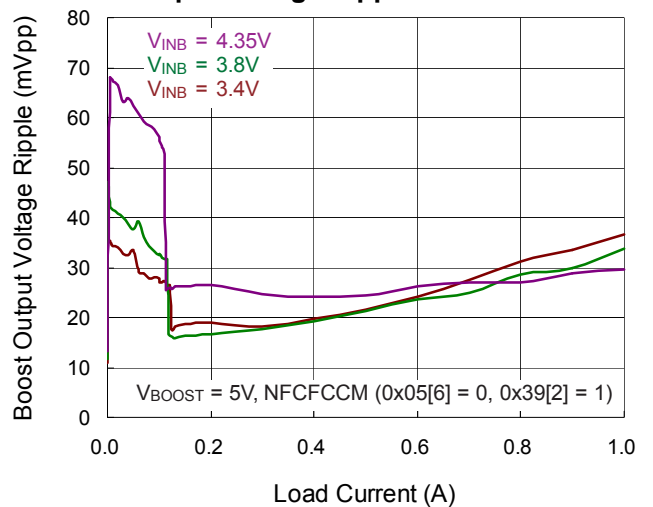
Boost Load Regulation

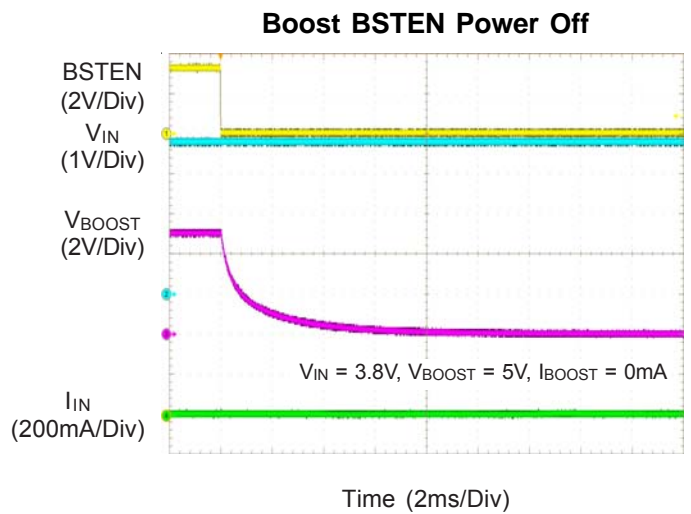
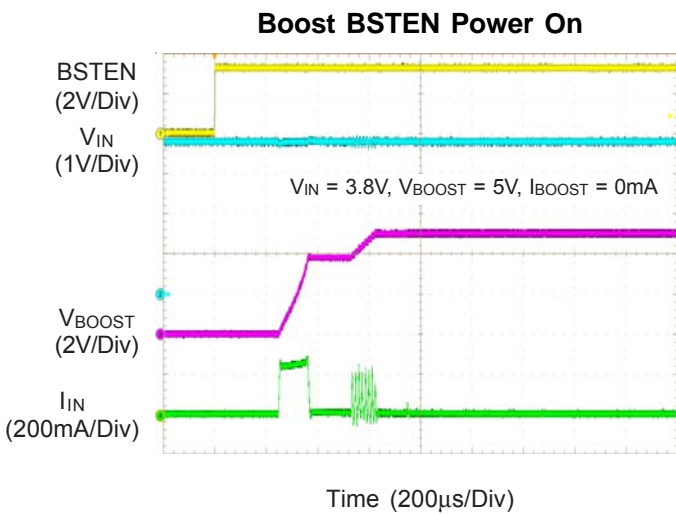
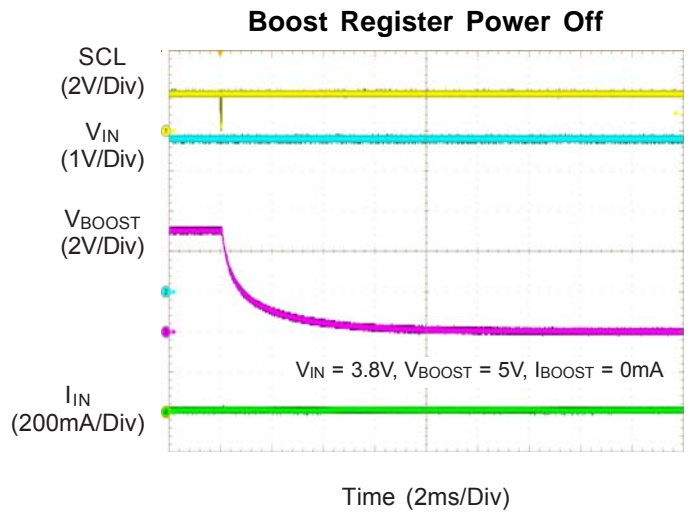
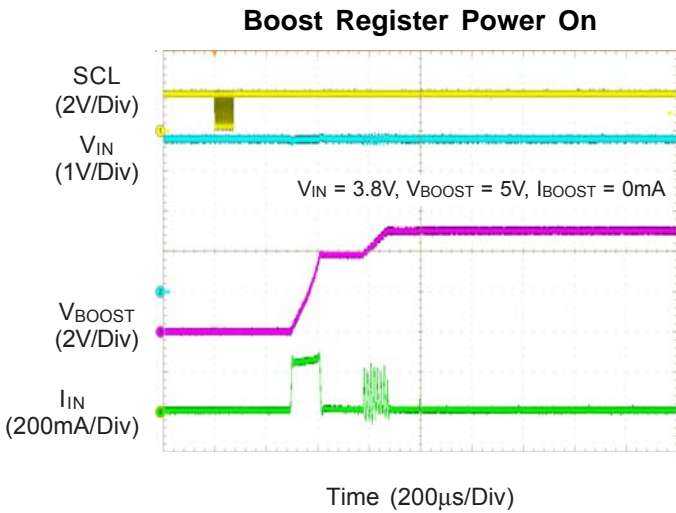
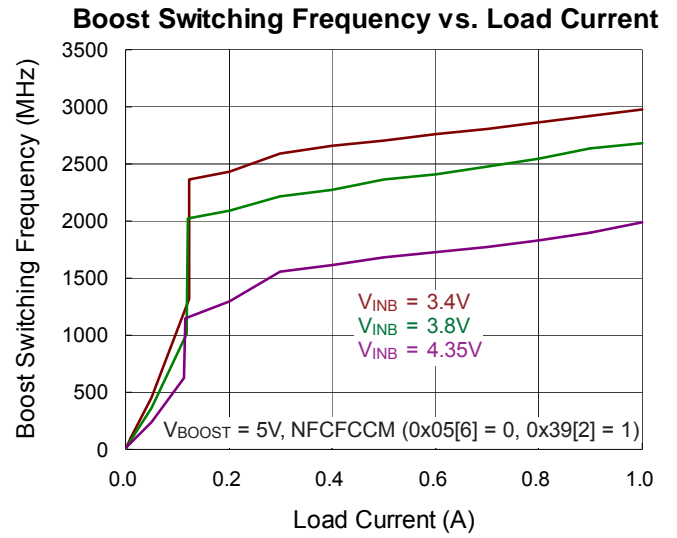
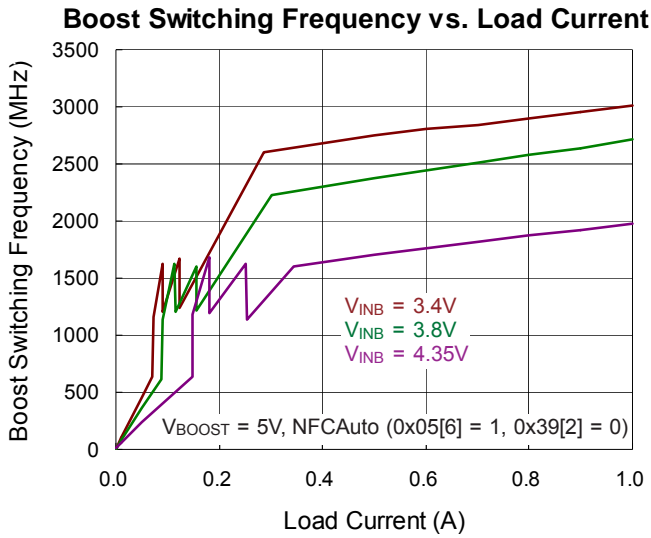


Boost Output Voltage Ripple vs. Load Current

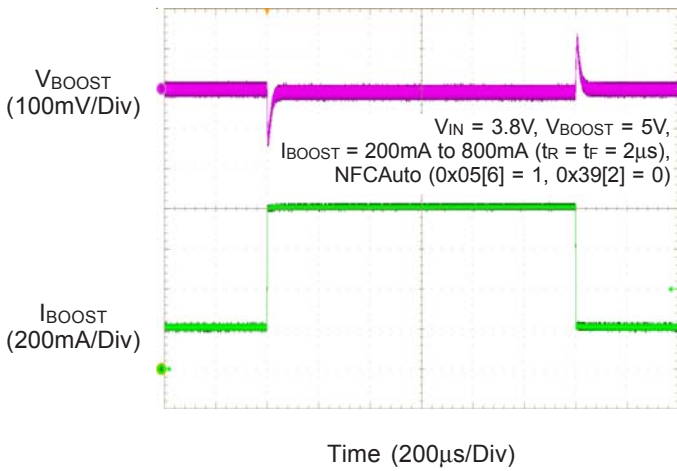


Boost Output Voltage Ripple vs. Load Current

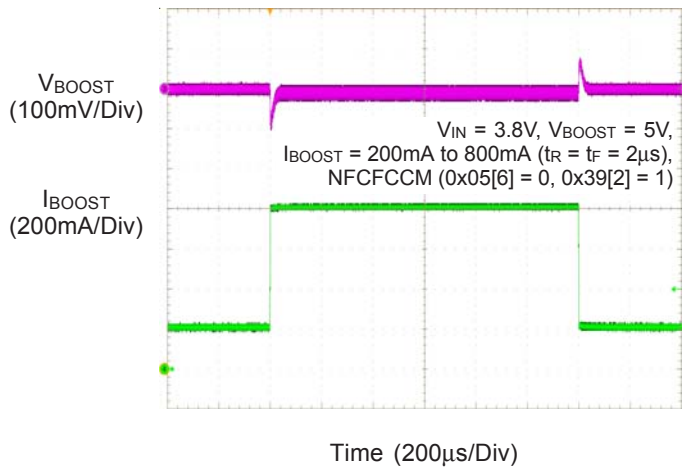




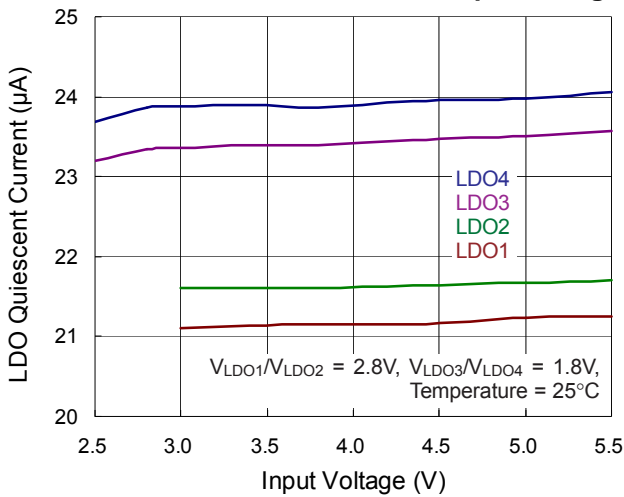
Boost Load Transient



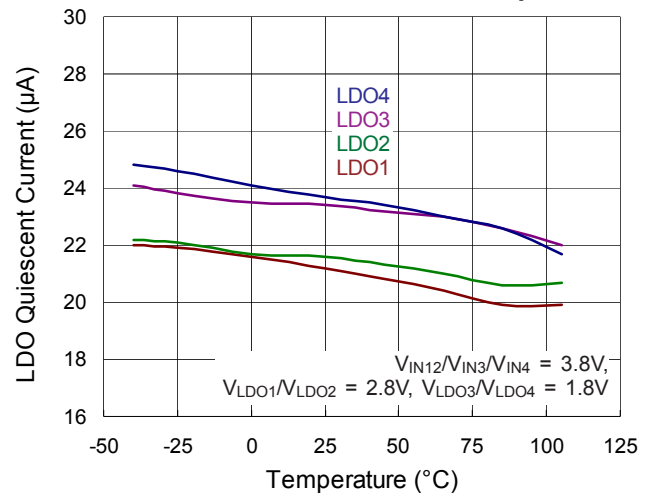
Boost Load Transient



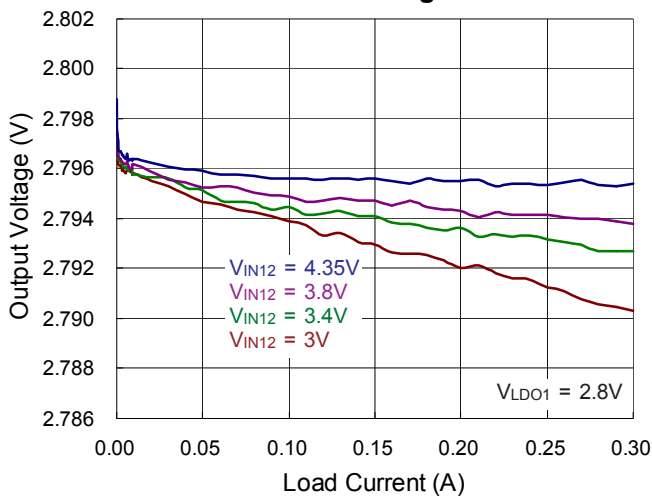
LDO Quiescent Current vs. Input Voltage



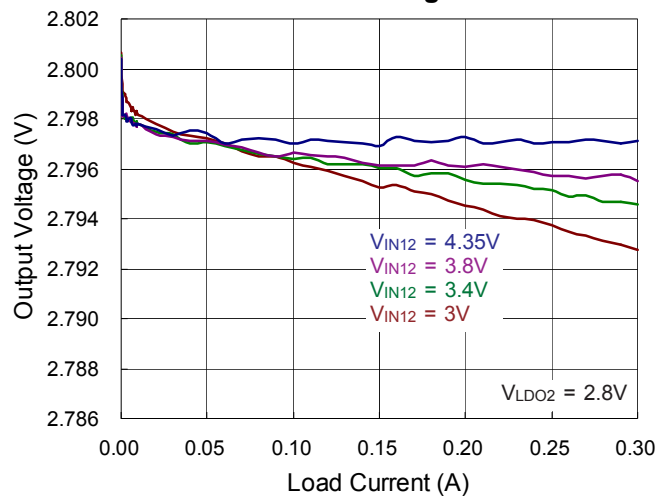
LDO Quiescent Current vs. Temperature



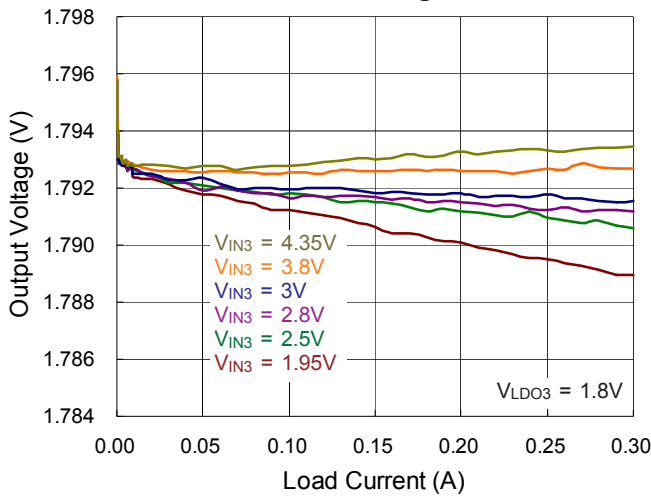
LDO1 Load Regulation



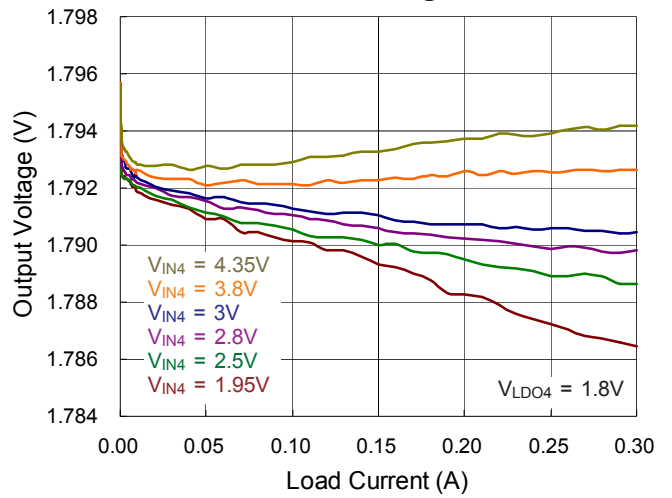
LDO2 Load Regulation



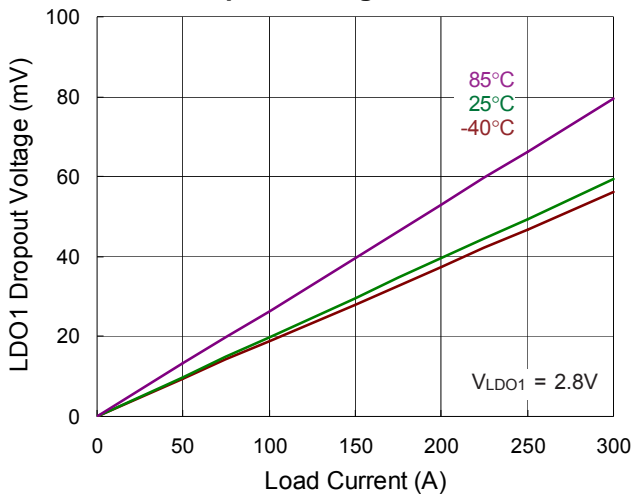
LDO3 Load Regulation



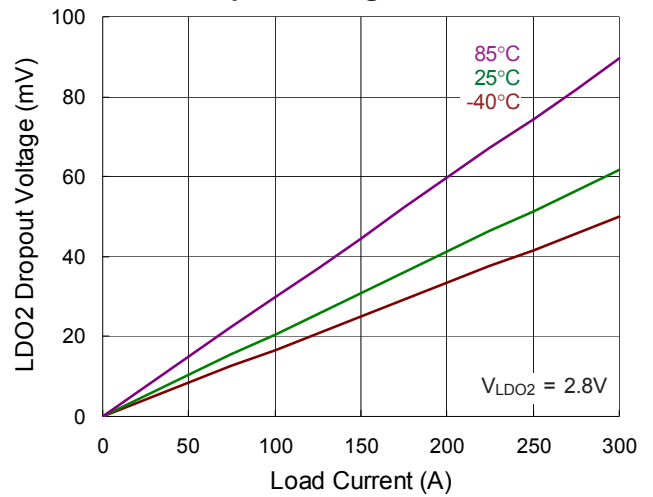
LDO4 Load Regulation



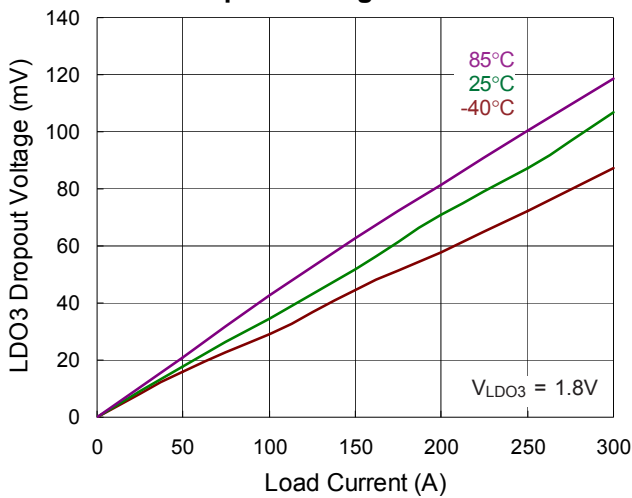
LDO1 Dropout Voltage vs. Load Current



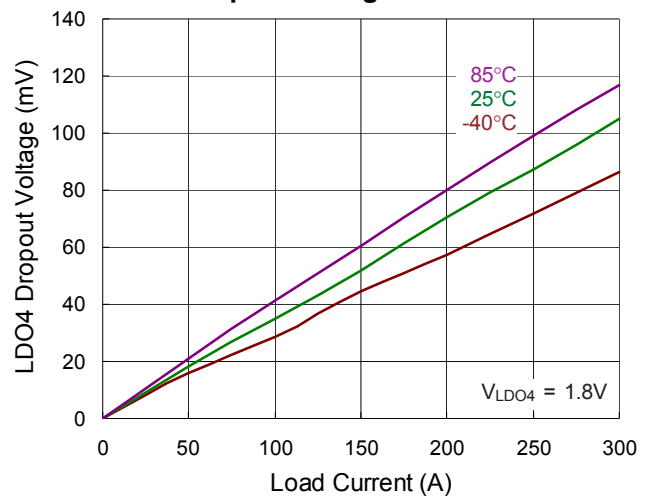
LDO2 Dropout Voltage vs. Load Current

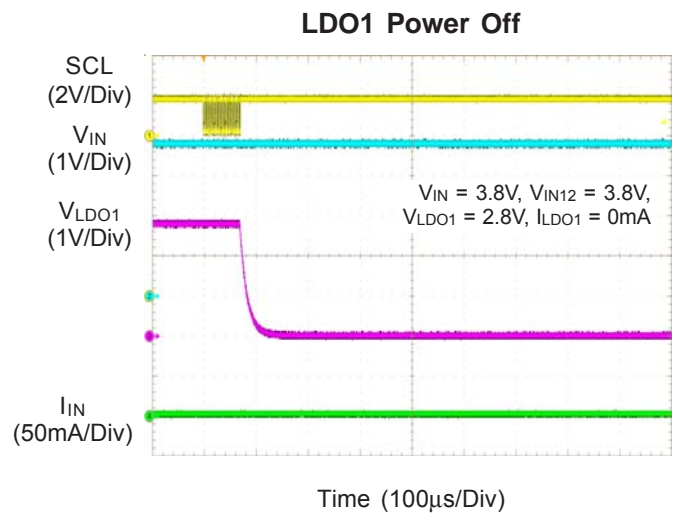
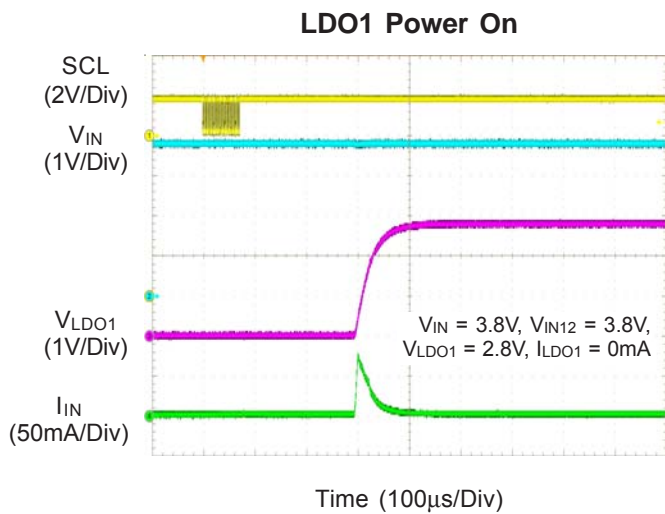
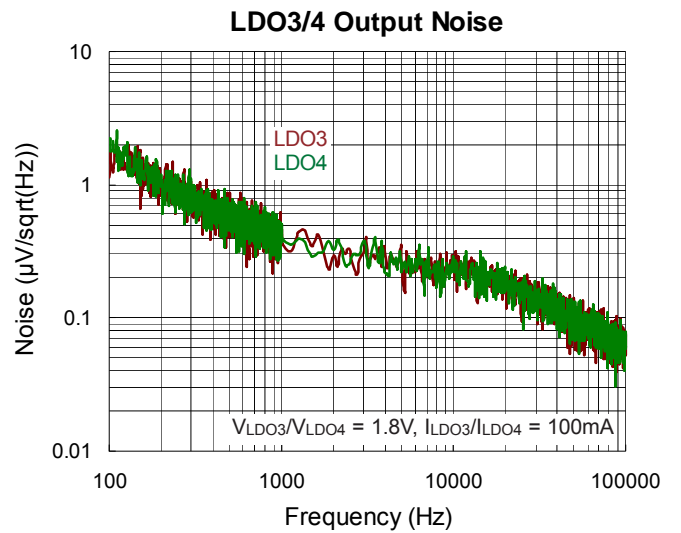
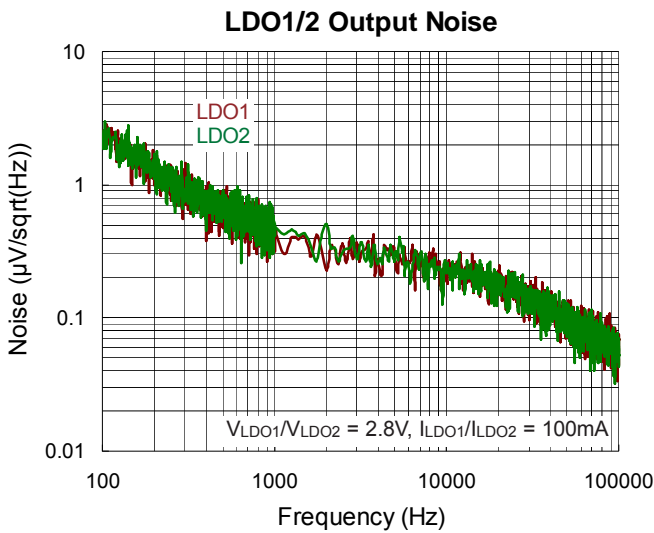
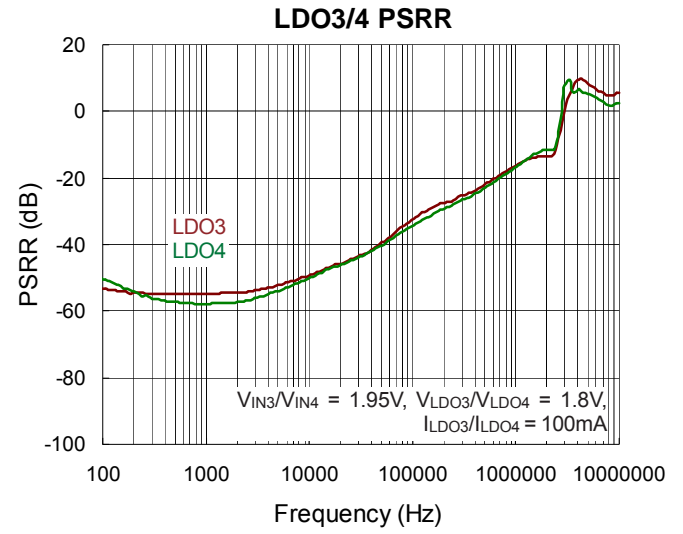
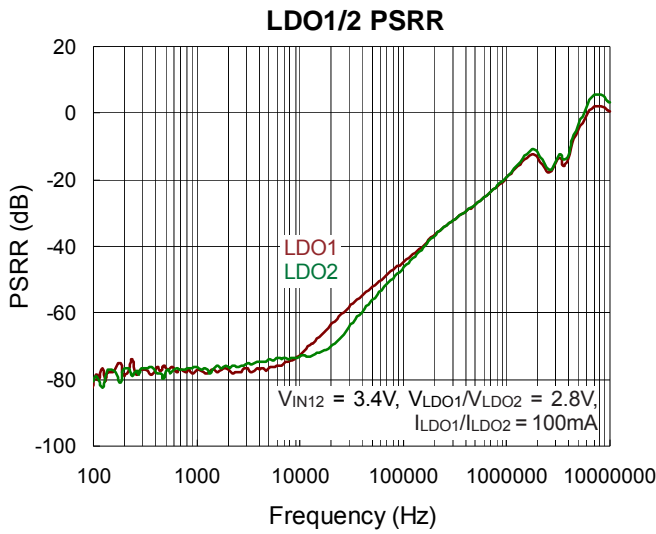


LDO3 Dropout Voltage vs. Load Current

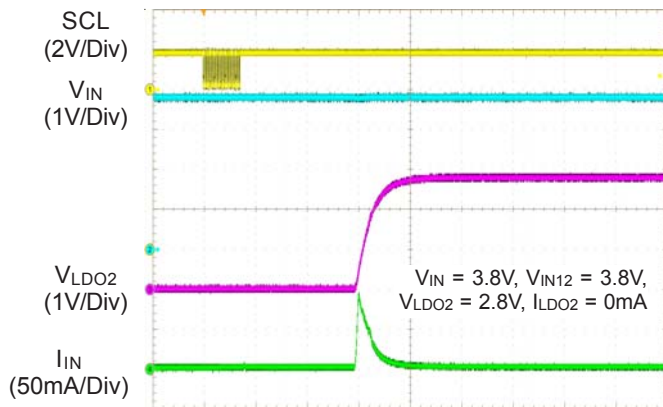


LDO4 Dropout Voltage vs. Load Current



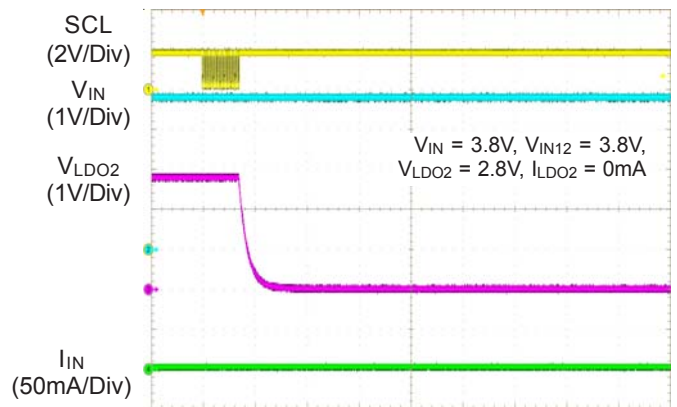


LDO2 Power On



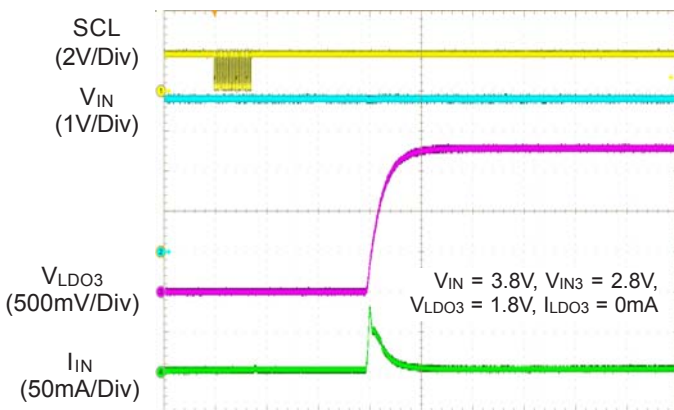
Time (100µs/Div)

LDO2 Power Off



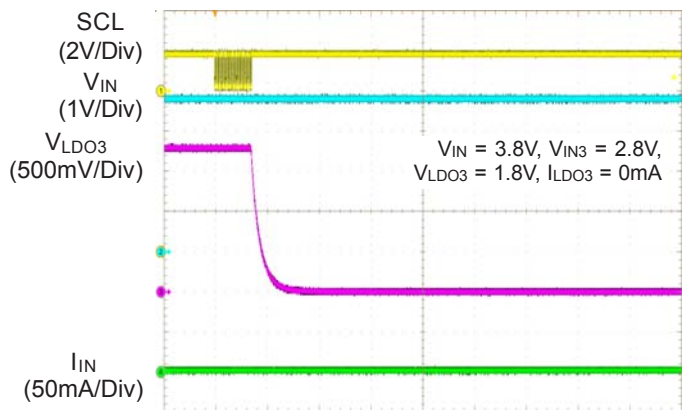
Time (100µs/Div)

LDO3 Power On



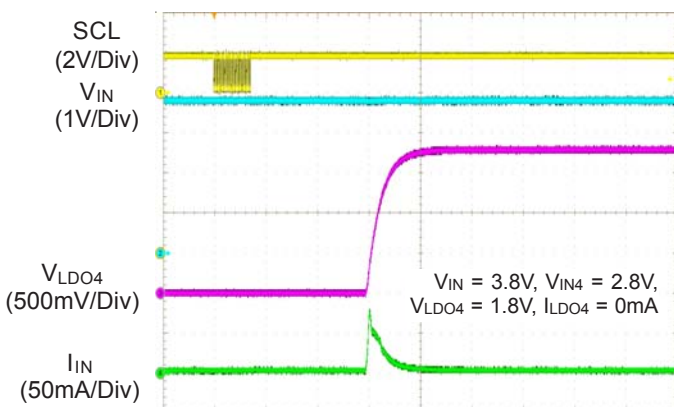
Time (100µs/Div)

LDO3 Power Off



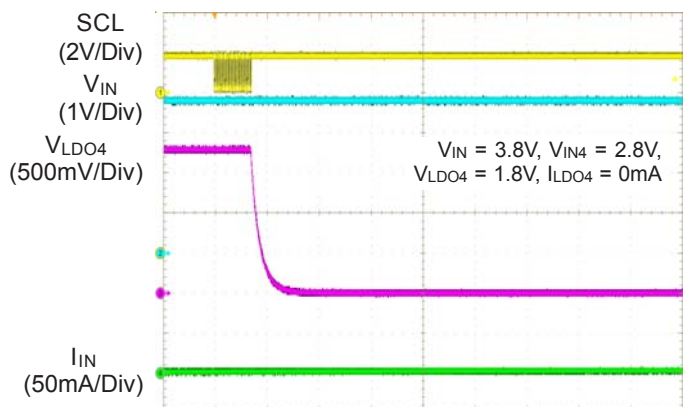
Time (100µs/Div)

LDO4 Power On



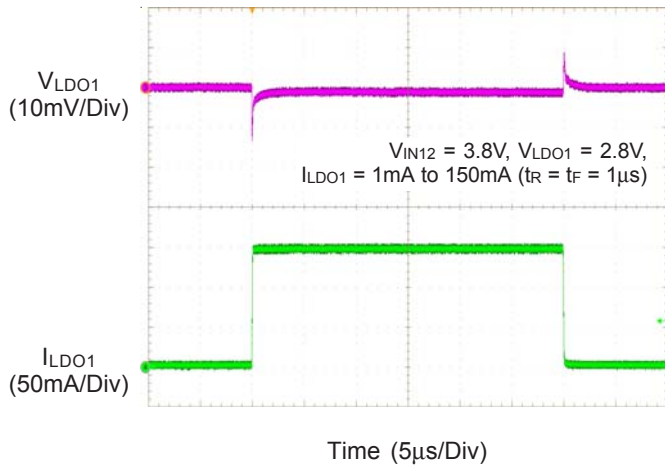
Time (100µs/Div)

LDO4 Power Off

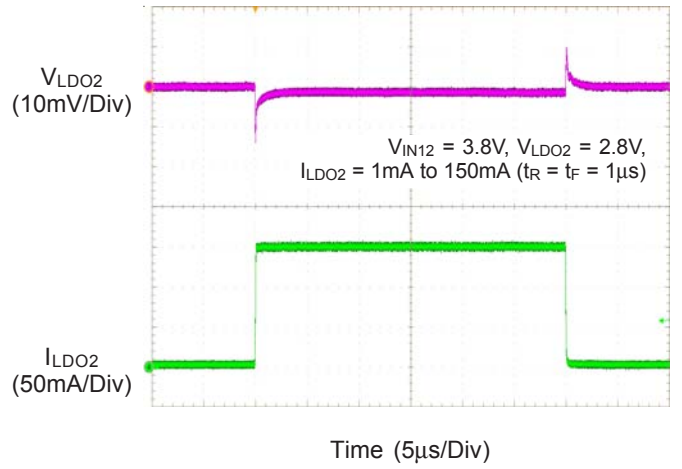


Time (100µs/Div)

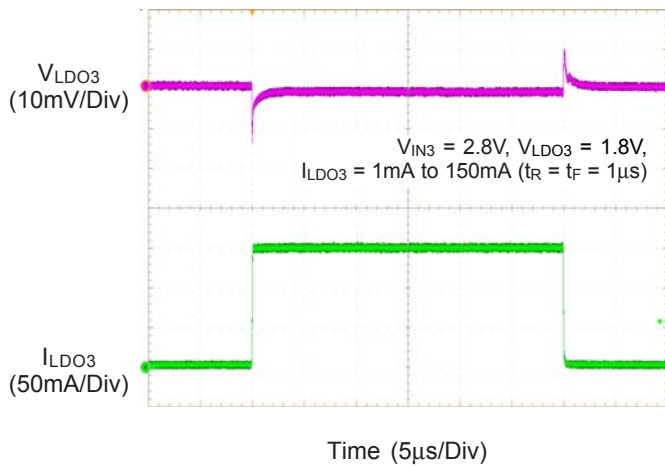
LDO1 Load Transient



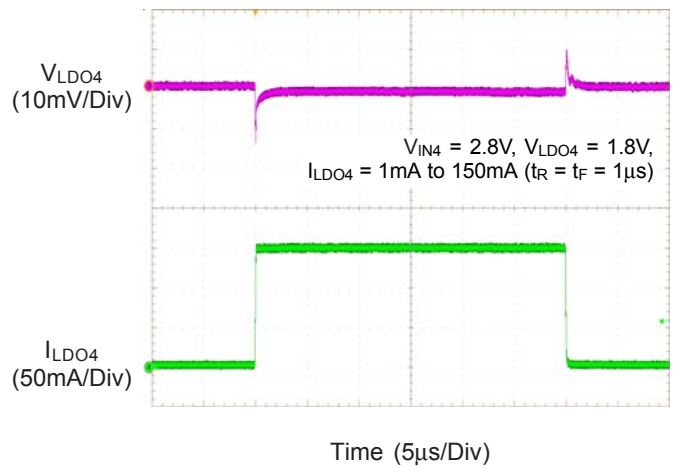
LDO2 Load Transient



LDO3 Load Transient



LDO4 Load Transient



Application Information

The RT5112 is a smart power-management integrated circuit (PMIC), which includes a Buck converter, a Boost converter and four LDOs.

System Under-Voltage Protection and Over-Voltage Protection

The device does not operate with V_{SYS} voltages below the Under-Voltage Lock Out (UVLO) level. There is a typical 100mV hysteresis implemented to avoid unstable on/ off behavior. The RT5112 is initialized in its default state after V_{SYS} voltage recovers from UVLO. When V_{SYS} voltage reaches the Over Voltage Protection level, the RT5112 will disable Buck converter immediately to protect next stage circuit input. The V_{SYS} UV and OV status bits and interrupt bits will be set, and INTRB pin will be pulled low with corresponding to protection detected.

Thermal Protection

The RT5112 features over-temperature warning (OTW) and over-temperature protection (OTP). The OTW status bit and interrupt bit are set and INTRB pin will be pulled low when the junction temperature is higher than typical 125°C. If the junction temperature further exceeds typical 160°C, OTP will be triggered to shut down the device.

When the RT5112 recovers from OTP, it can re-start in three configurations with register 0x0A[4:3] bits.

- 0x0A[4:3] = 00, the RT5112 is manual re-start with default register values.
- 0x0A[4:3] = 01, the RT5112 is auto recovery with last register values before OTP.
- 0x0A[4:3] = 10, the RT5112 is latched off. Re-set V_{IN} or HWEN or BSTEN (if Boost is controlled by BSTEN) to re-start the RT5112 with default register values.

Enable and Disable Control

The HWEN pin controls the RT5112 start up without enabling channels. If HWEN pin is at low state, the RT5112 is in power down mode and I²C will return NACK to any request. Only when HWEN pin is at high state, all channels are controllable via I²C with corresponding ENABLE command. The BSTEN pin is only used to hardware control Boost converter enable or disable. There are both built-in resistors on HWEN and BSTEN pins to keep at low state if pins are left unconnected.

The below tables provide channels state with combinations of different ENABLE pins and register EN bits.

- **Buck and LDOs**

Table 1. Buck and LDOs Control

| HWEN pin | SEQ bits | EN bits | SEQ_CTRL bits Dependent | On / Off |
|----------|----------|---------|-------------------------|----------|
| Low | 000 | 0 | No | Off |
| Low | 000 | 1 | No | Off |
| Low | ≠000 | 0 | No | Off |
| Low | ≠000 | 1 | No | Off |
| High | 000 | 0 | No | Off |
| High | 000 | 1 | No | On |
| High | ≠000 | 0 | Yes | On |
| High | ≠000 | 1 | CTRL | On / Off |

Note : CTRL indicates several operating conditions as below.

- (1) SEQ_CTRL[1:0] = 00, set SEQ bits ≠ 000 and EN bit = 1, channel is turned off after 7 sequence slot count regardless EN bit.
- (2) SEQ_CTRL[1:0] = 01, set SEQ bits 000 and EN bit = 1, channel is turned on depends on EN bit.

▶ Sequence Control Setting

The RT5112 Buck and LDOs sequence on/off control setting can be programmed via I²C with dedicated registers as below.

◆ Sequence (7 slots)

Register 0x00[6:4] is used to control Buck sequence on/off slot.

Registers 0x01[6:4], 0x02[6:4], 0x03[6:4] and 0x04[6:4] are used to control LDOs sequence on/off slots.

◆ Slot Interval Time

Register 0x09[7:6] is used to control interval time between each slot.

◆ Soft Start Time

Register 0x09[7:6] is used to control Buck sequence on soft start time.

Register 0x11[1:0] is used to control LDOs sequence on soft start time.

◆ Sequence Control

Register 0x09[5:4] = 00 is used to enable sequence off with sequence setting \neq 000.

Register 0x09[5:4] = 01 is used to enable sequence on with sequence setting 000.

Note :

(1) Any changes in Sequence (7 slots), slot interval time and soft-start time during sequence on or off procedure is not valid and will not modify the RT5112 setting.

(2) Channel setting (output voltage, current limit...etc.) is fixed during on or off sequence.

(3) Register 0x09[5:4] = 11 will turn off all channels immediately.

(4) HWEN = 0 will turn off all channels and the RT5112 enters into power down mode.

▶ Normal Control Setting

When register bits 0x09[5:4] = 10, the Buck and LDOs on/off control depends on channel Enable bit.

◆ Register 0x00[7] is used to control Buck on/off.

◆ Register 0x01[7], 0x02[7], 0x03[7] and 0x04[7] are used to control LDOs on/off.

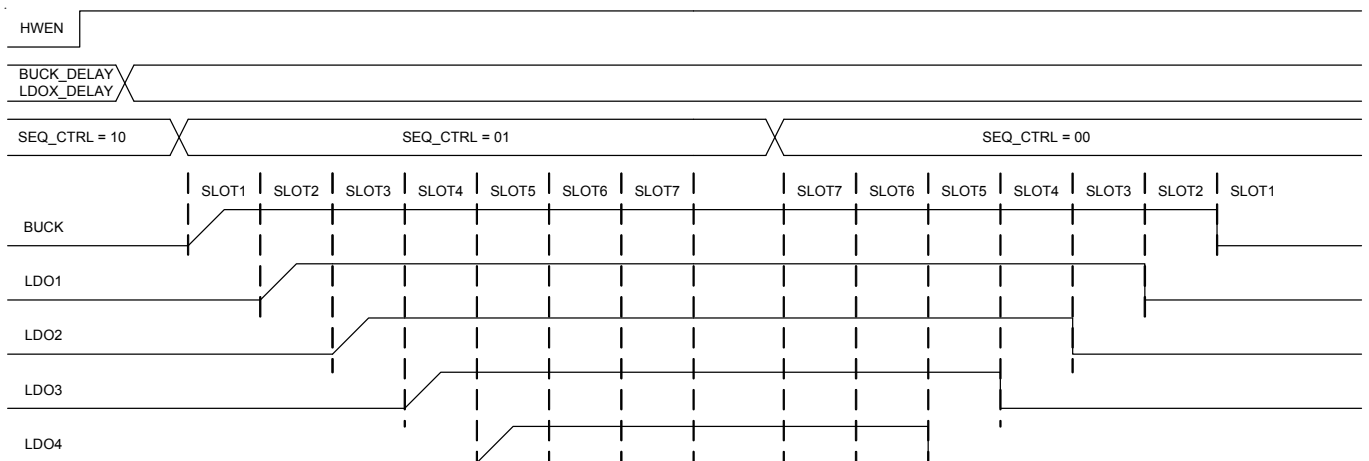


Figure 1.

Example for sequence on/off with BUCK assign to SLOT1, LDO1 assign to SLOT2, LDO2 assign to SLOT3, LDO3 assign to SLOT4 and LDO4 assign to SLOT5.

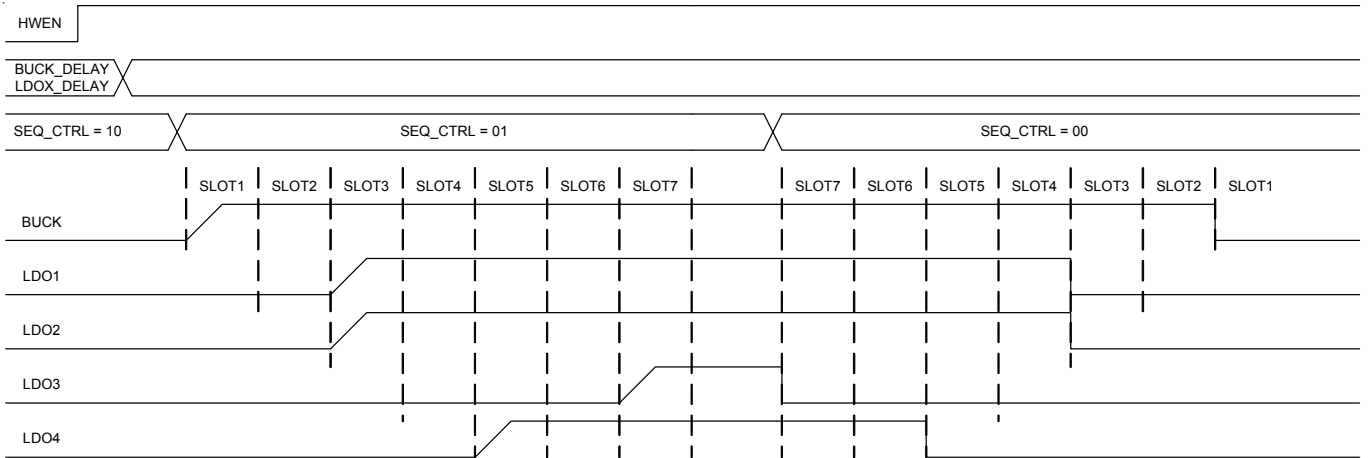


Figure 2.

Example for sequence on/off with BUCK assign to SLOT1, LDO1 assign to SLOT3, LDO2 assign to SLOT3, LDO3 assign to SLOT7 and LDO4 assign to SLOT5.

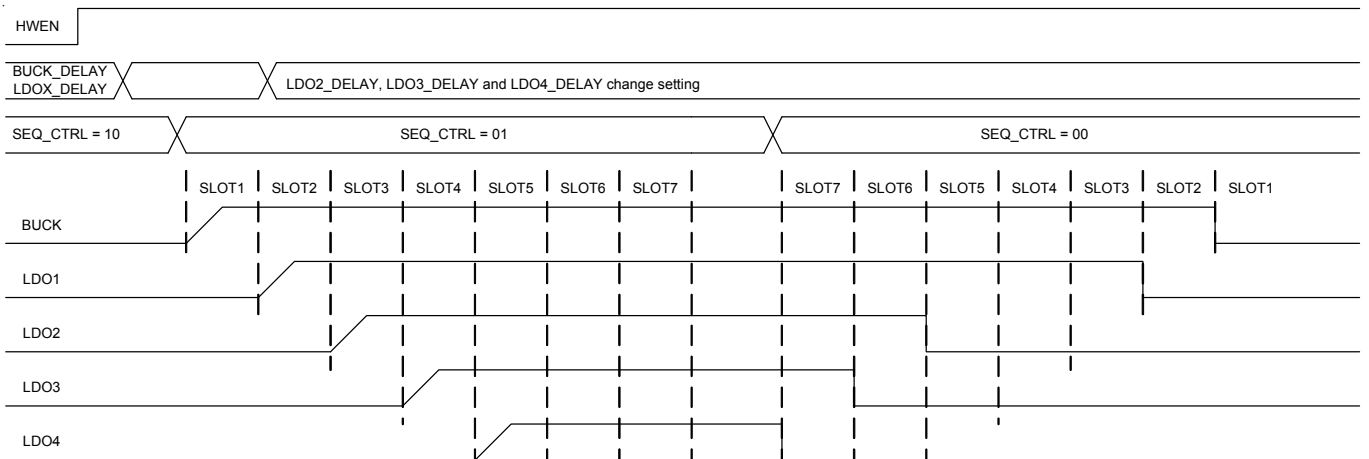


Figure 3.

Example for sequence slot change when on procedure. LDO2 assign from SLOT3 to SLOT5, LDO3 assign from SLOT4 to SLOT6 and LDO4 assign from SLOT5 to SLOT7. There is no influence with on procedure and new setting will executed after on sequence finish.

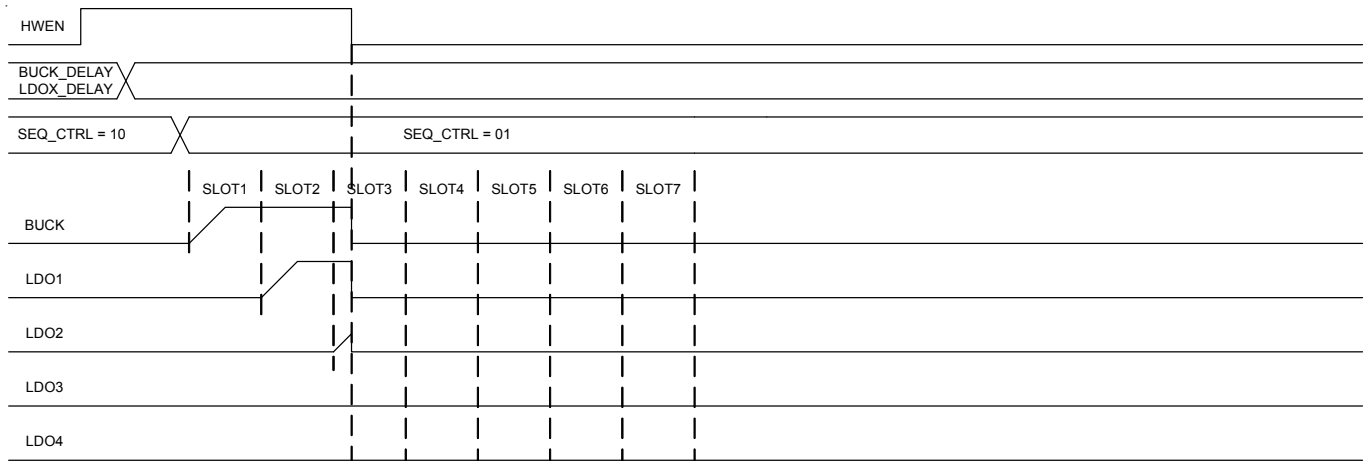


Figure 4.

Example for sequence on is interrupted by HWEN signal low. The RT5112 turns off all channels immediately.

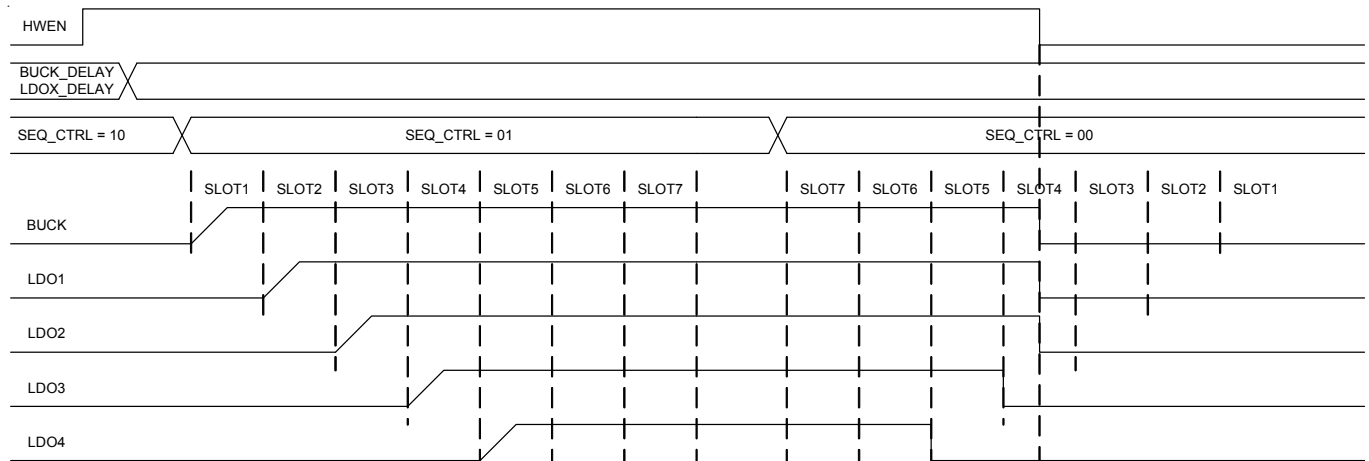


Figure 5.

Example for sequence off is interrupted by HWEN signal low. The RT5112 turns off all channels immediately.

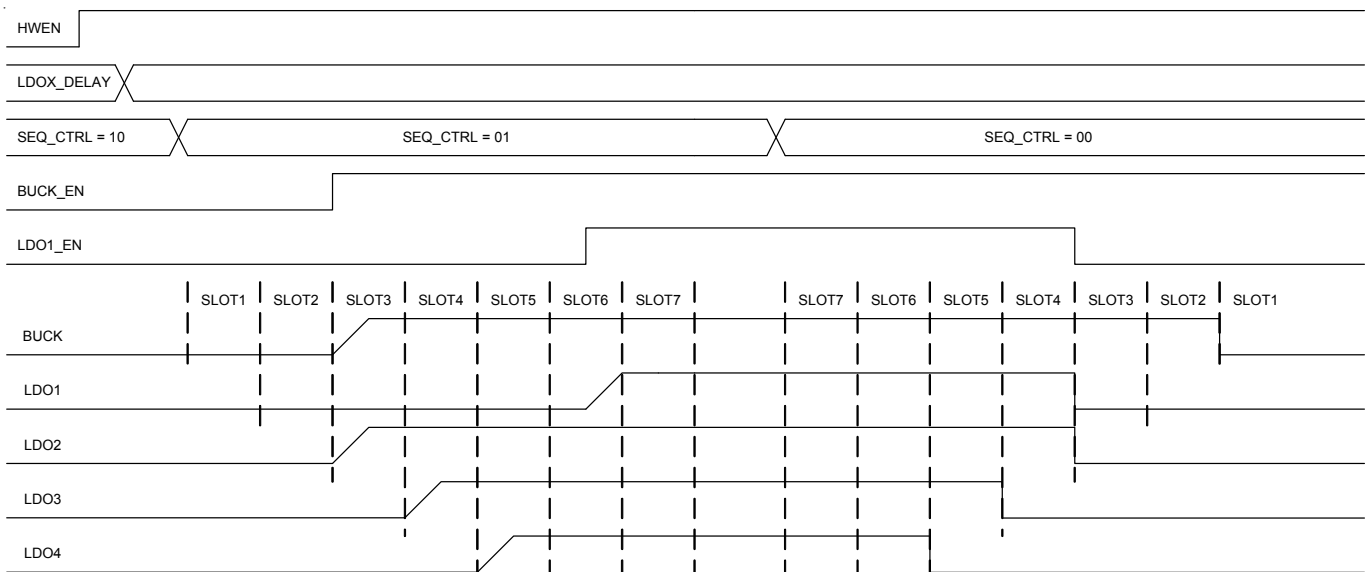


Figure 6.

Example for sequence control SEQ_CTRL change from 01 to 00. LDO2, LDO3, LDO4 are sequence off and LDO1 is turned off by itself enable bit. BUCK1 is turned off after 7 sequence slot count even itself enable bit is at high state.

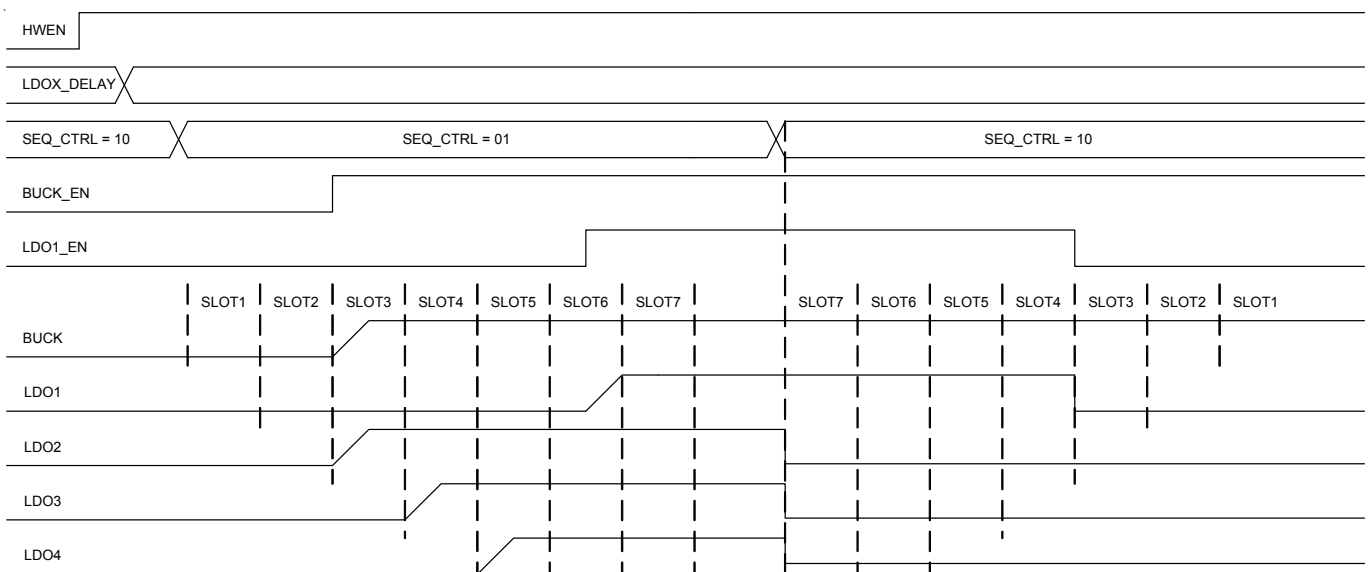


Figure 7.

Example for sequence control SEQ_CTRL change from 01 to 10. LDO2, LDO3, LDO4 are turned off and state of BUCK, LDO1 depends on itself enable bit.

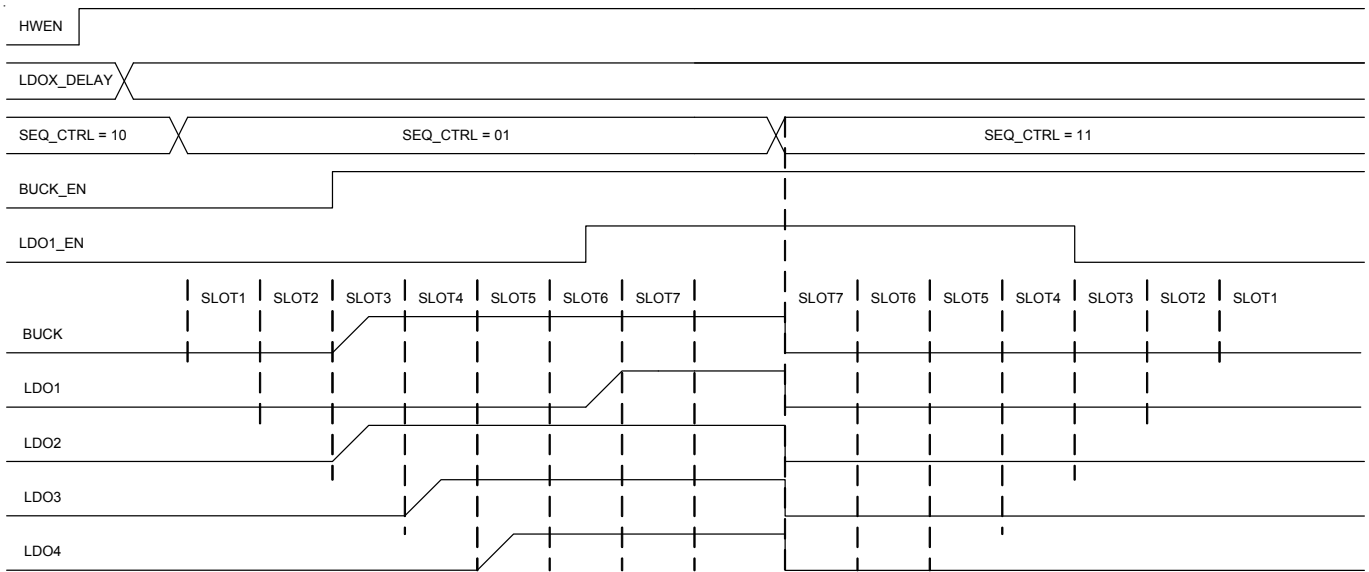


Figure 8.

Example for sequence control SEQ_CTRL change from 01 to 11. All channels are turned off immediately.

• Boost

Table 2. Boost Control

| HWEN pin | BSTEN pin | EN bits | On / Off |
|----------|-----------|---------|----------|
| Low | Low | 0 | Off |
| Low | Low | 1 | Off |
| Low | High | 0 | On |
| Low | High | 1 | On |
| High | Low | 0 | Off |
| High | Low | 1 | On |
| High | High | 0 | On |
| High | High | 1 | On |

Note : The Boost Control table above shows that the Boost operation requires either BSTEN pin to be high or a combination of HWEN pin high and one of the EN bits in register 0x08 needs to be set to 1.

► Normal Control Setting

The RT5112 Boost on/off control setting can be programmed via I²C with dedicated registers or external BSTEN pin.

- ◆ BSTEN pin to hardware control on/off.
- ◆ Register 0x08[7] to 0x08[0], each bit is able to software control on/off.

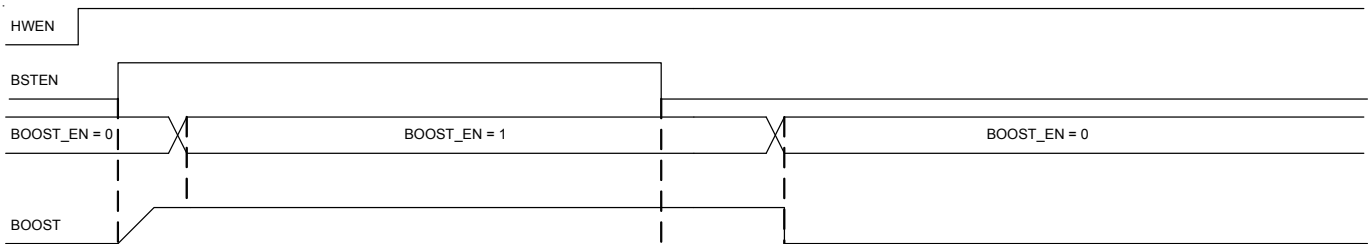


Figure 9.

Example for normal control with combination of BSTEN pin and EN bits.

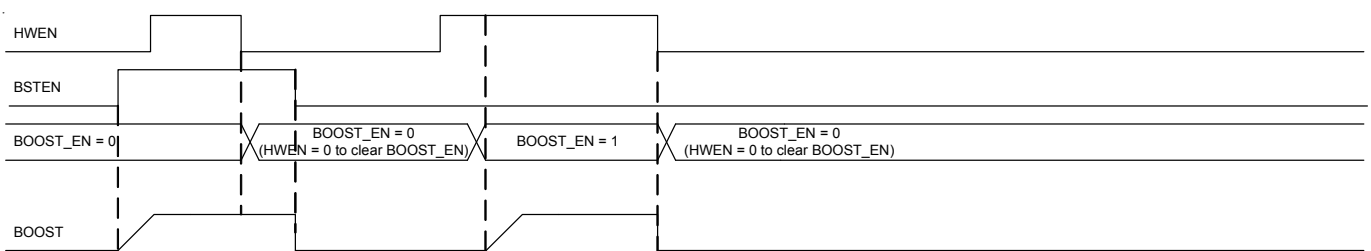


Figure 10.

Example for normal control with combination of BSTEN pin and EN bits. BSTEN pin is able to control Boost regardless of HWEN state.

Output Voltage Setting

The RT5112 output voltage can be programmed via I²C with dedicated registers.

• **Buck**

Register 0x0C[7:0] is used to control Buck output voltage.

Register 0x14[7:6] is used to control Buck voltage scaling slew rate.

• **Boost**

Register 0x11[7:2] is used to control Boost output voltage.

Register 0x14[3:2] is used to control Boost voltage scaling slew rate.

• **LDOs**

Registers 0x0D[7:1], 0x0E[7:1], 0x0F[7:1], 0x10[7:1] are used to control LDO1, LDO2, LDO3 and LDO4 output voltage.

Register 0x14[5:4] is used to control LDOs voltage scaling slew rate.

Operating Mode

The RT5112 provides different operating modes for Buck, Boost and LDOs for flexible application. Registers 0x00[1:0], 0x01[1:0], 0x02[1:0], 0x03[1:0], 0x04[1:0] and 0x05[1:0] are used to control the operating mode.

• **Buck and Boost**

▶ **Auto PFM (Pulse Frequency Modulation) Mode**

In order to save power and improve efficiency at low loads, the Buck/ Boost operate in PFM mode as the inductor drops into DCM (Discontinuous Current Mode). The switching frequency is proportional to loading to reach output voltage regulation. When load increases and inductor current becomes continuous again, the Buck/ Boost automatically goes back to PWM fixed frequency mode. Additionally, the RT5112 will enters DSLP (Deep Sleep) to reach input low quiescent current at no load.

▶ **FPWM (Forced Pulse Width Modulation) Mode**

The switching frequency is forced into PWM mode operation. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM.

▶ **Normal Mode**

The operation is same as Auto PFM mode. The only one difference is that there is no DSLP in this mode.

▶ **Ultra-Sonic Mode**

To avoid acoustic noise problem when operation, the switching frequency is designed to be always higher than 20kHz even there is no load at output.

● **LDOs**

▶ **Auto Mode**

This mode is for general use.

▶ **EN Forced Mode**

When EN Forced Mode is selected, the RT5112 can provide higher PSRR (Power Supply Rejection Ratio) to mitigate interference from input voltage. However, it brings out higher quiescent current to get the function.

▶ **Bypass Mode**

LDO internal power MOSFET is fully turned on. Input voltage will pass through it to the output terminal directly.

Operating Mode for NFC module (Only Boost)

The RT5112 provides two ways to avoid Boost switching frequency situated at around 847 ± 106 kHz during NFC module operation duration. Registers 0x05[6] and 0x39[2] are used to select the method.

● **Auto NFC (0x05[6] = 1, 0x39[2] = 0)**

When switching frequency is close to 600kHz (typ.), the RT5112 will activate Auto NFC function to increase the switching frequency to around 1.1MHz (typ.). When the switching frequency continues to increase to 1.6MHz (typ.) with increasing load, it will leave Auto NFC mechanism. If the present switching frequency is situated at range 600kHz to 1.1MHz when leaving, it will re-activate Auto NFC function to increase switching frequency again. Once the present switching frequency

(depends on load) is always higher than 1.6MHz, it goes back to normal operating.

● **FCCM NFC (0x05[6] = 0, 0x39[2] = 1)**

When the loading is increased to 130mA (typ.), the RT5112 will activate FCCMNFC function to transit Boost into FPWM mode operation. The operating switching frequency is 3MHz (typ.) which is much higher than 847 ± 106 kHz to interfere NFC module.

Channel Protection Features

The RT5112 equips Over-Current Protection, Under-Voltage Protection and Over-Voltage Protection to prevent the device from damages causing by abnormal operation or fault conditions. (over-load, short-circuit, soldering issue...etc.)

● **Over-Current Protection (OCP)**

▶ **Behavior after OCP**

Register 0x37[7:5] is used to select the operation after over-current failure detected.

▶ **OCP Mechanism**

◆ **Buck**

When the inductor current reaches the high-side MOSFET peak current limit threshold, the high-side MOSFET will be turned-off. The low-side MOSFET turns on to discharge the inductor current until the inductor current trips below the low-side MOSFET valley current limit threshold. After high-side MOSFET peak current limit triggered, the maximum inductor current is decided by the inductor current rising rate and the response delay time of the internal network.

◆ **Boost**

When the loading current is increased such that the inductor current is above the high-side MOSFET valley current limit threshold, the off-time is increased until the inductor current is decreased to valley current threshold. The maximum inductor current is decided by the high-side MOSFET valley current limit level and internal designed inductor current ripple.

◆ **LDOs**

When the loading reaches the current limit threshold, the current sent to the output will kept at current limit level.

● **Under-Voltage Protection (UVP)**

▶ **Behavior after UVP**

Register 0x0A[7:5] is used to select the operation after under voltage failure detected.

● **Ovrt-Voltage Protection (OVP)**

▶ **Behavior after OVP**

Register 0x0A[2:0] is used to select the operation after over voltage failure detected.

Table 3. Protection

| Channel | Type | Threshold (typ.) | Deglintch Time (typ.) | Protection | Reset and Threshold (typ.) |
|---------|---------|---|-----------------------|--|---|
| System | UVLO | $V_{SYS} < 2.35V$ $V_{SYS} \leq 2.25V$ (after IC Operation) | 525 μ s | IC Shutdown | $V_{SYS} \geq 2.35V$ |
| | OVP | $V_{SYS} \geq 5.9V$ | 200 μ s | Buck Disable | $V_{SYS} \leq 5.6V$ |
| | OTW | Temperature $\geq 125^{\circ}C$ | 50 μ s | Report only | Temperature $\leq 105^{\circ}C$ |
| | OTP | Temperature $\geq 140^{\circ}C$ | 50 μ s | IC Shutdown | Selection by 0x0A[4:3] 00 : Manual recovery after TSD with reset register 01 : Auto recovery after TSD with no reset register 10 : Latch off after TSD with reset register |
| BUCK | UVP | $V_{BUCK} \leq V_{BUCK_SET} \times 80\%$ | 50 μ s | Selection by 0x0A[7] 0 : Hiccup mode 1 : Latch-off mode | $V_{BUCK} \geq V_{BUCK_SET} \times 92\%$ |
| | OVP | $V_{BUCK} \geq V_{BUCK_SET} \times 120\%$ | 50 μ s | Selection by 0x0A[2] 0 : Discharge mode 1 : Latch-off mode | $V_{BUCK} \leq V_{BUCK_SET} \times 109\%$ |
| | OCP | $I_{LXBUCK_peak} \geq 2A$ $I_{LXBUCK_valley} \geq 1.5A$ (peak - 0.5A) | 8 μ s | Selection by 0x037[7] 0 : Hiccup mode 1 : Latch-off mode | $I_{LXBUCK_peak} < 2A$ $I_{LXBUCK_valley} < 1.5A$ (peak - 0.5A) |
| BOOST | UVP | $V_{BOOST} \leq V_{BOOST} \times 80\%$ | 50 μ s | Selection by 0x0A[5] 0 : Hiccup mode 1 : Latch-off mode | $V_{BOOST} \geq V_{BOOST} \times 92.3\%$ |
| | OVP | $V_{BOOST} \geq V_{BOOST} \times 117\%$ | 8 μ s | Selection by 0x0A[0] 0 : NA 1 : Latch-off mode | $V_{BOOST} \leq V_{BOOST} \times 106\%$ |
| | ABS OVP | $V_{BOOST} \geq 6.5V$ | 8 μ s | Stop switch | $V_{BOOST} \leq 5.8V$ |
| | OCP | $I_{LXBOOST_valley} \geq 2.5A$ | 8 μ s | Selection by 0x037[5] 0 : Hiccup mode 1 : Latch-off mode | $I_{LXBOOST_valley} < 2.5A$ |

| Channel | Type | Threshold (typ.) | Deglintch Time (typ.) | Protection | Reset and Threshold (typ.) |
|---------|------|-------------------------------------|-----------------------|--|-------------------------------------|
| LDOs | UVP | $V_{LDO} \leq V_{LDO} \times 80\%$ | 50 μ s | Selection by 0x0A[6] 0 : Hiccup mode 1 : Latch-off mode | $V_{LDO} \geq V_{LDO} \times 90\%$ |
| | OVP | $V_{LDO} \geq V_{LDO} \times 120\%$ | 50 μ s | Selection by 0x0A[1] 0 : Discharge mode 1 : NA | $V_{LDO} \leq V_{LDO} \times 110\%$ |
| | OCP | $I_{LDO} > 415\text{mA}$ | 8 μ s | Selection by 0x037[6] 0 : Hiccup mode 1 : Latch-off mode | $I_{LDO} \leq 415\text{mA}$ |

Interrupt

● **Fault Event and Status**

The RT5112 interrupt controller continuously monitors the device operation. Once the fault is ever detected, the fault event bit will be set to 1 and the open drain interrupt indicate pin INTRB will be driven to ground level. Meanwhile, the fault status bit will also be set to 1 to show the present fault. When the host reads the fault event bit and set interrupt clear bit 0x14[0] = 1, the INTRB pin will be released to high impedance. The fault status bit goes back to 0 only till the fault condition is cleared.

Table 4. Interrupt

| Fault Event | Fault Status | Description |
|-------------------------|--------------------------|----------------------------|
| BUCK_UV_EVT 0x15[7] | BUCK_UV_STAT 0x2B[7] | BUCK output under-voltage |
| LDO1_UV_EVT 0x15[6] | LDO1_UV_STAT 0x2B[6] | LDO1 output under-voltage |
| LDO2_UV_EVT 0x15[5] | LDO2_UV_STAT 0x2B[5] | LDO2 output under-voltage |
| LDO3_UV_EVT 0x15[4] | LDO3_UV_STAT 0x2B[4] | LDO3 output under-voltage |
| LDO4_UV_EVT 0x15[3] | LDO4_UV_STAT 0x2B[3] | LDO4 output under-voltage |
| BOOST_UV_EVT 0x15[2] | BOOST_UV_STAT 0x2B[2] | BOOST output under-voltage |
| BOOST_FAULT_EVT 0x15[0] | BOOST_FAULT_STAT 0x2B[0] | BOOST internal fault |
| BUCK_OV_EVT 0x16[7] | BUCK_OV_STAT 0x2C[7] | BUCK output over-voltage |
| LDO1_OV_EVT 0x16[6] | LDO1_OV_STAT 0x2C[6] | LDO1 output over-voltage |
| LDO2_OV_EVT 0x16[5] | LDO2_OV_STAT 0x2C[5] | LDO2 output over-voltage |
| LDO3_OV_EVT 0x16[4] | LDO3_OV_STAT 0x2C[4] | LDO3 output over-voltage |
| LDO4_OV_EVT 0x16[3] | LDO4_OV_STAT 0x2C[3] | LDO4 output over-voltage |
| BOOST_OV_EVT 0x16[2] | BOOST_OV_STAT 0x2C[2] | BOOST output over-voltage |
| BUCK_OCP_EVT 0x17[7] | BUCK_OCP_STAT 0x2D[7] | BUCK over-current |
| LDO1_OCP_EVT 0x17[6] | LDO1_OCP_STAT 0x2D[6] | LDO1 over-current |
| LDO2_OCP_EVT 0x17[5] | LDO2_OCP_STAT 0x2D[5] | LDO2 over-current |
| LDO3_OCP_EVT 0x17[4] | LDO3_OCP_STAT 0x2D[4] | LDO3 over-current |

| Fault Event | Fault Status | Description |
|-----------------------|------------------------|----------------------|
| LDO4_OCP_EVT 0x17[3] | LDO4_OCP_STAT 0x2D[3] | LDO4 over-current |
| BOOST_OCP_EVT 0x17[2] | BOOST_OCP_STAT 0x2D[2] | BOOST over-current |
| TWARN_EVT 0x19[7] | TWARN_STAT 0x2F[7] | Thermal warning |
| TSD_EVT 0x19[6] | TSD_STAT 0x2F[6] | Thermal shutdown |
| VSYSUV_EVT 0x19[5] | VSYSUV_STAT 0x2F[5] | System under-voltage |
| VSYSOV_EVT 0x19[4] | VSYSOV_STAT 0x2B[4] | System over-voltage |

Fault Event Mask

The host can set the fault event mask bits to hide the fault events. When the mask bit is set to 1, the corresponding fault is hidden and the interrupt indicate pin INTRB will keep high impedance without being pulled to ground level. The host requires to read the fault event bits to clear its value to 0, otherwise the interrupt indicate pin INTRB will be driven to low level again when mask bits being set to 1. The mask bits will be reset to default value with conditions : HWEN voltage goes to low level or IC power shutdown.

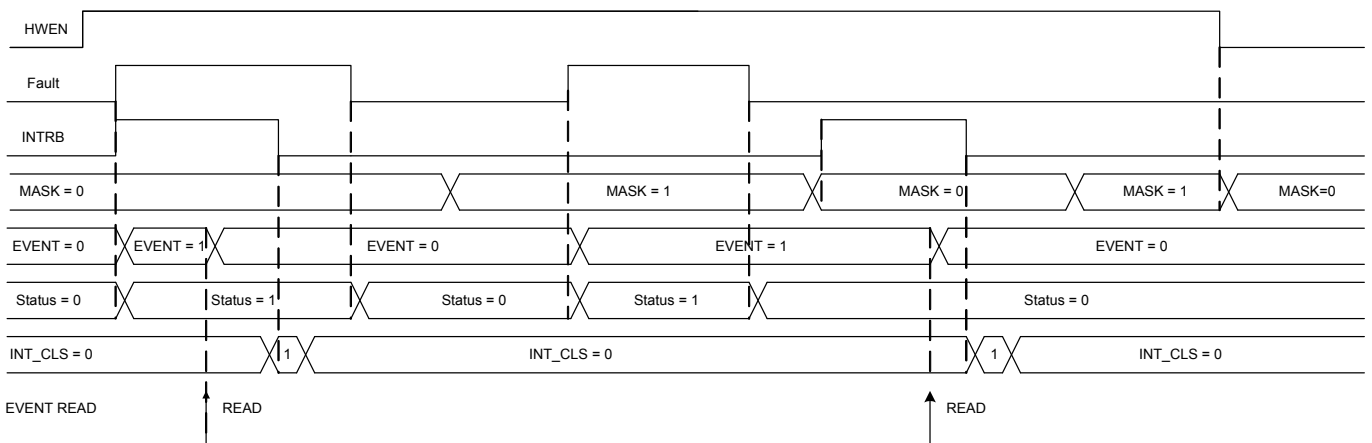


Figure 11.

Component Selection

Inductor Selection

The recommended nominal inductance 1μH/0.47μH for Buck/ Boost converter. The inductor saturation current must be chosen carefully considering the current limit level. It is suggested to select an inductor with the low DCR to provide good performance and efficiency for application.

Input and Output Capacitor Selection

Buck and Boost

It is recommended at least a 10μF (6.3V) input capacitor for Buck and Boost, a 10μF (6.3V) output

capacitor for Buck and a 22μF (6.3V) output capacitor for Boost. The ripple voltage is an important index for choosing output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The output ripple can be calculated as below.

Buck

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT1} + \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where $\Delta V_{ESR} = I_{COUT_RMS} \times R_{COUT_ESR}$

◆ Boost

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT1} = \Delta V_{ESR} + \frac{I_{OUT} \times D}{f_{SW} \times C_{OUT}}$$

where $\Delta V_{ESR} = I_{COUT_RMS} \times R_{COUT_ESR}$

▶ LDOs

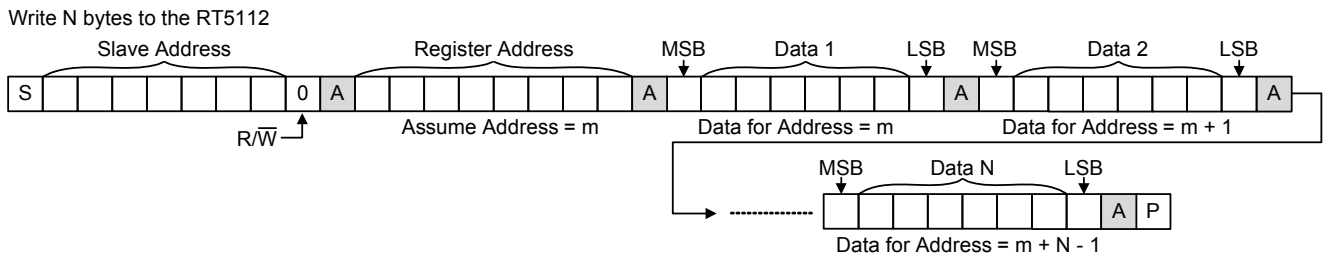
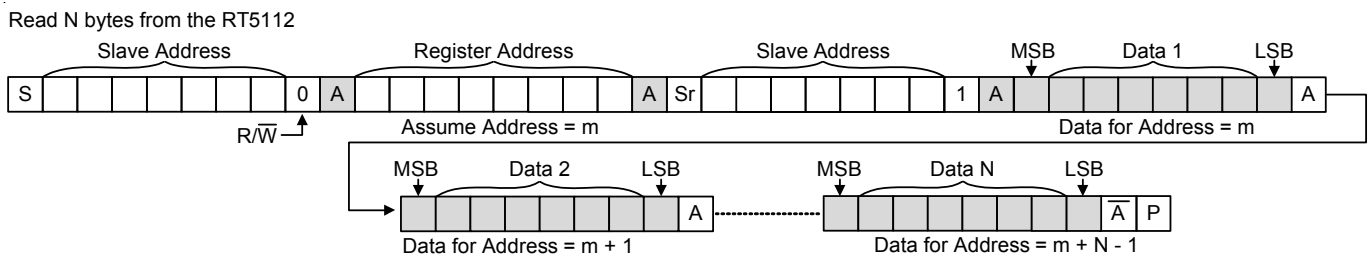
Like any low dropout regulator, the external capacitors of the RT5112 must be carefully selected for regulator stability and performance. Using a capacitor of at least 2.2 μ F (X5R or X7R) is suitable.

I²C Interface

The following table shows the RT5112 unique address as below.

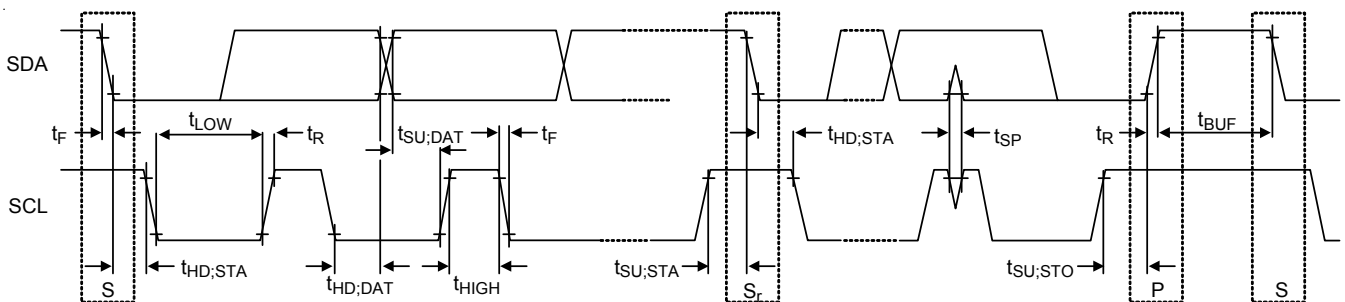
| RT5112 I ² C Slave Address | | | |
|---------------------------------------|-----|---------|-------|
| MSB | LSB | R/W bit | R/W |
| 010000 | 0 | 1/0 | 41/40 |

The I²C interface bus must be connect a resistor 2.2kΩ to power node and independent connection to processor, individually. The I²C timing diagrams are listed below.



□ Driven by Master, ■ Driven by Slave, P Stop, S Start, Sr Repeat Start

I²C Waveform Information



I²C Register Table

R : Read only.

RC : Read then Clear.

RW : Read and Write.

WC : Write "1" then clear to "0" after this procedure finish.

Note : Below registers setting are only available on the RT5112A.

0x06, 0x0B[2], 0x12, 0x13[5:4], 0x15[1], 0x16[1], 0x17[1], 0x2B[1], 0x2C[1], 0x2D[1], 0x30[1], 0x32[1], 0x33[1], 0x34[1],
0x3B[1], 0x43[4]

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|------------|---------|------|---|
| 0x00 | Buck_CTRL | 7 | BUCK_EN | 0 | RW | Buck enable. This bit is mask if REG0x00[6:4] : BUCK_DELAY ≠ 3'b000 0 : Disable (default) 1 : Enable Note : When Buck's latch-off protection happen, this bit will reset to "0" |
| | | 6:4 | BUCK_DELAY | 000 | RW | Buck power on/off delay time setting: 000 : Controlled by I ² C with REG0x00[7] : BUCK_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When Buck's latch-off protection happen, these bits will reset to "000" |
| | | 3:2 | BUCK_ILIM | 01 | RW | Buck current limit set bit. 00 : 1.5A 01 : 2A (default) 10 : 2.5A 11 : 3A |
| | | 1:0 | BUCK_MODE | 00 | RW | Buck operation mode : 00 : Auto PFM mode (default) 01 : Forced PWM mode 10 : Ultra sonic mode 11 : Normal mode |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|------------|---------|------|---|
| 0x01 | LDO1_CTRL | 7 | LDO1_EN | 0 | RW | LDO1 enable. This bit is mask if REG0x01[6:4] : LDO1_DELAY \neq 3'b000 0 : Disable (default) 1 : Enable Note : When LDO1's latch-off protection happen, this bit will reset to "0" |
| | | 6:4 | LDO1_DELAY | 000 | RW | LDO1 power on/off delay time setting: 000 : Controlled by I ² C with REG0x01[7] : LDO1_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When LDO1's latch-off protection happen, these bits will reset to "000" |
| | | 3:2 | LDO1_ILIM | 11 | RW | LDO1 current limit set bit. 00 : 150mA 01 : 250mA 10 : 300mA 11 : 360mA (default) |
| | | 1:0 | LDO1_MODE | 00 | RW | LDO1 operation mode : 00 : Auto mode (default) 01 : EN forced mode. (High PSRR mode). 10 : Bypass mode. LDO1 internal power MOSFET turns on fully. 11 : Bypass mode. LDO1 internal power MOSFET turns on fully. |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|------------|---------|------|--|
| 0x02 | LDO2_CTRL | 7 | LDO2_EN | 0 | RW | LDO2 enable. This bit is mask if REG0x02[6:4] : LDO2_DELAY \neq 3'b000 0 : Disable (default) 1 : Enable Note : When LDO2's latch-off protection happen, this bit will reset to "0" |
| | | 6:4 | LDO2_DELAY | 000 | RW | LDO2 power on/off delay time setting : 000 : Controlled by I ² C with REG0x02[7] : LDO2_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When LDO2's latch-off protection happen, these bits will reset to "000" |
| | | 3:2 | LDO2_ILIM | 11 | RW | LDO2 current limit set bit. 00 : 150mA 01 : 250mA 10 : 300mA 11 : 360mA (default) |
| | | 1:0 | LDO2_MODE | 00 | RW | LDO2 operation mode : 00 : Auto mode (default) 01 : EN forced mode. (High PSRR mode). 10 : Bypass mode. LDO2 internal power MOSFET turns on fully. 11 : Bypass mode. LDO2 internal power MOSFET turns on fully. |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|------------|---------|------|--|
| 0x03 | LDO3_CTRL | 7 | LDO3_EN | 0 | RW | LDO3 enable. This bit is mask if REG0x03[6:4] : LDO3_DELAY \neq 3'b000 0 : Disable (default) 1 : Enable Note : When LDO3's latch-off protection happen, this bit will reset to "0" |
| | | 6:4 | LDO3_DELAY | 000 | RW | LDO3 power on/off delay time setting : 000 : Controlled by I ² C with REG0x03[7] : LDO3_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When LDO3's latch-off protection happen, these bits will reset to "000" |
| | | 3:2 | LDO3_ILIM | 11 | RW | LDO3 Current limit set bit. 00 : 150mA 01 : 250mA 10 : 300mA 11 : 360mA (default) |
| | | 1:0 | LDO3_MODE | 00 | RW | LDO3 operation mode : 00 : Auto mode (default) 01 : EN forced mode. (High PSRR mode). 10 : Bypass mode. LDO3 internal power MOSFET turns on fully. 11 : Bypass mode. LDO3 internal power MOSFET turns on fully. |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|------------|---------|------|--|
| 0x04 | LDO4_CTRL | 7 | LDO4_EN | 0 | RW | LDO4 enable. This bit is mask if REG0x04[6:4] : LDO4_DELAY \neq 3'b000 0 : Disable (default) 1 : Enable Note : When LDO4's latch-off protection happen, this bit will reset to "0" |
| | | 6:4 | LDO4_DELAY | 000 | RW | LDO4 power on/off delay time setting : 000 : Controlled by I ² C with REG0x04[7] : LDO4_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When LDO4's latch-off protection happen, these bits will reset to "000" |
| | | 3:2 | LDO4_ILIM | 11 | RW | LDO4 current limit set bit. 00 : 150mA 01 : 250mA 10 : 300mA 11 : 360mA (default) |
| | | 1:0 | LDO4_MODE | 00 | RW | LDO4 operation mode : 00 : Auto mode (default) 01 : EN forced mode. (High PSRR mode). 10 : Bypass mode. LDO4 internal power MOSFET turns on fully. 11 : Bypass mode. LDO4 internal power MOSFET turns on fully. |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|------------|-----|------------|---------|------|--|
| 0x05 | BOOST_CTRL | 7 | LCH_ON | 0 | RW | Boost linear charge current : 0 : 400mA (default) 1 : 800mA |
| | | 6 | NFC_EN | 1 | RW | Boost NFC enable. 0x39[2] must set 0 when bit NFC_EN = 1. 0 : Disable 1 : Enable (default) |
| | | 5:4 | BOOST_SS | 00 | RW | Voltage scaling slew rate for Boost. 00 : 14mV/μs (default) 01 : 10mV/μs 10 : 6mV/μs 11 : 4mV/μs |
| | | 3:2 | BOOST_ILIM | 01 | RW | Boost current limit set bit. 00 : 2A 01 : 2.5A (default) 10 : 3A 11 : 3.5A |
| | | 1:0 | BOOST_MODE | 00 | RW | Boost operation mode: 00 : Auto PFM mode (default) 01 : Forced PWM mode 10 : Ultra sonic mode 11 : Normal mode |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|------------|-----|-------------|---------|------|---|
| 0x06 | Buck2_CTRL | 7 | BUCK2_EN | 0 | RW | BUCK2 enable. This bit is mask if REG0x06[6:4] : BUCK2_DELAY \neq 3'b000 0 : Disable (default) 1 : Enable Note : When Buck2's latch-off protection happen, this bit will reset to "0" |
| | | 6:4 | BUCK2_DELAY | 000 | RW | BUCK2 power on/off delay time setting : 000 : Controlled by I ² C with REG0x06[7] : BUCK2_EN (default) 001 : SLOT1 010 : SLOT2 011 : SLOT3 100 : SLOT4 101 : SLOT5 110 : SLOT6 111 : SLOT7 (delay time setting at on/off sequence are reverse) Note : When Buck2's latch-off protection happen, these bits will reset to "000" |
| | | 3:2 | BUCK2_ILIM | 01 | RW | BUCK2 current limit set bit. 00 : 1.5A 01 : 2A (default) 10 : 2.5A 11 : 3A |
| | | 1:0 | BUCK2_MODE | 00 | RW | BUCK2 operation mode: 00 : Auto mode (default) 01 : Forced PWM mode 10 : Ultra sonic mode 11 : Normal mode |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|------------|-----|---------|----------|------|-----------------------|
| 0x07 | Product ID | 7:0 | PID | 11001101 | R | Vendor identification |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|--------------|-----|-----------|---------|------|---|
| 0x08 | BOOST_ENABLE | 7 | BOOST_EN7 | 0 | RW | Enable bit #7 for the Boost. 0 : Disable (default) 1 : Enable |
| | | 6 | BOOST_EN6 | 0 | RW | Enable bit #6 for the Boost. 0 : Disable (default) 1 : Enable |
| | | 5 | BOOST_EN5 | 0 | RW | Enable bit #5 for the Boost. 0 : Disable (default) 1 : Enable |
| | | 4 | BOOST_EN4 | 0 | RW | Enable bit #4 for the Boost. 0 : Disable (default) 1 : Enable |
| | | 3 | BOOST_EN3 | 0 | RW | Enable bit #3 for the Boost. 0 : Disable (default) 1 : Enable |
| | | 2 | BOOST_EN2 | 0 | RW | Enable bit #2 for the Boost. 0 : Disable (default) 1 : Enable |
| | | 1 | BOOST_EN1 | 0 | RW | Enable bit #1 for the Boost. 0 : Disable (default) 1 : Enable |
| | | 0 | BOOST_EN0 | 0 | RW | Enable bit #0 for the Boost. 0 : Disable (default) 1 : Enable |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|----------|-----|--------------------|---------|------|--|
| 0x09 | SEQ_PROG | 7:6 | SEQ_SPE ED[1:0] | 10 | RW | Set slot period : 00 : 2.73ms 01 : 1.365ms 10 : 0.682ms (default) 11 : 0.341ms (slot period is the base unit of each SLOT, for example SLOT2 = 2*slot period; SLOT3 = 3*slot period) Set soft-start time slew rate (Buck_SR) : 00 : 1mV/μs 01 : 2mV/μs 10 : 4mV/μs (default) 11 : 7mV/μs (Buck's VOUT min. step = 12.5mV, f = 2.5MHz) (Once slot period is chose, corresponding soft start time slew rate is determined.) Note : Buck soft-start time (Buck_tss) 00 : 1ms/V x Vout 01 : 0.5ms/V x Vout 10 : 0.25ms/V x Vout (default) 11 : 0.143ms/V x Vout |
| | | 5:4 | SEQ_ CTRL[1:0] | 10 | RW | 2 bits to control LDOs and Buck's ON/OFF 00 : Power-Down, relative regulators (CHx_DELAY ≠ 3'b000) disable by power off sequence, others turn off by each EN bit 01 : Power-UP, relative regulators (CHx_DELAY ≠ 3'b000) enable by power on sequence, others turn on by each EN bit 10 : All regulators's ON/OFF depend on each EN bit. (default) 11 : All regulators turn off directly. |
| | | 3:0 | Reserved | 0000 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|----------------|---------|------|--|
| 0x0A | Latch | 7 | BUCK_UV_LATCH | 0 | RW | Buck hiccup or latch off mode selection after V _O UV. 0 : Hiccup mode; (continuously hiccup more than 3 times would enter latch-off mode ,select deglitch time by REG0x38[7:6], hiccup on/off time = 5/8ms) (default) 1 : Latch-off mode |
| | | 6 | LDO_UV_LATCH | 0 | RW | LDO hiccup or latch off mode selection after V _O UV. 0 : Hiccup mode; (continuously hiccup more than 3 times would enter latch-off mode ,select deglitch time by REG0x38[3:2], hiccup on/off time = 5/40ms) (default) 1 : Latch-off mode |
| | | 5 | BOOST_UV_LATCH | 0 | RW | Boost hiccup or latch off mode selection after V _O UV. 0 : Hiccup mode; (continuously hiccup more than 3 times would enter latch-off mode ,select deglitch time by REG0x37[3:2], hiccup on/off time = 11/100ms) (default) 1 : Latch-off mode |
| | | 4:3 | TSD[1:0] | 01 | RW | IC protection after thermal shutdown : 00 : Manual recovery after TSD with reset I ² C register. The power up sequence is initiated with default I ² C register value 01 : Auto recovery after TSD with no reset I ² C register. The power up sequence is initiated with I ² C register value (default) 10 : Latch off after TSD, all Reg reset. Restart by Vin start up or (BSTEN = 0 → 1 to restart Boost) or (HWEN = 0 → 1 to enable channel), i.e.BSTEN and HWEN need pull low to unlock 11 : No change, follow before setting |
| | | 2 | BUCK_OV_LATCH | 0 | RW | Buck discharge or latch off mode selection after V _O OV. 0 : R Discharge (default) 1: Latch-off mode |
| | | 1 | LDO_OV_LATCH | 0 | RW | LDO discharge mode selection after V _O OV. 0 : R Discharge; (During DVS period won't sent OV Event to INTRB) (default) 1 : NA |
| | | 0 | BOOST_OV_LATCH | 0 | RW | Boost latch off mode selection after V _O OV. 0 : NA (default) 1 : Latch-off mode |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|-----------|---------|------|---|
| 0x0B | DISCHARGE | 7 | BUCK_DIS | 1 | RW | Buck active output discharge. 0 : Disable 1 : Enable (default) |
| | | 6 | LDO_DIS | 1 | RW | LDO active output discharge. 0 : Disable 1 : Enable (default) |
| | | 5 | BOOST_DIS | 1 | RW | Boost active output discharge. 0 : Disable 1 : Enable (default) |
| | | 4 | Reserved | 0 | RW | Reserved |
| | | 3 | Reserved | 0 | RW | Reserved |
| | | 2 | BUCK2_DIS | 1 | RW | Buck2 active output discharge. 0 : Disable 1 : Enable (default) |
| | | 1 | BCTRL | 0 | WC | Boost registers keep and reset control. Self reset function: it can recover to 0 when set 1 : 0 : Keep Boost relative Reg value Register0x05[7], 0x05[5:2], 0x08[7:0], 0x0A[5], 0x0A[0], 0x14[3:2], 0x37[5], 0x37[3:2] Boost relative bits. (default) 1 : Boost relative Reg recover to default value. When HWEN OFF and BCTRL = 0 (default), Boost keeps relative Reg. When HWEN ON and BCTRL = 1, Boost recover to default value. BCTRL become 0 automatically, Boost relative Reg is kept. When HWEN ON and BCTRL = 0, Boost relative can be written normally. When write 1 then it will recover to 0. |
| | | 0 | Reserved | 0 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|-----------------|----------|------|--|
| 0x0C | Buck_Vout | 7:0 | Buck_Vout [7:0] | 00101000 | RW | Buck output voltage can be set default voltage from 0.8V to 3.3V with 12.5mV/step. 00000000 : 0.6V 00000001 : 0.6125V ... 00101000 : 1.1V (default) ... 11010111 : 3.2875V 11011000 : 3.3V ... 11111111: 3.3V |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|----------------|---------|------|---|
| 0x0D | LDO1_Vout | 7:1 | LDO1_Vout[6:0] | 1011000 | RW | LDO1 output voltage can be set default voltage from 0.6V to 3.775V with 25mV/step. 0000000 : 0.6V 0000001 : 0.625V ... 1011000 : 2.8V (default) ... 1111110 : 3.75V 1111111 : 3.775V |
| | | 0 | Reserved | 0 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|----------------|---------|------|---|
| 0x0E | LDO2_Vout | 7:1 | LDO2_Vout[6:0] | 1011000 | RW | LDO2 output voltage can be set default voltage from 0.6V to 3.775V with 25mV/step. 0000000 : 0.6V 0000001 : 0.625V ... 1011000 : 2.8V (default) ... 1111110 : 3.75V 1111111 : 3.775V |
| | | 0 | Reserved | 0 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|----------------|---------|------|---|
| 0x0F | LDO3_Vout | 7:1 | LDO3_Vout[6:0] | 0110000 | RW | LDO3 output voltage can be set default voltage from 0.6V to 3.775V with 25mV/step. 0000000 : 0.6V 0000001 : 0.625V ... 0110000 : 1.8V (default) ... 1111110 : 3.75V 1111111 : 3.775V |
| | | 0 | Reserved | 0 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|----------------|---------|------|---|
| 0x10 | LDO4_Vout | 7:1 | LDO4_Vout[6:0] | 0110000 | RW | LDO4 output voltage can be set default voltage from 0.6V to 3.775V with 25mV/step. 0000000 : 0.6V 0000001 : 0.625V ... 0110000 : 1.8V (default) ... 1111110 : 3.75V 1111111 : 3.775V |
| | | 0 | Reserved | 0 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|------------|-----|-----------------|---------|------|--|
| 0x11 | Boost_Vout | 7:2 | Boost_Vout[5:0] | 010100 | RW | Boost output voltage can be set default voltage from 4.5V to 5.5V with 25mV/step. 000000 : 4.5V 000001 : 4.525V ... 010100: 5.0V (default) ... 100111: 5.475V 101000: 5.5V ... 111111: 5.5V |
| | | 1:0 | LDO_SS | 01 | RW | Voltage scaling slew rate for LDO. 00 : 100mV/μs 01 : 50mV/μs (default) 10 : 25mV/μs 11 : 12.5mV/μs |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|------------|-----|-----------------|----------|------|--|
| 0x12 | Buck2_Vout | 7:0 | Buck2_Vout[7:0] | 10110100 | RW | Buck2 output voltage can be set default voltage from 0.6V to 3.3V with 12.5mV/step. 00000000 : 0.6V 00000001 : 0.6125V ... 10110100 : 2.85V (default) ... 11010111 : 3.2875V 11011000 : 3.3V ... 11111111: 3.3V |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|-------------------|---------|------|--|
| 0x13 | LX_SR | 7:6 | Buck_SR [1:0] | 01 | RW | Buck SW on/off speed set. Decrease SW speed can help the EMI performance. 00 : Slower 01 : Slow (default) 10 : Normal 11 : Fast |
| | | 5:4 | Buck2_SR [1:0] | 01 | RW | Buck2 SW on/off speed set. Decrease SW speed can help the EMI performance. 00 : Slower 01 : Slow (default) 10 : Normal 11 : Fast |
| | | 3 | Reserved | 0 | RW | Reserved |
| | | 2 | Reserved | 0 | RW | Reserved |
| | | 1:0 | Boost_SR [1:0] | 10 | RW | Boost SW on/off speed set. Decrease SW speed can help the EMI performance. 00 : Fast 01 : Normal 10 : Slow (default) 11 : Slower |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|-----------|---------|------|--|
| 0x14 | DVS | 7:6 | BUCK_DVS | 01 | RW | Voltage scaling slew rate for Buck. 00 : 7mV/μs 01 : 4mV/μs (default) 10 : 2mV/μs 11 : 1mV/μs |
| | | 5:4 | LDO_DVS | 01 | RW | Voltage scaling slew rate for LDO. 00 : 36mV/μs 01 : 14mV/μs (default) 10 : 8.5mV/μs 11 : 4mV/μs |
| | | 3:2 | BOOST_DVS | 01 | RW | Voltage scaling slew rate for Boost. 00 : 32mV/μs 01 : 15mV/μs (default) 10 : 8mV/μs 11 : 4mV/μs |
| | | 1 | Reserved | 0 | RW | Reserved |
| | | 0 | INT_CLS | 0 | WC | Interrupt clear pin. 0 : Normal operation (default) 1 : Refresh interrupt bits. (After write "1", the bit will auto return to "0".) |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|-----------------|---------|------|---|
| 0x15 | UV_EVT | 7 | BUCK_UV_EVT | 0 | RC | Buck under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck UV event detected |
| | | 6 | LDO1_UV_EVT | 0 | RC | LDO1 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO1 UV event detected |
| | | 5 | LDO2_UV_EVT | 0 | RC | LDO2 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO2 UV event detected |
| | | 4 | LDO3_UV_EVT | 0 | RC | LDO3 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO3 UV event detected |
| | | 3 | LDO4_UV_EVT | 0 | RC | LDO4 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO4 UV event detected |
| | | 2 | BOOST_UV_EVT | 0 | RC | Boost under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Boost UV event detected |
| | | 1 | BUCK2_UV_EVT | 0 | RC | Buck2 under-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck2 UV event detected |
| | | 0 | BOOST_FAULT_EVT | 0 | RC | Boost SCP (VOUT < 0.7V) or VDS protect (VIN – VOUT > 300mV) or IL > 5A internal Boost FAULT 0 : Not fault or be masked (default) 1 : Boost fault event detected |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|--------------|---------|------|---|
| 0x16 | OV_EVT | 7 | BUCK_OV_EVT | 0 | RC | Buck over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck OV event detected |
| | | 6 | LDO1_OV_EVT | 0 | RC | LDO1 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO1 OV event detected |
| | | 5 | LDO2_OV_EVT | 0 | RC | LDO2 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO2 OV event detected |
| | | 4 | LDO3_OV_EVT | 0 | RC | LDO3 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO3 OV event detected |
| | | 3 | LDO4_OV_EVT | 0 | RC | LDO4 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO4 OV event detected |
| | | 2 | BOOST_OV_EVT | 0 | RC | Boost over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Boost OV event detected |
| | | 1 | BUCK2_OV_EVT | 0 | RC | Buck2 over-voltage threshold sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck2 OV event detected |
| | | 0 | Reserved | 0 | RC | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|---------------|---------|------|---|
| 0x17 | OCP_EVT | 7 | BUCK_OCP_EVT | 0 | RC | Buck over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck OCP event detected |
| | | 6 | LDO1_OCP_EVT | 0 | RC | LDO1 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO1 OCP event detected |
| | | 5 | LDO2_OCP_EVT | 0 | RC | LDO2 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO2 OCP event detected |
| | | 4 | LDO3_OCP_EVT | 0 | RC | LDO3 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO3 OCP event detected |
| | | 3 | LDO4_OCP_EVT | 0 | RC | LDO4 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : LDO4 OCP event detected |
| | | 2 | BOOST_OCP_EVT | 0 | RC | Boost over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Boost OCP event detected |
| | | 1 | BUCK2_OCP_EVT | 0 | RC | Buck2 over-current protection acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Buck2 OCP event detected |
| | | 0 | Reserved | 0 | RC | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|----------|-----|------------|---------|------|---|
| 0x19 | BASE_EVT | 7 | TWARN_EVT | 0 | RC | Thermal warning sense acknowledgement. (raising/falling trigger) 0 : No fault or be masked (default) 1 : Thermal warning event detected |
| | | 6 | TSD_EVT | 0 | RC | Thermal shutdown sense acknowledgement. (raising/falling trigger) 0 : No fault or be masked (default) 1 : Thermal shutdown event detected |
| | | 5 | VSYSUV_EVT | 0 | RC | VSYS under-voltage sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Under-voltage event detected |
| | | 4 | VSYSOV_EVT | 0 | RC | VSYS over-voltage sense acknowledgement. (raising trigger) 0 : No fault or be masked (default) 1 : Over-voltage event detected |
| | | 3:0 | Reserved | 0000 | RC | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-------------|-----|----------|----------|------|--|
| 0x2A | Revision ID | 7:0 | RID[7:0] | 00000011 | R | Chip revision 00000000 : 1 st Version 00000001 : 2 nd Version 00000010 : 3 rd Version 00000011 : 4 th Version (default) ... 11111111 : 256 th Version |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|------------------|---------|------|--|
| 0x2B | UV_STAT | 7 | BUCK_UV_STAT | 0 | R | Buck under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 6 | LDO1_UV_STAT | 0 | R | LDO1 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 5 | LDO2_UV_STAT | 0 | R | LDO2 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 4 | LDO3_UV_STAT | 0 | R | LDO3 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 3 | LDO4_UV_STAT | 0 | R | LDO4 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 2 | BOOST_UV_STAT | 0 | R | Boost under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 1 | BUCK2_UV_STAT | 0 | R | Buck2 under-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 0 | BOOST_FAULT_STAT | 0 | R | Boost SCP (VOUT < 0.7V) or VDS protect (VIN – VOUT > 300mV) or IL > 5A internal boost FAULT status. 0 : No fault occurs (default) 1 : Fault occurs |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|---------------|---------|------|---|
| 0x2C | OV_STAT | 7 | BUCK_OV_STAT | 0 | R | Buck over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 6 | LDO1_OV_STAT | 0 | R | LDO1 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 5 | LDO2_OV_STAT | 0 | R | LDO2 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 4 | LDO3_OV_STAT | 0 | R | LDO3 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 3 | LDO4_OV_STAT | 0 | R | LDO4 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 2 | BOOST_OV_STAT | 0 | R | Boost over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 1 | BUCK2_OV_STAT | 0 | R | Buck2 over-voltage threshold sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 0 | Reserved | 0 | R | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|----------|-----|----------------|---------|------|--|
| 0x2D | OCP_STAT | 7 | BUCK_OCP_STAT | 0 | R | Buck over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 6 | LDO1_OCP_STAT | 0 | R | LDO1 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 5 | LDO2_OCP_STAT | 0 | R | LDO2 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 4 | LDO3_OCP_STAT | 0 | R | LDO3 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 3 | LDO4_OCP_STAT | 0 | R | LDO4 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 2 | BOOST_OCP_STAT | 0 | R | Boost over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 1 | BUCK2_OCP_STAT | 0 | R | Buck2 over-current protection status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 0 | Reserved | 0 | R | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|-------------|---------|------|---|
| 0x2F | BASE_STAT | 7 | TWARN_STAT | 0 | R | Thermal warning sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 6 | TSD_STAT | 0 | R | Thermal shutdown sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 5 | VSYSUV_STAT | 0 | R | VSYS under-voltage sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 4 | VSYSOV_STAT | 0 | R | VSYS over-voltage sense status. 0 : No fault occurs (default) 1 : Fault occurs |
| | | 3 | SEQ_ON | 0 | R | It indicates status of the internal SEQ_ON signal. 0 : SEQ OFF (default) 1 : SEQ ON |
| | | 2:0 | Reserved | 000 | R | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|--------------|---------|------|--|
| 0x30 | EN_FLG | 7 | BUCK_EN_FLG | 0 | R | Indicate Buck final enable status. 0 : Disable (default) 1 : Enable |
| | | 6 | LDO1_EN_FLG | 0 | R | Indicate LDO1 final enable status. 0 : Disable (default) 1 : Enable |
| | | 5 | LDO2_EN_FLG | 0 | R | Indicate LDO2 final enable status. 0 : Disable (default) 1 : Enable |
| | | 4 | LDO3_EN_FLG | 0 | R | Indicate LDO3 final enable status. 0 : Disable (default) 1 : Enable |
| | | 3 | LDO4_EN_FLG | 0 | R | Indicate LDO4 final enable status. 0 : Disable (default) 1 : Enable |
| | | 2 | BOOST_EN_FLG | 0 | R | Indicate BOOST final enable status. 0 : Disable (default) 1 : Enable |
| | | 1 | BUCK2_EN_FLG | 0 | R | Indicate Buck2 final enable status. 0 : Disable (default) 1 : Enable |
| | | 0 | Reserved | 0 | R | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|------------------|---------|------|---|
| 0x32 | UV_MASK | 7 | BUCK_UV_MASK | 0 | RW | Buck under-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 6 | LDO1_UV_MASK | 0 | RW | LDO1 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 5 | LDO2_UV_MASK | 0 | RW | LDO2 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 4 | LDO3_UV_MASK | 0 | RW | LDO3 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 3 | LDO4_UV_MASK | 0 | RW | LDO4 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 2 | BOOST_UV_MASK | 0 | RW | Boost under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 1 | BUCK2_UV_MASK | 0 | RW | Buck2 under-voltage threshold sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 0 | BOOST_FAULT_MASK | 0 | RW | Boost SCP (VOUT < 0.7V) or VDS protect (VIN – VOUT > 300mV) or IL > 5A internal boost FAULT mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|---------------|---------|------|--|
| 0x33 | OV_MASK | 7 | BUCK_OV_MASK | 0 | RW | Buck over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 6 | LDO1_OV_MASK | 0 | RW | LDO1 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 5 | LDO2_OV_MASK | 0 | RW | LDO2 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 4 | LDO3_OV_MASK | 0 | RW | LDO3 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 3 | LDO4_OV_MASK | 0 | RW | LDO4 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 2 | BOOST_OV_MASK | 0 | RW | Boost over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 1 | BUCK2_OV_MASK | 0 | RW | Buck2 over-voltage threshold mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 0 | Reserved | 0 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|----------|-----|----------------|---------|------|---|
| 0x34 | OCP_MASK | 7 | BUCK_OCP_MASK | 0 | RW | Buck over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 6 | LDO1_OCP_MASK | 0 | RW | LDO1 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 5 | LDO2_OCP_MASK | 0 | RW | LDO2 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 4 | LDO3_OCP_MASK | 0 | RW | LDO3 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 3 | LDO4_OCP_MASK | 0 | RW | LDO4 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 2 | BOOST_OCP_MASK | 0 | RW | Boost over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 1 | BUCK2_OCP_MASK | 0 | RW | Buck2 over-current protection mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 0 | Reserved | 0 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|-------------|---------|------|--|
| 0x36 | BASE_MASK | 7 | TWARN_MASK | 0 | RW | Thermal warning sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 6 | TSD_MASK | 0 | RW | Thermal shutdown sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 5 | VSYSUV_MASK | 0 | RW | VSYS under-voltage sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 4 | VSYSOV_MASK | 0 | RW | VSYS over-voltage sense mask. 0 : Interrupt is not masked (default) 1 : Interrupt is masked |
| | | 3:0 | Reserved | 0000 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|----------------|---------|------|--|
| 0x37 | CHx_PT | 7 | BUCK_OC_LATCH | 0 | RW | Buck Hiccup or latch off mode selection after current limit. 0 : Hiccup mode; (Hiccup 3 times will enter latch-off mode. Hiccup on/off time = 4ms / 8ms) (default) 1 : Latch-off mode. |
| | | 6 | LDO_OC_LATCH | 0 | RW | LDO Hiccup or latch off mode selection after current limit. 0 : Hiccup mode; (Hiccup 3 times will enter latch-off mode. Hiccup on/off time = 2ms/40ms) (default) 1 : Latch-off mode. |
| | | 5 | BOOST_OC_LATCH | 0 | RW | BOOST Hiccup or latch off mode selection after current limit. 0 : Hiccup mode; (Hiccup 3 times will enter latch-off mode, hiccup on/off time = 10ms/100ms) (default) 1 : Latch-off mode. |
| | | 4 | Reserved | 0 | RW | Reserved |
| | | 3:2 | BST_UV_DT[1:0] | 11 | RW | Boost UV deglitch time selection : 00 : 10μs 01 : 15μs 10 : 25μs 11: 50μs (default) |
| | | 1:0 | Reserved | 00 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-------------------|-----|-----------------|---------|------|---|
| 0x38 | CHx_deglitch time | 7:6 | Buck_UV_DT[1:0] | 11 | RW | Buck UV deglitch time selection : 00 : 5µs 01 : 10µs 10 : 15µs 11 : 50µs (default) |
| | | 5:4 | Buck_OV_DT[1:0] | 11 | RW | Buck OV deglitch time selection : 00 : 10µs 01 : 15µs 10 : 20µs 11 : 50µs (default) |
| | | 3:2 | LDO_UV_DT[1:0] | 11 | RW | LDO UV deglitch time selection : 00 : 10µs 01 : 15µs 10 : 30µs 11 : 50µs (default) |
| | | 1:0 | LDO_OV_DT[1:0] | 11 | RW | LDO OV deglitch time selection : 00 : 5µs 01 : 10µs 10 : 25µs 11 : 50µs (default) |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|----------------------|-----|----------------|---------|------|--|
| 0x39 | BASEPT_deglitch time | 7:6 | VSYSUV_DT[1:0] | 11 | RW | VSYSUV deglitch time selection : 00 : 70µs 01 : 135µs 10 : 265µs 11 : 525µs (default) |
| | | 5:4 | VSYSOV_DT[1:0] | 10 | RW | VSYSOV deglitch time selection: 00 : 20µs 01 : 50µs 10 : 180µs (default) 11 : 360µs |
| | | 3 | VSYSOV_PT | 0 | RW | VSYSOV turn off Buck 0 : When Vsys_OV occur will turn off BCK (default) 1 : When Vsys_OV occur will not turn off BCK |
| | | 2 | BST_NFC_Force | 0 | RW | NFC load detection. 0x05[6] must set 0 when bit BST_NFC_force = 1. 0 : AUTO NFC (default) 1 : FCCM by load, turn off NFC |
| | | 1 | Reserved | 0 | RW | Reserved |
| | | 0 | Reserved | 0 | RW | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|------------------|---------|------|--|
| 0x3A | SEQ_ON | 7:6 | SEQ_ON_STAT[1:0] | 00 | R | It indicates the states of power on sequence 00 : SEQ_ON hasn't started or needless (default) 01 : SEQ_ON is carrying out (During SLOT1 to SLOT8 + 4ms) 10 : There are fail soft-start channels during power on sequence 11 : SEQ_ON has completed |
| | | 5:3 | SEQ_COUNT [2:0] | 000 | R | It indicateds the fault SLOT during power on sequence at SEQ_ON_STAT = 2'b10 000 : SLOT1 (default) 001 : SLOT2 010 : SLOT3 011 : SLOT4 100 : SLOT5 101 : SLOT6 110 : SLOT7 111 : SEQ_ON has completed |
| | | 2:0 | Reserved | 000 | R | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|-----------|-----|-------------|---------|------|--|
| 0x3B | SSEND_CHx | 7 | sSSEND_BCK | 0 | R | It indicates Buck soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end |
| | | 6 | sSSEND_LDO1 | 0 | R | It indicates LDO1 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end |
| | | 5 | sSSEND_LDO2 | 0 | R | It indicates LDO2 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end |
| | | 4 | sSSEND_LDO3 | 0 | R | It indicates LDO3 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end |
| | | 3 | sSSEND_LDO4 | 0 | R | It indicates LDO4 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end |
| | | 2 | sSSEND_BST | 0 | R | It indicates Boost soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end |
| | | 1 | sSSEND_BCK2 | 0 | R | It indicates Buck2 soft-start end or not 0 : Not soft-start end (default) 1 : Soft-start end |
| | | 0 | Reserved | 0 | R | Reserved |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|---------|-----|---------------|---------|------|--|
| 0x42 | INT_SET | 7:6 | Reserved | 00 | RW | Reserved |
| | | 5:4 | INT_DEG[1:0] | 00 | RW | Interrupt reflash pulse width timing. 00 : disable (default) 01 : 2µs 10 : 4µs 11 : 8µs |
| | | 3:0 | SEQ_STAT[2:0] | 0000 | R | Indicate PMU's State 0000 : IDLE (default) 0001 : ONSEQ (slot1 to slot7 + 4ms, when 4ms clock end will trigger ONSEQ_END) 0010 : ONSEQ_END 0011 : ENSEQ 0100 : OFFSEQ 0101 : OFFSEQ_END (slot7 to slot1, when slot1 sequence end will trigger OFFSEQ_END) 1111 : Else |

| Addr | RegName | Bit | BitName | Default | Type | Description |
|------|----------|-----|----------|----------|------|---|
| 0x43 | PMU_STAT | 7:0 | PMU_STAT | 00000000 | R | BST latch off (BSTEN) 0 : Release (default) 1 : Latch off |
| | | | | | | BST latch off (HWEN) 0 : Release (default) 1 : Latch off |
| | | | | | | BCK1 latch off 0 : Release (default) 1 : Latch off |
| | | | | | | BCK2 latch off 0 : Release (default) 1 : Latch off |
| | | | | | | LDO1 latch off 0 : Release (default) 1 : Latch off |
| | | | | | | LDO2 latch off 0 : Release (default) 1 : Latch off |
| | | | | | | LDO3 latch off 0 : Release (default) 1 : Latch off |
| | | | | | | LDO4 latch off 0 : Release (default) 1 : Latch off |

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WL-CSP-25B 2.2x2.3 (BSC) package, the thermal resistance, θ_{JA} , is 31.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (31.5^\circ\text{C/W}) = 3.05\text{W for a WL-CSP-25B 2.2x2.3 (BSC) package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 12 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

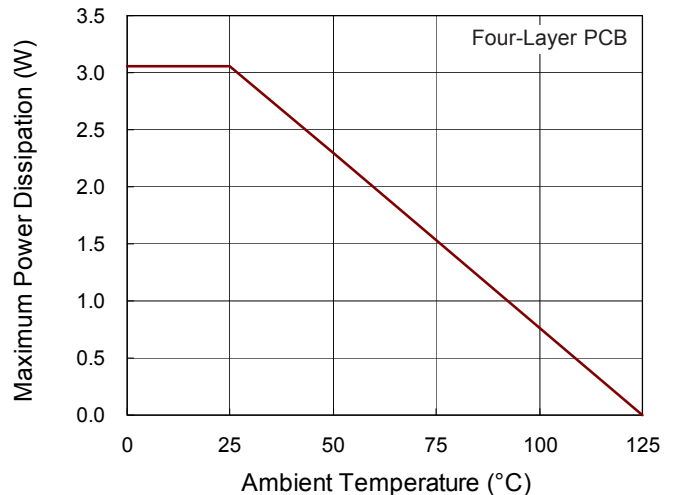


Figure 12. Derating Curve of Maximum Power Dissipation

Layout Considerations

The PCB layout is an important step to maintain the high performance of the RT5112. Both the high current and the fast switching nodes demand full attention to the PCB layout to keep the robustness of the RT5112 through the PCB layout. Improper layout might lead to the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT5112, the following PCB layout guidelines must be strictly followed.

- ▶ The trace from switching node to inductor should be as short as possible to minimized the switching loop for better EMI.
- ▶ Place the input and output capacitors close to the input and output pins respectively for good filtering.
- ▶ Keep the main power traces as wide and short as possible.
- ▶ Connect the AGND, DGND, GNDB and GNDBST to a strong ground plane for maximum thermal dissipation and noise protection.
- ▶ Directly connect the Buck output capacitors to the feedback network to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

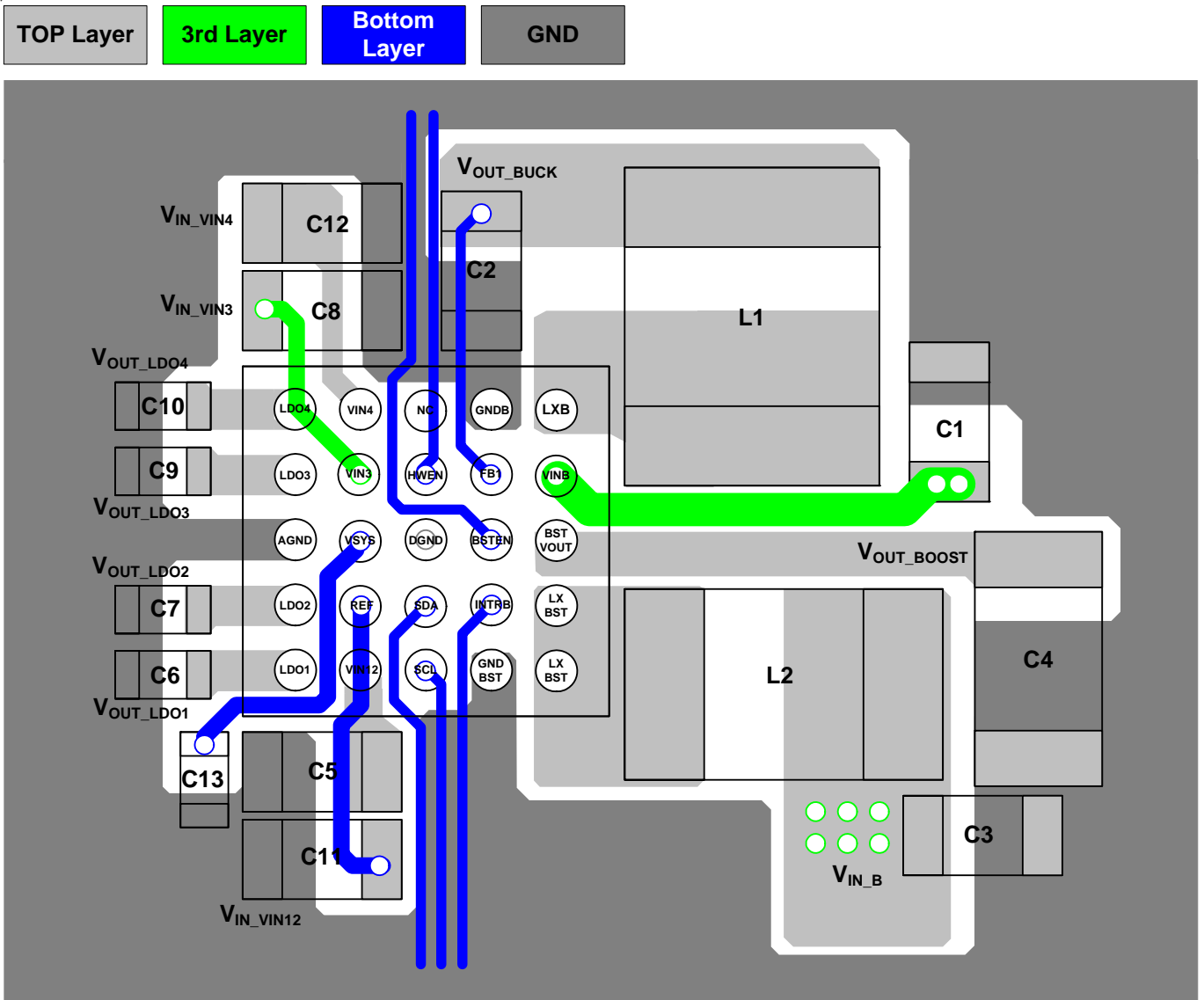
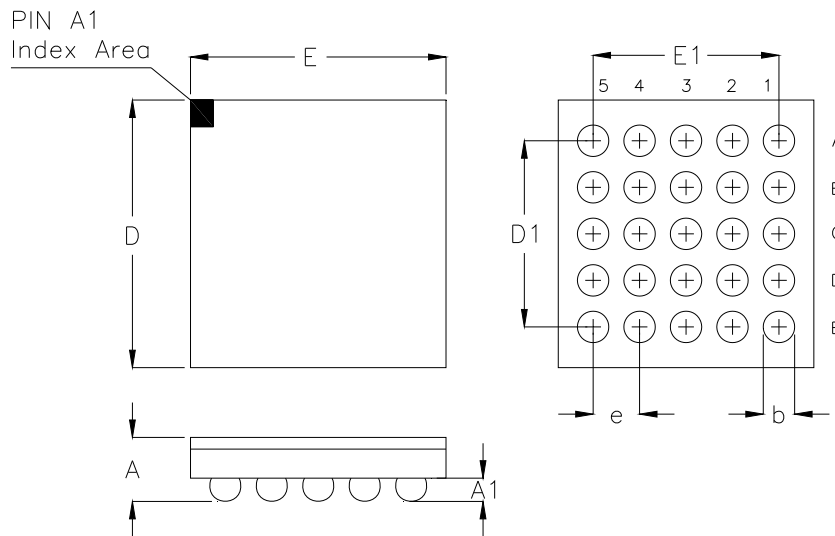


Figure 13. PCB Layout Guide

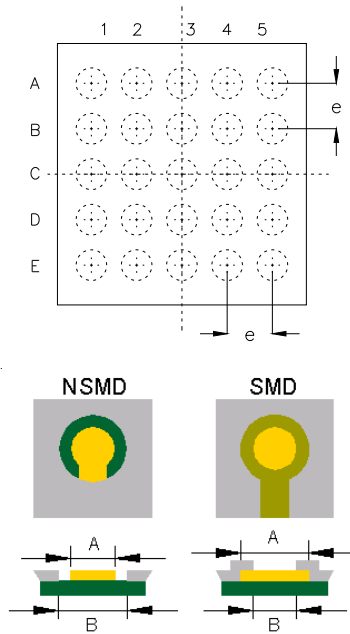
Outline Dimension



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | 0.170 | 0.230 | 0.007 | 0.009 |
| b | 0.240 | 0.300 | 0.009 | 0.012 |
| D | 2.260 | 2.340 | 0.089 | 0.092 |
| D1 | 1.600 | | 0.063 | |
| E | 2.160 | 2.240 | 0.085 | 0.088 |
| E1 | 1.600 | | 0.063 | |
| e | 0.400 | | 0.016 | |

25B WL-CSP 2.2x2.3 Package (BSC)

Footprint Information



| Package | Number of Pin | Type | Footprint Dimension (mm) | | | Tolerance |
|-----------------------|---------------|------|--------------------------|-------|-------|-----------|
| | | | e | A | B | |
| WL-CSP2.2x2.3-25(BSC) | 25 | NSMD | 0.400 | 0.240 | 0.340 | ±0.025 |
| | | SMD | | 0.270 | 0.240 | |

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