

LOW EMI PWM INTELLIGENT POWER HIGH SIDE SWITCH

Features

- Integrated bootstrap for 100kHz switching
- Optimized EMI switching
- Charge pump for DC operation
- Over temperature shutdown
- Over current shutdown
- 3.3V logic level
- Ground loss protection
- ESD protection

Applications

- 24V loads
- Injectors
- Valves
- DC motors

Description

The Device is a five terminal Intelligent Power Switch (IPS) for use in a high side configuration. It features short circuit, over-temperature, ESD protection, inductive load capability and diagnostic feedback. An integrated bootstrap diode allows fast switching.

Product Summary

Rds(on)	35mΩ max.
Vbr	75V min.
I shutdown	20A min.

Package

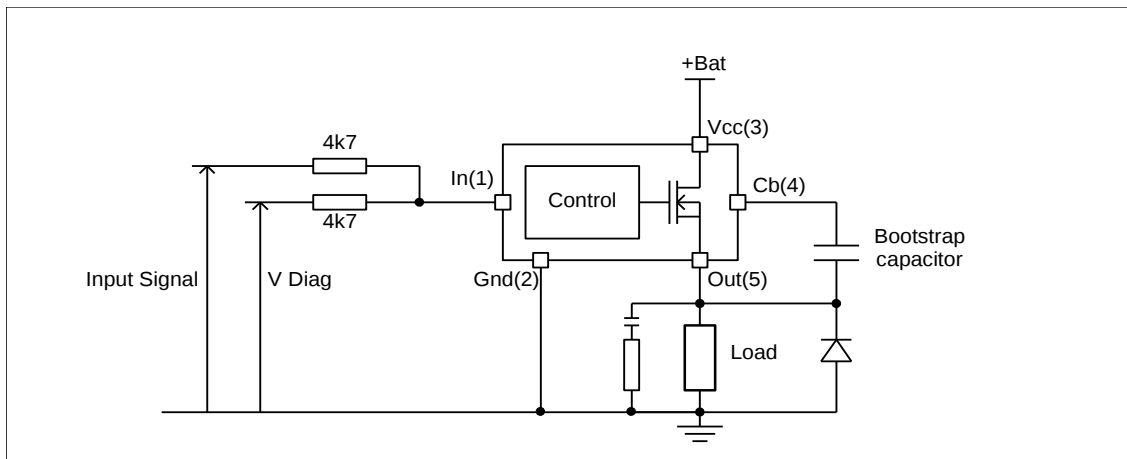


D-Pak – 5 Leads

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIPS72211R	D-Pak-5-Leads	Tube	75	AUIPS72211R
		Tape and reel left	3000	AUIPS72211RTRL

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (Tj= -40°C..150°C, Vcc=6..60V unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units
Vout	Maximum output voltage	Gnd-3	Vcc+0.3	V
Vin	Maximum input voltage	-0.3	5.5	
Vcc max.	Maximum Vcc voltage	—	65	
I in max.	Maximum input current	-3	10	mA
Pd	Maximum power dissipation (internally limited by thermal protection) Rth=50°C/W 1"sq. footprint	—	2.5	W
Tj max.	Max. storage & operating temperature junction temperature	-40	150	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
Rth1	Thermal resistance junction to ambient	50	—	°C/W
Rth2	Thermal resistance junction to case	1.2	—	

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
VIH	High level input voltage	2.7	5.5	V
VIL	Low level input voltage	0	0.9	
Rin	Recommended resistor in series with IN pin	2(1)	10(2)	kΩ
Rdg	Recommended resistor in series with dg pin	2(1)	10(2)	
F max.	Max. switching frequency	—	100	kHz
Cboot	Bootstrap capacitor	30	50	nF

(1) Limited by the maximum input current

(2) Limited by the input capacitor

Static Electrical Characteristics

$T_j = -40..150^{\circ}\text{C}$, $V_{cc} = 6..60\text{V}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Rds(on)	ON state resistance $T_j = 25^{\circ}\text{C}$	—	30	35	$\text{m}\Omega$	$V_{in} = 5\text{V}$, $I_{out} = 5\text{A}$
	ON state resistance $T_j = 150^{\circ}\text{C}$	—	50	70		$V_{in} = 5\text{V}$, $I_{out} = 5\text{A}$
Vcc op.	Operating voltage range with short circuit protection	6	—	60	V	
Icc Off	Supply current when Sleep mode	—	0.2	5	μA	During sleep mode $V_{in} = 0\text{V}$, $V_{out} = 0\text{V}$ $T_j = 25^{\circ}\text{C}$, $V_{cc} = 28\text{V}$
Iout Off	Output leakage current	—	0.2	5		
Icc On	Supply current when On	—	4	10	mA	$V_{in} = 5\text{V}$ $T_j = 25^{\circ}\text{C}$, $V_{cc} = 28\text{V}$
Iout On	Output current when Off	—	10	—	mA	$V_{in} = 0\text{V}$ $T_j = 25^{\circ}\text{C}$, $V_{cc} = 28\text{V}$
Vih	Input high threshold voltage	—	1.9	2.2	V	
Vil	Input low threshold voltage	1	1.6	—		
In hyst.	Input hysteresis	0.1	0.3	0.5		
I in, on	Input current when the part is on	—	15	30	μA	$V_{in} = 5\text{V}$
Vin, off	Input voltage when the part is in fault mode	—	0.1	0.4	V	$I_{in} = 5\text{mA}$

Switching Electrical Characteristics

$V_{cc} = 28\text{V}$, Resistive load $= 2\Omega$, $V_{in} = 5\text{V}$, $T_j = 25^{\circ}\text{C}$

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Tdon	Turn-on delay time to 20%	—	1	—	μs	
Tr	Rise time from 20% to 80% of Vcc	—	0.8	—		
Tdoff	Turn-off delay time to 80%	—	2.2	—		
Tf	Fall time from 80% to 20% of Vcc	—	0.4	—		

Protection Characteristics

$T_j = -40..150^{\circ}\text{C}$, $V_{cc} = 6..60\text{V}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _{sd} on	Over current shutdown	20	30	40	A	$V_{out} = 0\text{V}$
T _{sd}	Over temperature threshold	150(3)	165	—	$^{\circ}\text{C}$	
UV H	Under voltage during turn on	—	5	6.2	V	
UV L	Under voltage during turn off	—	4	5		
T _{diag}	Diagnostic time	—	10	—	ms	see figure 1
T _{sleep}	Time to enter in sleep mode	7	15	30		see figure 2
T _{reset}	Time to enter in sleep mode and reset the fault	—	5	—		see figure 1
T _{wkp}	Time to leave the sleep mode	—	0.05	0.5	μs	$R_{in} = 4\text{k}\Omega$ see figure 2 & 3
T _{pw on rst}	Power on reset duration	4	8	12		

(3) Guaranteed by design

1- In
 2- Gnd
 3- Vcc
 4- Cb
 5- Out

3- Vcc
 1 2 3 4 5
 D Pak

All values are typical



Sleep_mode / Diagnostic

Sleep_mode block manages the diagnostic and the sleep_mode. The device enters in sleep mode if input is inactive during a delay higher than T_{sleep} .

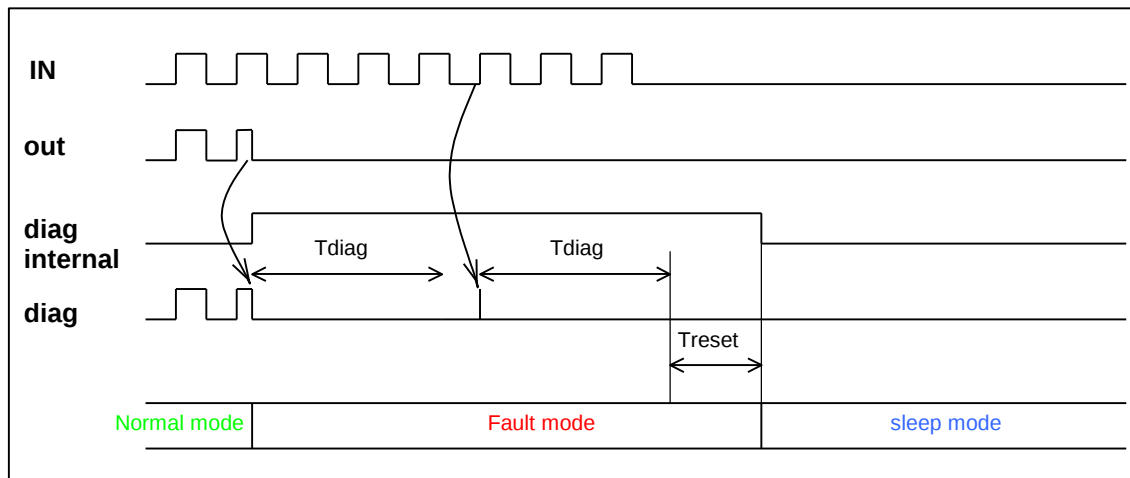


Figure 1

Bootstrap

The AUIPS7221 integrates a bootstrap regulator to maintain a fixed voltage on the bootstrap capacitor for any battery voltage. The regulator is off during the sleep mode to reduce the current consumption.

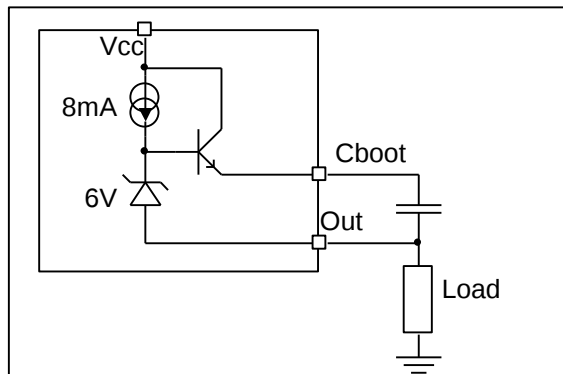


Figure 2

The 8mA current source flows permanently on the output when the output is off and the part is not in sleep mode. In case of an open load condition, the output voltage will be at $V_{cc}-6V$.

Wake up sequence

To wake up the part from the sleep mode, the input must be activated at least during T_{wkp} , then the bootstrap regulator is switched on and the bootstrap capacitor is charged. The output will be not activated during T_{pw} on rst.

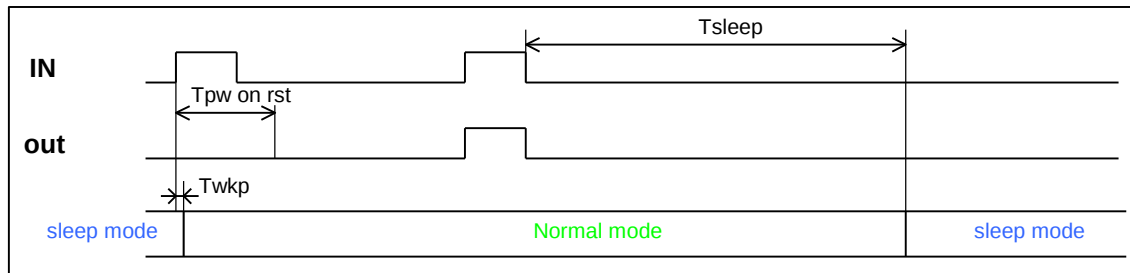


Figure 3

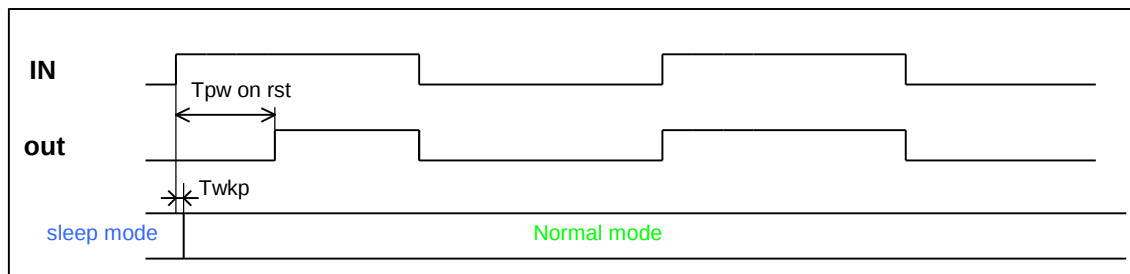


Figure 4

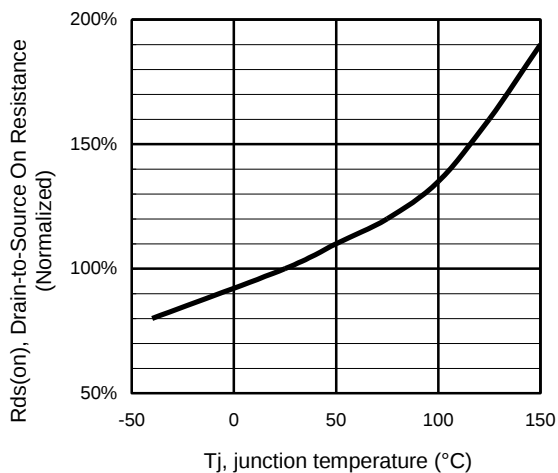


Figure 5 - Normalized R_{ds(on)} (%) Vs T_j (°C)

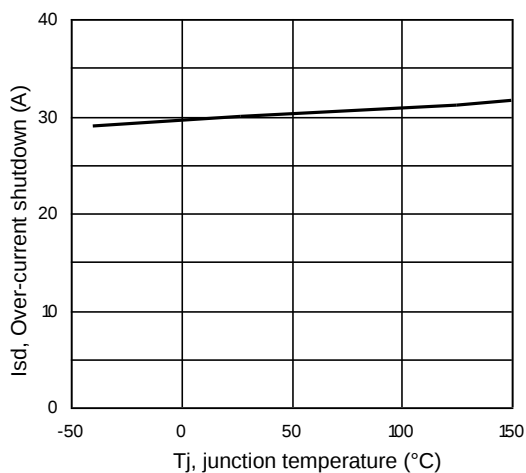


Figure 6 – I_{sd} (A) Vs T_j (°C)

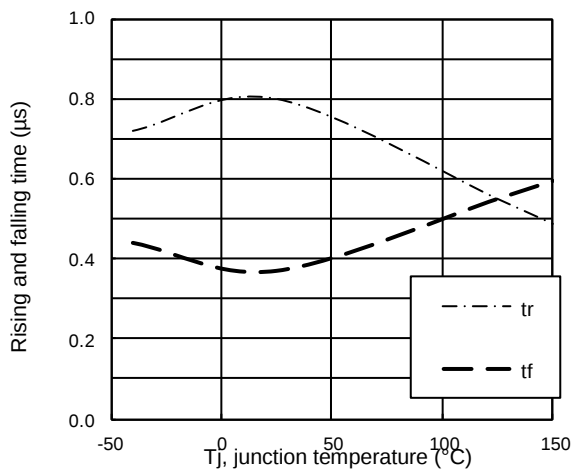


Figure 7 – t_r / t_f (μs) Vs T_j (°C)

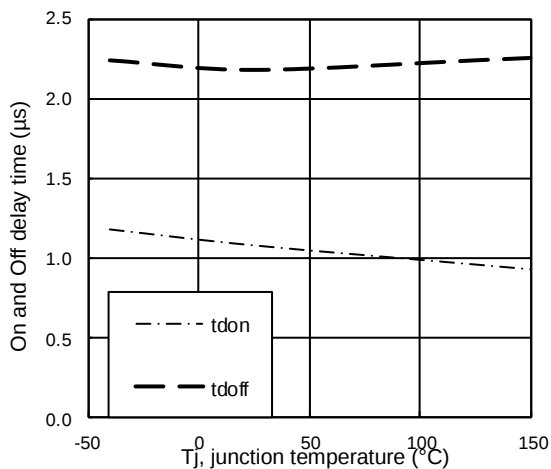
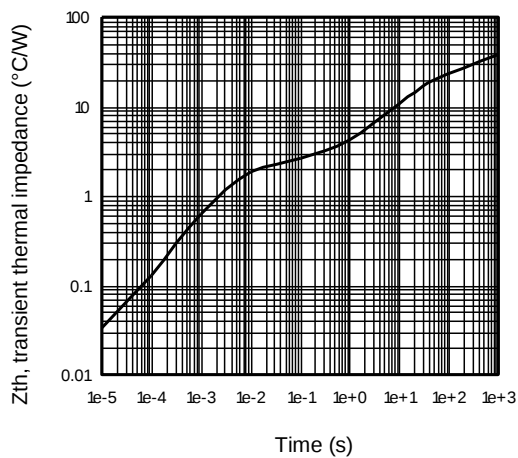


Figure 8 – t_{don} / t_{doff} (μs) Vs T_j (°C)



**Figure 9 – Transient thermal impedance (°C/W)
Vs time (s)**

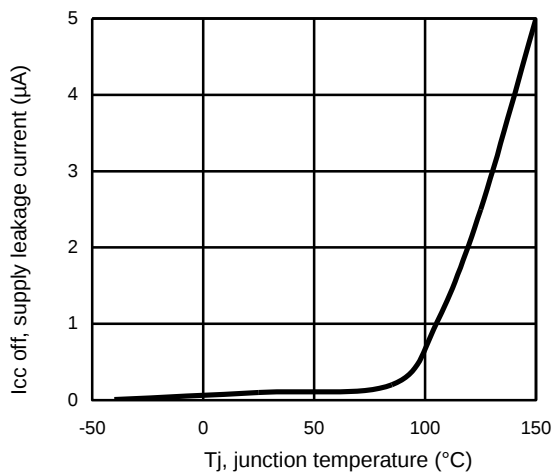


Figure 10 – I_{cc off} (µA) Vs T_j (°C)

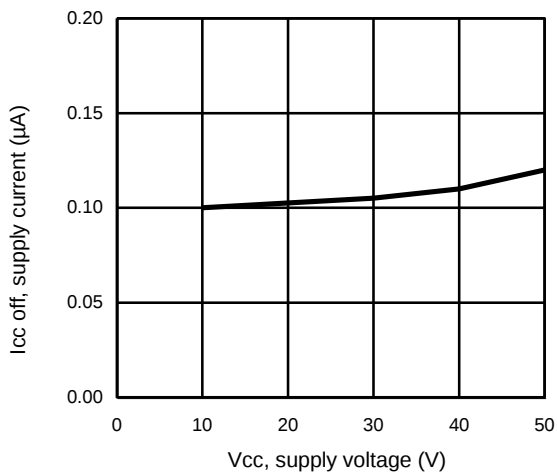
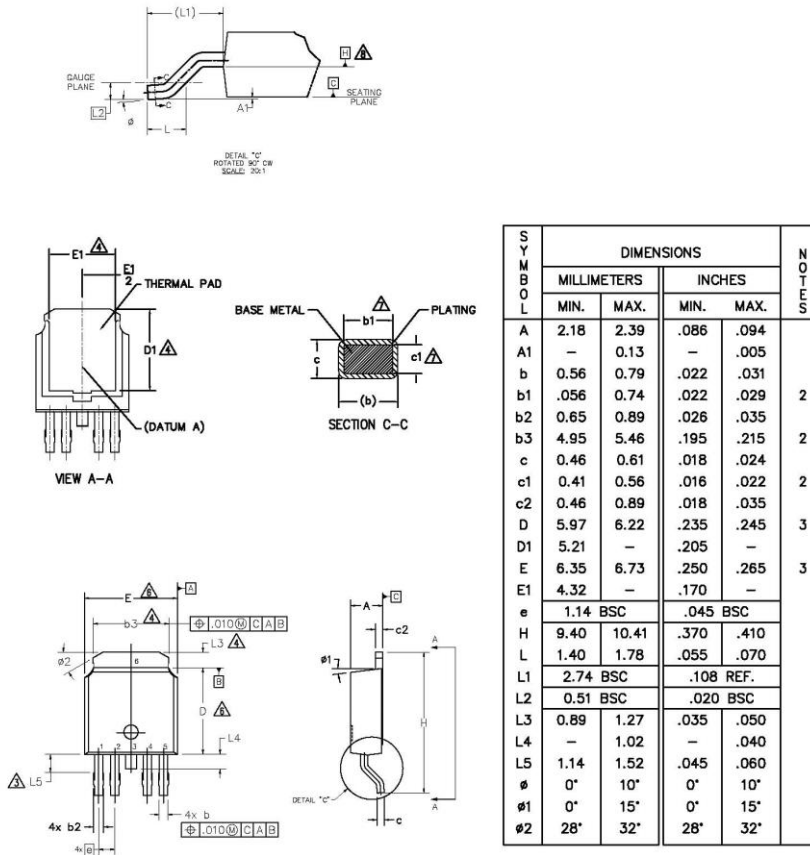


Figure 11 – I_{cc off} (A) Vs V_{cc} (V)

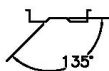
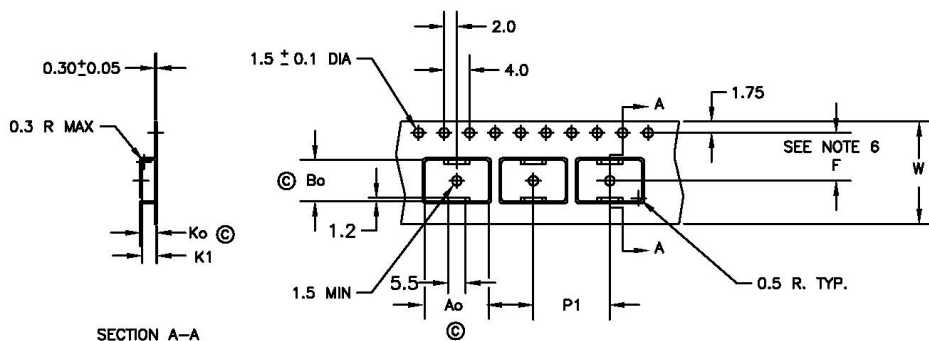
Case Outline 5 Lead – DPAK



NOTES:

- 1.— DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
- 2.— DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.— LEAD DIMENSION UNCONTROLLED IN L5.
- 4.— DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.— SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.— DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.— DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.— DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.— OUTLINE CONFORMS TO JEDEC OUTLINE TO-252.
10. LEADS AND DRAIN ARE PLATED WITH 100% Sn

Tape & Reel 5 Lead – DPAK

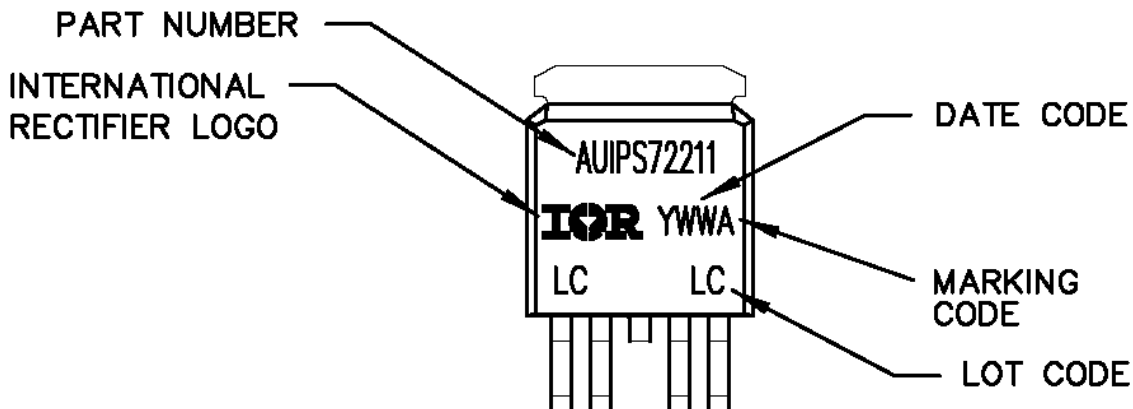


$A_o = 10.5 \text{ mm}$
 $B_o = 7.0 \text{ mm}$
 $K_o = 2.8 \text{ mm}$
 $K_1 = 2.4 \text{ mm}$
 $F = 7.5 \text{ mm}$
 $P_1 = 12.0 \text{ mm}$
 $W = 16.0 \pm .3 \text{ mm}$

NOTES:

1. 10 SPROCKET HOLE PUNCH CUMULATIVE TOLERANCE ± 0.02
2. CAMBER NOT TO EXCEED 1mm IN 100mm
3. MATERIAL: CONDUCTIVE BLACK POLYSTYRENE
4. A_o AND B_o MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET
5. K_o MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
6. POCKET POSITION RELATIVE TO THE SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
7. VENDOR: (OPTIONAL)
8. MUST ALSO MEET REQUIREMENTS OF EIA STANDARD #EIA-481A, TAPING OF SURFACE-MOUNT COMPONENTS FOR AUTOMATIC PLACEMENT.
9. TOLERANCE TO BE MANUFACTURER STANDARD
10. SURFACE RESISTIVITY OF MOLDED MATL: MUST MEASURE LESS THAN OR EQUAL TO 10^8 OHMS PER SQUARE. MEASURED IN ACCORDANCE TO PROCEDURE GIVEN IN ASTM D-257 & ASTM D-991 (REF. C-9000 SPEC.)
11. TOTAL LENGTH PER REEL MUST BE 79 METERS
12. © CRITICAL DIMENSION

Part Marking Information



Qualification Information

Qualification Level		Automotive (per AEC-Q100)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		DPAK-5L	MSL1, 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (150V) (per AEC-Q100-003)	
	Human Body Model	Class H1A (500V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

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Revision History

Revision	Date	Notes/Changes
A	August 4th, 2011	Initial release
Rev 1.1	March 6th, 2017	'Part Marking information' updated